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Two-Stage Metal-Catalyst-Free Growth of High-Quality Polycrystalline Graphene Films on Silicon Nitride Substrates

*Jianyi Chen, Yunlong Guo, Yugeng Wen, Liping Huang, Yunzhou Xue, Dechao Geng, Bin Wu, Birong Luo, Gui Yu, and Yunqi Liu**

Graphene, a single layer of sp^2-bonded carbon atoms packed into a two-dimensional (2D) honeycomb crystal lattice, has attracted significant attention due to its distinctive band structure and fascinating physical properties.[1,2] Since the first samples were produced in 2004 by mechanical cleavage of graphite,[3] many methods have been developed to prepare graphene.[3–8] Recent development of large-scale graphene synthesis by chemical vapor deposition (CVD)[5,6] opened the possibility of a wide range of applications of graphene in electronics. Currently, metal layers or films provide ideal substrates for producing graphene due to their matching crystal structures and lattice parameters. Graphene films with monolayer or few-layer coverage have been synthesized on many metals (e.g., Ni, Cu, Fe, and Co) via a chemical vapor deposition (CVD) process.[5,6,9–11] High-quality graphene films can also be prepared on insulating SiC and sapphire substrates.[4,12] The epitaxial graphene nanoribbons on SiC showed an on-off ratio of 10 and carrier mobilities up to 2700 $cm^2\ V^{-1}\ s^{-1}$ at room temperature.[13] However, the complicated transfer techniques for metal-catalyzed graphene or the high cost of the single crystal SiC and sapphire substrates have limited the wide application of these graphene in nanoelectronics.

For this reason, many CVD approaches have been developed to synthesize graphene samples on insulating substrates. Levendorf et al.[14] reported a metal-catalyzed transfer-free method, and subsequently a few modified routes have been investigated by several research groups,[15–17] wherein graphene films grown on the top or bottom surface of a sacrificial metal are allowed to adhere onto SiO_2 substrates by a metal wet-etching or evaporation process. However, by these techniques, it is difficult, if not impossible, to avoid metal contamination completely. Alternatively, the direct metal-catalyst-free growth of high-quality graphene on cheaper dielectric substrates shows its advantages due to today's transistor technology needing an insulating layer separating the transistor gate from the channel.[18] Much work, to date, has been done to explore the catalyst-free growth of graphene on dielectric substrates.[19–21] Our research group has reported the direct growth of high-quality polycrystalline graphene on SiO_2 substrates via an oxygen-aided method.[22] However, the applications of this graphene are restricted, due to charge transfer, adsorbates, and electron-phonon scattering of graphene on standard SiO_2/Si substrates.[23] High mobilities of graphene have only been observed on octadecyltrimethoxysilane self-assembled monolayers (OTMS SAMs)modified SiO_2/Si substrates and boron nitride substrates.[23,24] Thus, it is highly desired to prepare graphene films on high-quality substrates where the deleterious effects of the substrate can be minimized. Here, we demonstrate the preparation of large-area graphene films on silicon nitride (Si_3N_4) layers via a two-stage metal-catalyst-free CVD process. Graphene sheets can successively grow along a slightly rough Si_3N_4 surface, and merge together to form a polycrystalline graphene film, as confirmed by atomic force microscopy (AFM) measurements. Raman spectroscopy and transmission electron microscopy (TEM) illustrate that the polycrystalline graphene films have high quality. The graphene films have been fabricated into field-effect transistors (FETs), and the carrier mobilities can reach 1510 $cm^2\ V^{-1}\ s^{-1}$ in air and 1518 $cm^2\ V^{-1}\ s^{-1}$ in N_2, which are about three times the values of those grown on SiO_2/Si substrates,[22] and are better than some of metal-catalyzed graphene.[25–29]

Figure 1 illustrates the procedure for the two-stage synthesis of graphene films on insulating Si_3N_4 substrates. A clean Si_3N_4/SiO_2/Si chip was placed in the center of a quartz tube mounted inside a high-temperature furnace (Figure 1a). The procedure consists of the nucleation of graphene, followed by graphene growth on a Si_3N_4 surface (Figure 1b). In the first stage (nucleation), a small amount of CH_4 (2.3 sccm) with a larger flow of Ar (300 sccm) was introduced into the CVD system, which resulted in the formation of discrete graphene nanocrystals on the Si_3N_4 substrates. In the subsequent growth stage, a carbon source gas with a higher percentage of H_2 (CH_4:H_2 = 5:50 sccm) was used to realize the growth of high-quality graphene film. The relevant experimental parameters including the temperature profile, gas composition, and flow rates are described in the Experimental Section and in Figure S1 in the Supporting Information.

Figure 2 shows the changes in the AFM images of the Si_3N_4 surface topography before and after the formation of graphene. The polycrystalline Si_3N_4 layer on SiO_2/Si substrate, deposited by a low-pressure CVD technique, is characterized by close-packed nanoparticles (Figure 2a,b). The average roughness of the Si_3N_4 surface is 0.702 nm, and the height of the raised Si_3N_4 particles is ≈2.561 nm according to the AFM measurements

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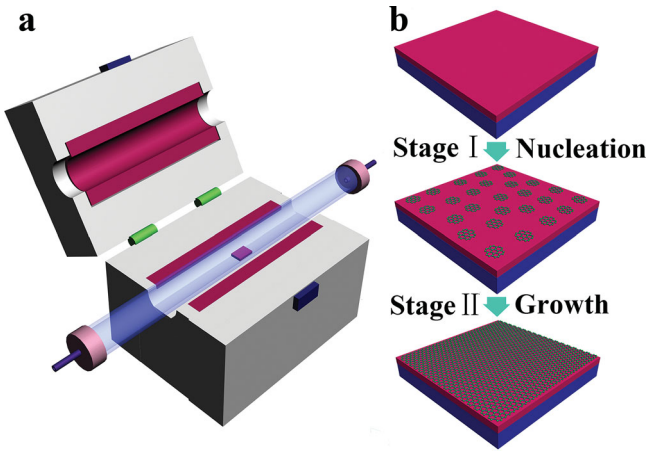

Figure 1. a) CVD system for graphene growth on a Si_3N_4 substrate. b) Schematic diagram of the two-stage process for graphene growth.

(Figure 2a). After the first-stage growth, there is little change in surface roughness (Figure 2c, $R_a \approx 0.775$ nm), but the surface obviously undergoes significant modifications and becomes covered with individual graphene nanocrystals (Figure 2d). We can easily tune the number and size of the graphene nanocrystals by changing the carbon flow as shown in Figure S2 in the Supporting Information. The AFM phase image (Figure 2d) marked with the black circle reveals a clear contrast between the graphene and the Si_3N_4 substrate, and the lateral dimensions of the graphene nanocrystals are about 30–40 nm. Similar to the graphene growth on Cu,[30] the surface roughness has a positive role for graphene nucleation (Supporting Information, Figure S2,S3).

Figure 2e,f show the AFM images of a typical graphene film. The graphene morphology in the AFM height image (Figure 2e) is not easily distinguished from the underlying Si_3N_4 layer due to the similar surface roughness ($R_a \approx 0.887$ nm), but in the AFM phase image (Figure 2f), the graphene film shows a clear outline, which allows it to be easily distinguished from the Si_3N_4 substrate. The graphene film is composed of closely linked graphene sheets. Graphene wrinkles often occur along the boundary between two sheets (Figure 2f). According to AFM images, the lateral dimension of the graphene sheets can reach about 1 μm and the height of the graphene wrinkle is about 1.851 nm (Supporting Information, Figure S4). Kim et al.[31] reported that a flat plane able to hold the carbon species is inevitably necessary in preparing graphene on various substrates. However, our results illustrate that the growth of graphene is not influenced by the polycrystalline nature of the substrate, and graphene sheets can successfully cross Si_3N_4 nanoparticles and form a continuous film on a slightly rough surface.

Figure 3a shows a photograph of a graphene film on a Si_3N_4 substrate. The surface is covered with graphene after the two-stage CVD growth. The graphene film appears uniform when viewed by optical microscopy (Figure 3b). To explore the microstructure of the graphene film, we show a high-resolution scanning electron microscopy (SEM) image of the graphene film in Figure 3c. The graphene films display different images compared with those grown on metal foils, which can be explained by the electron-beam-induced current on the insulator surface.[32] The high-resolution SEM image shows contrast indicative of predominantly monolayer coverage with the small grey

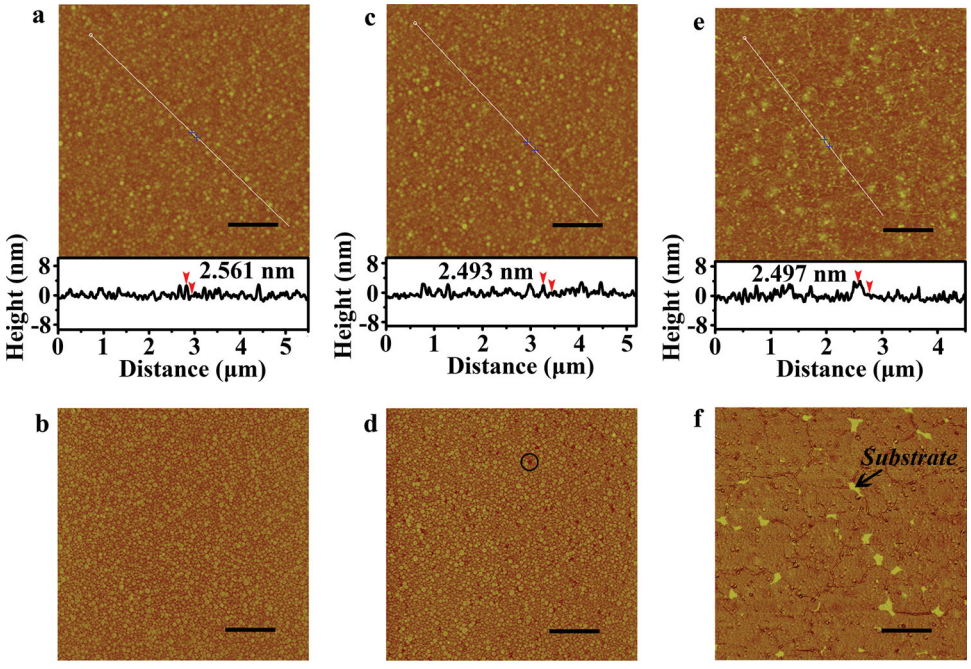

Figure 2. a,b) AFM images of Si_3N_4 substrate. c,d) AFM images of the Si_3N_4 substrate after nucleation. The lateral dimension of the graphene nanocrystals is about 30–40 nm, which is marked by a black circle. e–f) AFM images of the Si_3N_4 substrate after growth. Height images (a,c,e). Phase images (b,d,f). Scale bars = 1 μm.

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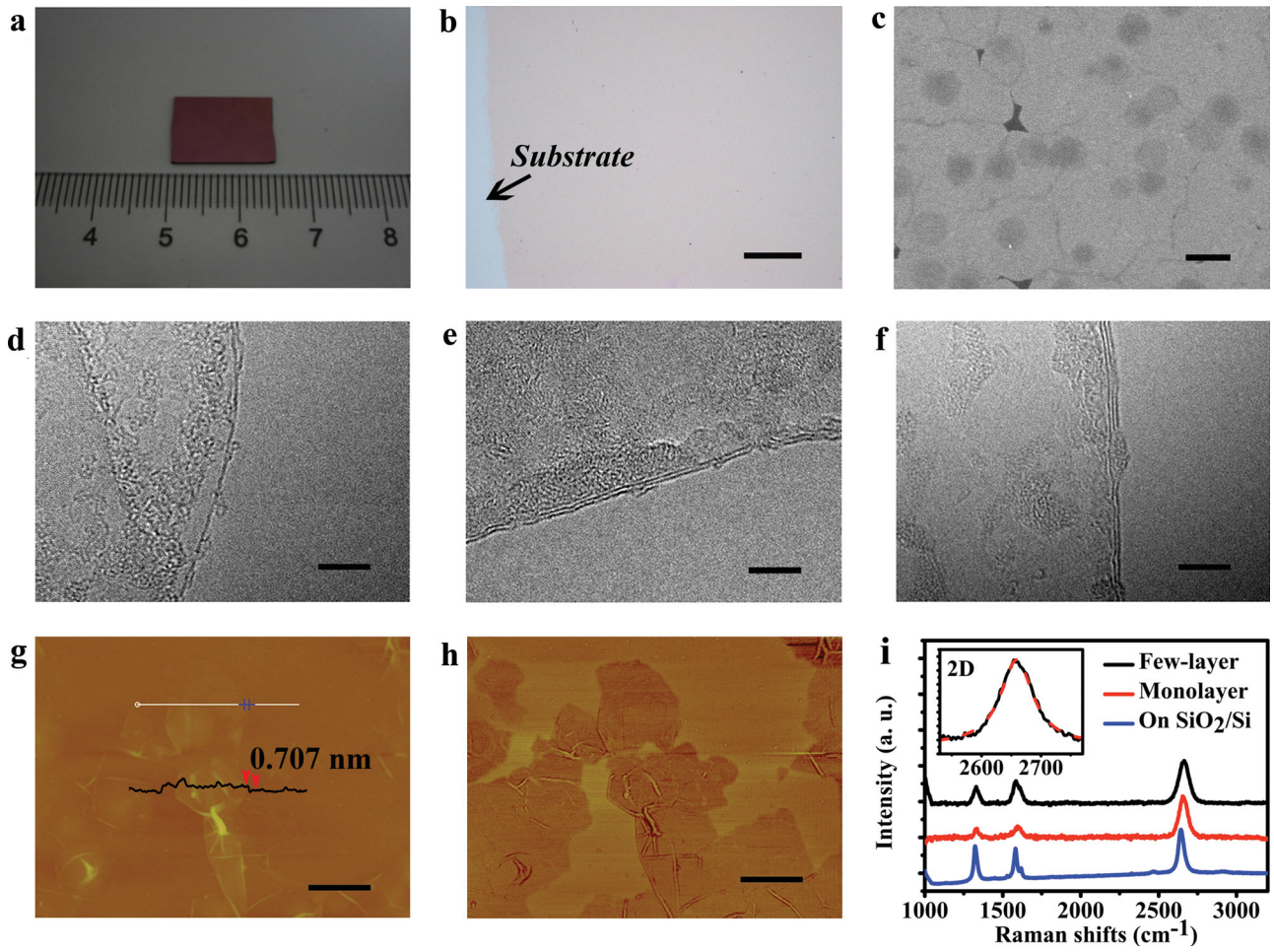

Figure 3. a) Photograph of graphene film on Si_3N_4 substrate. b) Optical micrograph of a graphene film on a Si_3N_4 substrate. Scale bar 50 µm. c) SEM image of graphene film. Scale bar = 500 nm. d–f) High-resolution TEM images of graphene films. Scale bars: 5 nm. g,h) AFM images of transferred graphene on SiO_2/Si substrates: height image (g), phase image (h); scale bars = 300 nm. i) Raman spectra (633 nm laser wavelength) of the graphene films on a Si_3N_4 substrate and the transferred graphene on a SiO_2/Si substrate. The inset shows the enlarged 2D peak of single-layer graphene with its fitted single Lorentzian curve.

or black regions indicative of areas of few-layer graphene or the Si_3N_4 substrate, as has also been confirmed by Raman spectroscopy analysis and AFM measurements (Figure 2f, and Supporting Information, Figure S5). Compared with the SiC epitaxial technique,[4,13] the metal-catalyst-free CVD growth results in graphene films with superior transfer behavior, facilitating characterization by TEM. After transferring the graphene film to copper grids by using our method reported previously (Supporting Information, Figure S6),[22] the TEM images display a clear layer structure (Figure 3d–f), which is consistent with previously reported results.[5,6] Selected area electron diffraction (SAED) patterns (Supporting Information, Figure S6) indicate clearly that our graphene has a high quality despite the fact that no metal catalysts were employed during the graphene growth. To observe further the detailed structure of our graphene, we also measured the morphology and thickness of the samples transferred onto a SiO_2/Si substrate by AFM. In Figures 3g,h we show typical AFM images of the graphene. The graphene sheets on the SiO_2/Si substrate display wrinkled morphologies that are similar to those of graphene made by other methods. The line scan at the end (Figure 3g) illustrates that the step height between the surface of the sheet and the substrate is ≈0.707 nm, which is in accord with reports for one-atom-thick graphene.[33,34]

Raman spectra were recorded in order to ascertain the quality of the graphene. All of the spectra collected using a laser with an excitation wavelength of 633 nm show G, D, and 2D bands (Figure 3i). The 2D peak stems from a double-resonance electron–phonon scattering process,[35] which is widely used to distinguish mono- and few-layer graphene. The spectrum (inset) reveals a sharp and symmetric 2D peak located at ≈2660 cm^{-1} with a high ratio (>4) of its intensity relative to that of the G band (I_{2D}/I_G), confirming the presence of monolayer graphene.[33] The full width at half-maximum (FWHM) of the 2D peak is ≈65 cm^{-1}, which decreases to ≈40 cm^{-1} after transfer from the Si_3N_4 substrate to a SiO_2/Si substrate. However, the breakage of the graphene film in the transfer process causes a change in the relative intensity of the Raman signals.

The relatively larger width of the 2D peak of the graphene film on a Si_3N_4 substrate can be explained by a substrate effect and a non-uniform number of layers.[36] The low intensity of the D peak located at ≈1330 cm^{-1} may be caused by domain boundaries or a slight disorder of the graphene layer. Similar to our results reported previously,[22] the D, G, and 2D bands of graphene grown on the Si_3N_4 substrate are all blue-shifted with respect to the peaks of graphene after transfer onto SiO_2/Si substrates (≈11 cm^{-1} for D band; ≈16 cm^{-1} for G band; ≈17 cm^{-1} for 2D band), indicating the strong compressive strain effect between the graphene and the Si_3N_4 substrate.

In a general graphene-preparation process, the required carbon concentration for spontaneous nucleation of graphene is about twice the equilibrium concentration.[37,38] A higher CH_4 concentration favorable for nucleation thus cannot avoid repeated nucleation in the graphene growth. The separation of the nucleation stage and the growth stage allows great versatility in controlling the nucleation density (Supporting Information, Figure S2), and, furthermore, the quality of the graphene films. We can tune the growth of graphene grains by using different nucleation conditions, deposition times, and deposition temperatures (Supporting Information, Figure S7–S9). The maximum size of our graphene grains was about 1 μm, as is confirmed by the AFM image in Figure 2f. In order to probe the mechanism of graphene growth on the Si_3N_4 surface, we obtained low-angle X-ray photoelectron spectroscopy (XPS) (30°), Raman spectroscopy, and IR spectroscopy investigations, which are shown in Figure S10–S13 in the Supporting Information. There are no signals from metals such as Fe, Co, Ni, and Cu, indicating that metallic elements are not involved in graphene growth.[22] We did not detect signals from SiC due to thermal reduction of the carbon (Supporting Information, Figure S11–S13). However, an upshift of the Si 2p XPS spectrum was found after graphene growth (Supporting Information, Figure S10), indicating the formation of SiO_2, which may come from the quartz tube or from thermal oxidation of the Si_3N_4. Moreover, the presence of oxygen could result in the oxygen-based nucleation of graphene on an insulating substrate.[22,39] Once graphene nanocrystals are formed on the Si_3N_4 surface in the nucleation stage, supersaturated active carbon species arising from the decomposition of CH_4 would result in the growth of graphene in the growth stage.[40]

To evaluate further the quality of our graphene films, a series of back-gated field-effect transistors (FETs) (Supporting Information, Figure S14) with different transport channels (channel length L = 40–140 μm, channel width W = 1200 μm) were fabricated on graphene films, which directly grown on Si_3N_4/SiO_2/Si substrates (Si_3N_4:SiO_2 = 100:300 nm). **Figure 4**a shows the typical output characteristics (drain current I_{DS} versus drain voltage V_{DS}) for a graphene device (L = 125 μm, W = 1200 μm) in N_2 (with a vacuum treatment of 10 days before measurement). The I_{DS} increases with increasingly negative gate voltage (V_G), which is in accordance with results for previously reported graphene FETs.[22,33] The transfer curves (I_{DS} versus V_G) for the corresponding device are presented in Figure 4b. The device shows a bipolar behavior (inset) in N_2 with the Dirac point located at ≈89 V, which might be mainly attributed to the strong doping of the substrate. The field-effect mobilities of carriers in N_2 based on the slope I_{DS}/V_G fitted to the linear regime of the transfer curves are about 1518 cm^2 V^{-1} s^{-1} for holes, and 478 cm^2 V^{-1} s^{-1} for electrons. After exposure to air (for 3 days), the mobility of the holes showed little change (remaining at

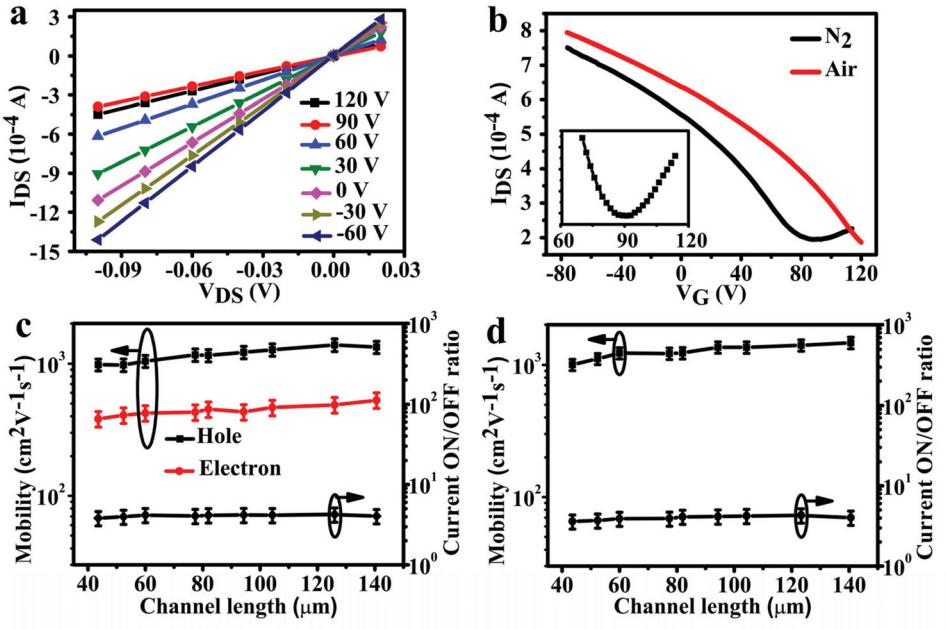

Figure 4. a) Drain current (I_{DS}) versus drain–source voltage (V_{DS}) recorded at different gate voltages for a device with a channel length L = 125 μm and channel width W = 1200 μm in N_2. b) Transfer characteristics (current (I_{DS}) versus gate voltage (V_G)) for the device at V_{DS} = 0.05 V in air (black) and N_2 (red). The inset shows an enlarged image of the transfer line in N_2. c,d) Mobilities and ON/OFF current ratios as a function of channel length in N_2 (c) and air (d).

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≈1510 cm^2 V^{-1} s^{-1}), but the doping of the physisorbed molecular oxygen caused the Dirac point to shift to a more-positive gate voltage.[41,42] The carrier mobility and "ON/OFF" current ratio with respect to the transport channel length are plotted in Figure 4c,d. The graphene FETs show the same characteristics regardless of channel length in both air and a N_2 atmosphere, indicative of the uniformity of our graphene films.

In summary, we have developed a practical, two-stage method to produce high-quality graphene on polycrystalline insulating substrates. In the process, the separation of the nucleation stage and the growth stage facilitates the control of the nucleation density and grain size in graphene films. AFM, TEM, Raman spectroscopy, and electrical-transport measurements illustrate that the graphene films have high quality, even though no metal catalysts were employed during the graphene growth. The carrier mobilities of the graphene films can reach 1510 cm^2 V^{-1} s^{-1} in air and 1518 cm^2 V^{-1} s^{-1} in N_2. The observed mobilities are highest in current metal-catalyst-free graphene FETs using the same back-gated FET configuration, and are comparable with those obtained using metal-catalyzed CVD graphene samples, reflecting the good quality of the graphene lattice. The two-stage metal-catalyst-free-growth procedure avoids a complicated postgrowth transfer process, and is compatible with current Si processing techniques.

Experimental Section

Preparation of Graphene: Graphene films were directly grown on Si_3N_4 substrates by using a two-stage metal-catalyst-free method. Typically, the Si_3N_4 substrates were loaded into a horizontal silica tube mounted inside a high-temperature furnace. The CVD system was evacuated and back-filled with Ar and H_2 three times to remove air. The furnace was heated to 1150 °C and stabilized about 15 min under 250 sccm H_2 and 300 sccm Ar. Nanocrystalline graphene growth was performed at 1150 °C under a reaction gas mixture of 300 sccm Ar, 5 sccm H_2, and 2.3 sccm CH_4 for about 1 h. Subsequently, the growth temperature was quickly dropped to 900 °C and then raised to 1150 °C (over about 15 min) again under 50 sccm H_2 and 300 sccm Ar to eliminate the influence of the turbulence of the carbon source on the graphene growth. After stabilizing the system for about 15 min at 1150 °C, 50 sccm H_2 and 5.0 sccm CH_4 were introduced again for about 3 h to grow graphene films on Si_3N_4 substrates.

Characterization: AFM images were obtained using a NanoMan VS microscope in the tapping mode. SEM images were obtained using a Hitachi S-4800 scanning electron microscope. TEM was performed using a Tecnai G2 F20 U-TWIN transmission electron microscope operated at 200 kV. XPS was carried out on an ESCALAB 220I-XL spectrometer using Al K_α X-rays as the excitation source. The base pressure was about 3×10^{-9} mbar, and the binding energies were referenced to the C 1s line at 284.8 eV. The Raman spectra were recorded at room temperature using a Renishaw inVia Raman microscope with laser excitation at 633 nm, and scans were taken over an extended range (100–3200 cm^{-1}) with an exposure time of 150 s. Fourier transform infrared (FTIR) spectroscopy was conducted using an RT-DLaTGS 27 spectrometer.

Device and Electrical Measurements: Back-gated graphene FETs were fabricated on $Si_3N_4/SiO_2/Si$ wafers with Au as the source–drain electrodes and the doped Si substrate as the back gate. Au source–drain electrodes (≈50-nm-thick) were deposited on the graphene films by thermal evaporation through a shadow mask. A Keithley 4200SC semiconductor parameter analyzer was used to measure the electrical properties. The FET measurements were carried out in air and N_2 at room temperature. The mobility was calculated as:

$$\mu = \frac{L}{WC_{ox}V_{DS}}\frac{\partial I_{DS}}{\partial V_G} \quad (1)$$

where W and L are the channel width and length, C_{ox} is the gate oxide capacitance, V_{DS} is the source–drain voltage, I_{DS} is the source–drain current, and V_G is the gate voltage. The "ON/OFF" ratios were calculated as:

$$r_{ON/OFF} = \frac{I_{DS}(max)}{I_{DS}(min)} \quad (2)$$

where I_{DS} (max) and I_{DS} (min) are the maximum and minimum values of I_{DS} respectively.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

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