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Evaluation and comparison of GHz-range LC oscillators using time-varying root-locus

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SUMMARY

This paper presents a comprehensive comparison between complementary metal-oxide-semiconductor (CMOS) *LC*-oscillator topologies often used in GHz-range transceivers. The comparison utilizes the time-varying root-locus (TVRL) method to add new insights into the operation of different oscillators. The paper focuses on the treatment of the TVRL trajectories obtained for different oscillators and establishes links between the trajectories and physical phenomena in oscillators. The evaluation of the root trajectories shows the advantages of the TVRL method for comparing oscillator topologies, which is also extended towards the analysis of voltage-controlled oscillators. The necessary circuit simplifications required in closed-form root-locus analysis are avoided by the TVRL, which allows precise oscillator comparison and reveals details on the topology specifics. The derived conclusions have been verified by the Cadence Spectre-RF simulator on 130-nm CMOS process. Copyright © 2011 John Wiley & Sons, Ltd.

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KEY WORDS: oscillator; cross-coupled oscillator; Colpitts; VCO; phase noise; root-locus; TVRL

1. INTRODUCTION

Theoretical studies of phase noise in oscillators have helped in understanding noise phenomena and the construction of high-performance oscillator topologies [1,2], mostly as stand-alone blocks, and they are optimized as such. A typical measure of overall oscillator performance is the widely accepted Figure-of-Merit (FoM), which takes into account the oscillator phase noise achieved in given power supply conditions. Although the adopted FoM compares different oscillators, its use may lead to misleading results. For instance, the best oscillator FoM is typically achieved in low-voltage conditions [2,3], but the oscillator phase noise may not satisfy the specifications. In such cases, the voltage swing is raised until the phase noise goal is met. This solution comes at the expense of extra power consumption; it is limited by the breakdown voltages of the active devices, and it drives the oscillator away from its FoM optimum. Second, the voltage-controlled oscillator (VCO) in some frequency synthesizers is usually followed by frequency dividers. An increased input voltage swing improves the divider phase noise, and it can also reduce their power consumption [4,5]. Thus, a 'sub-optimum' oscillator, which generates large voltage swing, can improve the entire system performance, while the 'optimum' oscillator remains a theoretical possibility. Third, in low-voltage oscillators, the difference between oscillator voltage supply and, for example, a mobile phone battery of 3.6 V becomes significant. A linear regulator compensates this difference, but involves significant power losses. For instance, a 1.2-V-operated VCO from a 3.6-V battery utilizes only a

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third of the total power delivered by the battery, which corresponds to ~4.8-dB loss of FoM performance. A high-efficient switching-type regulator would break this dependence, but they are rarely employed near RF blocks due to their interference.

Given the reasons above, an 'optimum' oscillator from the FoM point of view is a vague design target. Since practical oscillator designs have to consider various specifications, such as oscillation frequency, tuning range, phase noise, power supply condition, etc., a complete oscillator comparison is difficult to make. In addition, the large variety of oscillator topologies in the literature confirms that different oscillator architectures have specifics that may be beneficial in some cases, and sub-optimum in others.

The goal of this paper is to evaluate and compare different oscillator topologies by adding new insights derived from time-varying root-locus (TVRL) [6]. The extended comparison brought by the TVRL method gives more guidelines on which topology could serve better for certain specific cases. Furthermore, the evaluation of the TVRL trajectories in different oscillators helps to refine the treatment of the method by underlining its advantages and limitations.

The paper is organized as follows. Section 2 describes the evaluated *LC* oscillators and gives a brief topology comparison. Section 3 derives the TVRL trajectories of simplified oscillator models corresponding to oscillator large-signal operation. The oscillator start-up behavior, active-device bias trajectories and power-conversion factor (PCF) are discussed in Sections 4, 5 and 6 respectively. Section 7 makes a detailed comparison of the oscillator topologies based on the TVRLs obtained in large-signal conditions. The TVRL trajectories are linked to physical processes in the oscillators and to their phase noise performance. Section 8 outlines the TVRL specifics in a VCO.

2. *LC*-OSCILLATORS UNDER EVALUATION

This paper compares some of the most popular oscillator topologies used in wireless transceivers: the double-cross-coupled oscillator (abbreviated here as '1 L' due to the single inductor employed), single-cross-coupled oscillator (abbreviated as '2 L' due to the two coils in use), and differential Colpitts oscillator (D-Colpitts). Cross-coupled topologies are found in the low-GHz range and in high-GHz range applications, while the D-Colpitts has larger popularity in the high GHz range. Cross-coupled topologies have a parasitic node associated with the current mirror, which makes them vulnerable at high frequencies [7]. Since all parasitic capacitances in the Colpitts topology can be associated with one of the tank capacitors, the unpredictable parasitic capacitances accumulate in the resonance tank [7]. Nevertheless, cross-coupled topologies are also popular at high frequencies due to their simplicity of design and the accumulated design expertise from low-GHz-range applications. Other oscillator topologies with improved phase noise are found in the literature [2,3], but they have not yet gained large popularity. Thus, without apparent loss of generality, this work limits the investigation to the main topologies: 1 L, 2 L and D-Colpitts. These topologies exhibit structural modifications, a few of which are covered here.

The evaluated modifications of the 1 L oscillator are shown in Figure 1. The two bias inductors L_{TOP} and L_{BOT} in the 1 L + 2bL topology improve the oscillator phase noise performance through noise filtering and Q-factor preservation of the resonance tank [1]. The values of the passive components and transistor sizes are taken from previously reported VCO [8]. The switched-capacitor bank is modeled with a finite Q-factor capacitor C_O for the purpose of the TVRL investigation. The oscillators evaluated in Subsection 7.1, bottom-biased 1 L and 1 L + 2bL oscillator, have a similar structure, but the bias transistors M_{p3} and M_{p4} are replaced with NMOS transistors having the same W/L aspect ratio. Figure 2 shows the evaluated modifications of the top-biased 2 L oscillator built with NMOS or PMOS cross-coupled pair, with or without bias inductors [1,7]. The transistor sizes and passive components of the 2 L oscillators are the same as those used by the 1 L oscillator in Figure 1 in order to make a fair comparison. The supply voltage of the 2 L oscillators is reduced to 1.5 V in order to keep a similar voltage headroom for the current mirror M_{p3}-M_{p4}. The similar headroom causes comparable current-mirror nonlinearities that affect in the same way the oscillators' TVRL trajectories.

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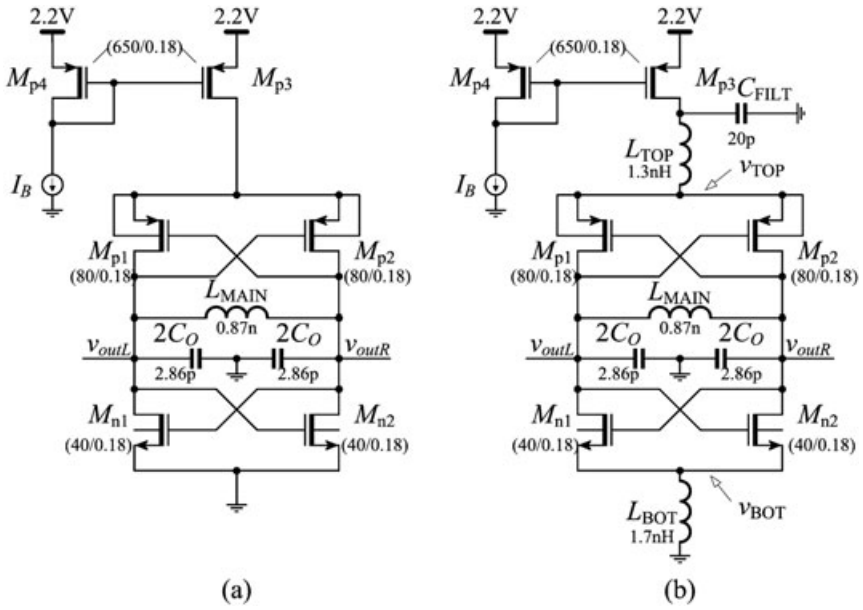

Figure 1. Top-biased 1L oscillators: (a) main oscillator topology (1L); (b) oscillator topology enhanced with two bias inductors (1L + 2bL).

Figure 3 shows the D-Colpitts build with the same passive and active components as the 1 L and 2 L topologies. The resonance-tank inductance is doubled (two inductors L_{MAIN}) to achieve the same oscillation amplitude with the same switching transistors and similar power consumption. The feedback ratio n is around 1/3 ($n \approx C_{fb}/(C_{fb}+2C_F)$), which is an optimum value for achieving low phase noise [7]. The bias network is built with NMOS transistors with the same size as the PMOS biasing transistors in Figure 1 and Figure 2. The oscillation frequency is adjusted with the tank capacitance (C_1 and C_2) to be near 4 GHz. The presence of the feedback capacitors in the D-Colpitts architecture has two effects: 1) the effective tank capacitance is reduced and, correspondingly, the achievable tuning range and 2) a larger MOS transconductance is needed to create the required loop gain for sustained oscillations.

The design issues and the phase noise performance of different *LC* oscillators are compared in several works, among which the work of Andreani performs an analytical comparison based on the ISF theory and draws conclusions about the oscillator operation [7,9,10]. The oscillator phase noise is linked to the properties of the resonance tank, the generated voltage swing, and the transistor properties as in [7,10]

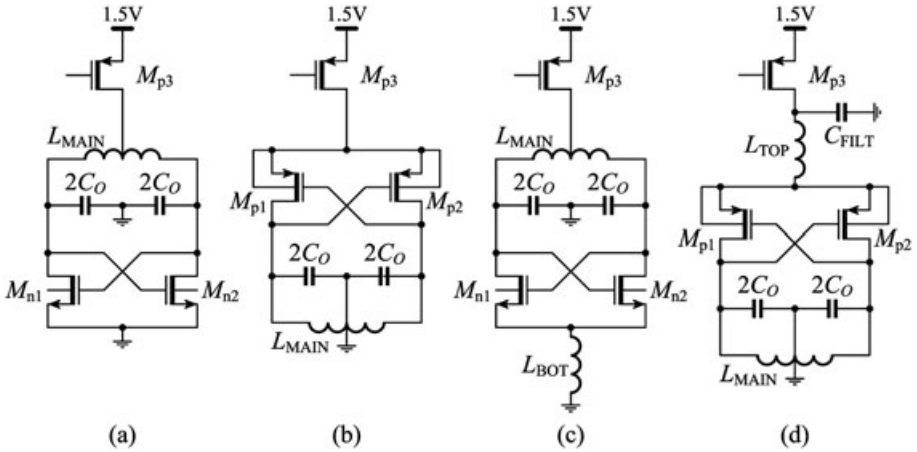

Figure 2. Top-biased 2 L oscillator modifications using: (a) NMOS cross-coupled pair; (b) PMOS pair; (c) NMOS pair and bias inductor L_{BOT}; (d) PMOS pair and bias inductor L_{TOP}.

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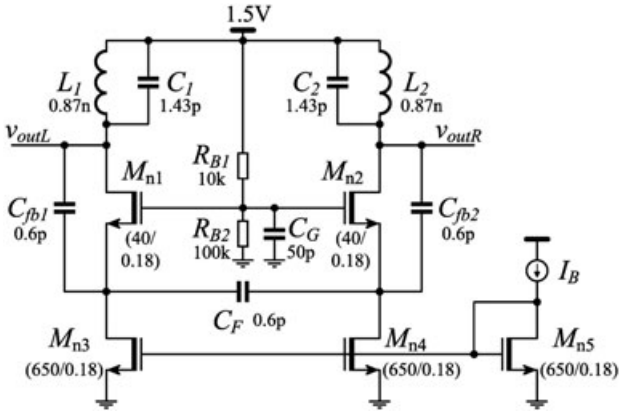

Figure 3. Schematic of differential Colpitts.

$$\mathcal{L}_{1L}(\Delta\omega) = 10\log\left[\frac{k_B T}{C^2 \cdot A_{1L}^2 \cdot R \cdot \Delta\omega^2}\left(1 + \frac{\gamma_n + \gamma_p}{2}\right)\right], \tag{1}$$

$$\mathcal{L}_{2L}(\Delta\omega) = 10\log\left[\frac{k_B T}{C^2 \cdot A_{2L}^2 \cdot R \cdot \Delta\omega^2}(1 + \gamma_n)\right], \tag{2}$$

$$\mathcal{L}_{COLP}(\Delta\omega) = 10\log\left[\frac{k_B T}{2 \cdot C^2 \cdot A_{COLP}^2 \cdot R \cdot \Delta\omega^2}\left(1 + \gamma_n \frac{1-n}{n}\right)\right], \tag{3}$$

where $\mathcal{L}$ is the oscillator phase noise, k_B is the Boltzmann constant, T is the absolute temperature, C is the equivalent tank capacitor, A is the amplitude of the resonator voltage, R is the equivalent tank resistance at the oscillation frequency, $\Delta\omega$ is the offset frequency, $\gamma_{n(p)}$ is the channel noise factor for NMOS (PMOS) transistors, while the subscripts (1 L, 2 L and COLP) denote the corresponding oscillator.

The 1 L oscillator produces double voltage swing for a given bias current in a current-limited regime. Since the noise contributed by the active transistors in the two architectures is essentially the same (the multiplying term in (1) and (2)), an operation with constant bias current results in 6-dB lower phase noise displayed by the 1 L oscillator ($\mathcal{L}_{1L}(\Delta\omega) = \mathcal{L}_{2L}(\Delta\omega) - 6$ dB) [10]. However, the maximum achievable FoM for the two oscillators is the same ([10], eq. (44)). The 2 L-VCO requires twice as much current to produce the same voltage swing, but needs approximately half of the power supply; thus, the consumed power is almost the same [10]. The derivation of (1) assumes that the tank capacitance is connected between the two oscillator nodes, and there is no capacitance connected between the oscillator nodes and ground [10]. A severe departure of (1) from the simulated phase noise is shown in [10] when this condition is not satisfied. In practical VCOs, however, the tuning varactor and/or switched-capacitor bank may contribute to a big portion of the tank capacitance being connected to ground. For instance, the *off*-state capacitance of a switched-capacitor bank is connected between one of the *LC* resonator nodes and ground, i.e. the departure of (1) from the simulated phase noise is expected at the high end of the VCO tuning range. A comparison between D-Colpitts and cross-coupled oscillator is given in [2,7], where the phase noise of a D-Colpitts is expressed as a function of its design parameters with (3). The bias noise is excluded from (3), and n is the feedback ratio formed by the capacitors in the Colpitts oscillator.

A comparison between the phase noise equations (1)–(3) of the three topologies leads to important conclusions. The 1 L and the 2 L oscillators produce the same phase noise at a given resonator voltage swing ($A_{1L} = A_{2L}$), assuming similar noise properties of the NMOS and PMOS transistors ($\gamma_n \approx \gamma_p$), which explains why they often achieve the same performance in practice. On the other hand, the transistors in the D-Colpitts architecture contribute more noise (the multiplier in (3)) compared to its competitors, which limits the D-Colpitts performance. Other second-order effects, such as velocity

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saturation and large overdrive, make the phase noise performance of the Colpitts topology even worse [7]. Recently, a further development of the Colpitts topology led to the so-called Class-C oscillator [2], which takes advantage of a second feedback and realizes Class-C operation to achieve excellent FoM performance. The evaluation of the Class-C topology is outside the scope of this work, as not much experience has been gained in the literature, and there are only a few design examples using this topology.

3. OBTAINING THE ROOT TRAJECTORIES OF LARGE-SIGNAL OSCILLATORS

The TVRL computes the system roots for one oscillation period and evaluates their trajectories [6] using the steady-state time-domain periodic solution obtained by the Cadence SpectreRF simulator [11]. The circuit is linearized for all instants of the periodic solution, and the roots of the characteristic equation are computed. The active-device linearization is done by SpectreRF. The roots are computed with the QZ method applied to the **G** and **B** nodal matrices. The behavior of large-signal oscillators is analyzed using the trajectory of the main complex-conjugated pair λ_0. The analysis using the λ_0 trajectories highlights the differences between the 1 L and the 1 L + 2bL oscillator in [6]. The method explains the phase noise improvement achieved by the 1 L + 2bL oscillator through the limited swing of λ_0 in the right-half plane (RHP) and in the left-half plane (LHP) for a given voltage swing. The λ_0 trajectory goes deeper into the LHP due to higher resonator loading, which consequently deteriorates the oscillator phase noise. On the other hand, the λ_0 trajectory goes deeper in the RHP with bigger negative conductance, which is related to bigger transistor transconductance, higher device noise and results in higher phase noise.

The goal of this section is to analyze the behavior of the roots for simplified *LC*-oscillator models obtained in large-signal conditions. The root trajectory evaluation for the simplified models helps to explain the root behavior of the actual oscillators. The simplified models correspond to real oscillator topologies, where the active transistors are replaced with variable conductances modeling the large-signal nonlinearities of the transistor. Typically, a closed-form root-locus analysis is applied to the analysis of simplified oscillators, but the closed-form analysis often requires second-order polynomial [12,13], which poses serious limitations to the circuits that can be analyzed. Instead of closed-form root-locus analysis, this section utilizes the QZ computation method for precise root evaluation even for simplified oscillator models, and thus it requires no further simplifications needed to arrive at second-order polynomial.

3.1. The RLC tank model

The simplest model of an oscillator is a parallel *RLC* tank with a conductance g_0 ($g_0 = 1/R$) accounting for both the tank losses and the negative conductance created by a cross-coupled pair. The complex-conjugated pair corresponding to the second-order *RLC* tank is

$$\lambda_{1,2} = -g_0/(2C_0) \pm j\sqrt{1/(L_0C_0) - g_0^2/\left(4C_0^2\right)}. \tag{4}$$

The magnitude of the root is constant and independent of g_0 ($|\lambda_{1,2}| = (L_0C_0)^{-1/2}$). During large-signal operation, the oscillator injects energy into the *RLC* tank for part of the period ($g_0 < 0$), while it dissipates energy for the rest of the period ($g_0 > 0$) [12]. Varying g_0 forces the complex-conjugated pair to travel in a circle with a radius of $(L_0C_0)^{-1/2}$ ([14], Figure 3.11).

Figure 4(a) shows a more realistic model of a cross-coupled *LC* oscillator with differentially connected capacitors with their mid-point grounded, and conductances g_1 and g_2 associated with the cross-coupled-pair transistors. The topology in Figure 4(a) is characterized by a third-order system having one real pole and a complex-conjugated pair given by the characteristic polynomial

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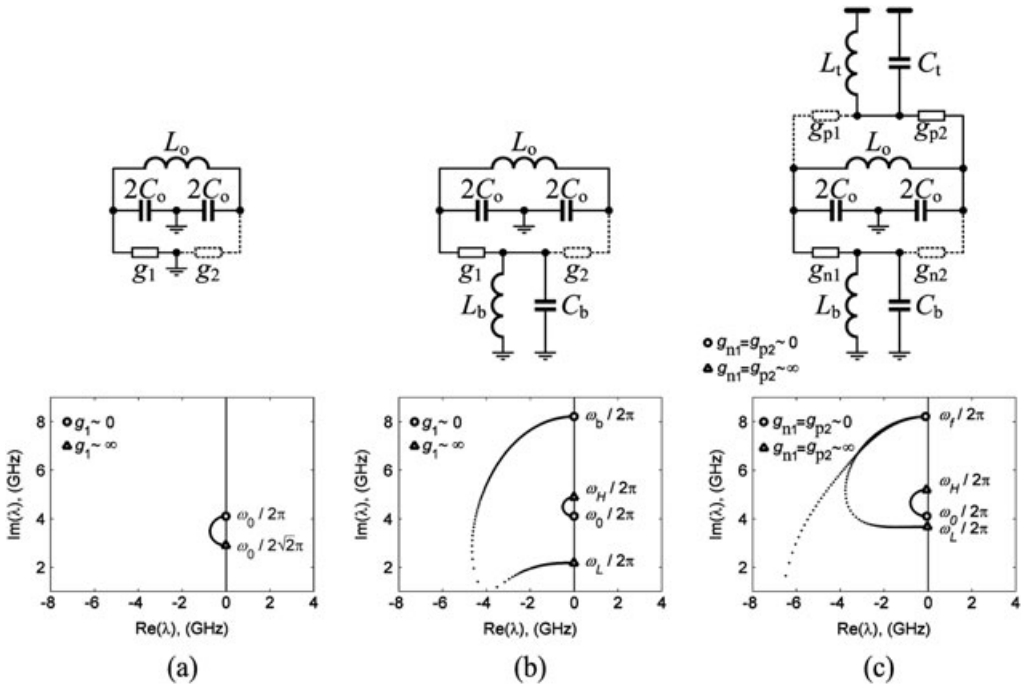

Figure 4. Simplified oscillator models and their root-loci obtained with variable conductance g: (a) *RLC* tank with grounded capacitors and conductances; (b) grounded *RLC* tank with L_bC_b filter; (c) double-cross-coupled oscillator model with two *LC* filters.

$$P = s{\cdot}L\left(s^2{\cdot}C^2 + s{\cdot}2gC + g^2\right) + s{\cdot}2C + 2g = 4\left(s{\cdot}\frac{C}{2} + \frac{g}{2}\right)\left(s^2{\cdot}L\frac{C}{2} + s{\cdot}\frac{g}{2}L + 1\right), \tag{5}$$

where $g = g_1 = g_2$ and $C = 2\,C_0$. The complex-conjugated pair is identical to (4) and its trajectory is defined by a circle in the complex plane. The real pole is $\lambda_3 = -g/C$, which is strictly negative for positive values of g.

However, the fully differential condition $g_1 = g_2$ is satisfied only at the oscillator start-up and near the voltage zero-crossings. During large-signal operation, one of the MOS transistors goes in the triode region ($g_1 >> 0$), the other in the cut-off region ($g_2 \approx 0$), and the cross-coupled pair does not generate negative conductance. The root trajectories of the third-order system can be evaluated by varying g_1 corresponding to one MOS transistor operating in the triode region. Since a closed-form solution of an arbitrary third-order polynomial is hard to comprehend [15], the root trajectories are obtained numerically, and we evaluate the extreme cases of g_1 ($g_1 = 0$ and $g_1 = \infty$), while keeping $g_2 = 0$. When $g_1 = 0$, the resonance tank consists of the main inductor L_0 and the two capacitors forming a complex conjugated pair at $\lambda_{1,2} = \pm j\sqrt{1/(L_0C_0)}$ and a real root at $\lambda_3 = 0$. When $g_1 = \infty$, g_1 shortens one of the $2\,C_0$ capacitors, which doubles the tank capacitance of the *RLC* tank and moves the complex conjugated pair to $\lambda_{1,2} = \pm j\sqrt{1/(2L_0C_0)}$. Compared to the simple *RLC* tank, where $g_0 = \infty$ transforms the complex-conjugated pair into one root at the origin and another one at infinity, the grounded *RLC* tank features root trajectory transforming one complex pair into another complex pair with $\sqrt{2}$ lower frequency. The root trajectory in this case does not follow the circle defined in the parallel *RLC* tank. The imaginary part of $\lambda_{1,2}$ drops with the MOS transistor entering the triode region during large-signal operation.

3.2. Single cross-coupled pair with LC filter

The oscillator model shown in Figure 4(b) approximates the large-signal operation of a cross-coupled pair degenerated with an L_bC_b filter. The conductances g_1 and g_2 are relatively small when the

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transistors are in the active region, and the resulting two complex-conjugated pairs are determined by the two *LC* tanks ($\omega_{1,2}$=$\omega_0 = (L_0C_0)^{-1/2}$ and $\omega_{3,4}$=$\omega_b = (L_bC_b)^{-1/2}$). Negative conductance is applied across the main resonator and forces oscillations at ω_0. During large-signal operation, however, g_1 becomes significant, while g_2 becomes very small, modeling the triode and the cut-off region respectively. This scenario corresponds to two *LC* tanks coupled with a conductance, which results in a fourth-order resonator with complicated dependence of the circuit roots from the passive components. In the extreme case of g_1 representing short circuit and g_2 representing open circuit, the pole frequencies associated with the fourth-order resonator are [16]

$$\omega_{L,H}^2 = \frac{L_bC_1 + L_0C_2 + L_bC_2}{2L_0L_bC_1C_2} \pm \frac{\sqrt{(L_bC_1 + L_0C_2 + L_bC_2)^2 - 4L_0L_bC_1C_2}}{2L_0L_bC_1C_2}, \tag{6}$$

where $C_1 = C_\mathrm{b} + 2\,C_0$ and $C_2 = 2\,C_0$. Thus, under a large-signal condition, the original pole frequencies ω_0 and ω_b are transformed into ω_L and ω_H given by (6). The values of ω_0 and ω_b are design parameters to achieve respectively the desired oscillation frequency and proper noise filtering ($\omega_b \approx 2\omega_0$) [1], but the frequencies ω_L and ω_H are a complex function of the passive components building the two resonators.

In Figure 4(b) are plotted root trajectories obtained by varying g_1 from zero to infinity, which demonstrate the evolution of ω_0 and ω_b into ω_L and ω_H ($L_0 = 1$nH, $C_0 = 1.5$ pF, $L_\mathrm{b} = 0.5$nH, $C_\mathrm{b} = 0.75$ pF). The main root λ_0 approaches one of the angular frequency defined by the fourth-order tank (6). The approached frequency is usually ω_H with reasonable component values ($\omega_H > \omega_0$, Figure 6(b)), while ω_b transforms to ω_L.

The root trajectories shown in Figure 4(b) could be explained as follows. When g_1 increases, part of the tank capacitance ($2\,C_0$) becomes connected to the filtering network $L_\mathrm{b}C_\mathrm{b}$ and λ_b drops. The 'vanishing' part of the tank capacitance forces the imaginary part of λ_0 to increase. Thus, the presence of $L_\mathrm{b}C_\mathrm{b}$ filter causes Im(λ_0) to rise from its nominal value as the active devices enter the triode region, which is opposite to the roots behavior in cases without $L_\mathrm{b}C_\mathrm{b}$. The root trajectories in Figure 4(b) are obtained with large conductance variations; thus, only part of root-loci can be observed in practice (λ_0 will never reach ω_H). Another important observation is that high values of g_1 do not severely harm the oscillator operation when an $L_\mathrm{b}C_\mathrm{b}$ filtering is used. The main root λ_0 goes deep into the LHP in the case without *LC* filter, and its *Q*-factor deteriorates drastically. In contrast, the use of $L_\mathrm{b}C_\mathrm{b}$ filter limits the excursion of λ_0 in the LHP and preserves the tank *Q*-factor. The degree of *Q*-factor preservation depends on the specific values used in $L_\mathrm{b}C_\mathrm{b}$, with bigger L_b inductance corresponding to better *Q*-factor preservation.

3.3. Double cross-coupled pair with LC filters

A double cross-coupled-pair oscillator may utilize two *LC*-filters to degenerate both cross-coupled pairs, which is modeled with the circuit in Figure 4(c), where the MOS transistors are replaced with conductances $g_{\mathrm{n}1,2}$ and $g_{\mathrm{p}1,2}$. The effect of the MOS transistor conductance can be neglected ($g_{\mathrm{n}1,2}$ and $g_{\mathrm{p}1,2}$) at the oscillator start-up, and the roots are

$$\omega_0 \cong (L_0C_0)^{-1/2}; \omega_b \cong (L_bC_b)^{-1/2}; \omega_t \cong (L_tC_t)^{-1/2}. \tag{7}$$

During the maxima of the voltage swing, two of the conductances are large ($g_{\mathrm{n}1}$ and $g_{\mathrm{p}2}$), while the other ones are negligible ($g_{\mathrm{n}2} \approx g_{\mathrm{p}1} \approx 0$). One of the tank capacitors, $2\,C_{0,}$ is connected in parallel to the $L_\mathrm{b}C_\mathrm{b}$ filter and the second $2\,C_0$ capacitor is in parallel with the L_tC_t filter in the extreme case of $g_{\mathrm{n}1} \approx g_{\mathrm{p}2} \approx \infty$. The new systems poles include two complex-conjugated pairs given by

$$\omega_{L,H}^2 = \frac{A}{2B} \pm \frac{\sqrt{A^2 - 4B(L_0 + L_b + L_t)}}{2B}, \tag{8}$$

where

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$$\begin{aligned} A &= L_0L_bC'_b + L_0L_tC'_t + L_bL_t\left(C'_b + C'_t\right) \\ B &= L_0L_bL_tC'_bC'_t \\ C'_t &= C_t + 2C_0; C'_b = C_b + 2C_0 \end{aligned}.$$

The numerically evaluated root trajectories are presented in Figure 4(c) for a set of passive components in order to demonstrate the effect of the two *LC* filters. Ideal passive components are used with values such that $\omega_b=\omega_t=2\cdot\omega_0$ ($L_0=1$nH, $C_0=1.5$ pF, $L_b=L_t=0.5$nH, $C_b=C_t=0.75$ pF). The imaginary part of λ_0 increases, due to the fact that part of the tank capacitance is transferred to the filtering network, and λ_0 reaches ω_H. The poles associated with the *LC* filters (ω_b and ω_t) drop in frequency and they head towards ω_L and the origin. The behavior of λ_0 is similar to the trajectory presented in Figure 4(b) for the single cross-coupled-pair topology. Since λ_0 and the filter poles travel in different directions, the frequency relationship needed to achieve filtering functions ($\omega_b \approx 2\omega_0$ [1]) is not satisfied, and the filtering becomes less effective during the maxima/minima of the oscillator waveform.

3.4. Differential Colpitts

Figure 5(a) shows a simplified large-signal model of the D-Colpitts, where $g_{1,2}$ are the $M_{n1,2}$ drain–source conductances and $g_{3,4}$ are the drain–source conductances of the bias transistors $M_{n3,4}$. The conductances g_1–g_4 can be neglected when all transistors are in the active region, and the frequencies of the two complex-conjugated pole pairs are

$$\omega_{1,2}^2 = \frac{1}{L_0(C_0+2C_a)}; \omega_{3,4}^2 = \frac{1}{L_0C_0}, \tag{9}$$

where $C_a = C_{f1}||C_F||C_{f2}$. If the main transistor M_{n1} goes to the deep triode region ($g_1>>0$), its drain–source conductance shortens the feedback capacitor C_{f1}. In the extreme case of $g_1=\infty$, the expression of the pole frequencies is again given by (9), but $C'_a = C_F||C_{f2}$. Thus, the oscillation frequency $\omega_{1,2}$ decreases, while $\omega_{3,4}$ is not affected ($\omega_{3,4}$ is independent of g_1). If the bias transistor M_{n3} goes to the deep triode region ($g_3>>0$), then the feedback between the two oscillator sections is effectively broken, leading to complex-conjugated roots at

$$\omega_{1,2}^2 = \frac{1}{L_0\left(C_0+C_{fb1}\right)}; \omega_{3,4}^2 = \frac{1}{L_0\left(C_0+C_{fb2}||C_F\right)}, \tag{10}$$

A variation of g_3 affects both poles, with the main pole going higher in frequency. It is interesting to observe that the main pole follows the part of circuit which still has a working biasing circuitry. The lower frequency pole ($\omega_{1,2}$) does not provide conditions for oscillations, since the increase of g_3

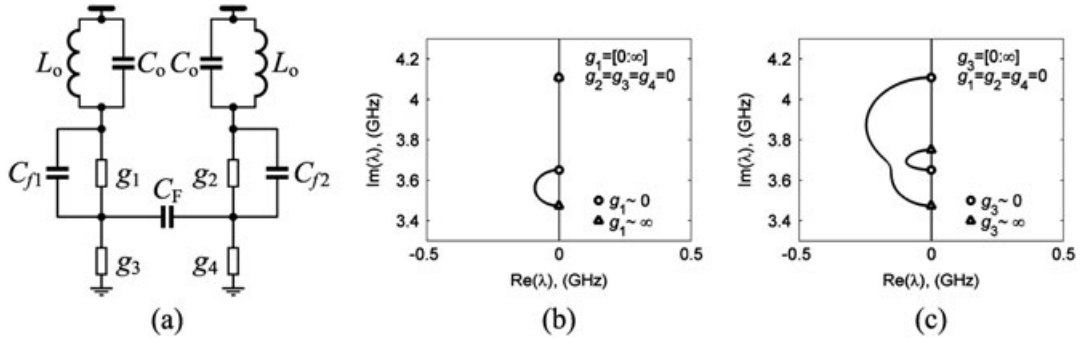

Figure 5. Large-signal D-Colpitts: (a) simplified model of large-signal conditions; (b) root-loci obtained by varying g_1; (c) root-loci obtained by varying g_3.

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shortens the feedback to the M_{n1} transistor. The behavior of the two cases is demonstrated in Figure 5 (b) and Figure 5(c), where $L_0 = 1\text{nH}$, $C_0 = 1.5\,\text{pF}$ and $C_F = C_{f1} = C_{f2} = 0.6\,\text{pF}$.

However, it should be noted that active transistors in the D-Colpitts topology do not enter as deep into the triode region (shown in the next section) as the transistors in the cross-coupled topologies, and the above behavior can be hardly observed in practice. Furthermore, the change of g_1 and g_3 is correlated with the drain and source node voltages of M_{n1}, which are almost in phase, and they force both conductances to increase or decrease at the same time. Since g_1 and g_3 move the main pole in different directions (shown in Figure 5(b) and Figure 5(c)), the correlated change of g_1 and g_3 helps to keep small variations of the main pole under large-signal conditions.

4. OSCILLATOR START-UP

4.1. Main root trajectory at start-up as a function of I_B

The root-locus method is an efficient tool to evaluate the start-up behavior of oscillators [17,18]. As the roots evaluation using TVRL is based on circuit-description matrices and accounts for the full complexity of the oscillator, the method avoids typical feedback-loop-breaking operations [6]. The complex-conjugated pair with the most positive real part, which crosses the imaginary axis of the *s*-plane, is the one responsible for the oscillations.

The root loci of the 1 L and 2 L architectures from Figure 1 and Figure 2 are plotted in Figure 6(a) with varying I_B. The main root λ_0 enters the RHP as the bias current I_B is increased, which corresponds to a larger negative conductance generated by the cross-coupled pair(s). The 1 L oscillator requires smaller I_B to cross the $j\omega$-axis due to the second cross-coupled pair. However, the second cross-coupled pair slightly increases the parasitic capacitance connected to the resonance tank and $\text{Im}(\lambda_0)$ is decreased. The operation of the 1 L and the 2 L oscillator can be assumed as small-signal and differential at start-up. The common node of the cross-coupled pair is connected to virtual ground, and the impedance connected to this node has no effect on the start-up. This is confirmed in Figure 6(a), where the start-up root-loci for the oscillators employing bias inductors overlap with those without inductors. Therefore, the bias inductors affect mostly the large-signal oscillator operation, and its benefits should be evaluated under such operation.

The start-up root loci for the D-Colpitts is illustrated in Figure 6(b) for different feedback ratio n realized by the feedback capacitor C_F. The larger feedback ratio increases the loop gain and it requires smaller MOS transconductance g_m, with respectively smaller I_B to meet the oscillation conditions. As C_F is decreased to achieve larger n, the effective tank capacitance is also decreased, which leads to higher oscillation frequency. The start-up behavior of the D-Colpitts oscillator is

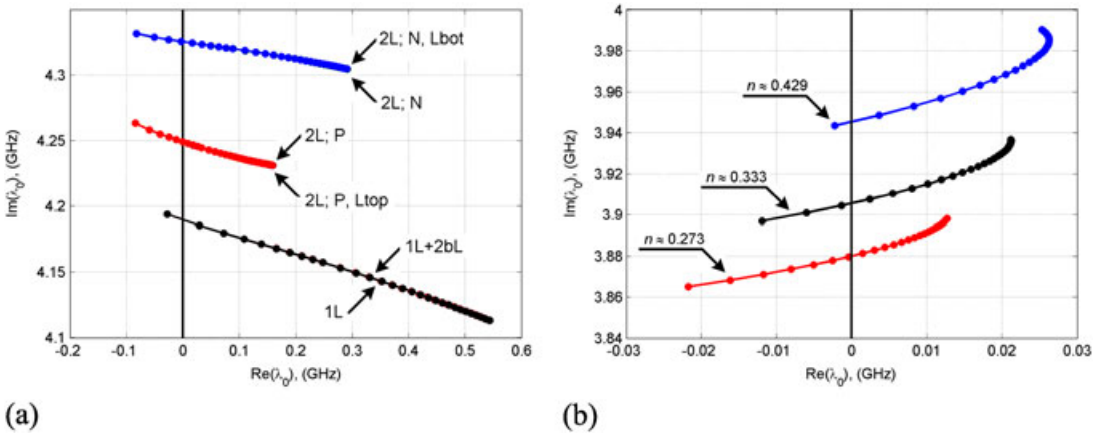

Figure 6. Trajectories of the main root at start-up as a function of I_B ($I_B = 0.1\,\text{mA}$–$5.0\,\text{mA}$) for: (a) cross-coupled oscillators; (b) D-Colpitts with different feedback ratios n.

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essentially different from the negative-resistance oscillators, because when using large g_m, the root-locus starts returning to the LHP [17].

4.2. *Proof of sinusoidal operation*

The existence of a complex-conjugated pair in a RHP is a necessary condition to start oscillations, but other undesired phenomena might also occur [19,20]. Undesired phenomena could be relaxation oscillations, chaos or even latch-up. A typical reason for relaxation oscillation is the presence of real pole in the RHP. Chaos and latch-up, on the other hand, might be triggered by specific nonlinearity or hysteresis produced by the active devices. In this subsection, we show that these undesired phenomena are avoided and the investigated oscillators produce sinusoidal waveforms.

Figure 7(a) shows the complete root-locus map of the 1 L + 2bL oscillator obtained at start-up with varying I_B, while Figure 7(b) shows the root trajectories at large-signal condition for one oscillation period. In both cases, only the main complex-conjugated pair λ_0 enters the RHP, and all real roots remain in the LHP. Thus, relaxation oscillations cannot be initiated at start-up, neither are they produced under large-signal conditions. Similar plots are obtained for all oscillator topologies presented in Figure 1– 3.

For further analytical proof, the condition $g_m \cdot r_L \geq 1$ required to obtain relaxation oscillations [19] is investigated, where g_m is the transconductance of the cross-coupled pair transistor and r_L is the series resistance of the inductor accounting for all tank losses. Note that the condition above implies a real pole in the RHP [19]. Using simulations of the complete *LC* resonator, we obtained r_L of approximately 3.32 Ω. Thus, the transistor g_m should be bigger than 300 mS in order to initiate relaxation oscillations. In the start-up root-loci plots shown in Figure 6, the maximum transistor g_m obtained for $I_B = 5$ mA does not exceed 200 mS. Furthermore, an oscillator operation with such a large current is somewhat impractical since the voltage swing reaches the power supply limits and unnecessary distortions are generated. Nevertheless, the above calculation shows a good safety margin that rules out relaxation oscillations.

Latch-up, on the other hand, can be triggered by the nonlinearity of the cross-coupled pair. Figure 8 (a) shows a piecewise approximation of the cross-coupled pair nonlinearity used for the analysis of latch-up in [19] and [20]. The piecewise approximation of the nonlinearity is divided into three segments: an inner segment modeled by a small-signal conductance g_0 and two outer segments modeled by a small-signal conductance g_1. The negative conductance g_0 compensates the tank losses in the inner segment of the nonlinearity and initiates oscillations. The positive conductance g_1 introduces losses to the resonance tank in the outer segments of the nonlinearity. The oscillator will unavoidably enter the outer segments as the oscillation amplitude grows in the inner segment. Latch-up will occur if the equilibrium points of the outer segment are real, i.e. the equilibrium point lies in the same outer segment, and the oscillator never returns to the inner segment. The possibility

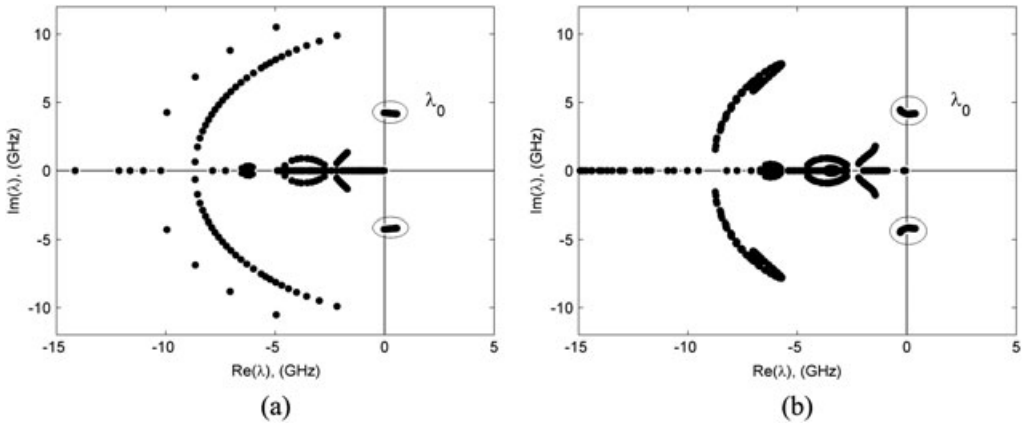

Figure 7. Full root-locus map at start-up for the 1 L + 2bL oscillator at: (a) start-up condition under I_B variations; (b) large-signal condition ($V_{PP} = 1.5$ V) as a function of time.

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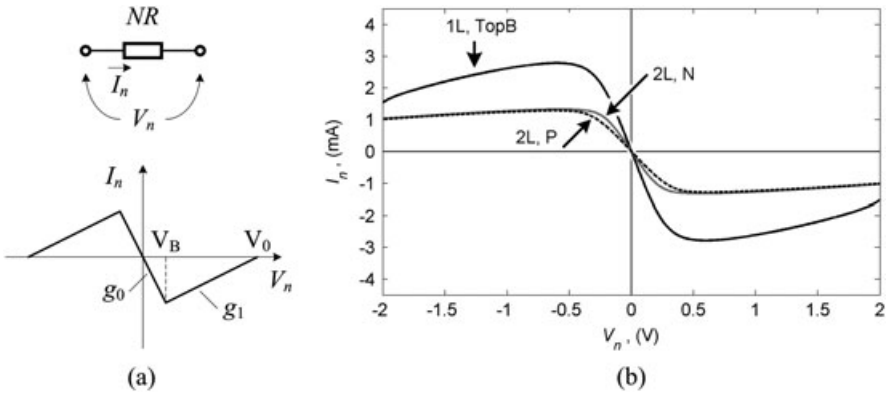

Figure 8. Cross-coupled pair nonlinearity: (a) simplified piecewise approximation; (b) simulated nonlinearity for the 1L oscillator and 2 L oscillator with NMOS and PMOS transistors.

for latch-up is studied by evaluating the position of the equilibrium point of the outer segment. Figure 8 (b) shows the simulated nonlinearity of the 1 L oscillator, and the 2 L oscillator using NMOS and PMOS transistor, all biased with $I_B = 2$ mA.

The equilibrium points of the other segments are equal to $\mp m\alpha/(m-1+\alpha)$ [20], where $m = V_0/V_B$, $\alpha = r_L/r$, $r = 1/g_0$, r_L is the inductor series resistance, V_0 and V_B are defined in Figure 8(a). The simulated nonlinearity of the 1 L oscillator is approximated with $V_0 = 4.14$ V, $V_B = 0.31$ V, $g_0 = 10.22$mS and $r_L = 3.32\Omega$. The calculated equilibrium point of the outer segments of the 1 L oscillator is approximately 36.5 mV, which is a magnitude below V_B. The calculations made for the 2 L oscillators are based on the 4D model [19], which is specially tailored to 2 L oscillators using two identical *LC* tanks. The equilibrium points of the 4D model in the outer segments are $\pm 0.5/(1+Q^2/\Delta_g)$, where Q is the tank quality factor and $\Delta_g = g_1/g_0$. The calculated equilibrium point of the outer segments for the 2 L-N oscillator is approximately 20.2 mV with $V_B = 0.245$ V, while the calculation for the 2 L-P oscillator shows an equilibrium point at approximately 14.5 mV with $V_B = 0.330$ V. In all three cases, the equilibrium points of the outer segments are not real, and therefore potential latch-up is avoided. Reference [19] suggests a minimization of total-harmonic distortions (THD) by reducing Δ_g, which can be effectively achieved by employing a current-mirror biasing of the cross-coupled pair. The current-to-voltage transfer function of a cross-coupled pair saturates at $I_B/2$ when ideal current mirror is used [21], which implies $g_1 \approx 0$ and $\Delta_g \approx 0$. Thus, a current-mirror biasing reduces THD and greatly omits the possibilities for latch-up by forcing the equilibrium points of the outer segments to be very close to the origin. The nonlinearity needed to obtain bounded oscillations is often embedded within the employed active devices, which limits the possibility for nonlinearity optimization and it requires an examination of the latch-up conditions. A separation of the critical nonlinearity from the oscillator structure is proposed in [22], which allows nonlinearity optimization with the target to avoid undesired oscillator behaviors.

A hysteresis in the nonlinear circuit is another possible reason for triggering a latch-up in oscillators [20]. The simulated nonlinearities shown in Figure 8(b) display no hysteresis. Simulations of the D-Colpitts oscillator also show no hysteresis, because there is no *dc* feedback that could eventually trigger such behavior. An analysis of Colpitts oscillator using the piecewise approximation approach is not done here, as the negative resistance of the Colpitts oscillator is created by the feedback capacitors, which is frequency dependent and does not require active-device nonlinearity.

SpectreRF transient simulations are performed for each evaluated oscillator in order to confirm that the oscillators generate proper sinusoidal signal. Figure 9(a) shows the start-up envelopes of the 1 L oscillator with $I_B = 2$ mA and $I_B = 5$ mA. The steady-state oscillations are demonstrated in Figure 9 (b) with THD computed for the first 10 harmonics. As is seen from the plots, sinusoidal signals are produced for a large range of bias currents with sensible distortions (THD of a square-wave signal is above 40%). All the investigated oscillators perform similarly with THD not exceeding 5% even for voltage swings reaching the power supply rails.

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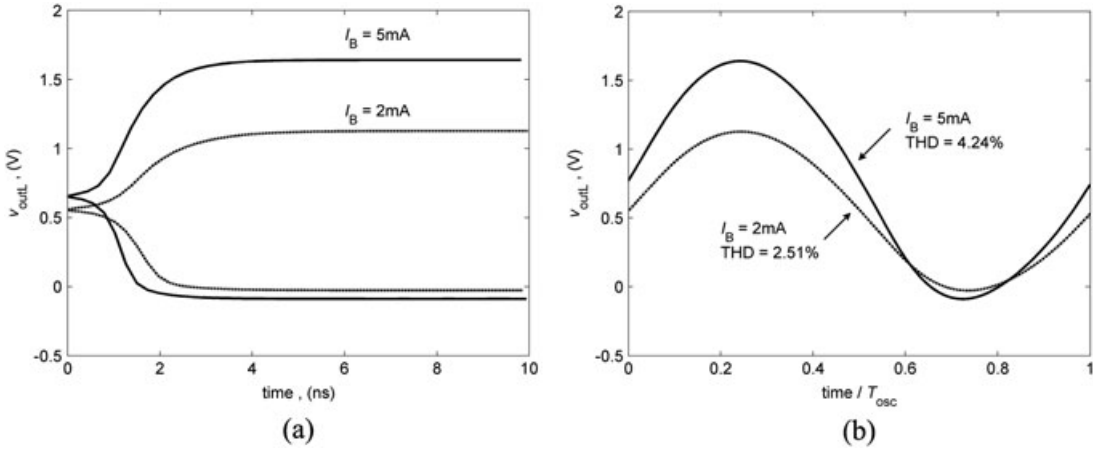

Figure 9. Transient response of the 1L oscillator for $I_B = 2\,\text{mA}$ and $I_B = 5\,\text{mA}$: (a) start-up envelope; (b) steady-state output voltage.

5. ACTIVE-DEVICE OPERATING TRAJECTORY COMPARISON

The large-signal operation of the *LC*-oscillator forces the transistors to operate both in linear and in nonlinear regions, which is seen as a variation of their bias conditions. The variable bias condition in periodic circuits forms a closed trajectory. Different oscillator topologies force different bias trajectories depending on the active device connection and on the voltage swing. The goal of this section is to compare the bias trajectories of the active devices imposed by the different oscillator topologies. The bias trajectory comparison is done for the same voltage swing generated by the oscillators ($V_{PP} = 1.2\,\text{V}$).

The bias trajectory of the active NMOS transistors in the top-biased 2 L oscillator (Figure 10(a)) displays an operation in all regions – cut-off, triode and active region. The sinusoidal differential output is applied to the transistors' drain and source, and thus it forces symmetrical bias trajectory for the rising and the falling part of the waveform. Among the other oscillators, the NMOS transistors of the top-biased 2 L oscillator enter deepest in the triode region, which corresponds to the most excessive losses and resonator loading. The additional inductor L_{BOT} limits the transistor operation in the triode region and respectively limits excessive losses. The triode operation is limited as an absolute value of the on-resistance, as well as for a reduced part of the period. However, the phase of the v_{BOT} node voltage is delayed with respect to the resonator voltages. The delayed phase of v_{BOT} causes an asymmetric bias trajectory and asymmetric root-locus during the rising and the

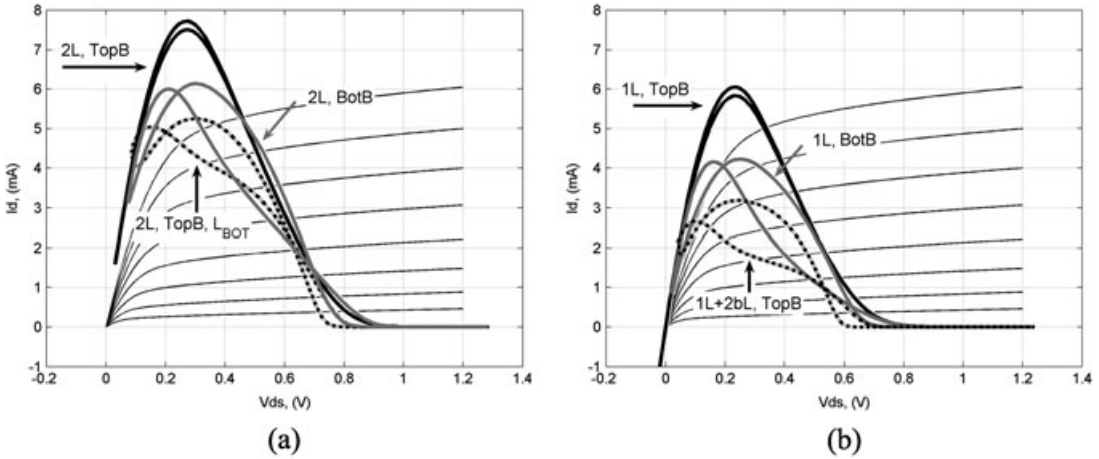

Figure 10. NMOS bias trajectory comparison between: (a) 2L oscillator modifications operating with $V_{PP} = 1.2\,\text{V}$; (b) 1L oscillator modifications operating with $V_{PP} = 1.2\,\text{V}$.

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falling part of the waveform. The asymmetry of the waveform gives a rise to the AM–PM frequency up-conversion [23,24]. Thus, the phase noise improvement achieved by the biasing inductor L_{BOT} is slightly reduced by the increased AM–PM noise up-conversion. The effect of the current mirror on the bias trajectory is similar to the effect caused by L_{BOT}. Although the transistor enters deeper in the triode region compared to transistors in the modification using L_{BOT}, the impedance of the current mirror acts as degeneration and does not allow excessive resonator losses. The node voltage v_{BOT} is delayed with respect to the resonator voltages, causing asymmetric operating point and asymmetric root-locus trajectory.

The bias trajectory comparison between the 1 L oscillator modifications is shown in Figure 10(b). The main transistors in the 1 L oscillator enter deep in the triode and cut-off region. The bias trajectory in the triode region is limited when using bias inductors or current mirror, but both techniques cause asymmetric bias trajectory. The bias trajectory of the basic 1 L oscillator may go even into the fourth quadrant when the drain voltage becomes smaller than the source voltage.

In comparison, the bias trajectory of the D-Colpitts is essentially different from the other oscillators obtained for the same voltage swing. Figure 11(a) shows the simulated node voltages and the drain current of M_{n1} for 1.2 V voltage swing, and Figure 11(b) shows the corresponding M_{n1} bias trajectory. The drain–source voltage and the drain current of M_{n1} are shifted with respect to the oscillator output $V_{d,n1}$. Points 'A' and 'B' in Figure 11 are two example instants with equal V_{ds} voltages in the falling and rising part of the output voltage. The M_{n1} drain current has different values for 'A' and 'B' due to the asymmetry of V_{ds} and I_d. The bias trajectory therefore forms a loop with large opening, underlining this asymmetry.

As shown in Figure 11(b), the M_{n1} transistor stays mostly in the active region, and only slightly enters the triode and cut-off region. Since the feedback voltage applied to the source of M_{n1} is almost in-phase with the resonator output, only a portion of the output voltage is applied to the transistor as drain–source voltage. The scaled drain–source voltage depends on the feedback ratio n. This feature of the Colpitts oscillator helps the active device to operate mostly in the active region for the same voltage swing. This advantage of the D-Colpitts can be utilized in advanced CMOS processes, where the maximum allowed voltages across the transistor limit the oscillator voltage swing. As shown in [25], the specifics of the oscillator topology can allow generation of large voltage swing without driving the transistors into breakdown regions.

6. OSCILLATOR COMPARISON USING POWER-CONVERSION FACTOR

The analytical derivations of voltage swing as a function of design parameters assume current-limited operation [1,7,10]. These derivations become inadequate and depart from actual oscillator behavior as

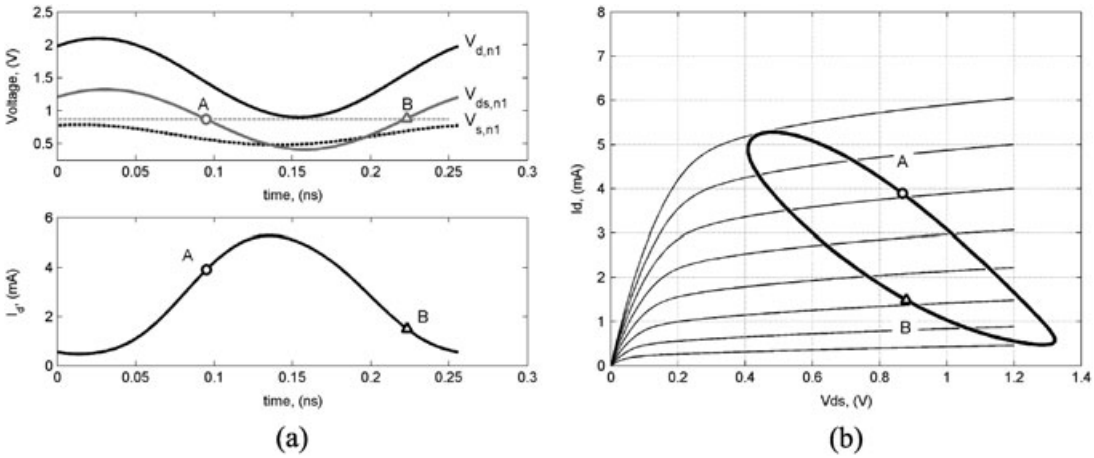

Figure 11. D-Colpitts bias trajectory evaluation at $V_{PP} = 1.2$ V: (a) node voltages and the drain current of M_{n1}; (b) M_{n1} bias trajectory.

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the voltage swing approaches the power supply rails. Reference [26] obtains in analytical form the steady-state oscillations in large-signal *LC* VCO, but the circuit model and transistor operation are simplified. The nonlinearities involved in the voltage-limited operation make it hard to derive precise analytical expression for the relationship between bias current and generated voltage swing. However, a large-signal operation is desired in low-noise oscillators to achieve low phase noise, especially at low-voltage power supplies.

This section evaluates the abilities of the different architectures to efficiently generate large voltage swings for a given power consumption. This ability is estimated using a PCF, which is defined as the ratio V_{PP}/I_{OSC} (V_{PP} is the peak-to-peak resonator voltage for given current I_{OSC} injected into the oscillator core). The evaluation of PCF is done numerically using the SpectreRF simulator. The power conversion factor has a dimension of impedance, and it is proportional to the parallel resistance of the resonator R_{eq} if the oscillator operates in a current-limited regime ($PCF = V_{PP}/I_{OSC} \approx (4/\pi)R_{eq}$, [7,23]) and gets smaller when the oscillator enters the voltage-limited regime. The current I_{OSC} may deviate significantly from I_B (I_B is injected in the current mirror) when the bias transistor M_{p3} enters the triode region due to large signal amplitudes. The current I_B is not taken into account, because it can be avoided in applications where the gate of M_{p3} is voltage-biased.

The obtained PCF for the investigated oscillator modifications is summarized in Table I as a function of the generated voltage swing. Once started, the D-Colpitts generates sufficiently large swing, which prevents the obtaining of reliable PCF for less than 1.0 V_{PP}. This is because the active transistors in D-Colpitts architecture operate mostly in the active region (Section 5), and relatively large swing is needed to force them to leave the active region such that further voltage growth is bounded. When the cross-coupled oscillators generate small swing (0.6 V_{PP}), the transistors also spend a significant part of the period in the active region, and the biasing inductors act only as a generation. This explains why the PCF of the oscillators without bias inductors is bigger than the PCF of the topologies with inductors. However, the oscillator modifications exploiting L_{TOP}/L_{BOT} have nearly independent PCF as a function of the voltage swing, which leads to an efficient use of I_{OSC} for increasing the voltage swing. On the other hand, the other topologies use less silicon area, but increasing their voltage swing is power inefficient. Since the PCF is nearly constant for the topologies using bias inductors, their utilization prevents quality-factor degradation caused by MOS transistors entering the triode region [1].

Similar to 1 L modifications, the PCF of the 2 L inductor-enhanced topologies remains nearly constant in large-signal conditions, while it drops for the classic architectures, displaying power losses. The power losses are the highest for the 2 L-N topology since the cross-coupled pair is grounded, while the PMOS cross-coupled pair in the 2 L-P topology is degenerated by a current mirror. The PCF of the 2 L oscillators is nearly half that of the 1 L oscillators. The same inductor is used in both topologies, but the oscillator current (I_{OSC}) in the 1 L architecture passes through the whole resonator, while in the 2 L architecture, I_{OSC} goes through the half resonator. Thus, for the same inductance and oscillator current, the 1 L topology generates almost twice as high swing [7,23].

Compared to the cross-coupled topologies without bias inductors, the D-Colpitts architecture has stable PCF, because the amplifying transistors (M_{n1} and M_{n2}) spend most of their time in the active region (Figure 11) and do not load the resonator extensively. Therefore, the behavior of the D-Colpitts under

Table I. PCF (V_{PP}/I_{OSC}) comparison between the evaluated *LC* oscillators.

	0.6 V_{PP}	0.8 V_{PP}	1.0 V_{PP}	1.2 V_{PP}	1.5 V_{PP}
TopB 1L	630.6	553.1	482.0	425.4	366.0
TopB 1 L + 2bL	540.5	536.4	530.9	526.1	523.3
BotB 1L	648.0	599.5	535.0	478.0	413.0
BotB 1 L + 2bL	549.6	542.4	536.9	532.3	526.1
2L, N	318.7	293.4	263.2	236.0	205.2
2L, N, L_{BOT}	261.5	261.8	262.0	262.4	262.0
2L, P	273.1	263.7	251.4	241.9	230.7
2L, P, L_{TOP}	254.3	256.4	256.9	257.5	257.2
D-Colpitts	-	-	203.3	220.7	231.4

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large-signal condition is more stable compared to the other architectures. Thus, the D-Colpitts oscillator should be selected if large signals have to be efficiently generated without extra bias inductors.

7. OSCILLATOR COMPARISON USING TVRL

The goal of this section is to compare the oscillator modifications using the TVRL method [6]. The oscillator TVRL trajectories are analyzed with respect to what is expected from the root trajectories obtained with the simplified oscillator models presented in Section 3. The evaluation of the TVRL trajectories and the explanation for their behavior use the information obtained with SpectreRF for the bias trajectories (Section 5), the PCF (Section 6), as well as the simulated phase noise. The auxiliary information given by the SpectreRF helps to explain the TVRL trajectories and to verify the conclusions drawn from the TVRL analysis.

7.1. 1L oscillator modifications

Figure 12(a) shows the λ_0 trajectories of the 1 L oscillator modifications depicted in Figure 1 and their bottom-biased counterparts obtained for a 1.2-V_{PP} voltage swing. The TVRL of the classic 1 L topologies approximates the behavior of the grounded *RLC* tank (Section 3.1). However, one of the cross-coupled pairs is degenerated with the current mirror, while the other one is grounded. Thus, the type of biasing (top-biasing or bottom-biasing) determines which pair would have bigger effect on the root-locus. The NMOS pair is grounded in the top-biasing case (Figure 1(a)) and the NMOS on-resistance has greater impact on the TVRL than the PMOS on-resistance. Similarly, the PMOS pair has a dominant effect in the bottom-biased oscillator. Although the trajectories obtained with the two biasing cases are similar, λ_0 of the top-biased architecture goes deeper in the LHP because the on-resistance of the NMOS transistor is smaller than that of the PMOS transistor. In order to compensate the excessive losses, λ_0 of the top-biased oscillator goes deeper also in the RHP. Following the reasoning outlined in [6], the bigger λ_0 swing of the top-biased oscillator both in the LHP and in the RHP suggests high switching-pair-transistor noise. This conclusion is verified by comparing the noise contributors presented in Table II for the different oscillators.

The λ_0 trajectories of the 1L + 2bL oscillators shown in Figure 12(a) are not visibly affected by the biasing scheme, which means that the additional inductors isolate the effects of the biasing network. The bias-network isolation suggests also that the bias noise would be hardly perceived by the oscillator. The root trajectories are governed by the sixth-order system (Subsection 3.3), which pulls the imaginary part of λ_0 upwards when the active devices enter the triode region.

The real part of λ_0 obtained for the different 1 L modifications are shown in Figure 12(b). Re(λ_0) is most positive at the oscillator's zero-crossing, corresponding to all active devices operating in the

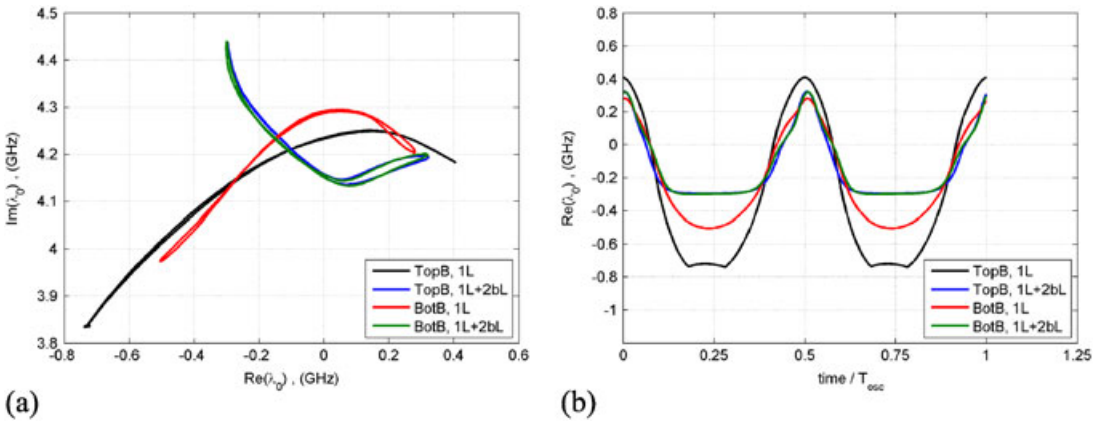

Figure 12. (a) Pole trajectories for the 1L oscillator modifications with $V_{PP} = 1.2$ V; (b) Re($\lambda_0(t)$) of the 1L oscillators.

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Table II. Noise contribution at 1-MHz offset for the 1 L oscillator modifications ($V_{DD} = 2.2$ V; $V_{PP} = 1.2$ V; noise in $10^{-15} \cdot V^2$/Hz).

	Top Biased		Bottom Biased	
	1 L	1 L + 2bL	1 L	1 L + 2bL
Resonator	13.66	13.32	14.76	13.49
$M_{n1,n2\ (flicker)}$	0.14	0.23	1.17	0.52
$M_{n1,n2\ (white)}$	30.73	4.53	9.19	4.18
$M_{p1,p2\ (flicker)}$	0.53	0.21	0.36	0.21
$M_{p1,p2\ (white)}$	11.62	4.13	17.03	4.18
$M_{BIAS\ (flicker)}$	94.59	13.42	399.70	28.53
$M_{BIAS\ (white)}$	27.13	3.50	74.00	4.52
PN @ 1 MHz	−120.1	−126.7	−115.5	−125.2
I_{DD}, (mA)	2.82	2.28	2.51	2.26
FoM	184.6	192.2	180.6	190.7

active region, while $\mathrm{Re}(\lambda_0)$ is the most negative at the maximum voltage, corresponding to one active device being in the triode region and the other device in the cut-off region. The cross-coupled pair does not generate negative conductance in the minima of $\mathrm{Re}(\lambda_0)$, but it adds positive conductance corresponding to resonator loading or *Q*-factor degradation. The amount of *Q*-factor degradation can be qualitatively estimated by how deep the TVRL goes into the LHP for the same voltage swing. The topologies utilizing the two bias inductors limit the *Q*-degradation and suggest better achievable phase noise.

Table II gives a detailed phase noise contribution of the main building blocks at 1-MHz frequency offset. Since the *LC* resonator and the voltage swing are the same, the resonance tank noise contribution is identical, which allows an evaluation of the oscillators rather than concentrating on the otherwise important properties of the resonator. The topologies using bias inductors have lower phase noise than their competitors. The reasons are two-fold: first is the limited *Q*-factor degradation, and second is the additional noise filtering provided by the two inductors. The limited *Q*-factor degradation is confirmed by comparing the noise contribution of the cross-coupled-pair transistors: for example, the $M_{n1,n2}$ contribution in classic 1 L topology is $30.73 \cdot 10^{-15} \cdot V^2$/Hz, which is reduced to $4.53 \cdot 10^{-15} \cdot V^2$/Hz for the 1 L + 2bL modification. The same conclusions can be drawn by comparing the noise contribution of the PMOS cross-coupled pair. The flicker noise contribution of the active devices is not affected as much, and since it is a few magnitudes lower than the other contributors, it can be said that the cross-coupled-pair flicker noise is not an issue for optimization. The limited *Q*-factor degradation has also another positive side – a lower bias current is needed to achieve the same voltage swing, which additionally helps achieving better FoM.

The noise filtering realized by the bias inductors can be observed by comparing both the white noise and the flicker noise contribution of the bias network (M_{BIAS}). As the bias noise is greater than the other noise sources, its reduction through the bias inductors has a big impact on the overall phase noise. As the noise filtering is a high-order effect, it is not directly observable on the oscillator TVRL shown in Figure 12(a).

The bottom-biased 1 L + 2bL oscillator has larger phase noise than the top-biased 1L + 2bL oscillator. Although the TVRL trajectories of the two oscillator modifications are essentially the same, which also makes the noise contribution of the cross-coupled transistor similar (Table II), the reason for the phase noise difference is traced back to the bias network. The NMOS bias transistor has the same size as the PMOS bias transistor, which corresponds to larger g_m and larger shot noise for the same bias current. Also, since the product W*L is the same, the NMOS transistor displays higher flicker noise. The increased bias white noise and bias flicker noise contribution in the bottom-biased topologies are confirmed by Table II.

7.2. 2L oscillator modifications

Figure 13(a) shows the λ_0 trajectories obtained for the 2L modifications operated with a voltage swing of $V_{PP} = 1.2$ V, while Figure 13(b) shows $\mathrm{Re}(\lambda_0(t))$ with respect to the oscillation period. The 2L-N

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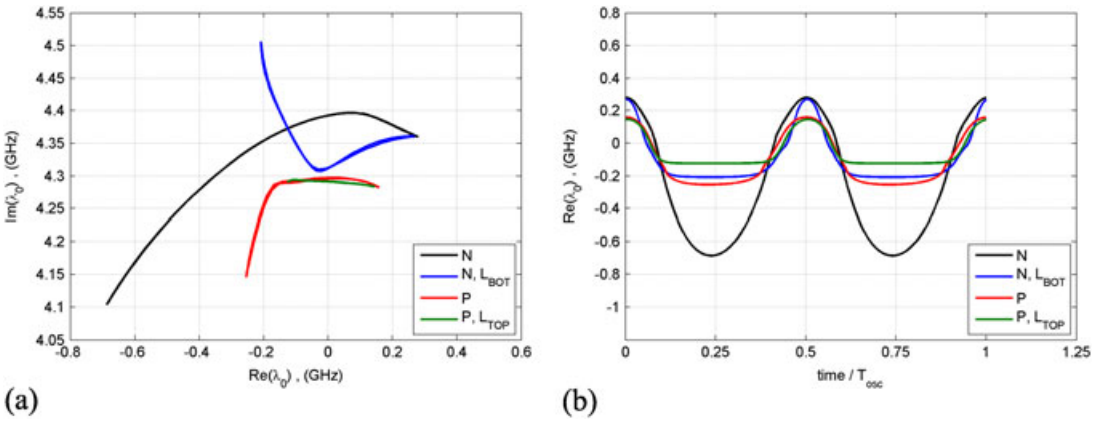

Figure 13. (a) Pole trajectories for the 2L oscillator modifications with $V_{PP} = 1.2$ V; (b) $\mathrm{Re}(\lambda_0(t))$ of the 2L oscillators.

modification utilizes a grounded NMOS cross-coupled pair, where the MOS on-resistance in large-signal condition is connected in parallel to the *LC* resonator, and it has a big impact on the TVRL trajectory. The NMOS transistor goes deep into the triode region with large amplitudes, and in turn, the TVRL trajectory goes deep into the LHP, corresponding to excessive energy loss. The inclusion of the bias inductor helps to minimize the losses in the 2L-N-L_{BOT} topology by limiting the TVRL swing in the LHP. Since the degeneration effect is not visible at the zero-crossings, the 2L-N and 2L-N-L_{BOT} topologies create the same maximum negative conductance, and TVRL reaches the same $\max(\mathrm{Re}(\lambda_0))$.

The TVRL of the 2L-P oscillator is reduced from both the positive and negative side compared to the 2L-N oscillator. The reduction of the positive TVRL is due to the smaller PMOS g_m. The reduction of the negative TVRL is due to the degeneration of the current mirror, which limits the resonator loading. At large voltage swings, however, the voltage headroom over the current mirror is reduced and the M_{p3} transistor may enter the triode region. The degeneration of the cross-coupled pair is significantly reduced when M_{p3} enters the triode region, which causes an abrupt drop of $\mathrm{Im}(\lambda_0)$ seen in the 2L-P TVRL (the red curve in Figure 13(a)). The abrupt drop of λ_0 is avoided by using the bias inductor L_{TOP}, which makes the degeneration of the cross-coupled pair almost insensitive to the voltage headroom over M_{p3}.

Table III gives a detailed contribution of the oscillator building blocks at 1-MHz offset frequency. Again, the topologies utilizing bias inductors display better phase noise due to *Q*-factor preservation and due to additional noise filtering of the bias network. The *Q*-factor deterioration is directly observed on the TVRL plot, while the noise filtering is not. The *Q*-factor preservation obtained with the bias inductors is confirmed by comparing the noise contributed by the switching pair ($M_{n1,n2}$/$M_{p1,p2}$) for the cases with and without inductors. The bias noise filtering provides additional benefits

Table III. Noise contribution at 1-MHz offset for the 2 L oscillators ($V_{DD} = 1.5$ V; $V_{PP} = 1.2$ V; noise in $10^{-15}\cdot V^2/Hz$).

	N	N, L_{BOT}	P	P, L_{TOP}
Resonator	14.55	14.62	13.97	13.44
$M_{n1,n2\ (flicker)}$	0.46	0.27	-	-
$M_{n1,n2\ (white)}$	39.68	11.03	-	-
$M_{p1,p2\ (flicker)}$	-	-	0.17	0.21
$M_{p1,p2\ (white)}$	-	-	16.43	9.28
$M_{BIAS\ (flicker)}$	12.72	1.04	23.97	2.22
$M_{BIAS\ (white)}$	2.78	2.18	9.38	0.43
PN @ 1 MHz	−124.1	−128.2	−124.5	−128.5
I_{DD}, (mA)	5.08	4.57	4.96	4.66
FoM	188.1	192.6	188.4	192.7

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for achieving low phase noise. The 2L-P topology has lower white and flicker noise contributed by the cross-coupled pair due to the lower MOS transconductance and lower K_f compared to the 2L-N topology.

The phase noise comparison here validates the conclusions drawn from the TVRL trajectories for the contribution of the cross-coupled pair. However, as was pointed out earlier, high-order effects such as noise filtering should be evaluated separately.

7.3. D-Colpitts

The λ_0 trajectories of the D-Colpitts are shown in Figure 14(a) for three voltage swings, while Figure 14(b) shows the voltage swings and the corresponding $\mathrm{Re}(\lambda_0(t))$ for one oscillation period. As outlined in Section 5, the active transistors spend a long time in active region, which corresponds to little variation of their small-signal parameters and in smaller TVRL trajectories compared to the 1 L and 2L oscillators. The cancelling effect of the transistor nonlinearities also contribute to the small trajectories, as outlined in Subsection 3.4. The main transistors behave differently during the rise and fall time of the oscillator waveform, because of the asymmetric transistor bias trajectory shown in Figure 11. The asymmetry affects the λ_0 trajectories, and it is seen as the maxima of $\mathrm{Re}(\lambda_0)$ being shifted from the oscillator zero-crossings. The minima of $\mathrm{Re}(\lambda_0)$ occurs close to the extrema of the oscillator voltage, but with a phase shift. The asymmetric phase shift depends both on the capacitive feedback ratio and on the voltage swing (Figure 14(b)).

Table IV gives a detailed phase noise contribution at 1-MHz offset frequency for the D-Colpitts. Increasing the voltage swing in D-Colpitts only slightly improves the oscillator phase noise since as the voltage swing grows, the active transistors M_{n1} and M_{n2} start to leave the active region, resulting in increased white noise. At the same time, the TVRL becomes more asymmetric (Figure 14(a)), which increases the AM–PM conversion of flicker noise. The increased AM–PM conversion is confirmed by comparing the bias noise in Table IV.

8. ANALYSIS OF THE TVRL SPECIFICS IN VCOS

This section evaluates the λ_0 trajectories in VCOs and compares them against the λ_0 trajectory of an oscillator. A VCO is usually built by adding a varactor block in parallel to the oscillator's resonance tank L_0C_0. The standard 1 L oscillator topology in Figure 1(a) is used for evaluating the TVRL specifics in VCOs.

8.1. Varactor block and its modeling

The varactor structure employed for this investigation is shown in Figure 15(a) [8]. The varactor structure uses differentially connected PMOS varactors with *dc*-decoupling network C_dR_d, where the varactor gate is *dc*-biased to ground with $R_{d1,2}$, and the control voltage V_C varies the potentials of

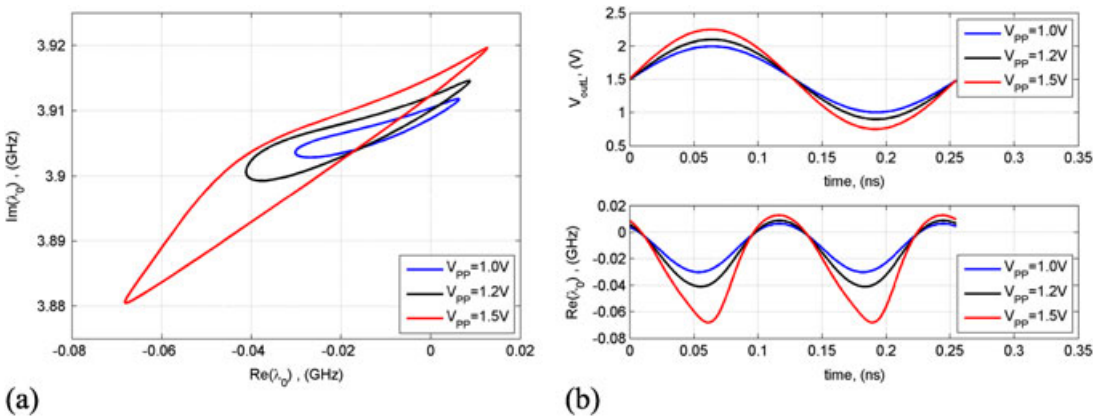

Figure 14. (a) D-Colpitts TVRL for different voltage swings; (b) Voltage swing and the corresponding real part of the main complex-conjugated root for the D-Colpitts oscillator.

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Table IV. Noise contribution at 1-MHz offset for the D-Colpitts ($V_{DD} = 1.5$ V; noise in $10^{-15} \cdot V^2$/Hz).

	$V_{PP} = 1.0$ V	$V_{PP} = 1.2$ V	$V_{PP} = 1.5$ V
$M_{n1,n2\ (flicker)}$	0.67	0.97	1.95
$M_{n1,n2\ (white)}$	48.14	50.82	54.37
$M_{BIAS\ (flicker)}$	7.61	11.24	22.64
$M_{BIAS\ (white)}$	45.01	50.98	60.87
PN @ 1 MHz	−119.9	−121.2	−122.4
I_{OSC}, (mA)	4.89	5.44	6.48
FoM	183.1	183.9	184.3

the PMOS drain and source. The small-signal model representing the varactor block for the TVRL computations is shown in Figure 15(b), where $C_{v1,2}$ and $r_{v1,2}$ are time-varying components modeling the varactor capacitance and series resistance. The extraction of the time-varying $C_{v1,2}$ and $r_{v1,2}$ is done prior to the TVRL computation, where each varactor is represented with its quasi-static model [27] and additional terminal resistances. The quasi-static model parameters for the varactor are obtained in the same way as for the active transistors of the oscillator core [6].

The extraction of C_v and r_v is done by computing the varactor impedance Z_V at the gate of the MOS device with its drain, source and bulk terminals being *ac*-grounded (V_{DD} and V_C are ideal voltage sources). An automatic model extraction composes the varactor circuit description in the form of $\mathbf{Y} = \mathbf{G} + s \cdot \mathbf{B}$ and computes the varactor impedance Z_V at a given frequency. The varactor equivalent parameters are

$$r_v = \Re(Z_V), \tag{11}$$

$$C_v = -1/(2\pi f_{extr} \cdot \Im(Z_V)), \tag{12}$$

where $\Re(Z_V)$ and $\Im(Z_V)$ are respectively the real and imaginary part Z_V. The computation is done for all data points within the oscillation period. An extraction frequency f_{extr} of 4 GHz is used for the initial r_v and C_v modeling, which is close to the oscillation frequency of the investigated VCO. Although the parameters r_v and C_v are frequency dependent, their relative variation over the frequency band of interest is less than 0.1% under various voltage swings and control voltages. This small variation is further reduced when referred to root computation, since the varactor block is connected in parallel with the tank capacitance C_0 and C_0 is dominantly determining the oscillation frequency.

An iterative procedure for adjusting f_{extr} is adopted in order to bring the oscillation and extraction frequency closer. The extraction frequency $f_{extr}(t)$ is corrected for each consecutive run, depending on the calculated $\lambda_0(t)$ from the previous step. The initial computation uses $f_{extr} = 4$GHz, and the deviation between $\lambda_0(t)$ and $f_{extr}(t)$ practically vanishes after 2–3 iterations. Even without any iteration, the error of the computed root $\lambda_0(t)$ is less than 10^{-6} GHz, and it goes below 10^{-12} GHz after the third iteration. Despite the small error when using fixed f_{extr}, a five-step iterative procedure is used for obtaining precise TVRL trajectories presented below.

8.2. *Time-varying varactor capacitance and its impact on the TVRL and phase noise*

Figure 16(a) and (b) show the equivalent capacitance $C_{V,eq} = (C_{V1} \| C_{V2})$ seen by the resonator for various control voltages obtained for 1.2-V_{PP} and 1.5-V_{PP} voltage swing respectively. The time-varying $C_{V,eq}$

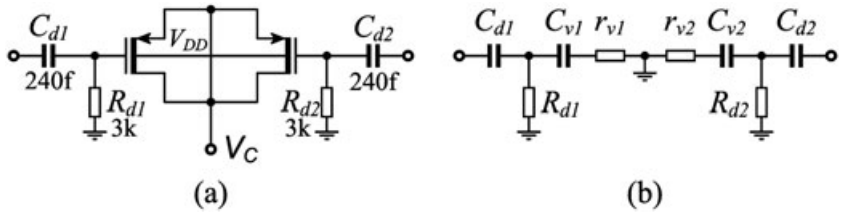

Figure 15. Varactor block: (a) schematic; (b) small-signal model representing the varactor block in TVRL computations.

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depends on the resonator voltage swing, because a scaled and dc-shifted version of the output voltage is applied to the varactor gate. An effective varactor capacitance for each control voltage determines the oscillation frequency, as it is known that the oscillator voltage swing has an effect on the frequency tuning range [24,28,29]. Increasing the voltage swing forces $C_{V,eq}$ to change quicker between its maximum and minimum value. The large swing introduces variations of the varactor capacitances even for control voltages where the varactor small-signal C–V curve is flat (in the beginning and at the end of the tuning range), which is known as a bias-dependent frequency tuning [24].

The variation of $C_{V,eq}$ for different V_C occurs at different instants along T_{OSC}, which affects the oscillator phase noise. In the beginning and at the end of the tuning range, $C_{V,eq}$ varies mostly around the extrema of the voltage swing – $\pi/2$ and $3\pi/2$ (0, π, and 2π are the voltage zero-crossings). Since the oscillator is less sensitive around $\pi/2$ and $3\pi/2$, less noise is transformed to phase noise due to AM–PM conversion. On the other hand, $C_{V,eq}$ changes rapidly around π and 2π for V_C in the range of 0.3 V–0.7 V, thus producing higher AM–PM conversion. Although the above results are generally known, the added value of the time-varying varactor investigation is the recognition that $C_{V,eq}(t)$ changes rapidly around the zero-crossing in the middle of the tuning range, thus increasing the noise sensitivity of the oscillator.

The obtained TVRL trajectories of the 1L-VCO are shown in Figure 17(a) for five control voltages. The trajectories look similar to the trajectory of the native oscillator (Figure 12(a)), but their behavior along the frequency tuning range has certain specifics. The λ_0 trajectory would simply move along the imaginary axis of the *s*-plane depending on the control voltage V_C if the varactor capacitance was time invariant. However, since $C_{V,eq}$ is time-(voltage-)dependent (Figure 16), the TVRL changes its shape. $C_{V,eq}$ can be assumed constant only for $V_C \approx 0$ V, 0.4 V and 1.2 V, and it is seen from Figure 17(a) that these TVRLs have almost the same shape, but are shifted in frequency. The λ_0 trajectory for $V_C = 0.2$ V comes closer to the 0-V trajectory in the RHP, but it comes closer to the 0.4-V trajectory in the LHP. The distorted TVRL shape for $V_C = 0.2$ V is due to the time-varying $C_{V,eq,}$ which has a smaller capacitance value around the zero-crossing and larger capacitance around the voltage extrema. Since the same physical effect causes AM–PM phase noise conversion, the AM–PM effect can be evaluated through the TVRL distortion from its nominal trajectory. Similarly, the 0.6-V trajectory comes close to the 1.2-V trajectory in the RHP, and close to the 0.4-V trajectory in the LHP.

Following the discussion above, the AM–PM conversion of flicker noise can be evaluated using the distorted TVRL. As the TVRL trajectory obtained for $V_C = 0.4$ V is nearly the same as the one of the native oscillator (but shifted in frequency), one can conclude that the AM–PM conversion is minimized, and good phase noise can be obtained around $V_C = 0.4$ V. It was shown in [29] that such an optimum exists, and it can be confirmed with SpectreRF simulations. The 1L-VCO phase noise at 10-kHz frequency offset, which is mostly governed by flicker noise, is shown in Figure 17(b), confirming that an optimum close-in phase noise can be obtained in the middle of the tuning range where the TVRL trajectory resembles the trajectory of the native oscillator. The phase noise

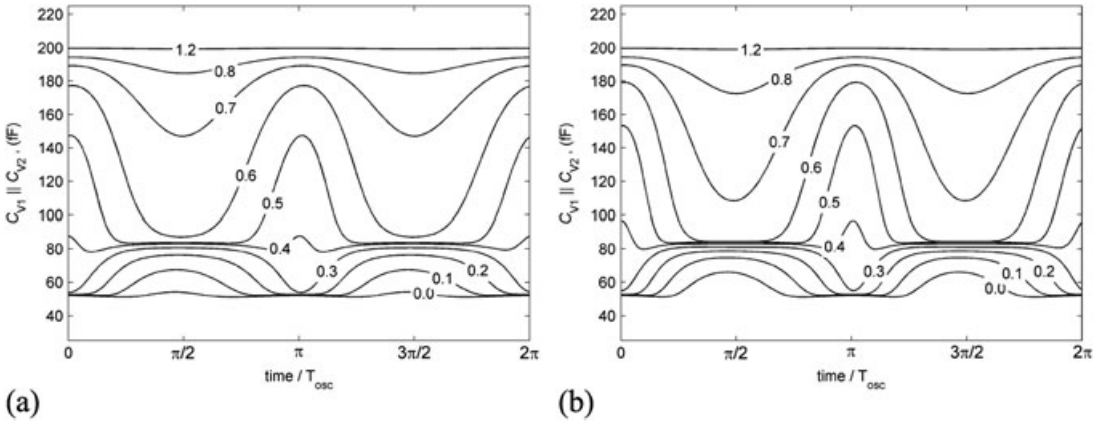

Figure 16. Equivalent time-varying varactor capacitance ($C_{V1}||C_{V2}$) seen by the main resonator of the 1 L-VCO for different V_C at: (a) $V_{PP} = 1.2$ V; (b) $V_{PP} = 1.5$ V.

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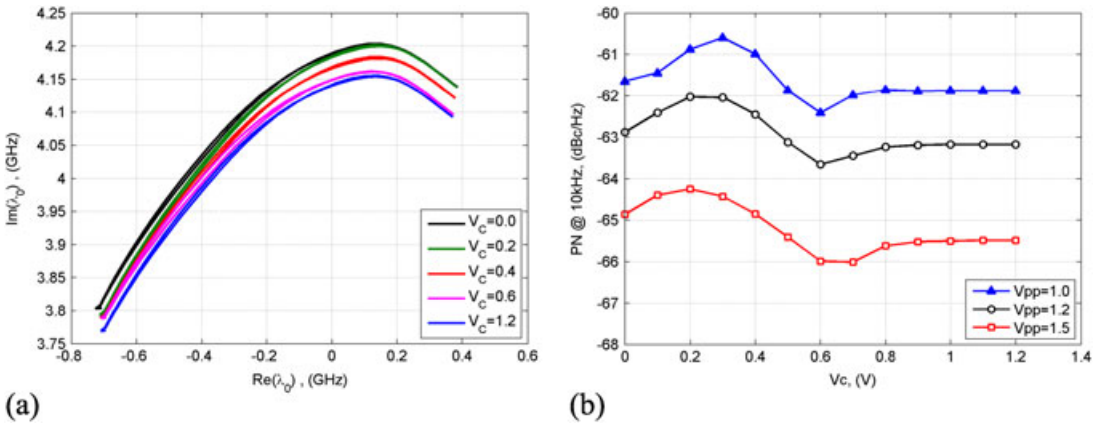

Figure 17. (a) 1 L-VCO TVRL for five V_C with voltage swing of 1.2-Vpp; (b) flicker noise optimum in the middle of the 1L-VCO tuning range for three voltage swings.

optimum is achieved around $V_C = 0.6$ V, which means that the time-varying intrinsic capacitances of the native oscillator at $V_C = 0.4$ V create visible AM–PM conversion, while they get compensated with the varactor capacitance at around $V_C = 0.6$ V.

The effect of the varactor on the TVRL is similar for all the oscillator topologies presented above when they are used for building a VCO.

9. SUMMARY AND CONCLUSIONS

The comparative study on GHz-range *LC* oscillators presented in this paper is meant to be used as a guideline for oscillator topology selection. The topology comparison is based on the TVRL method with conclusions that are verified with Cadence SpectreRF simulations. The main focus of this work is on the treatment of the TVRL trajectories in different oscillators provided with links to the physical process that are known from the literature.

The start-up process, phase noise performance and TVRL trajectories for the investigated oscillator modifications were presented in detail. The TVRL behavior is linked to the physical processes inside the oscillator to demonstrate its analytical capabilities. In addition, the oscillators' TVRL were first evaluated with simplified large-signal models that help in understanding the processes of the complete oscillators. Section 8 outlined the TVRL specifics in VCOs that are linked to the time-varying varactor capacitance and its cumulative effect on the VCO performance.

2L oscillator topology is more suitable for low-voltage application compared to 1 L topology, but it requires higher current consumption. In both 1L and 2 L oscillators, the large-signal oscillator operation drives the active devices in the triode region, causing *Q*-factor degradation. The *Q*-factor can be partly preserved by using appropriate biasing scheme or bias inductors, where the former is silicon hungry but provides better phase noise performance. The active transistors in the D-Colpitts topology operate with lower voltages for the same voltage swing, suggesting advantages in high-voltage applications, or high-swing generation with low-breakdown-voltage transistors. The TVRL is found usable in recognizing the AM–PM noise conversions in VCOs.

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