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ARTICLE *in* ADVANCED MATERIALS · JUNE 2005

Impact Factor: 17.49 · DOI: 10.1002/adma.200401174

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Microscopic Evidence for Spatially Inhomogeneous Charge Trapping in Pentacene**

By *Erik M. Muller* and *John A. Marohn**

The comparatively high mobility of pentacene and its ability to be deposited on flexible substrates at low temperature[1,2] make it an attractive alternative to amorphous silicon in low-cost large-area electronics applications. Potential applications of pentacene thin-film transistors include display drivers, smart cards, and radio-frequency identification tags.[2–4] While pentacene thin-film transistors have exhibited usefully large mobilities (≥ 1 cm^2 V^{-1} s^{-1}) and on–off ratios ($\geq 10^6$),[5] fabricating pentacene transistors with suitable performance for large-scale applications remains a challenge.

In polycrystalline films, mobility is extremely sensitive to processing conditions, being dependent on crystallite size,[6–10] the substrate,[9,10] exposure to oxygen and water,[11,12] and possibly on the purity of the pentacene.[13] Pentacene transistors, particularly on flexible substrates, exhibit undesirably small threshold slopes,[7] and threshold voltages that are too large[2] and which drift due to gate-dependent bias stress.[8] Bottom-contact transistors are likely to be required for low-cost applications yet, in this geometry, making a low-resistance contact between pentacene and a metal is problematic.[14,15]

Microscopic theories of these effects in polycrystalline pentacene—developed to explain the dependence of transistor behavior on time, temperature, or device dimensions—usually invoke charge traps. For example, threshold-voltage shifts have been explained as being the result of a slow structural change in the film that creates deep localized states near the interface.[9] The dependence of the mobility on gate voltage,[1,3,9,10,16,17] temperature,[9] and degree of unintentional doping[17] is usually modeled in terms of the filling of traps. The traps may[10,17,18] or may not[1,9,16] be explicitly associated with grain boundaries, depending on the model. The presumed increase in charge traps at smaller pentacene grains near the electrodes has been used to rationalize the lower apparent mobility in bottom-contact devices.[3]

Despite the apparently central role of charge traps in controlling charge injection and transport, the microscopic origin of charge trapping in polycrystalline pentacene is not known. Trap energies and concentrations have been estimated for pentacene using deep-level transient spectroscopy[19] and space-charge-limited current techniques.[20] Such macroscopic measurements, however, are unable to determine whether charge traps are a bulk phenomenon associated with chemical impurities, or a grain boundary effect, as is generally supposed. To our knowledge, charge traps in pentacene have never been observed microscopically.

In this communication, we use electric force microscopy (EFM) to directly observe and image long-lived trapped charges in a pentacene thin-film transistor as a function of gate voltage. We find that charge traps are distributed inhomogeneously throughout the pentacene film, but, unexpectedly, are not confined solely to grain boundaries. EFM has been used to study pentacene before, but prior work focused on understanding contact resistance by mapping the local potential of an operating thin-film transistor. Nichols et al. showed that contact resistance in a bottom-contact transistor could be controlled by varying the electrode metal[14] while Puntambekar et al. demonstrated that bottom-contact devices were typically contact limited, whereas top-contact devices were not.[15] We use EFM to study charge trapping because, compared to competing techniques, it does not require detailed understanding of the contacts or transport in the bulk.

Pentacene transistors were fabricated with bottom-contact source and drain electrodes recessed into the gate oxide

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[**] The authors thank Dr. Ricardo Ruiz and Prof. George Malliaras of Cornell University for assistance with pentacene deposition and for many useful discussions. This work was supported by Cornell University, the National Science Foundation (via CAREER award DMR-0134956, the Cornell Nanoscale Science and Technology Facility, and the Cornell Center for Nanoscale Systems, and the Cornell Center for Materials Research).

  DOI: 10.1002/adma.200401174

(Fig. 1a), as described in the Experimental section. Recessing the electrodes allowed the pentacene to form a continuous, constant-height film, which considerably simplified interpretation of subsequent EFM images. AFM measurements showed that recessing the electrodes did indeed produce a flat device (Fig. 1b). The device exhibited typical transistor behavior (Fig. 1c), with a threshold voltage of $V_T \approx -10$ V and a mobility, calculated in the saturation régime, of $\mu_{sat} = 2 \times 10^{-2}$ cm^{2}V^{-1}s^{-1}. These values are typical of a bottom-contact device prepared by evaporative deposition onto an untreated SiO_2 substrate.[21]

We detected the presence of charge traps in pentacene via their effect on contact potential. Local measurements of contact potential and capacitance were made using a custom-built electric force microscope.[22] The microscope employed a commercial, metal-coated cantilever, worked with the sample at room temperature in the dark, and operated at high vacuum (10^{-6} mbar) for highest sensitivity. Instead of measuring the cantilever amplitude, whose response time can be deleteriously long (many seconds) in vacuum, we followed instead the cantilever resonance frequency, f, which responded instantaneously to changing electrostatic-force gradients:[23]

$$\Delta f = f - f_0 \approx \frac{-f_0}{4k} C''(V_{tip} - \phi)^2 \quad (1)$$

Here, f_0 is the natural resonance frequency of the cantilever and k is the cantilever spring constant. The cantilever frequency depends on the voltage, V_{tip}, applied to the cantilever; on ϕ, the contact potential difference between the tip and the sample; and on $C'' = \partial^2 C/\partial z^2$, the second derivative of the tip–sample capacitance, C, with respect to z, the tip–sample separation. The approximation used to derive Equation 1 holds when electrostatic-force gradients are small compared to the mechanical spring constant of the cantilever, which is the case here.

Figure 2a shows a plot of cantilever resonance frequency versus tip voltage, acquired at a point over the pentacene transistor gap with the source, drain, and gate grounded. The observed parabola was fit to Equation 1 to obtain C'' and ϕ at that point. This procedure can, in principle, be repeated at each point to build up an image of C'' and ϕ. In practice, we find that Δf is dominated by, depending on experimental conditions, either the variation in C'' or ϕ alone. This simplifies data acquisition and analysis considerably. For example, if C'' is constant, then we can infer the local contact potential from an image of Δf acquired at constant V_{tip} using

$$\Delta\phi \approx \frac{\Delta f}{f_0} \frac{2k}{C'' V_{tip}} \quad (2)$$

We detected trapped charge by its effect on the local contact potential. To calculate the effect, we modeled the tip–sample interaction as that of a parallel-plate capacitor of the form metal 1/dielectric/vacuum/metal 2 (Fig. 3a). Here "metal 1" represents the gate, "metal 2" the tip, and "dielectric", the SiO_2. For simplicity, we neglected the pentacene because its thickness was much smaller than that of the SiO_2. Trapped charge at the SiO_2/pentacene interface will shift the apparent

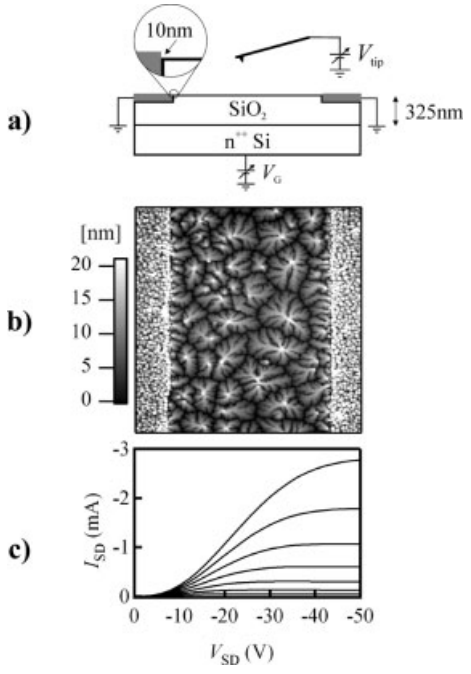

Figure 1. Pentacene thin-film transistor. a) Schematic of the device substrate (gap length, $L = 6.5$ μm and total transistor width, $W = 20.1$ cm). The zoomed-in feature shows the height difference between the gap and the recessed electrodes. Also shown is a metal-coated cantilever for atomic force microscopy (AFM) and EFM. b) 15 μm × 15 μm AFM image of the pentacene transistor. c) Current–voltage characteristics (I_{SD}: source–drain current; V_{SD}: source–drain voltage). Here V_G ranges from 0 V to –50 V in 5 V steps.

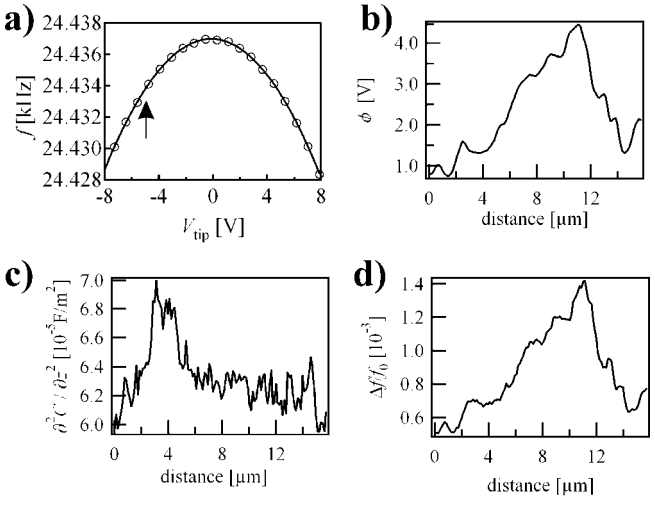

Figure 2. a) Cantilever resonance frequency versus tip voltage. The open circles are data points and the solid line is a fit to Equation 1. The cantilever is located 150 nm above the pentacene. Line scans over pentacene in the transistor gap, with charge traps occupied, of b) contact potential, c) capacitance derivative, and d) frequency.

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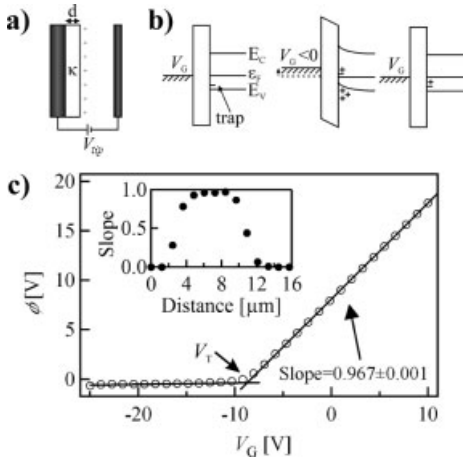

Figure 3. a) Model of the tip–sample interaction (see text for explanation). The + symbols represent trapped charges. b) Energy-level diagram of the pentacene transistor, showing a trap level near the pentacene–SiO_2 interface. The gate is on the left, SiO_2 in the middle, and the p-type pentacene layer on the right. The cantilever is omitted for clarity. The energy-level diagrams show the gate bias progressing from zero to negative, and then back to zero. c) $\phi(x)$ versus V_G. The inset shows the slope at positive gate bias versus the tip position across the device gap.

contact potential difference between metal 1 and metal 2 by an amount

$$\Delta\phi_{trap} \approx \frac{\sigma d}{\kappa\varepsilon_0} \quad (3)$$

where σ is the planar charge trap density, d and κ are the thickness and dielectric constant of the dielectric layer, respectively, and ε_0 is the permittivity of free space.

For this approach to work, we needed to create traps at the SiO_2/pentacene interface. This was easily accomplished by grounding the source and drain electrodes and applying a negative voltage to the gate electrode, as sketched in the second energy level diagram of Figure 3b. We also needed the gate and tip to behave like a parallel-plate capacitor. Unfortunately, this was not the case at the negative gate voltages required to populate the traps.

With source and drain grounded, we measured ϕ as a function of V_G (Fig. 3c). If the tip and gate behaved as a parallel-plate capacitor, then ϕ should track V_G, with a slope of one. This was indeed found to be the case when $V_G > 0$. When V_G was negative and below a threshold voltage ($V_T \approx -8$ V), however, charge accumulated at the pentacene/SiO_2 interface and shielded the tip from the gate, resulting in $\phi \approx 0$. (This can alternatively be explained using a model similar to that of Fig. 3a, with metal 1 now representing the pentacene accumulation layer. Since the traps reside in or near the accumulation layer, $d \approx 0$, and we expect $\Delta\phi_{trap} \approx 0$.) It is interesting to note that in Figure 3c, we are measuring the transistor threshold voltage *locally*.

When $V_G < V_T$, we predict that ϕ is completely insensitive to charge traps. This was observed experimentally. Figure 4a shows a frequency image of pentacene taken with $V_G = +2$ V, where no traps are present, and with $V_G = -50$ V, where we would predict a large trap concentration. The images are virtually identical. Subsequent analysis showed that the image contrast comes exclusively from topography-related variations in C''.

Figure 3b suggests an alternate approach to imaging charge traps. After setting the gate voltage to be negative for 30 s in order to charge the traps as above, we returned the gate voltage to zero before imaging. As depicted in the last energy-level diagram of Figure 3b, the free carriers quickly left the channel, while the charge traps remained out of equilibrium and occupied for many minutes—long enough to image with the electric force microscope. Figure 4b shows frequency images captured as a function of the charging voltage, $V_{charging}$. In contrast to Figure 4a, these images show a dramatic evolution in frequency variation as the gate voltage is increased.

We find that image contrast in Figure 4b arose predominantly from variations in contact potential. To determine this, we repeated the measurement of Figure 2a, finding ϕ and C'' along a representative line in the transistor gap (Figs. 2b,c). The location of this line is indicated by an arrow in Figure 4b. Using Equation 1, we estimated that 85 % of the variation in Δf observed along the line was due to the variation in contact potential. This can be seen qualitatively in Figure 2d, where we have constructed Δf from the measured $\phi(x)$ and $C''(x)$; the observed frequency tracks ϕ very closely. We are thus justified in treating C'' as constant and using Equation 2 to compute the local contact potential, ϕ, from the measured cantilever frequency. We attribute the variation in ϕ to long-lived traps, since the observed variation in ϕ across the transistor gap 1)

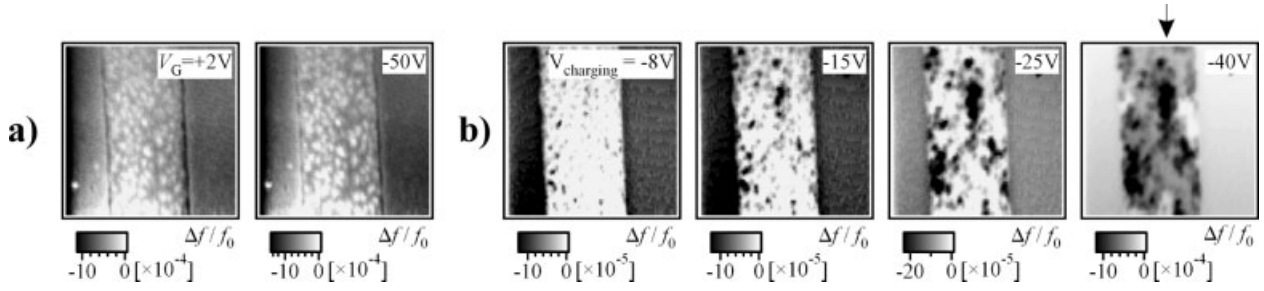

Figure 4. Cantilever frequency-shift images, taken at $V_{tip} = -5$ V (see arrow in Fig. 2) and $z = 150$ nm, using the protocol a) of Figure 3a and b) of Figure 3c. Note that in (b), the scale changes across the series.

was less than 50 mV before the gate voltage was increased above the threshold voltage, 2) increased with $V_{charging}$, and 3) disappeared after approximately 24 h.

Figures 4b,5 are the central result of this communication. The long-lived traps evident in Figure 4b at higher charging voltages are clearly *not* homogeneously distributed in space, and large variations in trap concentration are observed on a ≥300 nm length scale. Figure 5b displays the trap density, σ, versus $V_{charging}$ at selected points in the transistor gap. While the trap density increases as a function of $V_{charging}$ at most locations in pentacene, the amount of increase is simply not correlated with the apparent location of the grain boundaries, as generally supposed.[10,17,18]

The trap density can be calculated quantitatively using Equations 1–3; the known parameters k, κ, d, and V_{tip}; and the measured parameters Δf, f_0, and C''. Figure 5c displays histograms of trap density at various charging voltages. The mean trap density at $V_{charging} = -30$ V was 1.6×10^{11} holes cm^{-2}, or about one hole per 2.5×10^3 pentacene molecules (assuming that the accumulation layer was one monolayer thick). Using an effective tip diameter of approximately 300 nm (the apparent EFM imaging resolution as estimated by the smallest feature seen in Fig. 4b), we calculate that it should be possible to detect the contact-potential shift due to as few as ~3 trapped holes underneath the cantilever tip.

Interestingly, as the charging voltage increased, the trap distribution evolved from a Gaussian shape to a highly asymmetric distribution with a long exponential-like tail—a possible consequence of sites trapping charge at different rates. While a Gaussian distribution can arise from statistical fluctuations in the filling of a single well-defined trap energy level, an asymmetric distribution cannot. This suggests an exponential density of trap energies, in qualitative agreement with transport studies.[9,16,17]

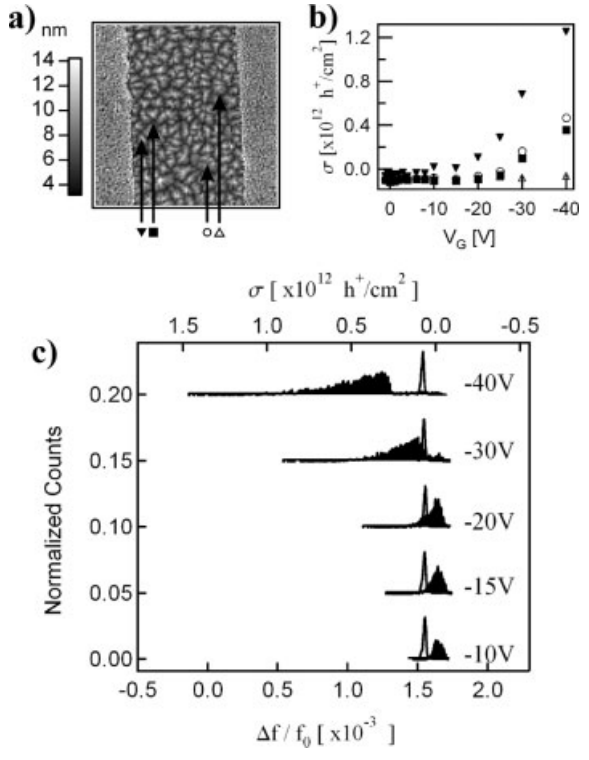

Figure 5. a) Selected points in the pentacene transistor gap; b) trap density versus charging voltage at the selected points; and c) histograms of trap density at various charging voltages.

Our findings can be used to eliminate a number of proposed trap candidates. We must begin by noting that trapping at grain boundaries near the buried pentacene/SiO_2 interface is not necessarily inconsistent with our data, since the grain boundaries at the buried interface need not correspond to the grain boundaries identified by AFM topography.[15] We, nevertheless, regard trapping at buried grain boundaries as an extremely unlikely possibility, since the observed charge traps simply do not appear to follow the shape expected of grain boundaries. Further EFM studies with thinner pentacene samples will allow us to establish a direct connection, if it exists, between grain boundaries and charge traps.

The long-lived traps observed here cannot be due to bulk trapping at randomly distributed chemical defects. Bulk traps should have well-defined energies, inconsistent with the observed trap-concentration statistics. Above a threshold, trap concentration increases approximately linearly with voltage, consistent with a polaron (cation) trapping mechanism. We find no evidence of a bipolaron (di-cation) trapping mechanism,[24] as has been proposed by Northrup and Chabinyc and co-workers for hydrogen- and oxygen-related defects in pentacene.[25]

Knipp et al. have found that the trap depth is different for pentacene transistors fabricated on a rough versus a smooth silicon nitride dielectric, suggesting that traps are associated with perturbations in pentacene energetics arising from the dielectric.[9] It is tempting to draw a similar conclusion from our data for the pentacene/SiO_2 interface, since our observations imply that there are sites in polycrystalline pentacene near the SiO_2 interface, *in addition* to grain boundaries, that act as traps. Surprisingly however, the ~300 nm length scale associated with charge-trap domains in the images of Figure 4b are much larger than the length scales associated with either a pentacene topography (Fig. 5a) or a SiO_2 topography (data not shown). It is hard to understand why the observed trapping domains are so large if the dielectric is determining the trap energies. Establishing a definitive connection between local chemical structure at the buried pentacene/dielectric interface will be challenging, since essentially no analytical tools exist for determining local structure at a buried solid–solid interface. As a next step, it will be interesting to image traps in pentacene deposited on various dielectrics.

In conclusion, we found that charge traps in polycrystalline pentacene are distributed inhomogeneously, but do not appear to be associated with grain boundaries. Using frequency-shift EFM to image traps is quite general and requires no assumptions about charge transport in either the bulk or at the contacts. In this study, we imaged traps that filled quickly (within < 30 s) and emptied slowly (> 20 min). We believe

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30 s is long enough to populate the majority of trap sites, since the current–voltage characteristics taken on this timescale showed good saturation behavior, and since the trap densities we measured are comparable to what has been estimated by others.[9] While the implementation described here is naturally suited to imaging long-lived traps (≥ 20 s), studying traps with shorter lifetimes (≤ 1 s) should be possible by following the cantilever frequency, point by point, as a function of time. It will be interesting in future work to use EFM to locally probe trapping and detrapping kinetics. By working with thinner pentacene samples and by operating the tip at closer distances, we should be able to explore trap energetics and kinetics with potentially single-charge sensitivity.[26]

Experimental

Device Fabrication: Device substrates were fabricated beginning with a heavily p-doped Si wafer (0.001–0.003 Ω cm; ⟨100⟩orientation). A 325 nm thick thermal oxide was grown as a gate dielectric. Source and drain electrodes were defined using optical photolithography. Prior to evaporating 5 nm of Cr and 70 nm of Au as the source and drain electrodes, shallow trenches (60 nm) were etched in the SiO_2 to recess the electrodes. Immediately prior to the pentacene deposition, the device substrates were cleaned with acetone and isopropanol. Pentacene from Aldrich was used without further purification. A 50 nm layer of pentacene was thermally evaporated in high vacuum at a rate of 0.1 Å s^{-1}, with the device substrate fixed at room temperature. The source and drain electrodes were composed of 34 interdigitated fingers with a gap length, L, of 6.5 μm. The resulting total width, W, of the transistor was 20.1 cm.

Current–voltage measurements were taken with Keithley source meters, model numbers 2400 and 6430. The entire current–voltage dataset was taken in approximately 1 min, with each I_{SD} versus V_{SD} curve taking 5–15 s. Because good saturation is observed in the current–voltage characteristics of Figure 1c on the timescale of 5–15 s, we conclude that the time required to occupy the majority of traps is comparable to this time or shorter. We chose 30 s as a sufficiently long trap-charging time in the EFM experiments.

Atomic and Electric Force Microscopy: We employed a commercial cantilever (model number NSC21, MikroMasch) with a spring constant, $k = 1$ N m^{-1}, resonant frequency, $f_0 = 24$ kHz, and a quality factor, $Q = 10^4$. The motion of the cantilever was detected using a fiber-optic interferometer capable of measuring 2 mÅ/$\sqrt{\text{Hz}}$ displacements at the resonant frequency of the cantilever [27]. The interferometer operated at 1310 nm, a wavelength well below the bandgap of pentacene. The cantilever was driven at its resonant frequency by sending the displacement signal from the interferometer through a phase-locked loop to a piezo mounted under the base of the cantilever, forming a positive-feedback loop. The amplitude of the oscillating voltage sent to the piezo was held constant. This amplitude was adjusted until the cantilever response reached 15 nm (root mean square). The resonant frequency of the cantilever was read out with a Stanford Research Systems SR620 frequency counter.

Received: July 21, 2004
Final version: December 15, 2004
Published online: March 24, 2005

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