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Designed Organophosphonate Self-Assembled Monolayers Enhance Device Performance of Pentacene-Based Organic Thin-Film Transistors

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Organic thin-film transistors (OTFTs)[1] are compatible with large area fabrication techniques, and they may yield new paradigms for manufacturing that would reduce device costs for large area circuits.[2] Pentacene-based OTFTs are well studied; yet they can be compromised with regard to critical device parameters: on/off ratios, carrier mobilities, sub-threshold performance, and threshold voltages. Surface treatments for the SiO_2 gate dielectric[2–8] can be effective; typically, however, improvement is realized in only one of these critical areas, often to the detriment of the others.[5,6,9–11] Here we show that systematic structural modification of self-assembled monolayers of phosphonates (SAMPs) fabricated on SiO_2 gate dielectrics can yield pentacene-based devices in which all four critical parameters are enhanced simultaneously. We hypothesize that phosphonate structural motifs enable two-dimensional SAMP surface coverage to translate to a three-dimensional one through controlled lateral spacing between vertically oriented acene units, which can affect crystallization of vapor-deposited pentacene.

Our approach to surface modification of the SiO_2 gate dielectric on a Si device is based on a simple procedure in which a dilute solution of a phosphonic acid is drawn down across the face of the Si substrate. This process, nicknamed the T-BAG,[12,13] enables formation of high quality SAMPs on these substrates under mild conditions. In previous work we showed that a surface chemistry design approach to transistor function optimization based on T-BAGged SAMPs, progressing from simple enhancement of surface wetting to inducing more specific SAMP-pentacene interactions, enabled systematic improvement in OTFT behavior.[14,15] Our best-performing OTFT was based on a SAMP of 9-phosphonanthacene (**1**). Anthracene-based phosphonates are electronically acceptable for SiO_2 gate dielectric modification: Their SAMP constituents should have a band gap larger than that of pentacene itself (1.86eV by optical absorption);[16] thus the SAMP would not create inherent trapping states. Furthermore, an anthracene-based SAMP and pentacene should have only C-H bond-π-system interactions, not stronger bonding ones that could, themselves, create trapping states in the semiconductor gap. Indeed, we found that OTFTs fabricated on 100 nm SiO_2 gate dielectrics terminated with a SAMP of **1** showed high on/off ratios, good threshold voltages, and subthreshold slopes as steep as 200 mV/decade[14,15] in contrast to devices prepared on untreated SiO_2 where subthreshold slopes on the order of about 5 V/decade, and threshold voltages of tens of volts are typical.[11] Pentacene-based devices fabricated with SAMPs of **1** were also compared to devices made with octadecyl trichlorosilane and with its SAMP analog, octadecylphosphonic acid. These three types of devices all had hole mobilities that were indistinguishable within experimental error.[14,15]

Tight molecular packing of **1** on the SiO_2 surface was measured by quartz crystal microgravimetry (QCM) to be 0.33 nmol/cm^2;[14,15] this corresponds to a molecular footprint of 49 Å^2, which is smaller than that in crystalline anthracene.[17] We interpreted these data in terms of a π-stacking morphology of anthracenyl units on the SiO_2 surface that is organized by a strong phosphonate-SiO_2 interaction, and we hypothesized that the acene monolayer-presenting SAMP surface of **1** could affect further pentacene deposition. As a bonus, molecularly dense SAMP formation also removed SiO_2 surface OH groups, which gave rise to the observed reduction in trap states measured for these devices. Unfortunately, carrier mobilities (0.8 cm^2/Vs) for devices built on **1** were no better than those of pentacene based OTFTs prepared by other means. Yet **1** was used as a starting point for further development of SAMP structure-OTFT function relationships: beneficial aspects of dense SAMP film formation would be maintained, but molecular orientation of SAMP constituents and film molecular spacings could be systematically varied as a means to improve device behavior.

To enhance transistor performance by SAMP design, monolayers of **2**, **3**, and **4** were prepared from phosphonoanthracenes **2'**, **3'**, and **4'** on the SiO_2 gate dielectric; these SAMPs should present phosphonate molecular orientations different from those of **1** with regard to the Si surface (**Figure 1**). SAMPs of **1** are surface conforming on SiO_2/Si as determined by AFM with a film thickness of 0.40 nm, consistent with individual molecules of **1** held normal to the surface with their distal edges essentially parallel to the surface (Figure 1). In contrast monolayers of **2**, **3**, or **4** would present a ridged surface, with terminal anthracene groups of the film constituents pointing away from the SiO_2 surface at an angle of about 60° from normal

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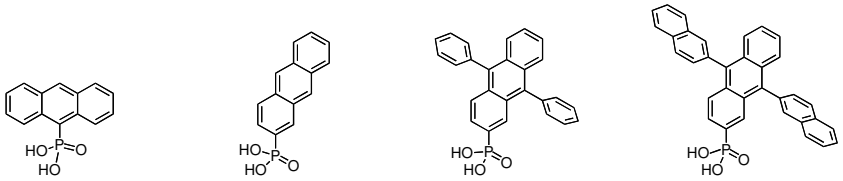

Figure 1. Phosphonoanthracene precursors of SAMPs **1**, **2**, **3** and **4**, respectively.

and with molecular spacing increasing from **2** to **4** by virtue of increases in lateral substituent group sizes. We hypothesized that it might be possible that these molecular spacings could serve to nucleate pentacene with morphologies different from what is obtained when it is deposited onto **1**.

Pentacene/bare SiO_2/Si (control) and pentacene/SAMP/SiO_2/Si transistors were fabricated in the top-contact geometry and were evaluated for performance with respect to the four critical transistor characteristics. First, a SAMP of anthracene-2-phosphonate (**2**) was grown on the SiO_2 to test the effect of orientation of anthracenyl units on device behavior. Next, a SAMP of 9,10-diphenylanthracene-2-phosphonate (**3**) was prepared; here molecular orientation of the film constituents is similar to that in **2**, and molecular spacing is controlled by the size of the substituent phenyl groups. Finally, a SAMP of 9,10-dinaphthylanthracene-2-phosphonate (**4**) was obtained; intermolecular spacing for **4** would be expected to be larger than for **3**, given the relatively larger size of the naphthyl substituent groups. All SAMP-treated devices showed transistor performance improvements compared to control ones in terms of uniformity in threshold voltage (V_{Th}) among numerous devices and slightly negative threshold voltages; current through the device is nearly zero with zero gate voltage. Devices treated with **1**[14,15] consistently had threshold voltages of -4.5 ± 0.100 and on-off ratios as high as 10^8. Off current was approximately two orders of magnitude smaller for these devices than for the control ones, which is attributed to lower dielectric leakage currents at lower gate voltages. The subthreshold slopes measured for devices using **1** (as low as 0.2 V/decade) are only about 3 times the minimum value calculated for this parameter at room temperature,[18] and were among the lowest values reported to date for this class of OTFT. When comparing subthreshold slopes (S) between different experiments, it is important to recall that $S \propto C_{ox}/N_{trap}$ for $S \gg k_BT/q$, where C_{ox} is the dielectric specific capacitance, and N_{trap} the density of charge trapping states near the Fermi energy. Sharp subthreshold turn-on can be realized in devices using ultrathin dielectrics or high permittivity materials that increase C_{ox} without reducing N_{trap}. Devices with modest C_{ox} (i.e., thicker dielectrics) with improved S more clearly demonstrate a reduction in N_{trap}. Devices made using **2**, **3**, or **4** all had sub-threshold slopes in the range of about 0.5V/decade. However, whereas hole mobilities for **1** were on the order of 0.8 cm^2/Vs, devices made using **2**, **3**, or **4** showed strikingly improved mobilities, which were strongly SAMP structure dependent. In particular, average values measured for **4** (2.5 cm^2/Vs) are comparable to that reported widely for single crystal pentacene devices,[19] and are far better those reported for other polycrystalline pentacene devices.[20,21] It is especially significant that these improvements in mobilities were made without concomitantly sacrificing performance in terms of on/off ratios, sub-threshold slopes, or threshold voltages (**Figure 2**).

Typical saturation and linear transfer characteristics of transistors made using **4** are shown in Figure 2. In each case, the degree of hysteresis between on-off and off-on scans (in that order) is very small, indicating a low density of deep charge trapping states at the semiconductor/dielectric interface. The square root of the current is plotted on a linear scale for the saturation transfer curve. Above threshold, the plot is quite linear, indicating a near-constant mobility above a well-defined threshold voltage. The linear data are plotted in the lower panel on logarithmic and linear scales for $V_{ds} = -1$ V. Note here, too, the small degree of hysteresis and the excellent linearity of the transfer curve. Best and average (or typical) values of all metrics are reported in **Table 1**. It is interesting that linear mobilities are rarely reported in the literature for OTFTs, and when they are, they are typically half (or lower) that of saturation

Table 1. Comparative transistor performance data correlated with phosphonate molecular packing densities for **1**–**4**.

Dielectric Surface Treatment	Control	1	2	3	4
Highest saturation mobility (cm^2/Vs)	0.8	0.9	2.4	3.6	4.7
Average saturation mobility (cm^2/Vs) Threshold Range (V)	0.5	0.8	1.6	1.8	2.5
Highest linear mobility (cm^2/Vs, $V_{ds} = -1$V)	0.4	0.64	1.0	1.3	1.8
Average linear mobility (cm^2/Vs, $V_{ds} = -1$V)	0.3	0.41	0.61	0.82	1.4
Typical sub-threshold slope (V/decade)	1.0–2.2	0.2–0.5	0.5–0.7	0.4–0.6	0.4–0.6
Charge trap density ($\times 10^{-12}/cm^2$)	5.2–6.7	0.5–1.7	1.7–2.6	1.3–2.0	1.3–2.0
Threshold voltage range (V)	−5 to +10	−3 to −4	−4 to −5	−4 to −5	−3 to −4
Typical On/off ratio	10^6	10^7	10^7	10^7	10^7
Phosphonate packing density by QCM (nmol/cm^2)		0.33	0.33	0.27	0.15
Molecular footprint by QCM (Å^2/molecule)		49	51	61	79
Calculated molecular footprint (Å^2/molecule)		58	55	71	105

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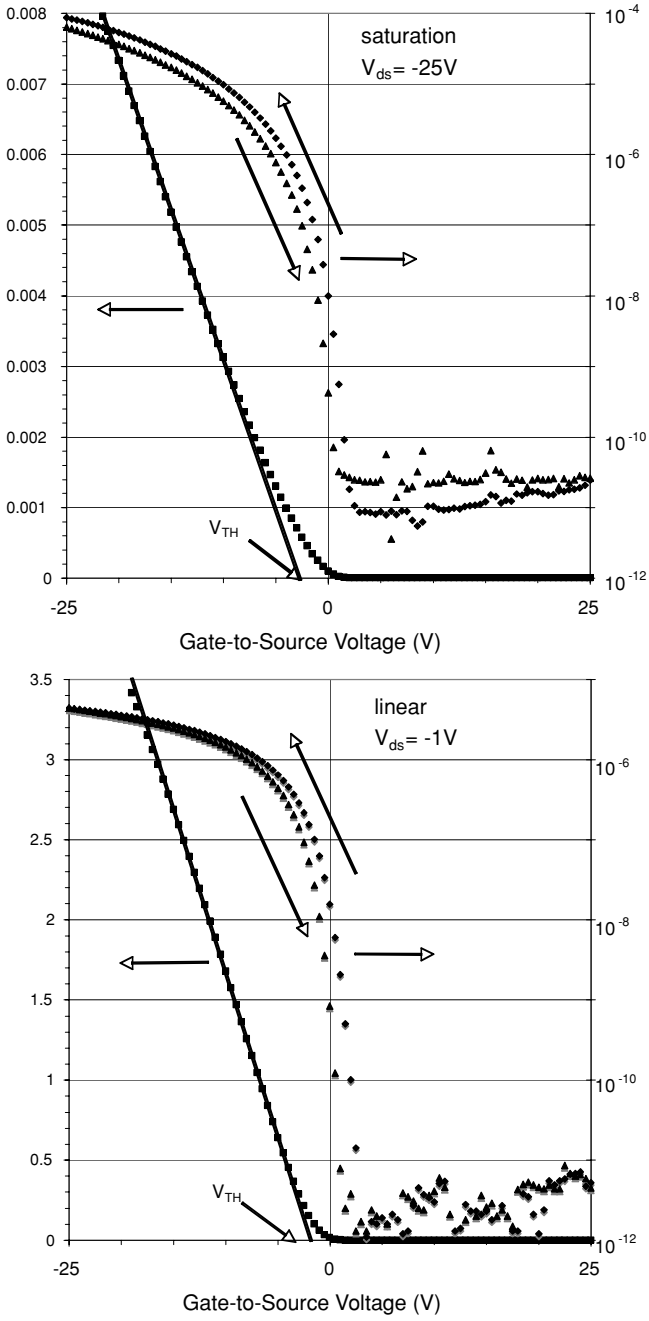

Figure 2. Transfer curves for a typical 9,10-dinaphthylanthracene-2-phosphonate/pentacene (**4**) transistor; W/L = 3.75. Top: saturation region, $V_{ds} = -25$V. Bottom: linear region, $V_{ds} = -1$V. In both cases, On-to-Off and Off-to-On scans (collected in that order) are shown.

mobilities.[22–24] Several explanations for these lower linear mobilities have been proposed; these include contact resistance, (in plane) field dependent mobilities, and short channel effects. The calculation of these lower mobilities may even be due to limitations in the applicability of the ideal field-effect transistor equations that are used to analyze OTFT data. We measured ratios of saturation to linear mobilities for devices built on **2**, **3** and **4**; they are comparable to those in the literature, and linear mobilities measured on devices using **4** are the highest that we are aware of.

The origin of the superior performance of devices built on **4** was probed. Contact angles for water wetting of SAMPs **2**, **3** and **4** were nearly the same. Therefore, since any differences in surface energy among these films are negligible, surface energy considerations cannot account for the marked differences in performance measured for devices based on these various monolayers. Indeed, our previous work on *n*–alkylphosphonate-treated pentacene-based transistors[5] showed that a simple relationship between surface energy of the monolayer and carrier mobility of the device does not exist: The contact angle increases monotonically with the length of the carbon chain from 6 to 18, but devices fabricated on C_8-phosphonate and C_{10}-phosphonate monolayers had the highest mobilities; in some cases mobility approached 2 cm^2/Vs.[5] In that work, we proposed that, because the degree of disorder in the *n*-alkylphosphonate monolayer varies with chain length,[25] less well-ordered short chain monolayers might yield a beneficial density of pentacene grain nucleation sites.

Structural features of the SAMPs, themselves, seem to be the dominant factors. As shown in Table 1, gravimetrically measured loadings on the SiO_2 surface decrease substantially as the lateral dimensions of the film constituent molecules increase from **2** to **4**; these measured surface loadings translate into geometrical projections of molecular "footprints" on the surface and provide a direct measure of film molecular compactness and spacing between the anthracenyl units (which are oriented about 60° from the surface normal). A comparison between these measured "footprints"[15] and calculated ones for **3**[26] and **4** as given in Table 1 provides a further indication of possible overlap of lateral phenyl and naphthyl groups, respectively (**Figure 3**): the better matched the calculated and measured footprints, the poorer the lateral group overlap, and *vice versa*.

An observation was made by AFM that we propose sheds light on the impact of changing SAMP structure on hole mobility. The lateral dimensions of the pentacene domains in **1** and **2** appear to be narrower, with a dendritic fern-like structure, than those in **4**, which appear to be thicker, less dendritic, and more densely packed (**Figure 4**). Such morphological changes are well known to affect hole mobility[21] and to be effected as a function

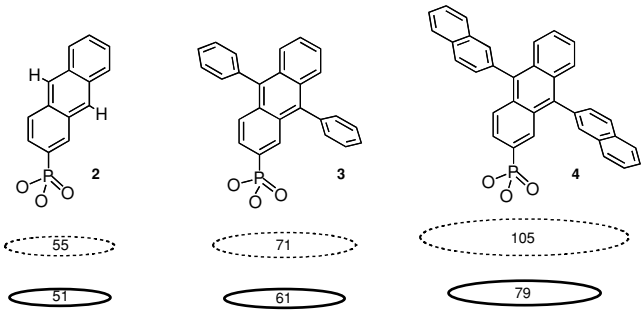

Figure 3. A comparison between calculated (dashed line) and quartz crystal microbalance (QCM) measured footprints (solid line), suggesting that for **3** and, especially, **4** spatial overlap of the lateral aryl groups of neighboring molecules can occur.

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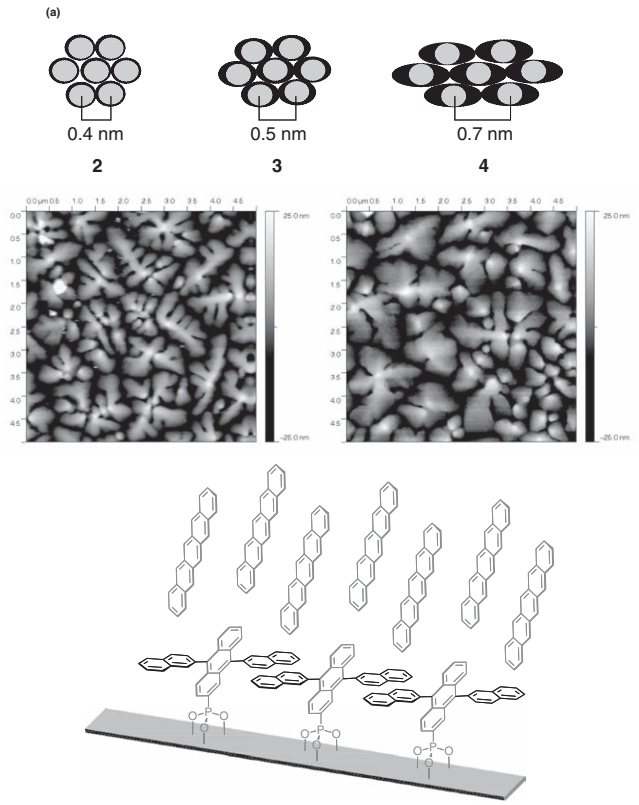

Figure 4. (a) A top view cartoon, showing how spacings of a close packed, two-dimensional monolayer can give rise to a three-dimensional template. The black oblongs represent the footprint of the SAMP constituent molecules, and the gray circles represent the vertical extension of the anthracenyl units. As the size of the 9,10- substituents increases, from H (**2**) to phenyl (**3**) to naphthyl (**4**) as shown in Figure 2, the footprints become larger and more oblate, but the anthracenyl units remain the same, which causes an increase in the anthracenyl-anthracenyl group spacing. (b) AFM images (5 μm × 5 μm) of 50 nm of pentacene on **2** (left) and **4** (right). (c) A side view cartoon showing that, at 0.7 nm template spacing between the anthracenyl phosphonate groups (gray) of **4**, pentacene (also gray) can intercalate into the SAMP. The 9,10-naphthyl substituents (black) are tilted by about 60° with regard to a surface normal.

of variation in pentacene deposition conditions.[21,27] In marked contrast, for **1**–**4** all pentacene deposition conditions were identical; thus we suggest that the different pentacene morphologies that we observe on **1** and **2** versus **4** are not only responsible for the changes in device behavior measured based on them, but that these different morphologies are a consequence of changes in the molecular structure in the underlying SAMPs.

Pentacene molecules vapor deposited onto a SiO_2 substrate "stand up" lengthwise on the surface to maximize the intramolecular herringbone interaction in which C-H bonds of one molecule interact with the π-system of a neighbor;[28] pentacene deposited onto an ordered film formed from octadecyltrichlorosilane also "stands up."[29,30] In our surface structural model based on QCM measurements, anthracenyl units in SAMPs of **2** or **3** are closely packed; this might allow for nucleation of pentacene crystallites through C-H bond π interactions that give rise to a typical herringbone pattern for the first layer of pentacene molecules nearly normal to the dielectric surface. In marked contrast to **2** and **3**, however, QCM measurement-based calculated spacing between the anthracenyl units in **4** is about 0.7 nm, which would create channels in the SAMP that are on the order of the "thickness" of an aromatic π system. Thus this spacing might allow for intercalation of pentacene units into these gaps; such intercalation could also involve C-H bond-π interactions between the pentacene and the lateral naphthyl groups of **4**, but also favor a π-stacking motif for this first pentacene layer. In short, we hypothesize that, whereas a closely packed film surface on an oxide (as in **2** or **3**) may simply convert the two-dimensional surface of the oxide into a two-dimensional surface of an organic, the increased molecular spacing in **4** could convert the two-dimensional surface of the oxide into a *three-dimensional* lattice that contains nucleation sites for pentacene growth (Figure 4). According to our hypothesis, this pentacene nucleation induces the growth of the large crystalline domains that we observe for pentacene vapor deposited on **4** by AFM. Further structural characterization of pentacene deposition onto **2**, **3**, and **4** is now under way.

Experimental Section

General considerations for transistor fabrication: Pentacene thin-film transistors (TFTs) were fabricated either on SAMP-treated or bare (control) SiO_2 substrates. All used heavily doped Si (Encompass Distribution, boron doped, <0.005Ω·cm) with a 100 nm thermally grown SiO_2 layer. The dielectric thickness was chosen as a compromise between a thicker one that would reduce electrical shorts through it and a thinner one that would yield reduced operating voltages and improve subthreshold performance. All substrates were subjected to the same cleaning procedure: 3 min in boiling trichloroethylene (TCE); 3 min in acetone; 3 min in boiling methanol; and blow dry with compressed air. For each pentacene deposition run, either one SAMP-treated sample and one control sample or two samples treated with different SAMPs were placed side-by-side in a vacuum deposition system (base pressure 1×10^{-6} torr) so that deposition conditions were identical for each pair. Pentacene was deposited through a shadow mask to a thickness of 500 Å, at ≈ 0.1 nm sec^{-1}, with substrates heated to approximately 70 °C. Patterning of the pentacene layer was done to reduce leakage currents between adjacent transistors. Gold source and drain electrodes were deposited, at approximately 1 Å sec^{-1}, through a shadow mask to a thickness of 500 Å, with the substrate at (nominally) room temperature. Arrays of transistors were fabricated with channel widths ranging from 0.5 to 1.5 mm and channel lengths ranging from 25 μm to 250 μm, allowing study of transistors with a range of W/L ratios, as shown in the overlaid shadow mask outlines previously described.[14] In general, between 50 and 100 transistors were tested for each type of SAMP and for the controls.

General method for preparing SAMPs of phosphonoanthracenes on SiO_2/Si: SAMPs were formed from a solution of the phosphonoanthracene in anhydrous THF (2.5 μM) by five cycles of T-BAG treatment[12,13] and heating (120 °C for 24 hours under argon). Any residual multilayer was removed after this heating step by solvent rinsing and gently wiping. Negligible changes in QCM frequencies were measured between the fourth and fifth T-BAG cycles, so film coverage was considered to be complete at that point. Films prepared under these conditions were surface conforming and had essentially no pin holes as determined by AFM; to estimate film thickness, incomplete films were intentionally prepared by one T-BAG cycle using 1.0 μM solutions. SAMP film quality was also evaluated by water wetting contact angle (Θ), RAIRS, XPS, and QCM (packing density) analyses.

SAMP of anthracene-9-phosphonate[14,15] *(1) on SiO_2/ Si*: Θ = 94°; film thickness by AFM: 0.40 nm (we erred in our earlier report[15] of the film thickness of [anthracene]phosphonate to be 0.95 nm because we

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neglected considerations of substrate surface roughness); RAIRS: $\nu_{P-O} \approx 1100\ cm^{-1}$, no peak for free phosphonic acid; XPS (P2s = 193 eV); QCM: 0.33 nmol/cm^2.

SAMP of Anthracene-2-phosphonate (2) on SiO_2/Si: $\Theta = 104°$; film thickness by AFM: 0.80 nm; RAIRS: $\nu_{P-O} \approx 1022\ cm^{-1}$, no peak for free phosphonic acid; QCM: 0.33 nmol/cm^2.

SAMP of 9,10-diphenylanthracene-2-phosphonate (3) on SiO_2/Si: $\Theta = 104°$; film thickness by AFM: 0.75 nm; RAIRS: $\nu_{P-O} \approx 1018\ cm^{-1}$, no peak for free phosphonic acid; QCM: 0.27 nmol/cm^2.

SAMP of 9,10-dinaphthylanthracene-2-phosphonate (4) on SiO_2/Si: $\Theta = 102°$; film thickness by AFM: 0.75 nm; RAIRS: $\nu_{P-O} \approx 1023\ cm^{-1}$, no peak for free phosphonic acid; QCM: 0.15 nmol/cm^2.

Fifty nanometer thick pentacene films deposited on each SAMP were imaged using contact mode AFM (Agilent AFM 5500, cantilevers: Veeco probes MLCT ~0.1 N/m, scan speed: 1–2 Hz). Images were post-processed using Gwyddion (gwyddion.net). The pentacene films were deposited at ~0.1 nm sec^{-1} with the substrate temperature held at 70 °C. Differences in morphology (grain size and shape) were analyzed to determine correlations between film morphology and electrical properties.[21,29,31]

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Supporting Information

Supporting Information is available online from Wiley InterScience or from the authors.

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