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# Controllable Shifts in Threshold Voltage of Top-Gate Polymer Field-Effect Transistors for Applications in Organic Nano Floating Gate Memory

By Kang-Jun Baeg, Yong-Young Noh,\* Henning Sirringhaus,\* and Dong-Yu Kim\*

Organic field-effect transistor (FET) memory is an emerging technology with the potential to realize light-weight, low-cost, flexible charge storage media. Here, solution-processed poly[9,9-dioctylfluorenyl-2,7-diyl]-co-(bithiophene) (F8T2) nano floating gate memory (NFGM) with a top-gate/bottom-contact device configuration is reported. A reversible shift in the threshold voltage ( $V_{Th}$ ) and reliable memory characteristics was achieved by the incorporation of thin Au nanoparticles (NPs) as charge storage sites for negative charges (electrons) at the interface between polystyrene and cross-linked poly(4-vinylphenol). The F8T2 NFGM showed relatively high field-effect mobility ( $\mu_{FET}$ ) ( $0.02 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ ) for an amorphous semiconducting polymer with a large memory window (ca. 30 V), a high on/off ratio (more than  $10^4$ ) during writing and erasing with an operation voltage of 80 V of gate bias in a relatively short timescale (less than 1 s), and a retention time of a few hours. This top-gated polymer NFGM could be used as an organic transistor memory element for organic flash memory.

## 1. Introduction

Organic and polymeric materials are very attractive for the individual components of many electronic device as active semiconductors, dielectrics, and electrodes that offer unique advantages over their inorganic counterparts.<sup>[1]</sup> These materials enable the deposition of uniform thin films, using simple and inexpensive solution processes, such as spin-coating,<sup>[2]</sup> inkjet printing,<sup>[3,4]</sup> screen printing,<sup>[5,6]</sup> and micro-contact printing.<sup>[7,8]</sup> Although organic materials are not currently suitable for electronics that require high-end performance, the advantages in the manufacturing process make them ideal for large-area, flexible, transparent, and disposable electronic devices, such as organic light-emitting diodes (OLEDs),<sup>[9]</sup> organic field-effect transistors (OFETs),<sup>[10–12]</sup> organic

photovoltaic cells (OPVs),<sup>[13–15]</sup> chemical and photo sensors,<sup>[16,17]</sup> and radio frequency identification (RFID) tags.<sup>[18]</sup> Organic nonvolatile memory (ONVM) is another emerging research field and a key area of application that is based on the advantages of organic materials. Progress has been made recently with a variety of approaches including cross-point-type organic bistable devices and organic transistor-based memory.<sup>[19–28]</sup>

Among the many possible device configurations for organic memory, OFET-based memory is considered a promising candidate for realization of the ultimate goal of organic flash memory because of its nondestructive read-out, complementary integrated circuit architectural compatibility, and single transistor realization.<sup>[26]</sup> Three classes of OFET-based memory have been researched to date: i) floating gate OFET memory, ii) polymer electret OFET memory, and iii) ferroelectric OFET memory.<sup>[19]</sup> To realize high-performance polymer electret and ferroelectric OFET memory, polymer electrets or ferroelectric materials must show both robust mechanical properties as a gate dielectric, and stable charge storage or dipole polarization as a memory element. It is technically difficult to find a suitable ferroelectric polymer that has both properties,<sup>[29]</sup> and to reduce the operating voltage without gate leakage in the polymer electret memory for stable charge storage.<sup>[26]</sup>

Floating-gate OFET memories with metal nanoparticles (NPs) embedded in the gate dielectric, in other words, organic nano floating gate memory (NFGM), is an alternative way to realize

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organic flash memory devices. While a variety of bistable organic memories using metal nanostructures between cross-point electrodes has been researched (Y. Yang et al. have published extensively on charge storage in metal NPs<sup>[20,30,31]</sup>), only limited research has been reported using Au NPs in OFET structures.<sup>[32–34]</sup> Furthermore, the reported transistor memory performance does not fulfill the criteria required for practical applications, while cross-point bistable devices have progressed recently and are now approaching a level of performance that is competitive with their inorganic counterparts.<sup>[35]</sup>

NFGM devices operate via a channel conductance change by stored charges in metal NPs, which cause reversible shifts in the threshold voltage ( $V_{Th}$ ) of OFETs. The NFG structure can therefore be utilized not only for the nonvolatile transistor memory, but also as an effective method for control of  $V_{Th}$  in OFET devices. It is necessary to intentionally control the device operation modes for practical applications. Pseudo complementary metal-oxide semiconductor (CMOS) circuits can be fabricated from transistors of one carrier type, and the sensory properties of OFETs can be optimized or diversified<sup>[36]</sup> like ion implantation techniques in silicon metal-oxide semiconductor FETs (MOSFETs). NFG is considered to be one promising strategy to achieve control of channel conductance or charge carrier density, similar to a self-assembled monolayer and polarizable gate dielectrics.<sup>[37,38]</sup>

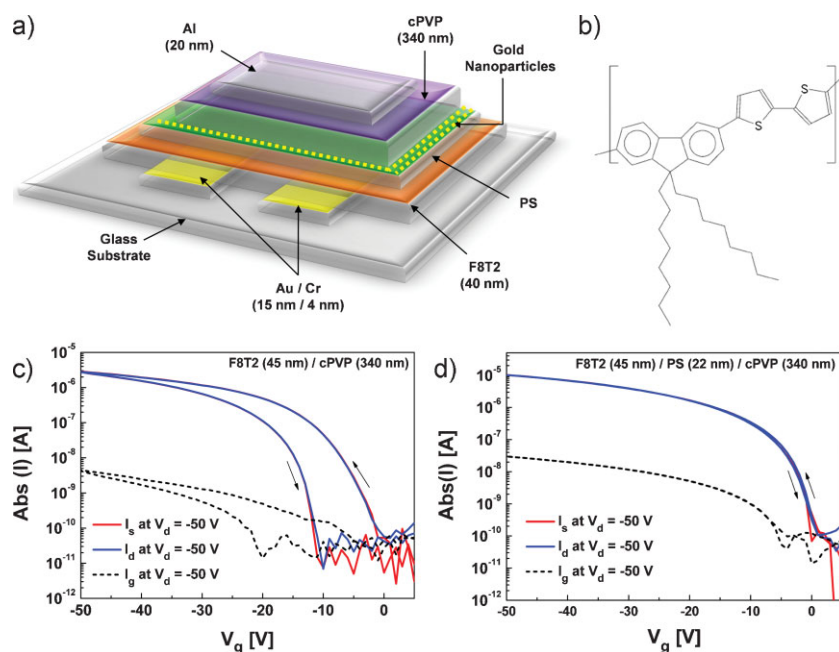
Here we report on a solution-processed poly[9,9-dioctylfluorenyl-2,7-diyl]-co-(bithiophene)] (F8T2) NFGM with a top-gate/bottom-contact (TG/BC) device configuration. The TG/BC configuration provides many crucial advantages over other device structures, such as easy formation of the gate line by direct printing, auto-encapsulation of relatively sensitive organic semiconductors by the gate electrode and gate dielectric deposited on top, and reduction of contact resistance for charge injection from source/drain electrodes into the semiconductor.<sup>[39]</sup> By embedding Au NPs at the interface between a layer of polystyrene (PS) and a layer of cross-linked poly(4-vinylphenol) (cPVP) used as charge injection and current blocking gate dielectrics, respectively, the  $V_{Th}$  of the polymer FET devices could be reversibly and systemically controlled by the application of external gate fields. The reversible shift in the  $V_{Th}$  could be utilized as polymer NFGM or tuning of transistor operation modes, the reversible shifts mainly originated from negative charge trapping in the Au NPs. The F8T2 NFGM showed a relatively high field-effect mobility ( $\mu_{FET} = 0.02 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ ) for an amorphous polymer with a large memory window (ca. 30 V), a high on/off ratio (more than  $10^4$ ) during writing and erasing with an operation voltage of 80 V of gate bias in a relatively short timescale (less than 1 s), and a retention time of a few hours.

## 2. Results and Discussion

For fabrication of the floating-gate organic transistor memory, TG/BC polymer FETs were

fabricated on glass substrates. F8T2 was used as the active channel layer because of its reliable p-channel FET properties and good stability in ambient air (Fig. 1b). Bilayered gate dielectrics with layers of PS and cPVP were spin-cast onto this F8T2 layer using orthogonal solvents. A detailed description of the fabrication process is given in the Experimental Section. The complete device is represented in Figure 1a. All F8T2 FETs showed typical p-channel transistor behavior. However, the characteristics of the OFETs were very dependent on the existence of the thin PS intermediate layer between the cPVP and F8T2. F8T2 FETs without the PS layer showed relatively low  $\mu_{FET}$  (ca.  $3.1 \times 10^{-3} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ ). Such values can commonly be obtained in devices with amorphous semiconducting polymers.<sup>[40]</sup> Moreover, the devices showed a large drain current hysteresis between forward and reverse gate bias scan (Fig. 1c). This could be attributed to the trapping of positive holes under accumulation conditions, either in the semiconductor states or in the gate dielectric at the interface.<sup>[41,42]</sup> It should be noted that the cross-linking of cPVP took place in the presence of moisture in air, and occurred very rapidly during spinning of the PVP solution.<sup>[43]</sup> Furthermore, a negative shift of the transfer curves during a subsequent second gate voltage scan was also observed. This behavior means that the interfacial energy states were relatively deep traps that prevented rapid detrapping during the timescale of the measurement.

The F8T2 FET characteristics were significantly improved by the introduction of a 22 nm thick PS intermediate layer between F8T2 and cPVP. The  $\mu_{FET}$  was increased by an order of magnitude up to ca.  $0.025 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$  and gate bias stress effects were much reduced (no hysteresis behavior and little shifts in the transfer

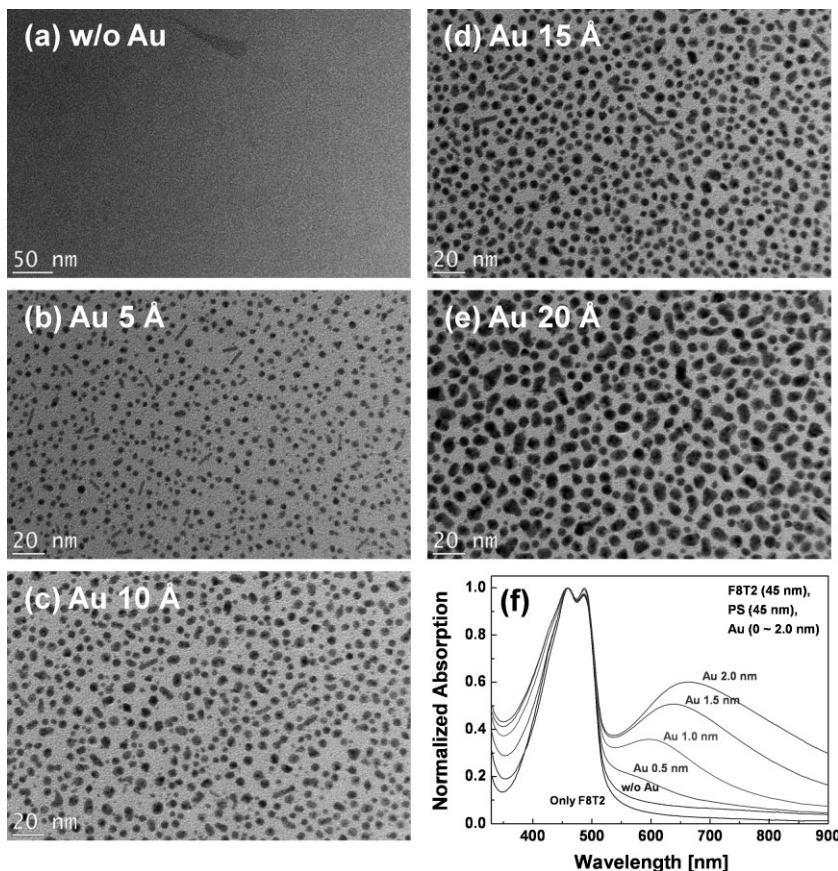


**Figure 1.** a) Schematic device configuration of a top-gate/bottom-contact polymer field-effect transistor and b) chemical structure of F8T2. Transfer characteristics of a F8T2 FET with length,  $L = 20 \mu\text{m}$ , and width,  $W = 1 \text{ mm}$  c) without a PS intermediate layer (dielectric capacitance of total dielectrics,  $C_i = 16 \text{ nF cm}^{-2}$ ), and d) with a 22 nm thick PS intermediate layer (total  $C_i = 13.9 \text{ nF cm}^{-2}$ ). The gate, source, and drain currents and the drain voltage are indicated by  $I_g$ ,  $I_s$ ,  $I_d$ , and  $V_d$ , respectively.

curves during subsequent gate potential,  $V_g$ , sweeps; Fig. 1d). The improvement of performance via insertion of a PS layer can be explained by i) a reduction of the energetic distribution of the trap states at the interface, and ii) passivation of the interfacial deep traps by the PS layer. It is known that high- $k$  insulators ( $k$  = dielectric constant) can adversely affect the charge carrier mobility, because they usually have randomly oriented dipoles near the interface, which increase the energetic disorder of trap states in the semiconductor.<sup>[44,45]</sup> The measured dielectric constants for PS and cPVP were approximately 2.6 and 6.2, respectively.

A  $V_{th}$  shift in the positive direction is more desirable than a shift in the negative direction for the utilization of p-channel OFETs as an element for floating-gate organic flash memory because an external gate bias is not required to read the programmed (high drain current  $I_d$  value) and erased states (low  $I_d$  value). The data reading at zero  $V_g$  enables low power consumption and reliable data storage, since no destructive high electric field is necessary. Although the F8T2 FETs with the PS intermediate layer showed good p-channel FET characteristics, we were unable to induce significant positive  $V_{th}$  shifts and reliable memory characteristics like those previously observed for pentacene FET memory with PS and SiO<sub>2</sub> double-layered dielectrics.<sup>[26,27]</sup> The absence of charge trapping in PS and cPVP double-layered dielectrics is explained in the Supporting Information (SI) as an aspect of the relationship between charging current and leakage current.

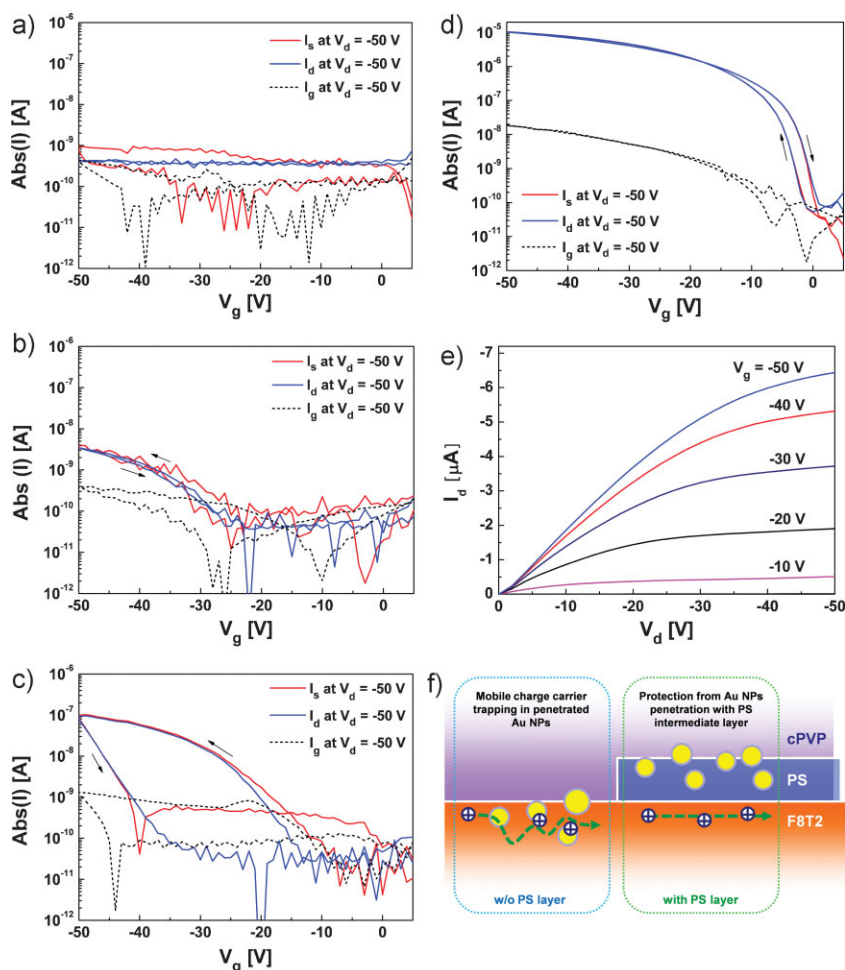
For the generation of charge storage sites, nanosized Au clusters were introduced by a thermal evaporation process at the interface between the PS and cPVP layers. The Au nanoclusters were selectively deposited in the transistor active region by shadow masking. A distinct color change in optical microscopy images clearly showed the existence of the 1 nm thick Au layer (Fig. S2 in SI). The existence and size distribution of Au clusters were also verified by transmission electron microscopy (TEM) and UV-vis absorption spectroscopy. TEM images showed that increasing the thickness of Au thermal deposition also increased the size of Au NPs from about 2 nm to more than 10 nm (Fig. 2a–e). Initially, small and sparsely distributed Au NPs were gradually coarsened and distributed more closely; they nearly came into contact with one another at an Au film thickness above 2.0 nm. The increased content of Au with increasing thickness was also clearly verified by energy dispersive spectroscopy (EDS; Fig. S3, SI). No Au absorption peak was observed from a bare sample (only typical F8T2 absorption peaks), but Au absorption peaks became evident as the thickness of deposited Au increased from 0.5 to 2.0 nm (Fig. 2f). Moreover, the absorption maxima of Au peaks were significantly red-shifted about 100 nm as the thickness of Au increased, due to localized surface plasmon resonance (LSPR), a well-known phenomenon.<sup>[46,47]</sup>



**Figure 2.** TEM images a) without Au, and after thermal evaporation of b) 5, c) 10, d) 15, and e) 20 Å of Au. f) UV-vis absorption spectroscopy with different sizes of Au NPs.

To identify the minimum thickness of the PS charge injection dielectric, TG/BC F8T2 FETs were fabricated with different PS thicknesses deposited on 1 nm thick Au. Very poor OFET performance was observed without the PS layer (Fig. 3a). This result might be explained by the penetration of Au atoms into the F8T2 thin film during the thermal deposition process. Noble metal atoms, such as Au, are known to penetrate deeply into the polymer layer during the evaporation process because the penetration depth of metal atoms into polymer films is generally inversely proportional to the reactivity of the metal atom.<sup>[48]</sup> Mobile charge carriers (holes) are easily trapped by Au impurities in the organic semiconductor film. The metal penetration into the organic semiconductor layer and its dramatic effect on charge transport is consistent with previous studies.<sup>[48,49]</sup> The OFET characteristics were significantly improved by the introduction of the PS as soon as a critical layer thickness was exceeded. The F8T2 FETs showed poor characteristics with PS layers under 25 nm thick. Only slight improvements were observed for a 22 nm thick PS layer, compared to a 10 nm thick film, indicating insufficient protection of the F8T2 active layer against Au penetration (Fig. 3b,c). Fully recovered characteristics were obtained with a PS layer at least 45 nm thick (Fig. 3d,e). The measured  $\mu_{FET}$  of F8T2 FETs with a 45 nm thick PS layer and 1 nm thick Au was  $0.02 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ , and the on/off ratio was more than  $10^5$ . A schematic diagram for this protection effect





**Figure 3.** Transfer characteristics of a F8T2 FET with  $L = 20 \mu\text{m}$  and  $W = 1 \text{ mm}$  after deposition of 1 nm thick Au, a) without PS ( $C_i = 16 \text{ nF cm}^{-2}$ ), b) with 10 nm thick PS ( $C_i = 15 \text{ nF cm}^{-2}$ ), c) with 22 nm thick PS ( $C_i = 13.9 \text{ nF cm}^{-2}$ ), d) with 45 nm thick PS intermediate layer ( $C_i = 12.2 \text{ nF cm}^{-2}$ ). e) Output characteristics of F8T2 FET with 45 nm thick PS layer. f) Schematic demonstration of charge transport mechanism.

exerted by the PS dielectric layer against Au penetration is shown in Figure 3f.

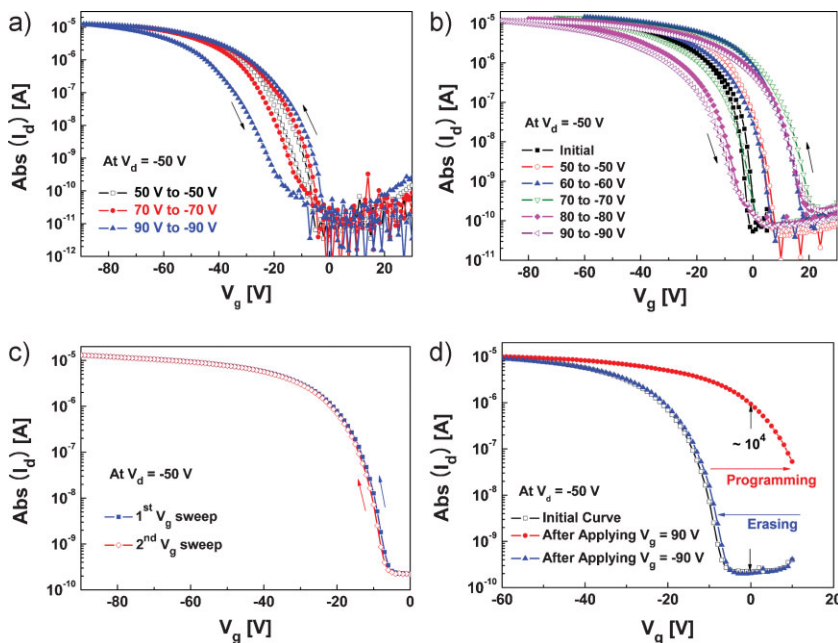
No positive shifts in the transfer curves of F8T2 FETs without Au NPs were observed under positive gate bias stress when the transfer curve started at a large positive gate bias (Fig. 4a). When the Au NPs were embedded between the PS and cPVP dielectric layers, however, we observed a reproducible positive shift of the transfer curves by more than 20 V (Fig. 4b). The magnitude of the  $V_{\text{Th}}$  shifts was investigated by varying the range of the gate voltages applied during the transfer curve. During the  $V_g$  sweep from 50 to  $-50 \text{ V}$ , the initial transfer curves were shifted by about 7 V to more positive values, but this shift did not return to its original state when negative gate voltages were applied during the transfer curve (no significant hysteresis behavior using organic transistor memory). More positive shifts were observed during the  $V_g$  sweep from 60 to  $-60 \text{ V}$ , which also did not completely recover to its initial state on the reverse scan from negative to positive gate voltages. However, a complete recovery during the reverse scan was obtained by applying  $V_g$  from 70 and  $-70 \text{ V}$ . Application of

$V_g = -70 \text{ V}$  erased the memory effect. It should be noted that the magnitude of positive shift in  $V_{\text{Th}}$  was not increased further by the application of more than 70 V of positive gate bias. This result might be explained by the limited number of charge storage sites, i.e., the number of thermally evaporated Au nanoclusters. Notably, the shift in the transfer curve was not observed during successive  $V_g$  scans from 0 to  $-90 \text{ V}$ , indicating that there is negligible negative gate bias stress in F8T2 FET devices with Au NPs (Fig. 4c). However, the transfer curves shifted significantly in a positive direction with the application of 90 V for a short time, below 1 s (Fig. 4d). The shifted transfer curve returned to its initial state with the application of a reverse negative gate bias ( $-90 \text{ V}$ ). The shifts in  $V_{\text{Th}}$  were reproducible and fully reversible. Therefore, this OFET device can be utilized in organic nonvolatile memory applications.

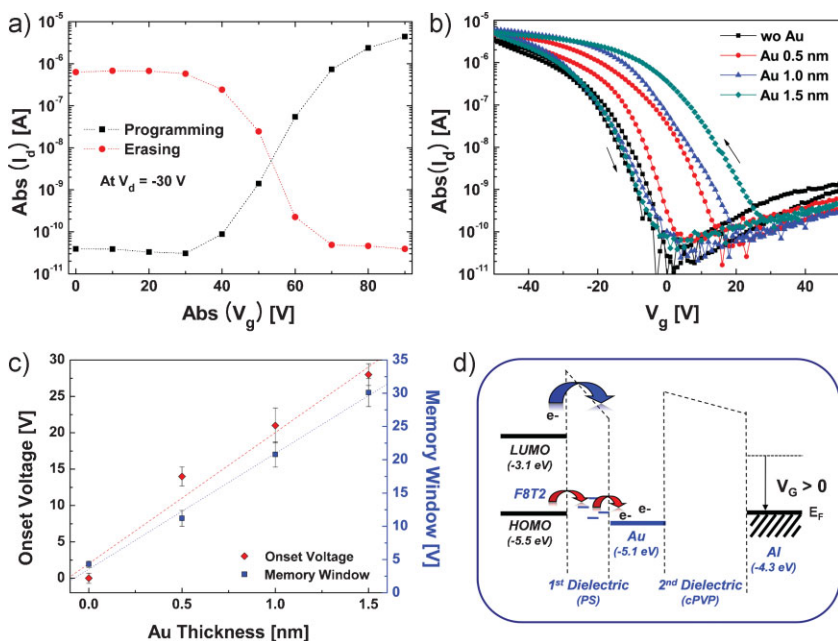
The drain current  $I_d$  was also measured at  $V_d = -30 \text{ V}$ ,  $V_g = 0 \text{ V}$ , after applying a positive gate bias  $V_g$  for about 1 s, in order to determine the accurate voltage range required for complete programming and erasing. In a typical measurement,  $I_d$  was found to increase strongly for gate programming voltages above 40 V and to saturate  $V_g > 80 \text{ V}$  (Fig. 5a). In the erasing process, on the other hand, the initially high current state of the F8T2 FET devices was returned to the off-current state above erase voltages of  $V_g = -40 \text{ V}$ . Within a range of 20 V of erase voltage, the drain current changed dramatically, by more than  $10^4$ . Complete erasing was observed above  $V_g = -70 \text{ V}$  (Fig. 5a). These results mean that application of +80 and  $-70 \text{ V}$  of  $V_g$  were necessary for complete writing and erasing in the NFGM. The programming and erasing characteristics obtained by applying pulsed gate voltage were

very similar to those obtained by continuous  $V_g$  scanning (Fig. 5b). This result indicates that the reversible shift of the transfer curve was mainly affected by the magnitude of the applied gate bias as opposed to the detailed waveform and duration of the bias stress. No further change in  $I_d$  was observed by applying a  $V_g$  higher than  $\pm 80 \text{ V}$ , because of the limited of charge storage sites created by deposited Au NPs. The effect of the number of charge storage sites on memory performance was investigated by measuring the characteristics of devices with different Au thicknesses. The memory window (the shifted range of the transfer curve with application of an appropriate programming and erasing gate bias) and the onset voltage of F8T2 FETs increased linearly with Au thickness proportional to the amount of deposited Au NPs (Fig. 5c). These results clearly show that the reversible and controllable shifts in  $V_{\text{Th}}$  mainly originate from the deposition of Au nanoclusters and trapping of negative charge carriers in the Au NPs under positive gate bias.

In a bilayered gate dielectric with a combination of relatively nonpolar (first layer,  $\epsilon_{\text{r,PS}} = 2.6$ ) and polar dielectrics (second layer,



**Figure 4.** Transfer characteristics of a F8T2 FET, a) without and b) with Au 1 nm thermal evaporation. The  $V_g$  sweeps ranged from 50 (–50) to 90 V (–90 V). c) Reproducible transfer characteristics, where first and second  $V_g$  sweeps were scanned from 0 to –90 V successively. d) Reversible shifts in transfer curves of F8T2 FET memory devices after application of gate bias for a relatively short time, about 1 s.



**Figure 5.** a) Programming and erasing characteristics of F8T2 FET memory devices. The drain currents were measured after application of different gate bias from 0 to 90 V and from 0 to –90 V for programming and erasing, respectively. b) Transfer characteristics of F8T2 FET devices after thermal evaporation of different thicknesses of Au, from 0.5 to 1.5 nm, when  $V_g$  were swept from 90 to –90 V. c) Change of onset voltages and the amount of memory window for polymer transistor memory. d) Schematic demonstration of a potential operation mechanism of floating-gate F8T2 FET memory devices.

$\epsilon_{\text{r,cPVP}} = 6.2$ ), the electric field is inversely proportional to the dielectric constant of the materials.<sup>[50,51]</sup> This means that a higher electric field is present in the first dielectric than in the second layer. The applied electric field in the first gate dielectric layer can be calculated from the following equation.<sup>[50]</sup>

$$E_1 = \frac{V_g}{d_1 + d_2 \left( \frac{\epsilon_1}{\epsilon_2} \right)} + \frac{Q}{\epsilon_1 + \epsilon_2 \left( \frac{d_1}{d_2} \right)} \quad (1)$$

where  $Q$  is the (negative) stored charge on the Au NPs,  $\epsilon_i$  are the dielectric constants, and  $d_i$  is the thickness of the two dielectric layers. At the initial stage of memory operation ( $Q = 0$  and  $V_g = 70$  V), the gate fields obtained in PS and cPVP were estimated to be about 3.7 and 1.6 MV cm<sup>–1</sup>, respectively. These high electric fields at the PS tunnel dielectric led to efficient injection of the negative charge carrier from the semiconductor and trapping in Au NPs, which can be attributed to direct band-to-band tunneling or Fowler–Nodheim tunneling (Fig. 5d).

The trapped charges in Au NPs perturbed and modulated a subsequently applied gate field, resulting in substantial shifts in the  $V_{\text{Th}}$  by the amount of Equation 2:

$$\Delta V_{\text{Th}} = -\frac{d_i Q}{\epsilon_i} = -\frac{Q}{C_i} \quad (2)$$

where  $C_i$  is the dielectric capacitance of total dielectrics and  $\Delta V_{\text{Th}}$  is the memory window. From Equation 2, we calculated the total number of trapped charges at Au NPs to be  $1.5 \times 10^{12} \text{ cm}^{-2}$  at  $C_i = 12.2 \text{ nF cm}^{-2}$  and  $\Delta V_{\text{Th}} = 20$  V for devices with 1 nm thick Au NPs. The calculated number of trapped charges was strongly correlated with the number density of Au NPs, which was estimated by TEM images. Figure 2c shows that, on average, five Au NPs were present within a 400 nm<sup>2</sup> area. From this rough estimation, we concluded that  $1.25 \times 10^{12} \text{ cm}^{-2}$  were embedded between the PS and cPVP. This number indicates that an average of one to two electrons was stored in one Au NP, and further electrons were not trapped in the charged Au NPs. In order to consider the Coulomb blockade effect in Au NPs, we roughly calculated the charging energy of the second electron,  $e^2/2C_1$ , in the charged Au NPs (where  $e$  is the elementary charge and  $C_1$  is the self-capacitance of Au NP, including the capacitance of the first dielectric layer). The charging energy was relatively smaller than the thermal energy at room

temperature ( $k_B T$ ;  $k_B$  and  $T$  are the Boltzmann constant and temperature, respectively), indicating no Coulomb blockade effect at room temperature. Therefore, the absence of further  $\Delta V_{Th}$  (saturation behavior of the memory windows) at  $V_g$  over  $\pm 80$  V might be due to an increase in leakage current and removal of the storing charge at high  $V_g$ . The limited charge density stored in Au NPs means that the number density of Au NPs must be increased to obtain a larger memory window and  $\Delta V_{Th}$ . However, the thermal evaporation of gold is not a suitable method to increase the density of embedded Au NPs, since the size of Au NPs simply increases via Ostwald ripening as film thickness increases. For the erasing process, the trapped charges in Au NPs were detrapped by applying a high reverse  $V_g$ . The detrapping process could take place either by direct electron injection from Au NPs to the F8T2 semiconductor or by positive charge injection in the PS and recombination with electrons trapped in Au NPs.

The trapped charges in Au NPs exhibited rapid relaxation characteristics. We observed that the shifted transfer curves returned to their original states after a few hours (not shown here). This relatively rapid relaxation of trapped charges can be explained by the relatively high bulk and surface conductivity of the second gate dielectric (cPVP). cPVP has moderately hydrophilic properties and exhibits high bulk and surface conductivity due to its polar dipole moments, residual mobile ions, and adsorbed moisture, which can lead to a rapid relaxation of trapped charges.<sup>[27]</sup> Typically, other memory devices with PVP dielectrics have shown poor characteristics, specifically a relatively short retention time, due to its poor insulating property.<sup>[27,33]</sup> Nevertheless, the main reason for using cPVP as a blocking dielectric is the ease with which an orthogonal solvent can be found to prevent dissolution and swelling of the underlying PS. Almost all popular hydrophobic polymer dielectrics, e.g., poly(methyl methacrylate), dissolve in similar solvents. The Coulomb repulsion between electrons confined in NPs could also be considered as the origin of the rapid charge decay phenomenon.<sup>[52]</sup>

The polymer NFGM devices were also fabricated on a flexible plastic substrate (polyethylene naphthalene—PEN, Tenjin Dupont; Fig.S4, S1). The memory devices operated well, like those on a glass substrate. By application of high gate fields ( $+70$  to  $-70$  V of  $V_g$  sweep), the flexible NFGM device with 1 nm thick Au thermal deposition showed a memory window and an on/off ratio of ca. 40 V and  $10^3$ , respectively. This result demonstrates that the polymer transistor memory can be used for low-cost, flexible and light-weight low-end commercial applications. However, the NFGM device still has two main challenges to be overcome: a relatively short retention time and a high operating voltage. The short retention time could be improved by more adequate selection of robust hydrophobic injection and blocking dielectrics, with ultralow leakage characteristics and careful lamination. The operating voltage is related to the capacitance and thickness of the dielectric materials. The operating voltage was reduced below 30 V using a thinner film of blocking dielectrics (100 nm thick cPVP), but the thickness of the injection dielectric (PS) must be also reduced to achieve a further reduction in working voltage. However, there are clear limitations on the use of very thin injection dielectrics, associated with penetration of the metal or generation of pinholes. One promising idea to overcome this problem is to utilize metal NPs embedded into a diblock copolymer as a gate dielectric for organic NFGM.<sup>[53]</sup> In this system, charge

storage sites, i.e., metal NPs, are only present on one block of a diblock copolymer, which prevent current percolation paths through randomly distributed metal NPs in the dielectric matrix. Investigations to resolve these issues are ongoing.

### 3. Conclusions

In conclusion, a TG/BC F8T2 NFGM with a dual-gate insulator was successfully demonstrated, and the operating mechanism was discussed in detail. A reversible shift of  $V_{Th}$  and reliable memory characteristics were achieved by the incorporation of thin Au NPs as charge storage sites for negative electrons at the interface between PS and cPVP. This top-gated polymer NFGM could be used as an organic transistor memory element. We have also outlined future work, through which the retention time and operating voltage of these NFGM devices could be further improved.

### 4. Experimental

**Device Fabrication:** Corning Eagle 2000 glass slides were used as substrates after sequential cleaning in an ultrasonic bath with deionized water, acetone, and isopropanol for 10 min each. Chrome (adhesion layer, 5 nm) and gold (source/drain electrodes, 20 nm) patterns were fabricated using conventional photolithography. The patterns had a channel width ( $W$ ) of 1 mm and channel lengths ( $L$ ) of 2, 5, 10, and 20  $\mu\text{m}$ . The semiconducting polymer F8T2 (Dow Chem.) was dissolved in anhydrous mixed xylene ( $10 \text{ mg mL}^{-1}$ ). Semiconductor films were formed by a spinning process and dried at room temperature overnight in a  $\text{N}_2$  purged glovebox with no thermal annealing to completely remove the residual solvent. For fabrication of dual polymer gate dielectric layers PS (Fluka, molecular weight,  $\text{MW} = 1000000$ ) and PVP (Aldrich) were used without further purification. PS and PVP solutions were filtered via a 0.2  $\mu\text{m}$  polytetrafluoroethylene (PTFE) syringe filter and were spin-coated onto the semiconductor. The solvents of the PS and PVP overlayers must be selected carefully to avoid dissolution of the underlying semiconducting layer and the first dielectric polymer layer of PS during the spinning process of PS and cPVP, respectively. *N*-Butylacetate and 1-butanol were used as orthogonal solvents for PS and PVP, respectively. After spin-coating PS (first dielectric layer), a thin Au layer was thermally deposited at thicknesses of 0.5, 1.0, 1.5, and 2.0 nm in a high-vacuum chamber, and subsequently thermally annealed at 100  $^\circ\text{C}$  for 10 min for the formation of Au NPs. The cPVP layer was also spin-coated onto the PS film with Au NPs in air. 1,6-Bis(trichlorosilyl)hexane ( $\text{C}_6$ ; Aldrich, without purification) was used as a cross-linking agent and  $\text{C}_6$  (10  $\mu\text{L}$ ) was mixed with the base PVP solution (1 mL). The film was annealed on a hot-plate at 80  $^\circ\text{C}$  for more than 1 h to completely remove the solvents. Top-gate transistors were completed by formation of a gate electrode via thermal evaporation of aluminum films (30 nm) through a metal shadow mask.

**Characterization:** The current–voltage characteristics of the F8T2 FET memory devices were measured using an HP 4155B semiconductor parameter analyzer. The transistor parameters, such as charge carrier mobility, were calculated in the saturation or linear regime using the standard formalism for FETs<sup>[50]</sup>. The UV–vis absorption spectroscopy was measured using a Perkin Elmer, Lambda 750, UV–vis spectrometer. TEM images and EDS spectra were obtained using transmission electron microscope, JEM-2100, JEOL.

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