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Performance improvement of GaN-based HEMT grown on silicon (1 1 1) substrate by inserting low temperature AlN layer

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ABSTRACT

By inserting low temperature AlN, a thicker GaN layer on Si substrate without crack was obtained. After comparing the pit densities, etching pit densities, and calculating the dislocations from XRD measurements, results indicated that adding more insertion layers further improved the crystalline quality. The electrical properties were studied by the fabrication of HEMT. The results showed that the off-state drain leakage current was reduced by about two orders magnitude from 1.6×10^{-1} mA/mm to 3.2×10^{-3} mA/mm. Moreover, $I_{DS,max}$ and $g_{m,max}$ could be optimally increased.

1. Introduction

In recent years, the III-nitride device market has focused on growing GaN on Si substrate based on commercial considerations. Compared with mature substrates (sapphire or silicon carbide) for nitride-based devices grown by metalorganic chemical vapor deposition (MOCVD), the Si substrate is not only conductive but also mature for large size mass production. However, the thermal and lattice mismatch between Si and GaN limit its applications. Films with high defect densities and crack patterns deteriorate the device's properties.

Many methods are used to solve problems [1–13], such as optimization of buffer layer, superlattice structure, insertion of compensation layer, and patterned substrates. Inserting low-temperature AlN (LT-AlN) is a simple method that not only reduces the dislocation density but also compensates for the strain. A crack-free surface is necessary and can be achieved by this method. However, the relationship between defect reduction and device performance remains unclear.

In this paper, we used LT-AlN insertion layers to grow GaN without crack. Samples of four different thicknesses with one to three insertion layers were used to fabricate the high electron mobility transistor (HEMT) device. The crystalline qualities of these samples were studied. The measured results demonstrated a significant reduction in defect densities, which were related to the drain leakage current. The reduction in defects was also related to the drain current density.

2. Experimental procedure

The GaN epitaxial layers were grown by a low-pressure MOCVD system on a two-inch n-type silicon (1 1 1) substrate. Trimethylgallium, trimethylaluminum, and ammonia were used as precursors of Ga, Al, and N, respectively. N_2 and H_2 were used as carrier gases. To obtain a clean surface, the Si (1 1 1) substrates were chemically cleaned by typical RCA process and dual HF solution before being loaded into the reactor.

The sample structures in this work are shown in Fig. 1. The conventional structure used as a reference is shown in Fig. 1(a). The buffer layer of this structure consisted of high-temperature AlN and linear-grade AlGaN interlayer, as reported in our previous work [14]. A 0.5 μm undoped GaN film and HEMT structure (20 nm $Al_{0.25}Ga_{0.75}N$ layer) were grown. To obtain a high-quality GaN film without cracks, as shown in Fig. 1(b)–(d), we inserted 720 °C AlN 30 nm to achieve a total GaN film thickness of 1 (sample B with one interlayer), 1.5 (sample C with two interlayers), and 2 μm (sample D with three interlayers), respectively. Scanning electron microscopy (SEM) measurements were used to determine all films without crack.

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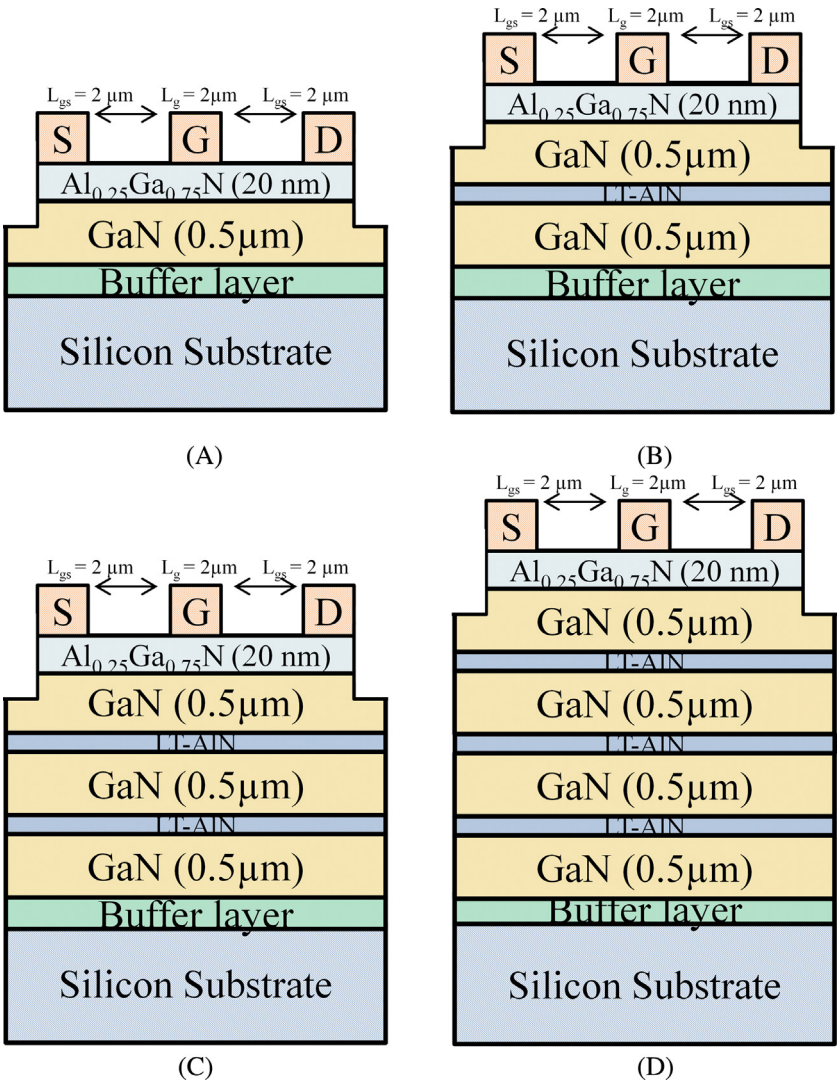

Fig. 1. The structures of (a) conventional structure and (b), (c), and (d) were the structures with LT-AlN insertion layer one to three layers, respectively.

HEMT was fabricated using Cl_2-based inductively coupled plasma to etch mesa with a depth of 300 nm. The Ti/Al/Ni/Au (25/125/45/55 nm) source/drain ohmic contacts were deposited by e-gun evaporator and then annealed using rapid thermal annealing at 850 °C for 30 s in an N_2 ambient. After the gate electrode was defined, Ni/Au (30/170 nm) was deposited as the Schottky contacts. The gate length (L_G), gate–drain distance (L_{GD}), gate–source distance (L_{GS}), and gate width were 2, 2, 2, and 200 μm, respectively.

Several phenomena brought by inserting LT-AlN layers were studied in this paper. The crystalline quality was analyzed by measuring the X-ray diffraction (XRD) rocking curves of the symmetrical (0 0 2) and asymmetrical (1 0 2) reflections. The defect density was analyzed by evaluating the pits from atomic force microscopy (AFM) images. In addition, the etch pit density (EPD) from the SEM images were calculated. Finally, a B1500 semiconductor parameter analyzer was used to measure the current–voltage (*I–V*) characteristic of the fabricated HEMTs.

3. Results and discussions

To enhance the device performance, high-quality GaN films without crack are necessary. With the insertion of a LT-AlN layer, the strain will be compensated, and samples A to D will have crack-free surfaces. The XRD rocking curves of samples A to D are shown in Fig. 2. The full width at half maximum (FWHM) values at the (0 0 2) plane of samples A, B, C, and D were 1137.3, 832.6, 719.7, and 562.8″, respectively. The (1 0 2) plane FWHM values of samples A, B, C, and D were 2072.5, 1325.4, 985.4, and 794.5″, respectively. A better film quality was obtained with the insertion of more LT-AlN layers. To quantify the dislocation density from FWHM values, the following equation should be used [15,16]:

$$D_{\text{screw}} = \frac{\beta^2_{(002)}}{9b^2_{\text{screw}}}, \quad D_{\text{edge}} = \frac{\beta^2_{(102)}}{9b^2_{\text{edge}}}, D_{\text{dis}} = D_{\text{screw}} + D_{\text{edge}}, \tag{1}$$

where D_{screw} is the screw dislocation density; D_{edge} is the edge dislocation density; $\beta_{(102)}$ and $\beta_{(002)}$ are the FWHM values measured by the XRD (1 0 2) and (0 0 2) plane rocking curves, respectively; and b represents the Burger vector length (b_{screw} = 0.5185 nm, b_{edge} = 0.3189 nm). The estimated dislocation densities for samples A, B, C, and D were about 4.35×10^{10}, 1.71×10^{10}, 8.93×10^{9}, and 5.89×10^{9} cm^{-2}, respectively. With the insertion of three LT-AlN layers, the dislocations revealed a reduction of about one order magnitude compared with the reference dislocation. Based on these XRD results, the insertion of LT-AlN could diminish the dislocations and improve the film quality.

To assess the film quality among these samples, we also counted the pit densities from the AFM images and EPD from the

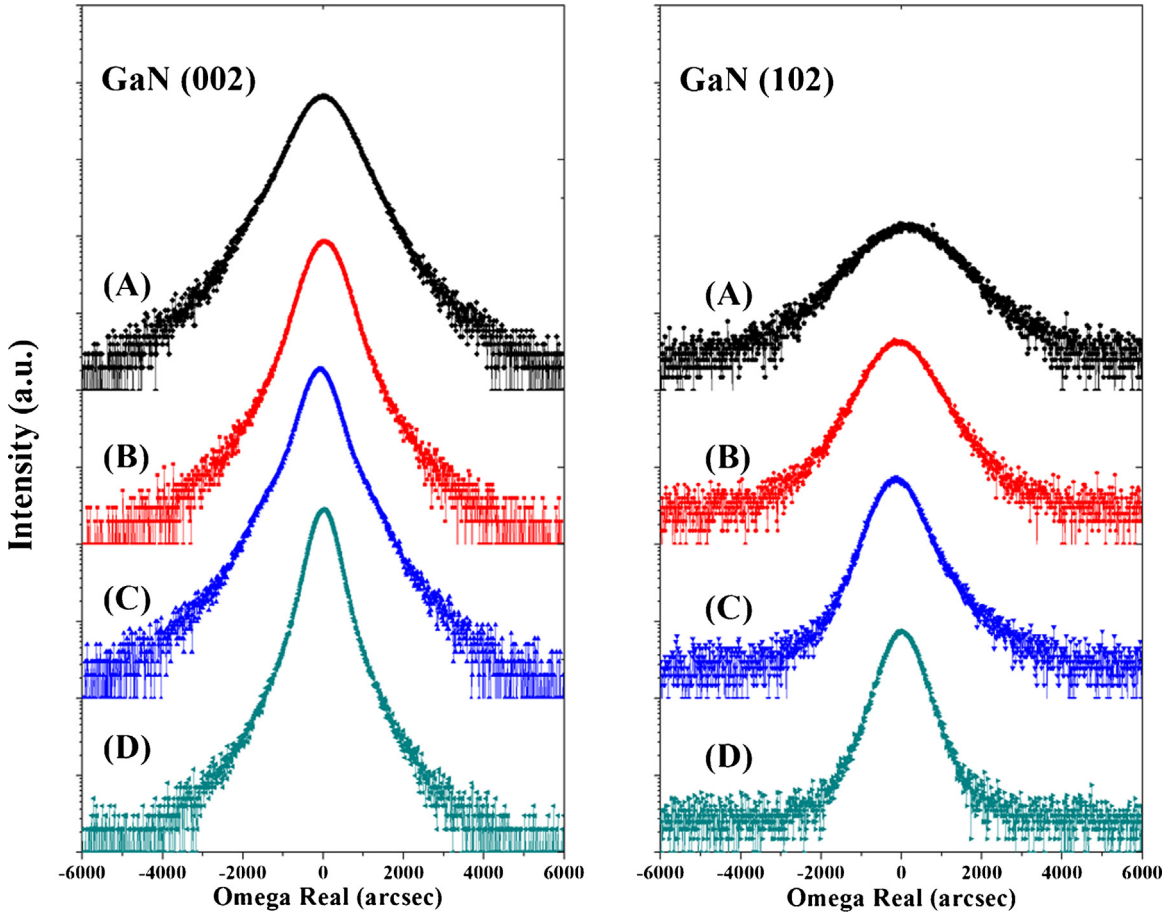

Fig. 2. XRD ω scan rocking curves of (0 0 2) and (1 0 2) reflection plane of GaN layers for Sample A to Sample D and they were labeled as (A) to (D), respectively.

SEM images. As shown in Fig. 3, the surface images from AFM 3 μm × 3 μm were scanned in tapping mode. After calculation, the pit densities for samples A to D were about 1.08×10^9, 8.56×10^8, 6.89×10^8, and 4.89×10^8 cm^{-2}, respectively. These results showed the same trend with the XRD formula. Given that a lower growth temperature could form a polycrystalline AlN insertion layer, the naturally rough surface of LT-AlN was accompanied with some fragmentary lateral growth region via the lateral growth mechanism. This phenomenon explains why the insertion of LT-AlN layers results in lower pit density. In addition, we obtained a film with lower pit densities with the insertion of layers, and the RMS roughness reduced from 2.83 nm (sample A) to 1.27 nm (sample D). Thus, the LT-AlN layer plays a vital role in dislocation formation and surface morphology.

The EPDs were also used to confirm the results. Studies showed that the etch pits originate from open-core screw dislocations [17]. The quantity of pit densities is proportional to the actual screw dislocation density. The samples were immersed in a mixture of H_3PO_4 and H_2SO_4 at 160 °C for 5 min during the EPD process. The pit density was then counted from the SEM images. Fig. 4 exhibits the results of samples A to D. Although a number of pits could be observed on all surfaces, the one with more insertion layers had a very low amount of pits. Based on these SEM images, the pit density was calculated to be 4.89×10^8 cm^{-2} in the reference case. By contrast, adopting LT-AlN layers reduced the density to around 4.14×10^8, 2.22×10^8, and 1.70×10^8 cm^{-2} for samples B, C, and D, respectively. This finding indicated that a GaN film with lower defects could be achieved by inserting a LT-AlN layer. Based on the results of XRD, AFM, and EPD analyses from SEM, we confirmed that the insertion layer could achieve a high-quality GaN film with low defect densities.

The electrical properties of this thin film are essential information. Thus, this proposed method was conducted on HEMT devices. In order to validate the presence of 2DEG, we took measurements of capacitance–voltage (C–V) using a capacitance meter of 1 MHz frequency (Fig. 5). From the inset in Fig. 5, a strong peak of a carrier density equals to 3.2×10^{20} cm^{-3} corresponding to the presence 2DEG at the interface AlGaN/GaN was obtained. The position of this peak proves that AlGaN layer thickness is about 20 nm. The output I_{DS}–V_{DS} characteristics of samples A, B, C, and D with sweeping V_{GS} from −6 V to 1.5 V at 1.5 V increments are shown in Fig. 6. All the samples showed good pinch-off characteristic at V_{GS} <−4.5 V, and the drain currents for samples A, B, C, and D at V_{GS} = 1.5 V and V_{DS} = 20 V were 93, 153, 243, and 328 mA/mm, respectively. The output characteristics were increased dramatically by the insertion layers. This improvement could be attributed to the increase in mobility. Although the growth trends of HEMT structure were similar, the surface morphology influenced mobility. Uneven surfaces limited carrier transit, thereby reducing carrier transit in the 2DEG channel. Moreover, the defects could be regarded as carrier dopant. For a given temperature, the mobility decreased with the increase in impurities, which can enlarge the possibility of impurity scattering [18]. On-resistance (R_{on}) could also be calculated from this figure. The calculated R_{on} for samples A, B, C, and D were 52.6, 35.8, 22.5, and 11.9 Ω-mm, respectively. The reduction in R_{on} was caused by the improvement in film quality. The results indicated that the film quality could be improved with the proposed method, and a high drain current density could be achieved.

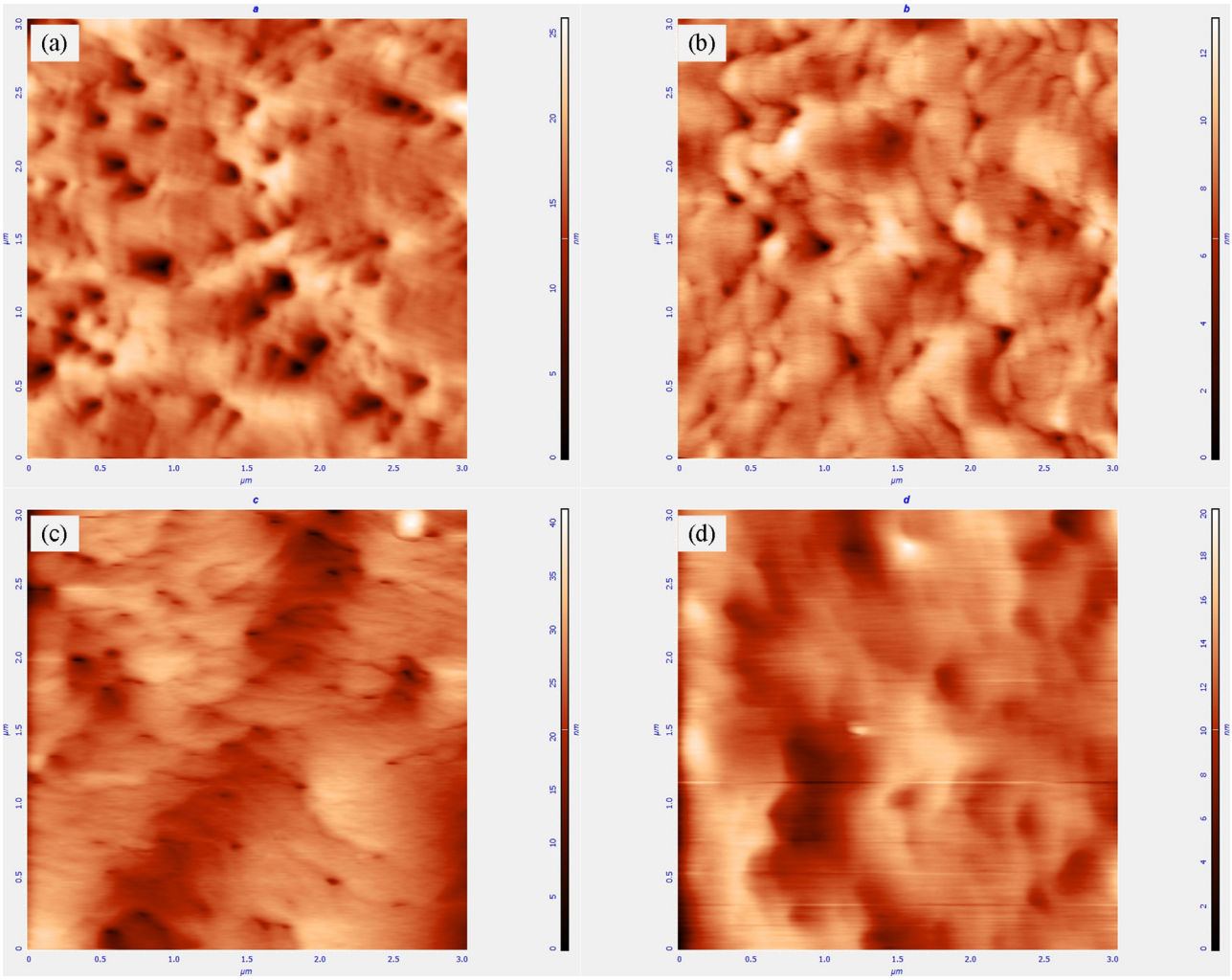

Fig. 3. Surface images from AFM 3 μm × 3 μm scan of Samples A to D.

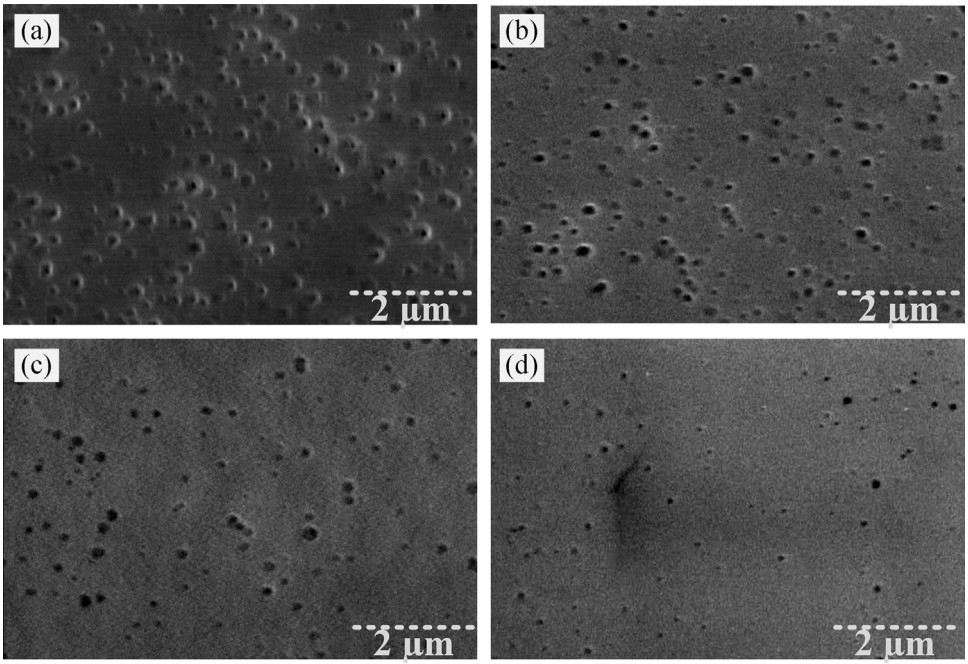

Fig. 4. Etching pits densities of the GaN epilayers from SEM for Samples A to D.

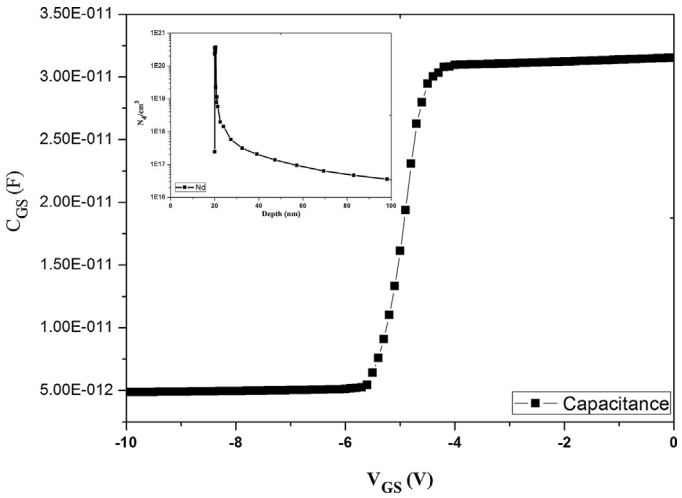

Fig. 5. Measured *C*–*V* characteristic of the HEMT structure, and the inset shows the concentration (N_d) versus the space charge width (W) profile.

Fig. 7 shows the transfer characteristics of samples A, B, C, and D with V_{DS} = 10 V. The maximum transconductance ($g_{m,max}$) for samples A, B, C, and D were 23, 41, 60, and 77 mS/mm, respectively. Measured transfer characteristics showed a significant improvement in $g_{m,max}$. Considering the large drain current density, the gate control ability also improved.

Fig. 7(a) shows the I_{DS}–V_{GS} characteristics. The leakage currents for samples A, B, C, and D at V_{GS} = −10 V were 1.6×10^{-1}, 8.3×10^{-2}, 1.3×10^{-2}, and 3.2×10^{-3} mA/mm, respectively. The inset in Fig. 8(a) shows subthreshold swing (S.S) for samples A to D, which was reduced from 1255 to 322 mv/dec. The leakage current and S.S for sample D significantly improved compared with that for sample A. The reduction in leakage was because the reduction in vertical leakage, which can be explained with a space-charge-limited current (SCLC) conduction model [19]. At reverse voltage, the drain ohmic contact provides free electrons and injects into the buffer layer. As the reverse bias increases, more acceptor traps get ionized and Fermi level can move up, thus more free electrons are generated and the leakage current increased. Besides, the breakdown mechanism also depends on the buffer thickness and traps concentration. Therefore, with more insertion layers and reduction in defects, the leakage current could be further suppressed.

The gate leakage current as a function of gate bias was measured, and the results are shown in Fig. 8(b). The gate leakage current for samples A, B, C, and D at V_{GS} = −10 V and V_{DS} = 0.1 V were 4.1×10^{-3}, 1.8×10^{-3}, 5.6×10^{-4}, and 3.8×10^{-4} mA/mm, respectively. Given that the insertion layer mainly enhanced the film quality, a slight improvement in the gate leakage current was observed. This improvement was attributed to the flatter surface.

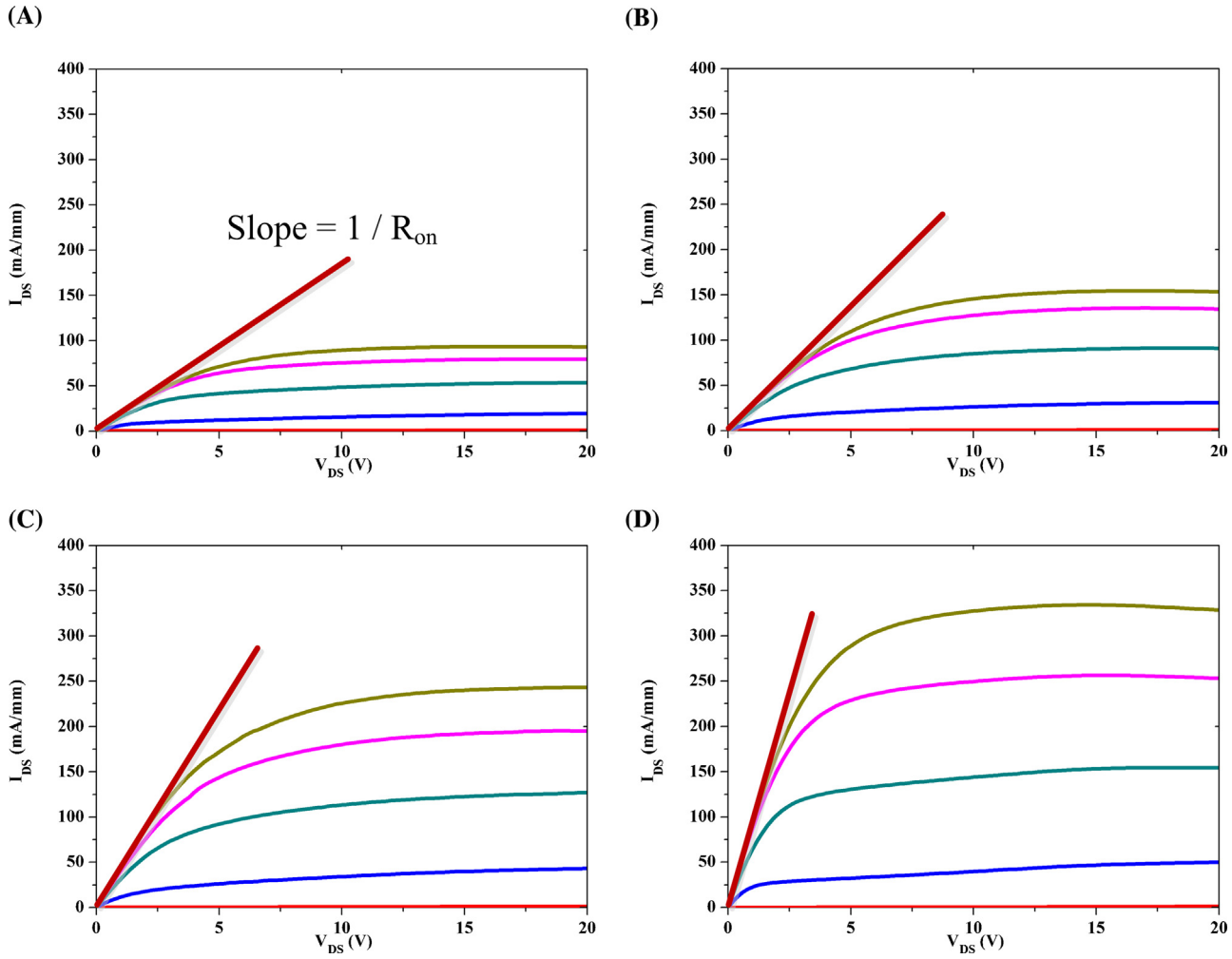

Fig. 6. Output I_{DS}–V_{DS} characteristics of AlGaN/GaN HEMT with sweeping V_{GS} from −6. V to 1.5 V at 1.5 V increment.

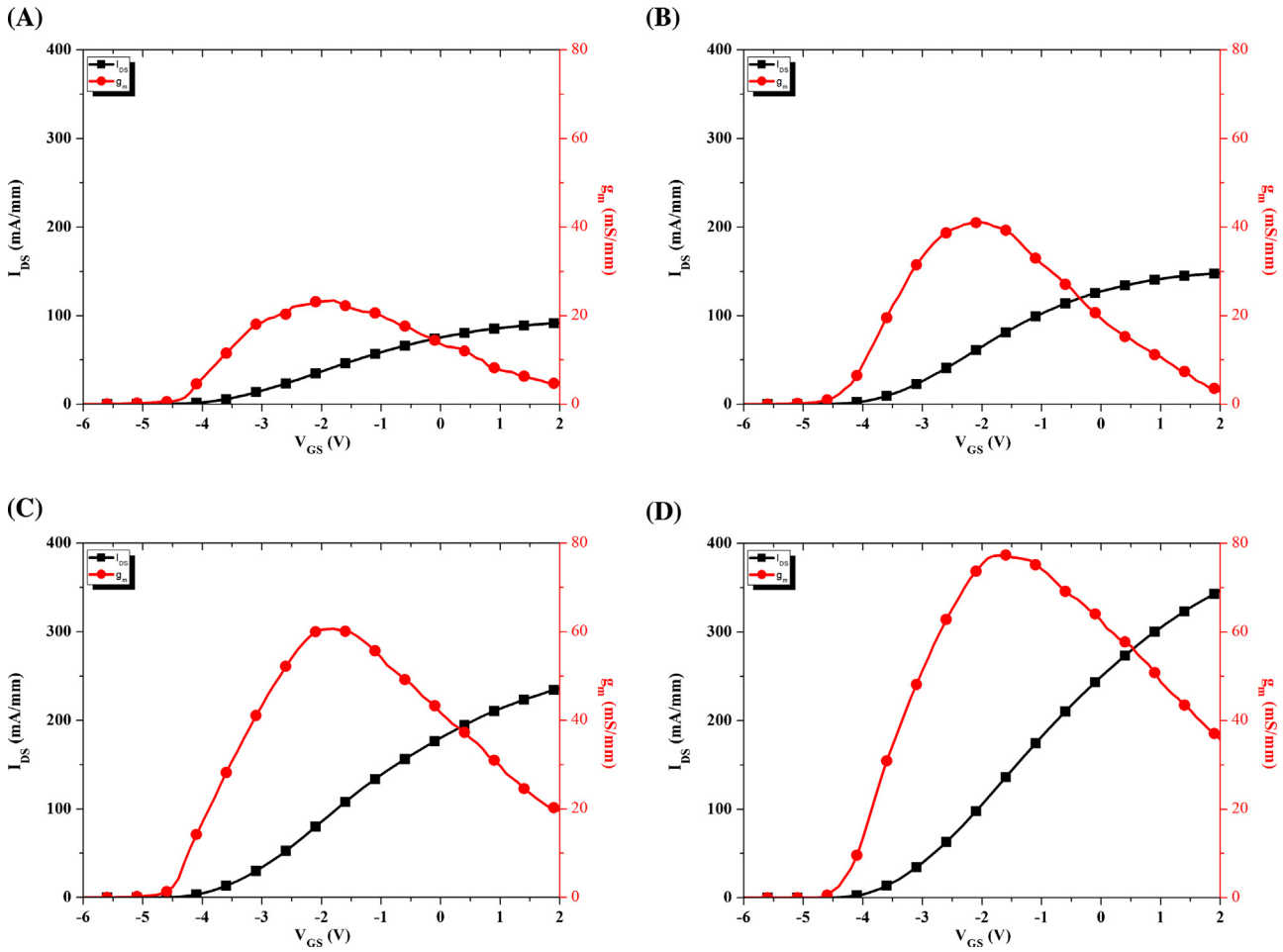

Fig. 7. Transfer characteristics of AlGaN/GaN HEMT (with V_{DS} = 10 V).

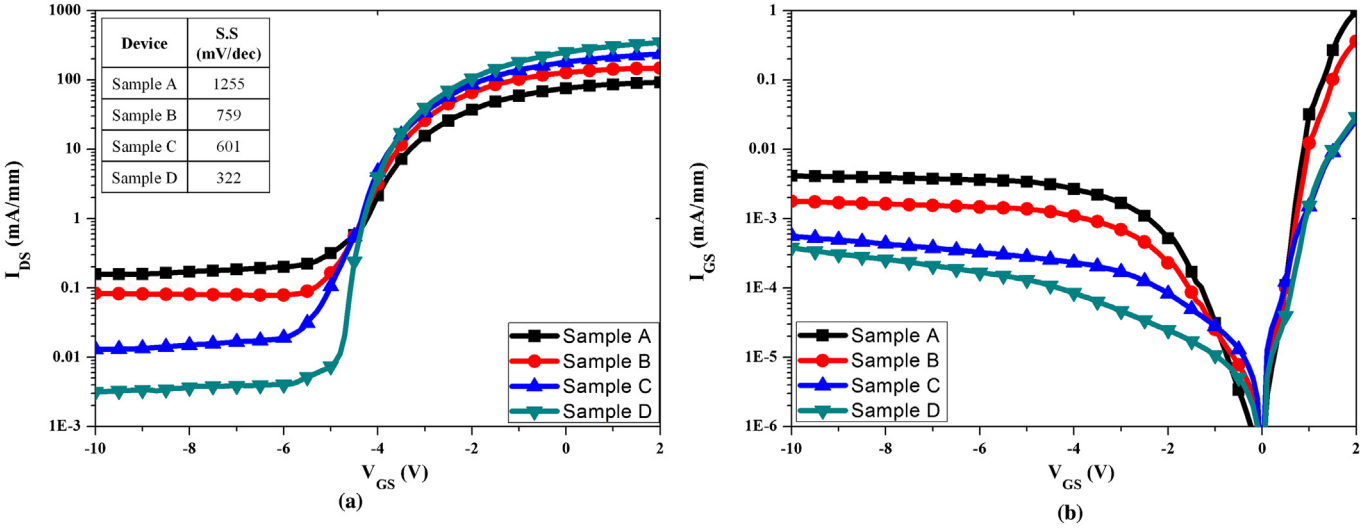

Fig. 8. (a) Measured I_{DS}–V_{GS} characteristics. (b) Measured gate leakage current as a function of gate bias.

4. Conclusion

We studied the influence of inserting LT-AlN on the upper or subsequent GaN. By inserting LT-AlN, a thicker GaN layer on the Si substrate without crack could be obtained. After comparing the pit densities from AFM images, analyzing the EPDs from SEM images, and calculating the dislocations from XRD for all samples, the results indicated that more insertion layers could further improve the crystalline quality. The electrical properties were studied by the fabrication of HEMT. Off-state drain leakage current was reduced from 1.6×10^{-1} mA/mm to 3.2×10^{-3} mA/mm, and the gate leakage current decreased from 4.1×10^{-3} mA/mm to

3.8×10^{-4} mA/mm at $V_{GS} = -10$ V and $V_{DS} = 0.1$ V. Thus, the insertion layers could reduce the leakage current by about two orders of magnitude. Moreover, $I_{DS,max}$ and $g_{m,max}$ could be optimally increased because of the increase in mobility.

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