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Effect of Interfacial Structure on the Transistor Properties: Probing the Role of Surface Modification of Gate Dielectrics with Self-Assembled Monolayer Using Organic Single-Crystal Field-Effect Transistors

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S *Supporting Information*

ABSTRACT: Single-crystal field-effect transistors based on 2,3-dimethylpentacene have been used to probe the effect of surface modification of the insulating dielectric SiO_2 layer on the transistor characteristics. Self-assembled monolayers (SAMs) of different chain lengths and functional groups were used to systematically modify the structure and property of the semiconductor/dielectric interface. The charge carrier mobility as a function of SAM used for surface modification was analyzed. The character of the terminal functional group, as well as the mechanic treatment (rubbing) of the monolayer, much influences the carrier mobility. Introduction of a polar end group (donor or acceptor type) decreases the mobility compared to a nonpolar end group. Prerubbing of the monolayer serves to increase the charge carrier mobility by a factor of 2−4-fold. The results are interpreted in terms of the orderliness of the monolayer which affects the contact at the monolayer/semiconductor interface, which in turn affects the trapping sites' density or the smoothness of the potential surface that the carriers experience while transporting along the interface.

KEYWORDS: self-assembled monolayer, surface modification, organic semiconductors, dimethylpentacene, single crystal, field-effect transistors
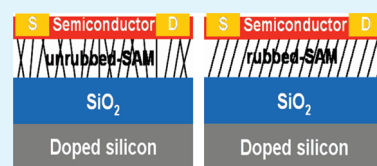
INTRODUCTION

Organic field-effect transistor (OFET) is an intensively pursued subject because it would play a key role in the promising era of organic and particularly flexible electronics.[1] A major goal in the development of OFETs is to achieve higher carrier mobility, so that higher current output can be obtained to drive other components in an organic electronic device. While theories and models have been developed to correlate the mobility for molecular materials with parameters such as reorganization energy for the molecule itself and electronic couplings between neighboring molecules,[2] it takes more than the material itself to achieve a high mobility. It is generally accepted that charge conduction in an organic thin film transistor takes place through the very first several layers of molecules near the organic semiconductor/gate dielectric interface.[3] The structure and property of this interface thus very much influence the charge transport behavior through the conducting channel nearby. There are many studies on the effect of structure of the gate dielectric on the mobility of a molecular film.[4] Materials of different capacitance have been used in the organic FETs to reduce the gate bias required to turn on the transistors.[5] Silicon dioxide (SiO_2) is frequently used as the gate dielectric because of its direct association with semiconductor silicon and the direct accessibility from silicon, although OFETs prepared on bare SiO_2 suffer from several problems. Rather thick layer (300 nm) is needed to prevent charge leakage between the gate electrode and source/drain. This would increase the bias voltage required to operate the device. It is also well-known that the bare SiO_2 surface contains abundant hydroxyl groups, which can trap charges in the channel or introduce additional charges

(residual carriers) into the channel.[6] Hydrophobation of the SiO_2 surface by hexamethyldisilazane (HMDS) or alkylsilane monolayer is a known and frequently used strategy to improve the mobility of many organic semiconductor films during transistor fabrication.[7] Modification of the surface with a polar or nonpolar monolayer also exerts different effects on the charge transport due to different interactions between the charge carriers and the dipoles,[8] so that the fluorinated monolayer is reported to enhance mobility and the amino-functionalized monolayer decreases the mobility. Yet there are also contradictory reports on the effect of the fluorinated surface,[9] so that the origin of the improvement is still unclear. Furthermore, we recently reported that rubbing of a monolayer adsorbed on the dielectric layer much increased the grain size of deposited pentacene films and improved the mobility.[10] Reduced number of nucleation sites on the substrate after rubbing is suggested to contribute to the growth of larger grains.

However, the origin of the impact of surface modification on the carrier mobility can be complicated. Any surface modification brings about changes not only in the local electric field which affects the charge transport but also in the number of trapping sites at the interface. Furthermore, there can be changes in the contacting interaction between the surface and the organic semiconductor, as well as changes in the surface roughness. These will manifest their effect in the film morphology (that is, crystallinity, grain sizes, as well as packing orientation), which

also plays a decisive role in the carrier mobility measured.[11] A separation of the parameters would facilitate the understanding of transport behavior and aid the design and fabrication of a device for higher mobility. In this regard, transistors made of organic single crystals free from morphology variations and intrinsic defects[12] are an ideal tool to probe the effect of interfacial structure on the carrier transport property. Very few reports are known on the effect of surface modification on single-crystal transistor devices.[13]

In this work, we used 2,3-dimethylpentacene (DMPT) single crystals as the conducting channel to fabricate bottom-gate/top-contact transistors on the Si/SiO$_2$ surface. While thin film transistors based on DMPT can be prepared,[14] this compound is particularly suitable for single-crystal field-effect transistors (SCFETs) than pentacene crystals because very thin plate-like single crystals can be prepared and good contact between the crystal and the dielectric surface can be reached. Various self-assembled monolayers with different chain lengths/polar or nonpolar terminal functional groups were used to systematically change the interfacial structure and property. These include n-octadecyltrichlorosilane (ODTS), n-nonyltrichlorosilane (NTS), hexamethyldisilazane (HMDS), 1H,1H,2H,2H-perfluorodecyltrichlorosilane (FDTS), 7-octenyltrichlorosilane (OCTS), 11-cyanoundecyltrichlorosilane (CUTS), and 12-aminododecyltrichlorosilane (ADTS). These are introduced as a buffer layer between the gate dielectric and the thin DMPT single crystal. The SAM-modified substrates were also prerubbed with a flannelette cloth before the DMPT single crystal was laid down for device fabrication. Furthermore, mixed monolayers with different alkyl chain lengths were used to create a "molecularly rough surface" as the substrate for device fabrication. The results show that the nonpolar, methyl-terminated, SAM-modified substrates gave higher mobility than the polar SAM-modified ones, whether it is a donor type or an acceptor type functional group. Rubbing of the SAM-modified surface always improves the mobility. It is suggested that the molecular scale smoothness and homogeneity of the surface potential created by the SAM contribute to the mobility change.

■ EXPERIMENTAL SECTION

Materials. 2,3-Dimethylpentacene (DMPT) was prepared by modifying literature procedures.[14] The product was purified by multiple sublimations in a gradient temperature furnace and fully characterized by NMR and mass spectrometry. HMDS, ODTS, FDTS, and OCTS were obtained commercially. NTS and CUTS were synthesized in the laboratory following standard procedures and fully characterized by NMR. n-Doped silicon wafers with a 300 nm thermally grown oxide layer were obtained from Siltronix (France).

Single-Crystal Growth. Dark-blue, plate-like DMPT single crystals were grown by the physical vapor transport method[15] using ultra pure argon as the carrier gas. The crystal size depends on the gas flow rate, temperature, and time. Thinner crystal with a smooth surface is the prerequisite for strong adhesion to the insulator surface in the bottom-gate device configuration. Very thin (0.4−5 μm) and plate-like crystals (Figure 1) were obtained by growing at 310 °C with an argon flow rate of 50 cm^3/min. It is noted that the DMPT single crystals are flexible and can be bent easily.

Preparation of Self-Assembled Monolayers. Heavily n-doped silicon substrates with a 300 nm thermally grown SiO$_2$ layer were cleaned in Piranha solution (H$_2$SO$_4$/H$_2$O$_2$ = 4:1) at 90 °C for 1 h and then thoroughly washed with deionized (DI) water, followed by ultrasonicating in DI water for 5 min and washing with fresh DI water again. Finally, the substrates were dried by a stream of nitrogen. The cleaned substrates were immersed in 1−10 mM solution of different functional trichlorosilanes in
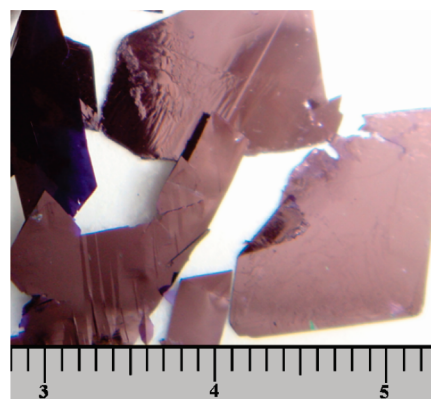

Figure 1. Digital image of a 2,3-dimethylpentacene single crystal.

dry toluene for 3−5 min at ambient conditions (for ODTS, NTS) or in a drybox (for FDTS, CUTS, and OCTS) to form a SAM on the SiO$_2$ insulator surface. Subsequently, the substrates were removed from the solution and rinsed with toluene, followed by 5 min ultrasonication in dry toluene and dried by a nitrogen flow. Mixed solutions of ODTS (C18) and NTS (C9) were prepared in dry toluene with different ratios (NTS/ODTS = 1:0.1, 1:0.33, and 1:1) to modify the substrate with mixed SAMs. To prepare the HMDS-modified silicon wafer, the substrate was immersed in 2.5% HMDS solution in dry toluene for 24 h.[16] ADTS-modified silicon substrate was prepared by reducing CUTS-modified substrate with lithium aluminum hydride (LAH). Thus the CUTS-treated substrates were dipped in a 10% solution of LAH in dry tetrahydrofuran (THF) for 3 h. The substrates were then removed from the solution and rinsed with DI water and sonicated in THF for 5 min and dried by a nitrogen flow. The obtained surface is designated as an ADTS-modified substrate. To eliminate the possible particle formation/presence on the surface, all of the SAM-modified substrates were first rubbed unidirectionally with a flannelette cloth.[10] These samples were designated as Si/SiO$_2$/r-SAM. The rubbed substrates were then sent back to the pure toluene bath and sonicated for 3 min. This step served to remove any possible orientation order introduced by the rubbing procedure. These samples were designated as unrubbed Si/SiO$_2$/SAM. The surfaces of these samples were free of particles when examined under an optical microscope. The structures of the SAM-forming molecules and devices are shown in Figure 2.

Device Fabrication. DMPT single-crystal devices were fabricated in the bottom-gate/top-contact geometry in order to minimize contact resistance.[17] DMPT crystals with a thickness of 0.4−2.5 μm were found to have good adhesion to the substrate surface, where there were no air bubbles observed between the crystal and the substrate. The crystals were cut into smaller pieces to fit the experiments. The direction along the break line is lined up with the rubbing direction. The crystals were also rotated 90° to measure the direction dependence, and the results were within the same range reported below. Thus no clear anisotropy was suggested. DMPT single-crystal devices were fabricated on both unrubbed and rubbed substrates for each SAM-forming molecule. Devices with bare Si/SiO$_2$ substrates were also fabricated as a reference. After DMPT single crystals were laminated on the substrate surface, 60 nm thick Au source−drain electrodes were deposited on the crystal surface through a shadow mask to complete the top-contact FETs. The device channel length (L) was 50 μm, and the width (W) varied depending on the crystals chosen. Typically, 10 devices were made in each type of substrate.

■ RESULTS AND DISCUSSION

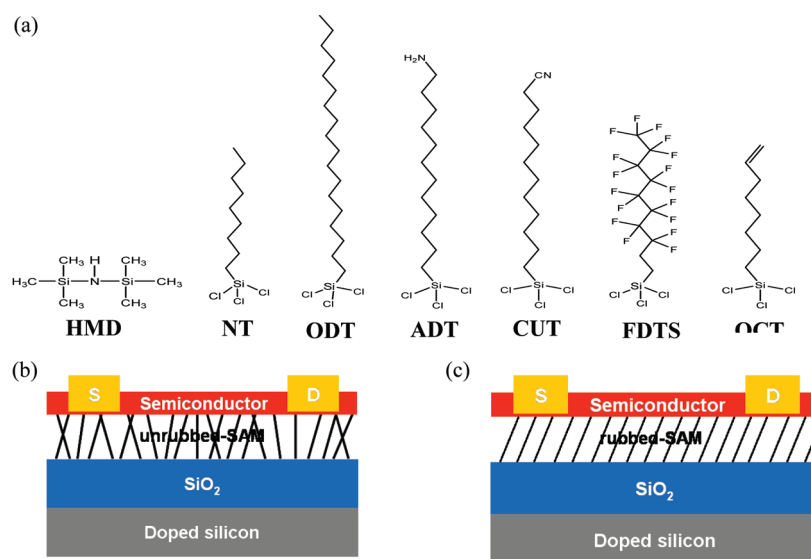**FET Characterization.** The DMPT single-crystal FETs were measured at ambient conditions in a dark chamber using a

Figure 2. (a) Molecular structure of organosilane molecules; (b) device structure of DMPT SCFETs on Si/SiO$_2$/SAM and (c) on Si/SiO$_2$/r-SAM.

computer-controlled Agilent HP4156 semiconductor parameter analyzer. The FETs were operated in the accumulation mode by applying a negative gate bias. The source electrode was grounded, and the drain electrode was negatively biased between 0 and −80 V. Figure 3 shows typical output characteristics (I_d vs V_g curve) of the devices on the unrubbed monolayer surface of Si/SiO$_2$/ODTS and Si/SiO$_2$/FDTS and on the rubbed monolayer surface of Si/SiO$_2$/r-ODTS and Si/SiO$_2$/r-FDTS substrates. The output characteristics for other SAM-modified substrates, rubbed or unrubbed, are shown in Supporting Information (Figures S1 and S2). Transfer characteristics of all FETs are shown in Figure 4. The charge carrier mobility is calculated in the saturation regime using the following equation.

$$I_d = \frac{W}{2L} C_i \mu (V_g - V_{th})^2 \qquad (1)$$

where C_i is the capacitance per unit area of the gate dielectric, μ is the carrier mobility, and V_{th} is the threshold voltage. The calculated mobilities and on/off ratios are summarized in Table 1. The data are analyzed as follows.

Effect of Rubbing. The output characteristics of DMPT SCFETs in Figure 3 show that higher currents were obtained for devices on rubbed ODTS-modified substrates than on unrubbed ODTS-modified substrate. This is true for FDTS-modified substrate as well as all other SAM-modified substrates. That is, prerubbing of the SAM surface will, in general, lead to higher currents. The mobility also increases by a factor of 2−4, except for the HMDS-modified surface, where the mobility stayed similar whether the surface had been rubbed or not. The threshold voltage nevertheless has different shifts with rubbing depending on the monolayer used. For nonpolar monolayers, such as ODTS-, NTS-, and HMDS-modified substrates, the threshold voltage shifts positively, from more negative voltages to less negative voltages or positive voltages. For polar monolayers, such as FDTS-, CUTS-, and ADTS-modified substrates, the threshold voltage shifts negatively, from more positive voltages to less positive voltages. In previous work,[10] it was shown that rubbing of the SAM-modified surface resulted in larger grains of higher crystallinity of pentacene films deposited on top. It was suggested that the SAM is a multidomained monolayer with numerous grain boundaries where the pentacene molecules can get trapped and start nucleation.

Rubbing in a specific direction smoothes the surface and reduces the density of grain boundaries and reduces the number of nucleation sites. The mobility increase can be due to larger crystalline grains. However, in current cases, the single crystals were used so that there were no morphology differences in the semiconductor channels. Still there were moderate increases in the mobility. One suggestion is that the grain boundaries in the monolayer are trapping sites. The trapped charges become scattering centers and retard the charge transport. Upon rubbing, the surface monolayer becomes smoother, with a reduced number of trapping sites so that the charge mobility increases. An alternative rationalization is that the multidomained organic monolayer is presenting molecular dipoles of various orientations and thus a "rough" potential surface. Charge carriers transporting along such a surface are slower than along a smoother potential surface. It is noted that similar rationalization has been proposed for several FETs where the rough insulator surface hinders charge transport by charge traps or by transport barriers.[18] For the shifts in threshold voltages, the rubbing reduces the number of trap states in a SAM and shifts the V_{th} toward the zero gate bias. Kang et al. also reported an increasing mobility and shift in threshold voltage with rubbed polyimide versus an unrubbed polyimide dielectric layer.[19]

Attempts to collect evidence of roughness difference in rubbed and unrubbed SAMs by atomic force microscopy (AFM) were not inconclusive, presumably the roughness is of molecular scale, much lower than the dimension of the typical AFM tip used. We nevertheless used mixed monolayers to support our assertion that molecular roughness influences the mobility. Thus binary mixed monolayers containing C18 ODTS and C9 NTS in various ratios were used to modify the dielectric surface. These mixed monolayers have been shown previously to be homogeneously mixed[20] and thus molecularly rough compared to the single-component monolayer. The SCFETs prepared on such surfaces had mobilities about 50% of that on a single-component monolayer-modified dielectric layer. (The output and transfer characteristics are shown in Figures S3 and S4 in Supporting Information.) All FETs on unrubbed mixed SAMs exhibited almost the same mobilities (up to 0.22 cm^2 V^{-1} s^{-1}). Rubbing improved the mobility but still less than that on a rubbed single-component SAM surface. Rubbed mixed SAM FETs also have
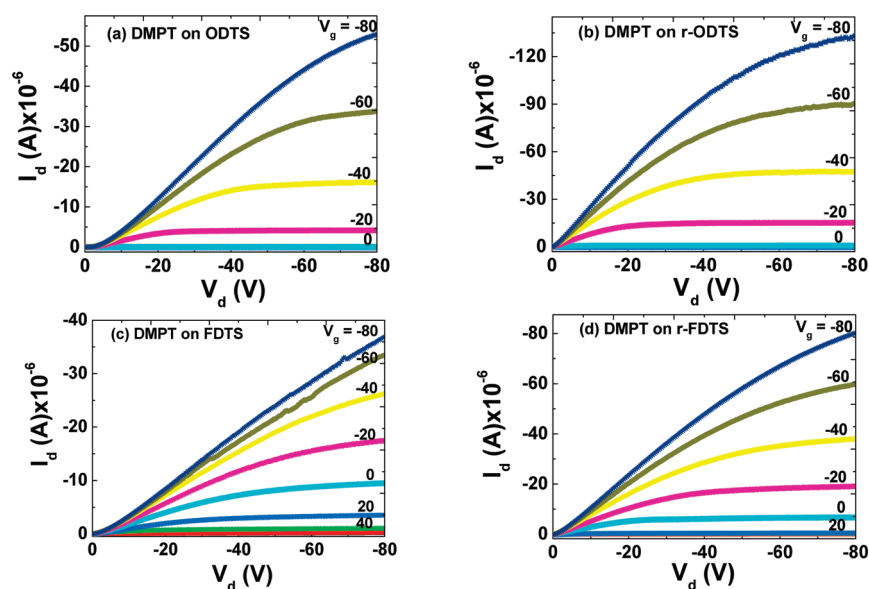
Figure 3. Output characteristics of DMPT SCFETs on (a) $Si/SiO_2/ODTS$, (b) $Si/SiO_2/r\text{-}ODTS$, (c) $Si/SiO_2/FDTS$, and (d) $Si/SiO_2/r\text{-}FDTS$.
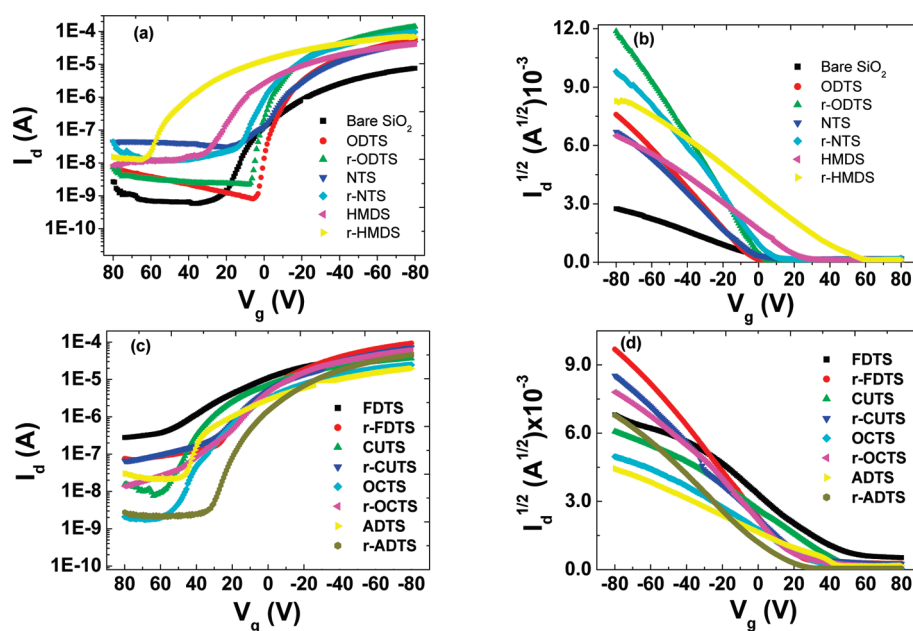

Figure 4. Transfer characteristics of DMPT SCFETs on unrubbed and rubbed nonpolar SAMs (a,b) and polar SAMs (c,d).

shown almost the same mobilities (up to 0.48 $cm^2\,V^{-1}\,s^{-1}$) (Table 2). More positive threshold voltages were observed for devices on a mixed monolayer.

Effect of Chain Length. The ODTS-, NTS-, and HMDS-modified surfaces are all nonpolar surfaces exposing methyl groups at the substrate surfaces. They differ in the chain length though. There were conflicting reports on the effect of chain length on the device mobility.[7,21−23] The quality of the SAM is suggested to influence the thin film growth and morphology obtained, which in turn affects the mobility. In current cases where single crystals were used, no morphology issue was involved. The ODTS-modified substrate gave a mobility (up to 0.57 $cm^2\,V^{-1}\,s^{-1}$) similar to but slightly higher than that of the

NTS-modified substrate (up to 0.49 $cm^2\,V^{-1}\,s^{-1}$). The HMDS-modified substrate has a mobility similar to that of the NTS-modified substrate (up to 0.46 $cm^2\,V^{-1}\,s^{-1}$). Thus there is little dependence on the chain length over the range of lengths tested here. Rubbing of the SAM surface led to mobility increases for ODTS- (up to 1.03 $cm^2\,V^{-1}\,s^{-1}$) and NTS-modified substrate (up to 0.80 $cm^2\,V^{-1}\,s^{-1}$) but not for HMDS-modified substrate. HMDS has only one carbon (trimethylsilyl group), and much less conformational disorder is involved. With only one carbon chain, the rubbing does not change the orientation of the trimethylsilyl groups, which may contribute to the density of grain boundaries and trapping sites in an alkylsilane SAM. This may explain the invariance of mobility with rubbing.

Table 1. DMPT SCFET Performance on Various SAM-Modified Dielectric Surfaces

SAM	mobility ($cm^2\,V^{-1}\,s^{-1}$)	on/off ratio	V_{th} (V)
SiO$_2$	0.05−0.11	10^2−10^4	5−29
ODTS	0.38−0.57	10^2−10^4	−5−(−11)
r-ODTS	0.60−1.03	10^4−10^7	−2−8
NTS	0.25−0.49	10^3−10^5	−4−5
r-NTS	0.51−0.80	10^3−10^5	6−14
HMDS	0.23−0.46	10^3−10^6	11−36
r-HMDS	0.25−0.47	10^3−10^6	34−50
FDTS	0.11−0.18	10−10^2	41−65
r-FDTS	0.38−0.63	10^2−10^4	18−30
CUTS	0.08−0.13	10^2−10^3	31−56
r-CUTS	0.33−0.48	10^3−10^4	26−39
OCTS	0.06−0.10	10^2−10^3	30−55
r-OCTS	0.29−0.41	10^3−10^6	20−32
ADTS	0.03−0.08	10^2−10^3	36−64
r-ADTS	0.24−0.37	10^4−10^6	−4−18

Table 2. DMPT SCFET Performance on Mixed SAM-Modified Dielectric Surfaces

mixed SAMs	mobility ($cm^2\,V^{-1}\,s^{-1}$)	on/off ratio	V_{th} (V)
NTS/ODTS (1:0.1)	0.08−0.22	10^2−10^4	10−18
r-NTS/ODTS (1:0.1)	0.21−0.39	10^3−10^6	20−34
NTS/ODTS (1:0.33)	0.12−0.21	10^3−10^4	16−20
r-NTS/ODTS (1:0.33)	0.21−0.48	10^3−10^7	21−32
NTS/ODTS (1:1)	0.11−0.22	10^2−10^4	9−15
r-NTS/ODTS (1:1)	0.22−0.48	10^3−10^4	16−27

Effect of Terminal Functional Group. In general, dielectric surfaces modified with polar SAMs (FDTS, CUTS, and ADTS) exhibited lower device mobility than those modified with nonpolar SAMs (ODTS, NTS, and HMDS), except for the one with the vinyl-terminated OCTS SAM. For example, substrate modified with a fluorinated chain (FDTS) gave lower mobility (0.11 to 0.18 $cm^2\,V^{-1}\,s^{-1}$) than that modified with hydrocarbon chain (0.49−0.57 $cm^2\,V^{-1}\,s^{-1}$). A rather high threshold voltage was observed (+41 to +65 V). This could be rationalized as the induction of hole carriers at the interface by the highly electronegative fluorine atoms, and a rather large positive bias is needed to turn off the device. Rubbing of the substrate increased the mobility (0.38 to 0.63 $cm^2\,V^{-1}\,s^{-1}$) but also reduced the threshold voltage to the range of 18−30 V. It is noted that pentacene thin film FETs on a FDTS-modified substrate exhibited 6 times lower mobility than that on the ODTS-treated substrate.[9b] However, morphology change was also involved in those devices. A device modified with cyano-terminated alkylsilane (CUTS) also gave a mobility (0.08−0.13 $cm^2\,V^{-1}\,s^{-1}$) lower than that of the alkylsilane-modified substrates. Like the FDTS-modified substrate, a large and positive threshold voltage was observed in the range of 31−56 V. FET mobilities increased (up to 0.48 $cm^2\,V^{-1}\,s^{-1}$) on rubbed substrates, and threshold voltage was also reduced to the range of 26−39 V. For an amino-terminated, silane-modified substrate, the mobility was also much lower (0.03−0.08 $cm^2\,V^{-1}\,s^{-1}$) than that of the alkylsilane-modified substrate, and high threshold voltage was observed in the range of 36−64 V. With the lone pair electron on the nitrogen atom, the amino group can be a trapping site for hole carriers. The device mobility increased (up to 0.37 $cm^2\,V^{-1}\,s^{-1}$), and threshold voltage shifted in the negative direction to the range of −4 to 18 V if the surface was rubbed before device fabrication. Of particular interest is the OCTS-modified substrate. The surface exposing vinyl groups are considered to be a nonpolar surface as the methyl-terminated ODTS surface. Yet the mobility was low (up to 0.1 $cm^2\,V^{-1}\,s^{-1}$) and the threshold voltage was high, in the range of 30−55 V.

Silane molecules with polar end functional groups tend to form disordered SAMs on the insulator surface due to the repulsive interactions between the terminal dipoles, and these SAMs may create a rough surface potential profile, which is responsible for the poor transport behavior. Huang et al. reported the FET performance of a solution-deposited semiconductor on several fluorinated SAMs, including FDTS. The mobility is reduced on the FDTS SAM, even though the FDTS SAM surface is highly hydrophobic (water contact angle ∼111°). The increasing roughness in the SAM with increasing chain length of fluorinated molecules was suggested to contribute to the deterioration of film morphology and performance.[9a] A similar suggestion was made by Park et al., who reported that pentacene FETs with the C$_{60}$-NH$_2$-functionalized SAM exhibited low carrier mobility in comparison with that of FETs on bare SiO$_2$.[24] However, in their cases, the morphology also changed with the surface modification.

The vinyl group at the terminal of the surface is not polar but more electron-rich than the saturated methyl group. F8T2 FETs with OCTS-treated substrate were shown to give carrier mobility lower than that of FETs with the FDTS-treated substrate and bare SiO$_2$.[22] Collet et al. also reported that the vinyl-terminated SAM is not completely organized, and they found the presence of gauche defects.[25] FETs with a rubbed OCTS substrate exhibited a mobility (up to 0.41 $cm^2\,V^{-1}\,s^{-1}$) higher than that of the unrubbed one, and the threshold voltage also shifted in the negative direction in the range of 20−32 V.

■ CONCLUSION

In conclusion, we have used DMPT single crystals to investigate the effect of dielectric surface modification on the FET device performance. The effect of morphological differences upon modification in thin film cases can be excluded to simplify the correlation. Various SAMs were used to systematically change the very top surface structure and property, which drastically affects the FET performance. The carrier mobility with unrubbed nonpolar SAM-treated devices is 3−5 times higher compared to that of unrubbed polar SAM-modified devices. SAMs with a polar end functional group may give a disordered SAM and thus a rougher potential surface, which hampers the carrier transport in the channel nearby. The rubbing process in all case improves the carrier mobility by 2−4-fold, except for HMDS, which gave similar mobility on the unrubbed substrate. Rubbing results in a smoother surface with more homogeneous potential surface and/or reduces the amount of trapping sites, both of which are advantageous for carrier transport. In the case of a thin film device, the morphology factor can further change the trend described here. Depending on the surface modification, the interaction of deposited molecules with the surface can be different and affect the diffusion/migration of the molecules. On a modified surface where higher crystallinity films or larger grains are obtained from vapor deposition, the mobility can change in the positive direction, whereas the reverse is true for poorer crystallinity and smaller grains.

■ ASSOCIATED CONTENT

ⓢ Supporting Information. Output characteristics of DMPT single-crystal FETs on NTS, r-NTS, HMDS, r-HMDS, CUTS, r-CUTS, OCTS, r-OCTS, ADTS, r-ADTS, mixed (NTS + ODTS), r-mixed (NTS + ODTS), bare SiO$_2$ and transfer characteristics on mixed (NTS + ODTS), r-mixed (NTS + ODTS). This material is available free of charge via the Internet at http://pubs.acs.org.

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■ ACKNOWLEDGMENT

■ REFERENCES

(1) (a) Murphy, A. R.; Frechet, J. M. J. *Chem. Rev.* **2007**, *107*, 1066–1096. (b) Gelinck, G.; Heremans, P.; Kazumasa Nomoto, K.; Anthopoulos, T. D. *Adv. Mater.* **2010**, *22*, 3778–3798. (c) Klauk, H. *Chem. Soc. Rev.* **2010**, *39*, 2643–2666. (d) Roberts, M. E.; Sokolov, A. N.; Bao, Z. *J. Mater. Chem.* **2009**, *19*, 3351–3363. (e) Dimitrakopoulos, C. D.; Malenfant, P. R. L. *Adv. Mater.* **2002**, *14*, 99–117.

(2) (a) Coropceanu, V.; Cornil, J.; da Silva Filho, D. A.; Olivier, Y.; Silbey, R.; Brédas, J.-L. *Chem. Rev.* **2007**, *107*, 926–952. (b) Brédas, J.-L.; Beljonne, D.; Coropceanu, V.; Cornil, J. *Chem. Rev.* **2004**, *104*, 4971–5004. (c) Marcus, R. A. *Rev. Mod. Phys.* **1993**, *65*, 599–610. (d) da Silva Filho, D. A.; Kim, E.-G.; Brédas, J.-L . *Adv. Mater.* **2005**, *17*, 1072–1076.

(3) (a) Kiguchi, M.; Nakayama, M.; Shimada, T.; Saiki, K. *Phys. Rev. B* **2005**, *71*, 035332. (b) Hayakawa, R.; Petit, M.; Chikyow, T.; Wakayama, Y. *Appl. Phys. Lett.* **2008**, *93*, 153301. (c) Fritz, S. E.; Martin, S. M.; Frisbie, C. D.; Ward, M. D.; Toney, M. F. *J. Am. Chem. Soc.* **2004**, *126*, 4084–4085. (d) Ruiz, R.; Papadimitratos, A.; Mayer, A. C.; Malliaras, G. G. *Adv. Mater.* **2005**, *17*, 1795–1798. (e) Dinelli, F.; Murgia, M.; Levy, P.; Cavallini, M.; Biscarini, F.; Leeuw, D. M. D. *Phys. Rev. Lett.* **2004**, *92*, 116802.

(4) (a) Veres, J.; Ogier, S.; Lloyd, G.; de Leeuw, D. *Chem. Mater.* **2004**, *16*, 4543–4555. (b) Facchetti, A.; Yoon, M.-H.; Marks, T. J. *Adv. Mater.* **2005**, *17*, 1705–1725. (c) Volksen, W.; Miller, R. D.; Dubois, G. *Chem. Rev.* **2010**, *110*, 56–110. (d) Yoon, M.-H.; Kim, C.; Facchetti, A.; Marks, T. J. *J. Am. Chem. Soc.* **2006**, *128*, 12851–12869. (e) Stassen, A. F.; de Boer, R. W. I.; Iosad, N. N.; Morpurgo, A. F. *Appl. Phys. Lett.* **2004**, *85*, 3899–3901.

(5) (a) Ortiz, R. P.; Facchetti, A.; Marks, T. J. *Chem. Rev.* **2010**, *110*, 205–239. (b) Jang, Y.; Kim, D. H.; Park, Y. D.; Cho, J. H.; Hwang, M.; Cho, K. *Appl. Phys. Lett.* **2006**, *88*, 072101. (c) Zhang, X.-H.; Tiwari, S. P.; Kim, S.-J.; Kippelen, B. *Appl. Phys. Lett.* **2009**, *95*, 223302. (d) Halik, M.; Klauk, H.; Zschieschang, U.; Schmid, G.; Dehm, C.; Schütz, M.; Maisch, S.; Effenberger, F.; Brunnbauer, M.; Stellacci, F. *Nature* **2004**, *431*, 963–966.

(6) (a) Suárez, S.; Fleiscli, F. D.; Schaer, M.; Zuppiroli, L. *J. Phys. Chem. C* **2010**, *114*, 7153–7160. (b) Wang, Z.-H.; Käfer, D.; Bashir, A.; Götzen, J.; Birkner, A.; Witte, G.; Wöll, C. *Phys. Chem. Chem. Phys.* **2010**, *12*, 4317–4323. (c) Goldmann, C.; Gundlach, D. J.; Batlogg, B. *Appl. Phys. Lett.* **2006**, *88*, 063501.

(7) (a) Kim, D. H.; Lee, H. S.; Yang, H.; Yang, L.; Cho, K. *Adv. Funct. Mater.* **2008**, *18*, 1363–1370. (b) Yang, H.; Shin, T. J.; Ling, M.-M.; Cho, K.; Ryu, C. Y.; Bao, Z. *J. Am. Chem. Soc.* **2005**, *127*, 11542–11543. (c) Kumaki, D.; Ando, S.; Shimono, S.; Yamashita, Y.; Umeda, T.; Tokito, S. *Appl. Phys. Lett.* **2007**, *90*, 053506.

(8) Kobayashi, S.; Nishikawa, T.; Takenobu, T.; Mori, S.; Shimoda, T.; Mitani, T.; Shimotani, H.; Yoshimoto, N.; Ogawa, S.; Iwasa, Y. *Nat. Mater.* **2004**, *3*, 317–322.

(9) (a) Huang, C.; Katz, H. E.; West, J. E. *Langmuir* **2007**, *23*, 13223–13231. (b) Pernstich, K. P.; Haas, S.; Oberhoff, D.; Goldmann, C.; Gundlach, D. J.; Batlogg, B.; Rashid, A. N.; Schitter, G. *J. Appl. Phys.* **2004**, *96*, 6431–6438.

(10) Weng, S.-Z.; Hu, W.-S.; Kuo, C.-H.; Fan, L.-J.; Yang, Y.-W.; Tao, Y.-T. *Appl. Phys. Lett.* **2006**, *89*, 172103.

(11) (a) Shtein, M.; Mapel, J.; Benziger, J. B.; Forrest, S. R. *Appl. Phys. Lett.* **2002**, *81*, 268–270. (b) Virkar, A. A.; Mannsfeld, S.; Bao, Z.; Stingelin, N. *Adv. Mater.* **2010**, *22*, 3857–3875. (c) Cicoira, C.; Santato, C.; Dinelli, F.; Murgia, M.; Loi, A. M.; Biscarini, F.; Zamboni, R.; Heremans, P.; Muccini, M. *Adv. Funct. Mater.* **2005**, *15*, 375–380.

(12) (a) Gershenson, M. E.; Podzorov, V.; Morpurgo, A. F. *Rev. Mod. Phys.* **2006**, *78*, 973–989. (b) Jiang, L.; Dong, H.; Hu, H. *J. Mater. Chem.* **2010**, *20*, 4994–5007. (c) Hasegawa, T.; Takeya, J. *Sci. Technol. Adv. Mater.* **2009**, *10*, 024314. (d) Reese, C.; Bao, Z. *Mater. Today* **2007**, *10*, 20–27. (e) de Boer, R. W. I.; Gershenson, M. E.; Morpurgo, A. F.; Podzorov, V. *Phys. Status Solidi A* **2004**, *201*, 1302–1331.

(13) Takeya, J.; Nishikawa, T.; Takenobu, T.; Kobayashi, S.; Iwasa, Y.; Mitani, T.; Goldmann, C.; Krellner, C.; Batlogg, B. *Appl. Phys. Lett.* **2004**, *85*, 5078–5080.

(14) Valiyev, F.; Huang, C. W.; Sheu, H. S.; Tao, Y. T. *Org. Electron.* Submitted for publication.

(15) Laudise, R. A.; Kloc, C.; Simpkins, P. G.; Siegrist, T. *J. Cryst. Growth* **1998**, *187*, 449–454.

(16) Mamada, M.; Kumaki, D.; Nishida, J.-i.; Tokito, S.; Yamashita, Y. *ACS Appl. Mater. Interfaces* **2010**, *2*, 1303–1307.

(17) Street, R. A.; Salleo, A. *Appl. Phys. Lett.* **2002**, *81*, 2887–2889.

(18) (a) Sirringhaus, H. *Adv. Mater.* **2005**, *17*, 2411–2425. (b) Völkel, A. R.; Street, R. A.; Knipp, D. *Phys. Rev. B* **2002**, *66*, 195336. (c) Steudel, S.; Vusser, S. D.; Jonge, S. D.; Janssen, D.; Verlaak, S.; Genoe, J.; Heremans, P. *Appl. Phys. Lett.* **2004**, *85*, 4400–4402. (d) Okamura, K.; Hahn, H. *Appl. Phys. Lett.* **2008**, *97*, 153114.

(19) Kang, S.-J.; Noh, Y.-Y.; Baeg, K.-J.; Ghim, J.; Park, J.-h.; Kim, D.-Y.; Kim, J. S.; Park, J. H.; Cho, K. *Appl. Phys. Lett.* **2008**, *92*, 052107.

(20) (a) Offord, D. A.; Griffin, J. H. *Langmuir* **1993**, *9*, 3015–3025. (b) Mathauser, K.; Frank, C. W. *Langmuir* **1993**, *9*, 3002–3008.

(21) (a) Suemori, K.; Uemura, S.; Yoshida, M.; Hoshino, S.; Takada, N.; Kodzasa, T.; Kamata, T. *Appl. Phys. Lett.* **2007**, *91*, 192112. (b) Fukuda, K.; Hamamoto, T.; Yokota, T.; Sekitani, T.; Zschiechang, U.; Klauk, H.; Someya, T. *Appl. Phys. Lett.* **2009**, *95*, 203301.

(22) Jedaa, A.; Burkhardt, M.; Zschieschang, U.; Klauk, H.; Habich, D.; Schmid, G.; Halik, M. *Org. Electron.* **2009**, *10*, 1442–1447.

(23) Salleo, A.; Chabinyc, M. L.; Yang, M. S.; Street, R. A. *Appl. Phys. Lett.* **2002**, *81*, 4383–4385.

(24) Park, B.; Paoprasert, P.; In, I.; Zwickey, J.; Colavita, P. E.; Hamers, R. J.; Gopalan, P.; Evans, P. G. *Adv. Mater.* **2007**, *19*, 4353–4357.

(25) Collet, J.; Vuillaume, D. *Appl. Phys. Lett.* **1998**, *73*, 2681–2683.