

# Energy-Band Engineering for Improved Charge Retention in Fully Self-Aligned Double Floating-Gate Single-Electron Memories

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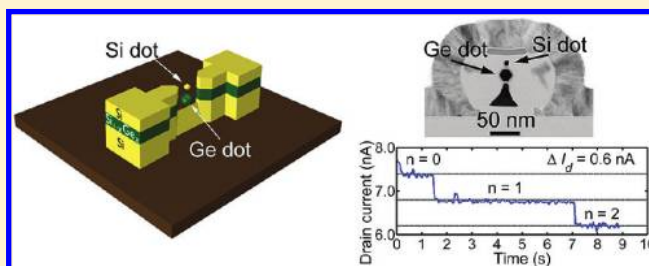
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**ABSTRACT:** We present a new fully self-aligned single-electron memory with a single pair of nano floating gates, made of different materials (Si and Ge). The energy barrier that prevents stored charge leakage is induced not only by quantum effects but also by the conduction-band offset that arises between Ge and Si. The dimensions and position of each floating gate are well-defined and controlled. The devices exhibit a long retention time and single-electron injection at room temperature.

**KEYWORDS:** Double floating-gate single-electron memory, heterostructure, quantum effects, conduction-band offset



To meet strict requirements of low power consumption, fast access speed, and high integration density, Si,<sup>1</sup> Ge,<sup>2,3</sup> metallic,<sup>4</sup> and other material<sup>5–7</sup> nanocrystals (NCs) are considered as the most promising candidates to replace the planar floating gates (FGs) in the upcoming generations of flash memory devices. The largest drawback of NC memory devices is the poor charge retention time caused by a very thin tunnel oxide. To fulfill 10-year retention times, double NC floating-gate memory devices were proposed. In the literature, the NCs of the double FG memories are generally made of the same material (either metal<sup>8,9</sup> or Si<sup>10,11</sup>). In the former case, Au and Ag NCs are the most appropriate materials to serve as FGs and Coulomb blockade effects arising between the upper and lower FGs prevent the electron stored in the upper FG from leaking into the channel, therefore improving retention time. However, metallic NCs easily diffuse into the channel region, tunnel, and control oxides during the subsequent high-temperature processes and are, therefore, not compatible with CMOS technology. In the Si case, quantum confinement and Coulomb blockade effects (hereafter referred to as “quantum effects”) in the lower Si FG induce an energy barrier that prohibits charge leakage from the upper FG to the channel, resulting in a longer retention time. Enabling these quantum effects at room temperature requires the diameter of the lower FG to be less than 5 nm. Furthermore, the two FGs need to have different diameters to avoid having the same energy distribution of the density of states in the two NCs, which would increase tunneling in a reverse manner. In order to accurately align the upper and lower NC FGs, Kane<sup>12</sup> proposed

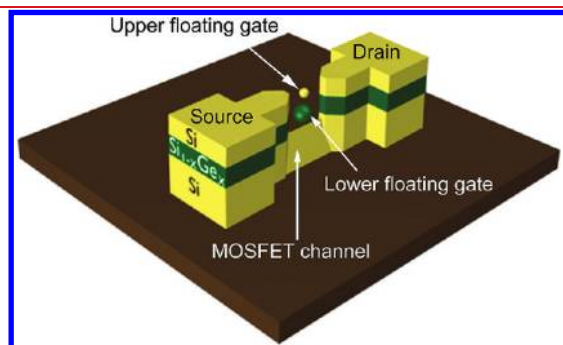
the formation of a lower FG mostly consisting of dopant atoms. Unfortunately, despite of the advances of modern technology, this approach remains impractical. As far as we know, most double NC FGs memory devices consist of two layers of NCs, formed by deposition or synthesis. This does not ensure uniform NC diameter and spatial distribution, and totally ignores the alignment of NCs forming a pair of FGs. Although self-aligned double NC FGs are obtained by oxidizing the amorphous Si layer below Si NCs,<sup>13</sup> each resulting device includes many pairs of NCs. The weakness of the multiple NC devices is the NC-to-NC lateral interference and the lateral direct tunneling current, which degrades device performance.<sup>14</sup> Particularly, the dispersions of the retention time and memory window due to single electron stochastic behaviors seriously affect the device reliability.<sup>15</sup> Clearly, the ultimate flash memory device would be a double FG single-electron memory, in which the storage of a single electron represents one bit and each memory cell only involves one set of FGs.

Nowadays, fabricating NCs and nanowires with a width less than 5 nm is not really an issue, but the difficult task is to use them as device components and to place them at the desired location. Here we present a new fabrication method for single-electron memory devices operating at room temperature based on the processing of a Si/Si<sub>1-x</sub>Ge<sub>x</sub>/Si heterostructure (Figure 1). The device features a single pair of NCs which act as FGs. These two

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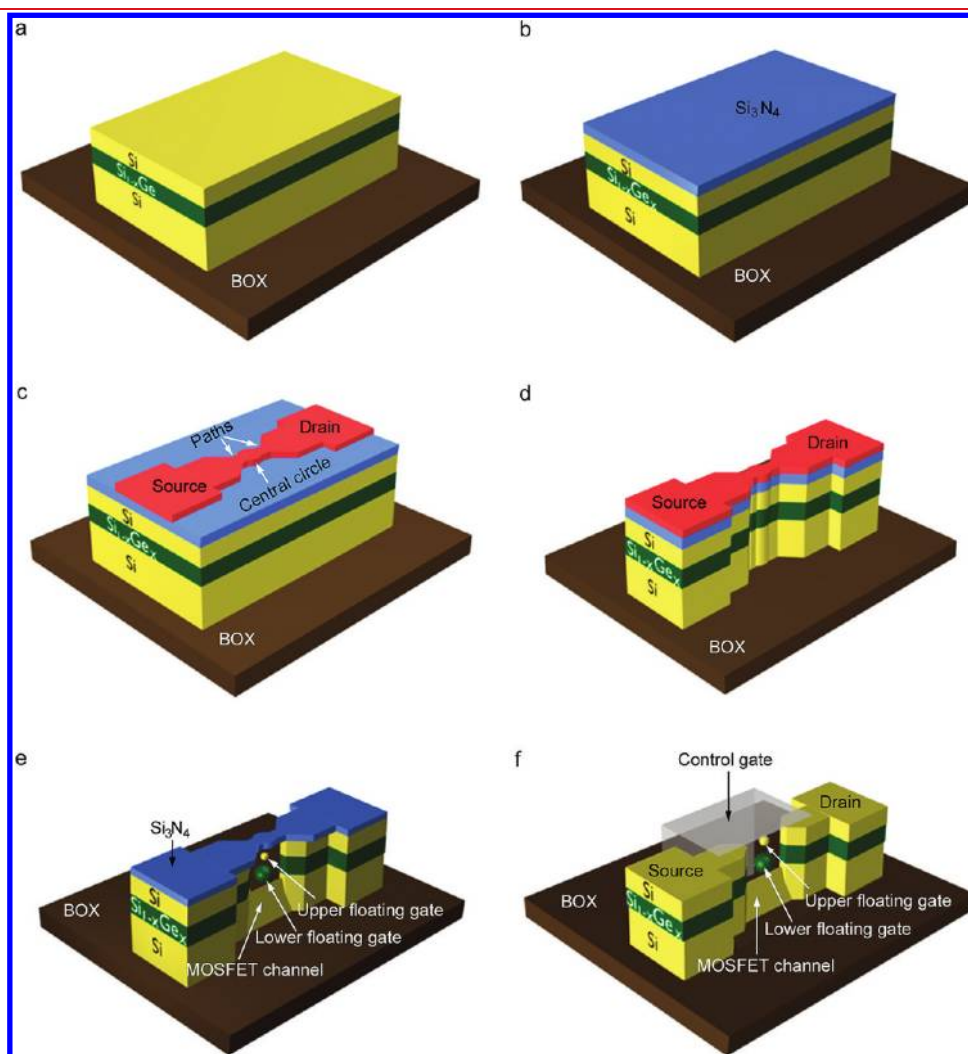
NCs are made of different materials (Si and Ge). Specifically, Si and Ge NCs are selected as the upper FG and the lower FG, respectively. Germanium  $\langle 100 \rangle$  has a smaller electron affinity



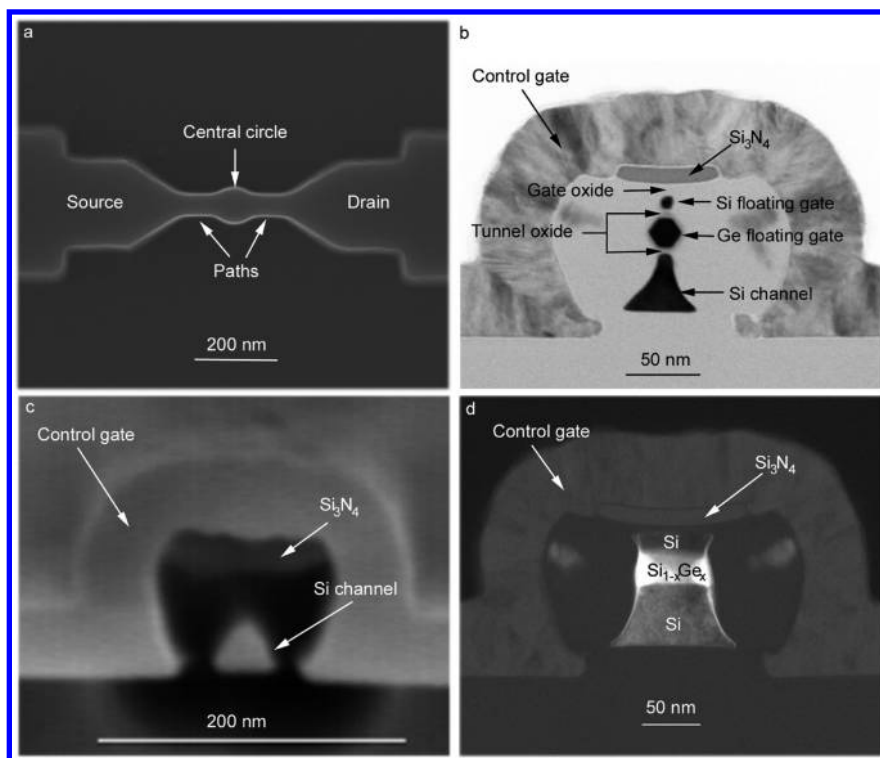
**Figure 1.** Schematic view of a fully self-aligned double floating-gate single-electron memory. The upper floating gate is a Si nanocrystal and the low floating gate is a Ge nanocrystal. Both floating gates are fully self-aligned to the channel of the nanowire MOSFET.

than silicon  $\langle 100 \rangle$ .<sup>16</sup> This creates a conduction-band offset between the Si and Ge NCs. In addition, the quantum confinement effect is stronger in the Ge NC because of lower effective mass. These facts translate to a high energy barrier between the upper FG and the channel of the memory device which makes it harder for electrons to leak out of the upper FG. Even if both NCs have the same size or if the lower NC has a diameter larger than 5 nm, the retention time is significantly improved. In our fabrication method, the size of each FG can be precisely defined and controlled by tuning the starting thicknesses of the Si and  $\text{Si}_{1-x}\text{Ge}_x$  layers. It is also important to note that both NCs are automatically self-aligned above the channel of the nanowire transistor.

The fabrication process is described in Figure 2. Layers of  $\text{Si}_{0.7}\text{Ge}_{0.3}$  and Si layers are successively grown by epitaxy<sup>17</sup> on a 50 nm thick, p-type silicon-on-insulator (SOI) wafer. Both grown layers have a thickness of 20 nm. The resulting heterostructure consists of a Si/ $\text{Si}_{0.7}\text{Ge}_{0.3}$ /Si (20/20/50 nm) stack on a 145 nm thick buried oxide (BOX), as shown in Figure 2a. A layer of  $\text{Si}_3\text{N}_4$  with a thickness of 10 nm is deposited on the heterostructure



**Figure 2.** Processing steps for fabricating the fully self-aligned double floating-gate single-electron memory: (a) a heterostructure composed of a Si/ $\text{Si}_{0.7}\text{Ge}_{0.3}$ /Si stack on a buried oxide (BOX), obtained by epitaxy; (b) a layer of  $\text{Si}_3\text{N}_4$  is deposited on the heterostructure surface to form a hard mask; (c) the device layout is composed of a central circle connected to wider source and drain regions by narrow paths; (d) the heterostructure is etched down to the BOX by reactive ion etching; (e) the upper Si floating gate and lower Ge floating gate are formed over the channel of the nanowire MOSFET by wet oxidation; (f) the control gate electrode is formed by a polysilicon or a metallic layer.



**Figure 3.** Electron microscope pictures of the device: (a) Scanning electron microscope (SEM) top view of the memory device before the formation of the control gate. The central circle is connected to wider source and drain regions by narrow paths. (b) Transmission electron microscope (TEM) cross-sectional picture of the center of the device showing the upper Si floating gate, the lower Ge floating gate, and the triangular Si channel of nanowire MOSFET. (c) SEM cross-sectional picture of the path region of the memory device, consisting of a Si triangular nanowire only. (d) SEM cross-sectional picture of the memory device in the source and drain regions. These regions are made of a Si/Si<sub>0.7</sub>Ge<sub>0.3</sub>/Si stack.

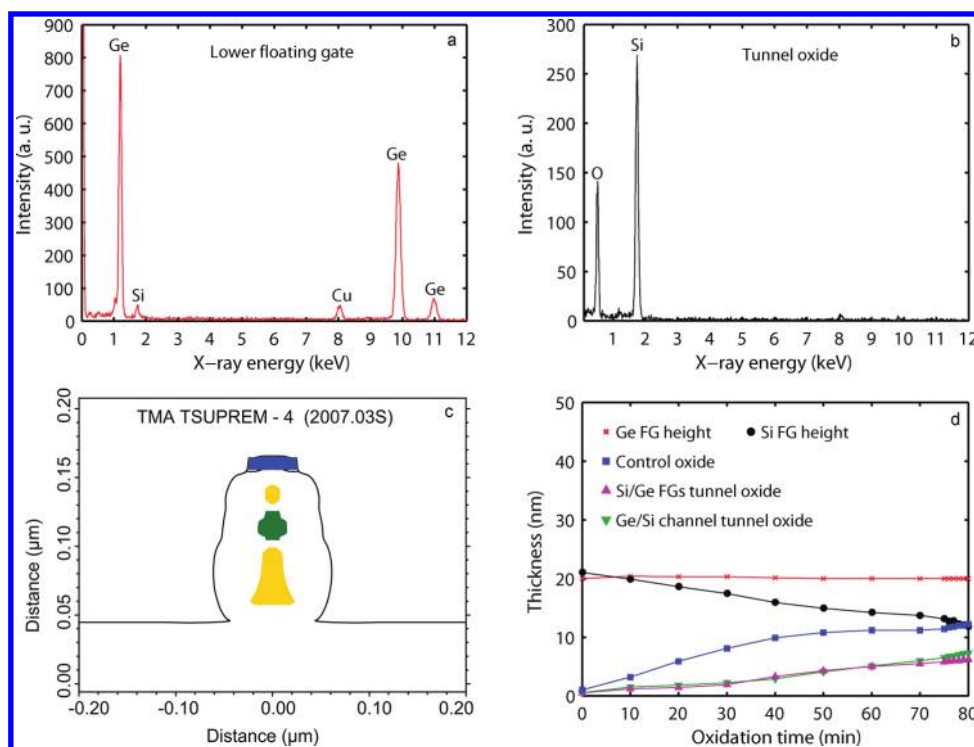
surface to form a hard mask (Figure 2b). The device layout (Figure 2c) is composed of a central circle with a diameter of 75 nm connected to wider source and drain regions (200 nm wide) by narrow paths (50 nm wide). The layout is patterned using electron-beam lithography, after which the heterostructure is etched down to the BOX using reactive ion etching (Figure 2d). Wet oxidation is next carried out at 750 °C for 75 min. During this step, both Si NC and Ge NC are simultaneously formed over a Si nanowire (Figure 2e) in the device center. The source/drain regions are doped using arsenic implantation at an energy of 140 keV and a dose of  $2 \times 10^{14} \text{ cm}^{-2}$ . Dopants are activated by rapid thermal annealing at 950 °C for 60 s. Finally, a control gate (Figure 2f) is deposited and patterned by electron-beam lithography.

Figure 3a shows a scanning electron microscope top view of a device before the formation of the control gate. Figure 3b is a cross-sectional transmission electron microscopy picture of the device center, in which a hexagonally shaped Ge NC with a thickness of 20 nm is found. It is vertically self-aligned to both the top Si NC (with a diameter of approximately 5 nm) and the bottom triangular Si nanowire. According to the theory of binary alloy oxidation,<sup>18</sup> oxide growth from an alloy depends on the alloy composition. For the oxidation of the Si<sub>0.7</sub>Ge<sub>0.3</sub> alloy, Si is preferentially oxidized due to the fact that SiO<sub>2</sub> has a larger negative Gibbs free energy than GeO<sub>2</sub>.<sup>19</sup> Si is thus first oxidized to form SiO<sub>2</sub>. Ge atoms pile up at the SiO<sub>2</sub>/Si<sub>0.7</sub>Ge<sub>0.3</sub> interface, forming a Ge-rich shell. Next, Si diffuses through the Ge-rich shell to react with oxygen which has diffused through the SiO<sub>2</sub> layer. Ge agglomerates continuously and the thickness of the Ge-rich shell

increases during oxidation. On the other hand, the oxygen concentration at the oxidation front decreases with the increase of the SiO<sub>2</sub> thickness. As a consequence, Ge itself is not oxidized and condensates instead, to form the Ge NC. The growth rate of the control gate oxide (10 nm) and double tunnel oxides is controlled by the density of point defects present at both the Si<sub>3</sub>N<sub>4</sub>/Si and Si/Si<sub>0.7</sub>Ge<sub>0.3</sub> interfaces. These point defects provide reaction sites for the formation of SiO<sub>2</sub>, thereby increasing the oxidation rate. Double tunnel oxides vertically separate the device center into a top Si NC, a middle Ge NC, and a Si bottom triangular nanowire, which are used as the upper FG, the lower FG, and the channel of the present memory device, respectively. The device layout shown in Figure 2c restricts both FGs to the device center since the top Si and Ge layers are completely consumed by oxidation in the narrow paths (Figure 3c). The source and drain regions (Figure 3d), where the 20 nm thick Si<sub>0.7</sub>Ge<sub>0.3</sub> layer appears as a brighter region, are wide enough to avoid the formation of the oxide layers at the interfaces. Thus, the oxidation process only exerts a negligible influence on the wide source and drain regions. As a result, both FGs are self-aligned to the channel and confined to the device center. It is noticeable that the diameter of the central circle in the layout is chosen in such a way that, after dry etching and wet oxidation, the diameter of the Si NC is less than 5 nm to guarantee single-electron injection at room temperature.

As expected, energy dispersive X-ray spectroscopy measurements confirm that the hexagonal lower FG is made of pure Ge as shown in Figure 4a. The theoretical calculation for the ratio of Si (33.5%) and O atoms (66.5%) also confirms that both tunnel





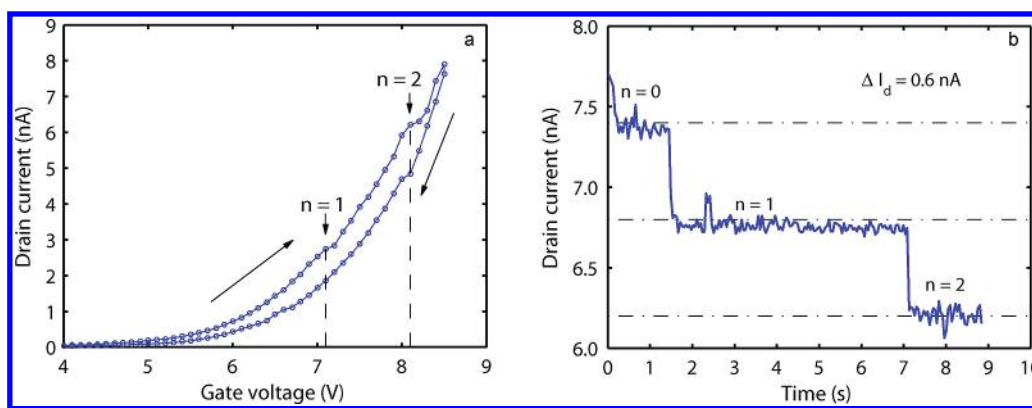
**Figure 4.** Energy dispersive X-ray spectroscopy (EDS) spectra and process simulation results: (a) EDS for the lower floating gate with an hexagonal shape, showing that it is made of pure Ge; (b) EDS for both tunnel oxides, indicating that it is a  $\text{SiO}_2$  layer; (c) simulated device center based on TSUPREM-4; (d) five main geometrical parameter evolutions of the double floating gate memory device (two floating gate heights, two tunnel oxide thicknesses and control oxide thickness) as a function of oxidation time at 750 °C.

oxides are  $\text{SiO}_2$  (Figure 4b). The fabrication process of the self-aligned double FG memory device is simulated by using TSUPREM-4. Figure 4c shows a simulation result for the device center. It is clearly seen that the double FG structure is formed during wet oxidation. We also evaluate five main geometrical parameters (two FGs heights, two tunnel oxide thicknesses, and control oxide thickness) required to be perfect control in the fabrication of the memory devices. Figure 4d plots of these parameters as a function of oxidation time. It is interesting to note that the height of the lower FG retains the initial thickness of the  $\text{Si}_{0.7}\text{Ge}_{0.3}$  layer (20 nm) during all the oxidation. Moreover, after 75 min, the height of the upper FG reaches saturation, self-limiting oxidation<sup>20</sup> making it difficult to be further reduced. In addition, after 50 min, the thicknesses of the three oxide layers become insensitive to the oxidation time. Compared to other anisotropic oxidation processes based on dopant enhancement<sup>21</sup> or pattern conversion,<sup>22</sup> both FGs are progressively separated. These facts indicate that the present process is well controlled thanks to the top nitride layer for protecting oxidation from the top and the  $\text{Si}_{0.7}\text{Ge}_{0.3}$  layer for enabling a tight control of the different geometrical parameters. Therefore, our process reproducibility and device reliability are very good so that it can be used for larger area memory fabrication.

In summary, the following distinctive advantages can be identified for the proposed architecture and the associated fabrication process: (i) The energy barrier height for preventing the charge leakage is increased by choosing two different materials for the floating gates. (ii) The size of both nanocrystal floating gates can be precisely controlled and defined by tuning the starting thicknesses of Si and  $\text{Si}_{0.7}\text{Ge}_{0.3}$  layers. (iii) Both

floating gates and the channel of the nanowire MOSFET are perfectly self-aligned. (iv) The control oxide and the two tunnel oxide layers are simultaneously formed in a single process step. (v) The fabrication process is reproducible and compatible with standard CMOS technology. (vi) The floating-gate lateral interference effect is fully avoided by using a single pair of nanocrystals. In addition, the proposed concept can be used not only for single/multiple memory device fabrication but also for other applications, such as quantum computing and logic circuits.<sup>12,23</sup>

An unambiguous signature of the single-electron injection in the FG is the drain current–gate voltage ( $I_d$ – $V_g$ ) hysteretic behavior with quantized threshold voltage shifts, where each current drop/jump corresponds to the injection of a single electron from the channel into the FG or the return of an electron from the FG to the channel.<sup>24,25</sup> Figure 5a demonstrates the hysteretic curve of a fully self-aligned double FG single-electron memory at room temperature. When the gate voltage is swept from 0 to 8.5 V, two current drops are observed. They are directly related to electrons from the channel that are injected into the FGs. Concerning the charging process of double-layer Si NCs, Lu et al.<sup>26</sup> experimentally reported that the electrons were charged by Fowler–Nordheim tunneling so that the electrons were first injected into the lower layer and then into the upper one. However, the simulation results of Yu et al.<sup>27</sup> indicated that the electron was first charged in the upper dot through the energy levels of the lower dot by direct tunneling. Here, we hypothesize that a first electron from the channel is injected into the upper FG through the lower FG at  $V_g = 7.1$  V, giving rise to the first current drop in the  $I_d$ – $V_g$  curve. Once this first electron is injected into the lower FG, it is energetically favorable to be



**Figure 5.** Electrical characteristics of a fully self-aligned double floating-gate single-electron memory device at room temperature: (a) hysteretic behavior at  $V_d = 500$  mV, showing two/one drain current drops/jump when the gate voltage is swept forth/back; (b) time evolution of drain current at  $V_g = 8.5$  V and  $V_d = 500$  mV, showing the quantized current steps.

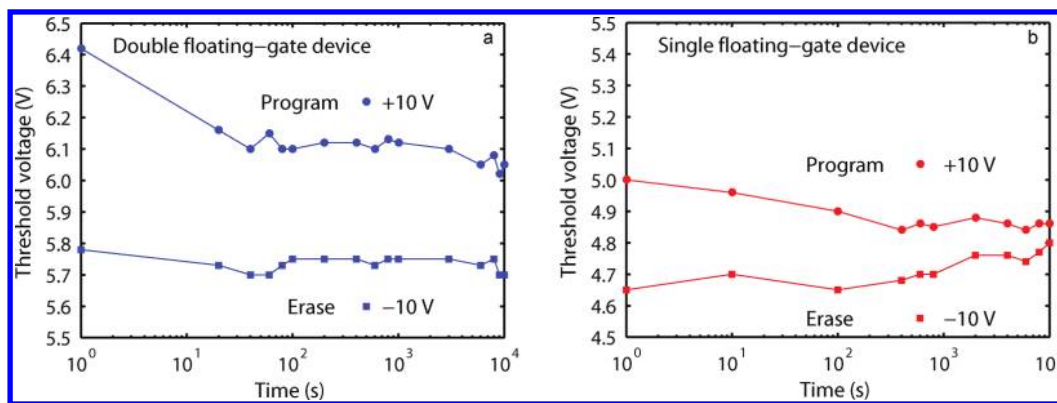
injected into the upper one as we will discuss later on. When  $V_g$  is further increased to 8.1 V, a second electron is injected into the upper FG by the same way. The condition to observe Coulomb blockade in a practical device requires the charging energy ( $q^2/2C_\Sigma$ ) to be at least 3 times larger than the thermal energy ( $k_B T$ ,  $\sim 26$  meV at 300 K). Ignoring the quantum confinement energy, we estimate the diameter  $d$  of a conducting sphere embedded in a  $\text{SiO}_2$  matrix to be 4.7 nm when  $q^2/2C_\Sigma = 3k_B T$ , where  $C_\Sigma (=2\pi\epsilon_{\text{ox}}d)$  is the self-capacitance of the sphere.<sup>28</sup> The upper FG diameter of approximately 5 nm in Figure 3b is similar to the estimated value. This suggests that single-electron charging takes place only in the upper FG since the charging energy corresponding to the lower FG of 20 nm is 18 meV. Even if the quantum confinement energy (13 meV) is taken into account, the characteristic energy (the sum of the quantum confinement energy and the charging energy) of the lower FG is still less than  $3k_B T$ . When the gate voltage is swept in reverse, only one visible jump is observed in the  $I_d$ – $V_g$  curve. This jump is more likely attributed to the return of electrons stored in the lower FG since the positive energy barrier existing between the upper and lower FGs impedes the return of electrons stored in the upper FG. Yu's simulation results also prove that the retention ability of the lower FG is very limited. It is worth noting that this device is not optimized to reach high performance so that a larger threshold voltage is obtained. Reference devices neither with Si FG nor with Ge FG are fabricated by the same process. They do not exhibit any hysteretic phenomena and current drop. This means that the electrons are stored within the FGs or in traps present at the interface of the FGs and  $\text{SiO}_2$  dielectric.<sup>29</sup>

To further investigate the single-electron injection mechanism, the time evolution of the drain current ( $I_d$ – $t$ ) is studied. First, a negative pulse of  $-10$  V for 1 s is applied to the control gate to remove the electrons stored in both FGs or set both FGs in their initial state. Then a voltage of 8.5 V is applied to the gate and maintained constant during the measurements. Figure 5b shows one typical  $I_d$ – $t$  characteristic curve measured at room temperature. After a short transient,  $I_d$  stabilizes at 7.4 nA. When the first electron is injected into the FGs, an abrupt reduction of  $I_d$  is observed at  $t = 1.5$  s. As time goes by, a second electron is injected into the FGs, at which point a second reduction of  $I_d$  appears ( $t = 7$  s). The quantization of the current steps,  $\Delta I = 0.6$  nA, confirms that the steps are the result of single-electron injection, which can only take place in the upper FG, rather than

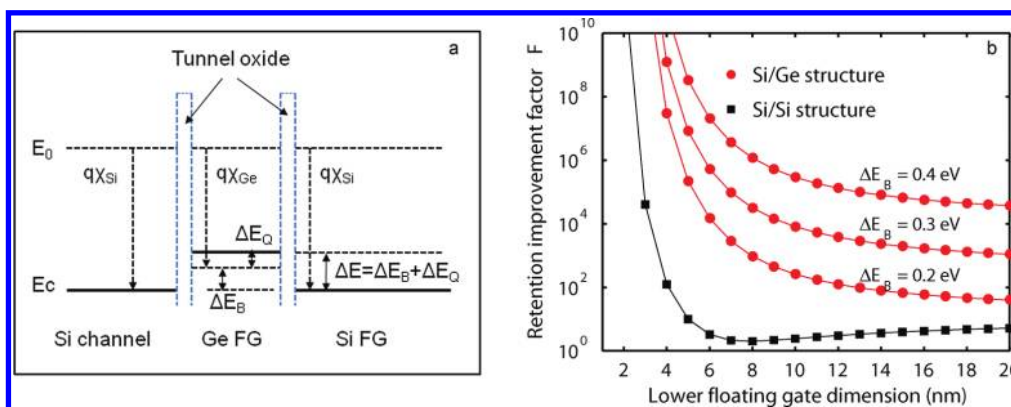
in the lower one because of its larger size. We also observed the quantization of the current steps in our previous memory device with a single Si floating gate of about 5 nm.<sup>30</sup> That indicates that the electrons are stored in the upper FG. By repeating the same measurement more than 100 times, we calculated the average injection time of the first electron to be 1 s at 8.5 V, which is of the same order of magnitude as that of our previous single FG memory device, with 0.7 s at 5.58 V.

Figure 6a presents the retention characteristics of the fully self-aligned double FG memory device, measured with  $\pm 10$  V, 10 s long gate pulses at room temperature. Taking into account the specifications of our device structure (two FGs and a thick control oxide layer), we define the threshold voltage as the gate voltage corresponding to  $I_d = 0.5$  nA at  $V_d = 500$  mV. During the first  $\sim 100$  s, there is a degradation of the memory window showing about 50% charge loss (i.e., one of the two stored electrons), after which the memory window remains stable up to  $10^4$  s. It can be speculated that the 50% charge loss of the device originates from electrons stored in the lower FG returning to the close Si channel because the negative energy barrier between the lower Ge FG and Si channel makes it easier for electrons to leak out of the lower FG. To compare the retention time of the double FG memory device with that of the single FG memory device, we also fabricated a single FG memory device with a Si FG of about 5 nm and a control oxide of 20 nm. The tunnel oxide thickness of this device approximately equals to the sum of the two tunnel oxide thickness in the double FG memory device. Figure 6b shows the memory window of the single FG memory device. The memory window width tends to zero with increasing time. Concerning the charge loss of the double and single FG memory devices, the former is 50% in  $10^4$  s and will remain stable afterward, while the latter will tend to zero after  $10^4$  s. This confirms that the lower FG plays an important role in the retention characteristics, which makes charge retention time longer than in the single FG.

More importantly, our double FG memory device shows a longer electron retention time compared to the memory device consisting of two layers of Si NCs.<sup>13</sup> The explanation is the following. We consider two double FG single-electron memory devices. For the first one, both FGs are made of Si (Si/Si structure), while for the other one, the upper and lower FGs are made of Si and Ge, respectively (Si/Ge structure). In both structures, the upper FG has the same size of 5 nm as the actual



**Figure 6.** Retention properties of the devices with single Si floating gate and double floating gates (Si/Ge) at room temperature: (a) Memory window of the double floating-gate memory device with programming/erasing at  $\pm 10$  V for 10 s. The threshold voltage was defined at  $I_d = 0.5$  nA and  $V_d = 500$  mV. After 100 s, the memory window width gets mostly saturated with time. (b) Memory window of the single floating-gate memory device with programming/erasing at  $\pm 10$  V for 10 s. The memory window width tends to zero with increasing time.



**Figure 7.** Energy-band diagram of the double floating-gate memory and the retention improvement factor for the double floating-gate devices with either two Si floating gates (Si/Si) or the combination of Si and Ge floating gates (Si/Ge). (a) Energy band diagram in a low or zero gate voltage configuration. The energy barrier  $\Delta E$  is the sum of the conduction-band offset  $\Delta E_B$  between Ge and Si and the characteristic energy  $\Delta E_Q$  induced by Coulomb blockade and quantum confinement effects. (b) Calculated retention improvement factors for two types of structures (Si/Si and Si/Ge) as a function of the lower floating gate dimension  $d$ .

device. All tunnel oxides are supposed to be equally thick. Under these conditions, the electron retention time is determined by the energy barrier height as shown in the energy band diagram (Figure 7a). In the Si/Ge structure, the electron affinity of Ge is smaller than that of Si in the  $\langle 100 \rangle$  direction.<sup>16</sup> Therefore, the energy barrier height  $\Delta E$  for the electron tunneling from the upper FG to the channel is the sum of  $\Delta E_Q$  and  $\Delta E_B$ , where  $\Delta E_Q$  is the characteristic energy originating from quantum effects in the lower FG, and  $\Delta E_B$  is the conduction-band offset between Ge and Si. In the Si/Si structure, the electrons stored in the upper FG only pass through  $\Delta E_Q$  to go back to the channel. But, in the Si/Ge structure (our case), the electrons have to overcome the larger  $\Delta E$  barrier. Therefore, the electron tunnel probability is lower, resulting in a longer retention time. To investigate the retention improvement brought by the energy band engineering, we make use of the model reported in ref 13 to calculate a retention improvement factor for both structures. The retention improvement factor  $F$  is defined by the ratio of the electron tunnel probability in the single and double FG memory devices, and at a low bias, it is given by

$$F = \left( \frac{2k_B T}{\Delta E} \right) \sinh \left( \frac{\Delta E}{k_B T} \right) \quad (1)$$

with

$$\Delta E = \Delta E_B + \Delta E_{Q, \text{lower}} - \Delta E_{Q, \text{upper}}/2 \quad (2)$$

where  $k_B$  is the Boltzmann constant,  $T$  is the temperature (300 K in this work),  $\Delta E_B$  is the energy-band offset between two FGs, and  $\Delta E_{Q, \text{lower}}$  and  $\Delta E_{Q, \text{upper}}$  are the characteristic energies of the lower and upper FGs, respectively. In the Si/Si structure,  $\Delta E_B = 0$ , while in the Si/Ge structure,  $\Delta E_B$  is the conduction-band offset. In this calculation, the upper FG size is set to 5 nm as the real device, the Coulomb charging energy is calculated using the electrostatic capacitance of a conducting sphere with a diameter  $d$ , and the quantum confinement energy is approximated assuming that the nanocrystal is a cube with a size similar to  $d$ . The calculation results are presented in Figure 7b. For the Si/Si structure (the line with square markers), we notice that only when the lower FG size is smaller than 5 nm, the retention time is significantly improved compared to the single FG device. But when the lower FG is larger than the upper one, the retention time improvement becomes very limited since  $\Delta E$  becomes negative (see eq 2). Therefore, the latter case could not serve as a memory cell. Concerning the Si/Ge structure, for a fixed retention improvement factor, a greater conduction-band offset  $\Delta E_B$  allows the lower FG to be larger.



Alternately, for a given lower FG size, the greater the conduction-band offset, the greater the retention improvement factor. This argumentation lends strong support to our experimental results and greatly relaxes the size constraints on the lower floating gate.

In conclusion, we report a new method for fabricating fully self-aligned double floating-gate single-electron memory devices using a Si/Si<sub>1-x</sub>Ge<sub>x</sub>/Si multilayered structure. The fabricated device contains only a single pair of floating gates: an upper Si nanocrystal floating gate (~5 nm) and a lower Ge nanocrystal floating gate (~20 nm). Both floating gates are automatically self-aligned to the channel of the nanowire transistor. The size of each floating gate can be precisely controlled by modulating the thickness of the initial Si and Si<sub>1-x</sub>Ge<sub>x</sub> layers and self-limiting oxidation. The energy barrier that prevents charge leakage from the nanocrystals arises both from quantum effects and from the conduction-band offset that exists between Ge and Si. This offset significantly increases the retention time of the memory device. This method opens a new perspective for future designs of multiple-level memory cells and quantum computers. The proposed memory device demonstrates two decisive advantages: a long retention time and a single-electron injection at room temperature.

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