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# Controlled Synthesis of Phase-Pure InAs Nanowires on Si(111) by Diminishing the Diameter to 10 nm

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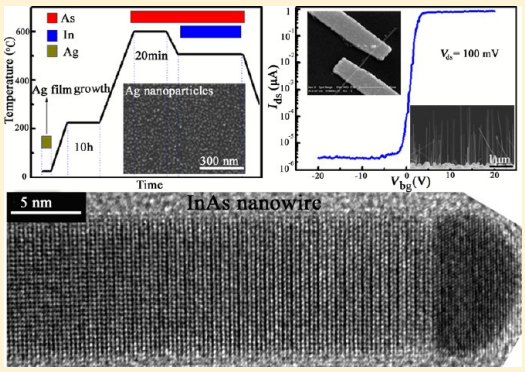
Supporting Information

**ABSTRACT:** Here we report the growth of phase-pure InAs nanowires on Si (111) substrates by molecular-beam epitaxy using Ag catalysts. A conventional one-step catalyst annealing process is found to give rise to InAs nanowires with diameters ranging from 4.5 to 81 nm due to the varying sizes of the Ag droplets, which reveal strong diameter dependence of the crystal structure. In contrast, a novel two-step catalyst annealing procedure yields vertical growth of highly uniform InAs nanowires ~10 nm in diameter. Significantly, these ultrathin nanowires exhibit a perfect wurtzite crystal structure, free of stacking faults and twin defects. Using these high-quality ultrathin InAs nanowires as the channel material of metal-oxide-semiconductor field-effect transistor, we have obtained a high $I_{ON}/I_{OFF}$ ratio of ~$10^6$, which shows great potential for application in future nanodevices with low power dissipation.




**KEYWORDS:** *InAs nanowires, pure phase, molecular-beam epitaxy, InAs nanowire-based FET*

Semiconductor nanowires have attracted increasing interest in recent years since they show great potential to be used as building blocks for nanophotonics, nanoelectronics, and biosensing devices.[1−6] As a technologically important III−V semiconductor, nanowires of InAs are promising candidates for applications in single-electron transistors,[7] resonant tunneling diodes,[8] and ballistic transistors[9] due to their very high electron mobility and narrow band gap. To date, much work has been done to grow InAs nanowires on various substrates.[10−14] Among them, InAs nanowires grown on Si substrates are of particular significance and have been investigated by many groups[15−20] since it may enable nanowire electronic devices with seamless integration with the Si platform. However, InAs nanowires usually exhibit random mixtures of wurtzite (WZ) and zinc-blende (ZB) crystal structures, which deteriorates the electrical properties of the InAs nanowires[21] and may pose problems in future nanoelectronic devices due to electron scattering at stacking faults or twin planes.[22,23] Therefore, achieving phase purity in InAs nanowires is a necessity for many device applications. So far, several approaches have been proposed to grow high-quality InAs nanowires, such as tailoring the basic growth parameters,[24−29] varying the nanowire growth direction,[30] and changing the nanowire diameter.[25,31] In particular, theoretical and experimental studies demonstrated that controlling the diameter down to a certain value, for example, 20 nm, is one of the effective methods to obtain excellent crystal phase purity for InAs nanowires.[32,33] Such thin nanowires show unique physical properties and potential applications in future nanodevices and nanocircuits.[34,35] Nevertheless, to the best of our knowledge, using approaches mentioned above, high-quality InAs nanowires have only been realized on substrates of III−V semiconductors rather than Si; controlling of the quality of InAs nanowires on Si substrates in terms of the crystal structure still remains a challenge.

In this Letter, we present Ag-catalyzed growth of high-quality InAs nanowires on Si (111) by molecular-beam epitaxy (MBE). It is found that the crystal structure of InAs nanowires varies strongly with the diameter. A pure WZ phase InAs nanowire can be achieved for the nanowires with smaller diameters (≤48 nm), but these nanowires densities are very low, and nanowire diameters are difficult to control since the conventional catalyst annealing process leads to large variations of Ag droplet size. To solve this problem, we develop a two-step catalyst annealing process, which produces Ag nanoparticles of uniform size. Consequently, InAs nanowires with an average diameter of 10 nm have been grown normal to the Si substrate surface with a

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perfect WZ crystal structure, free of stacking faults and twin defects. Such ultrathin InAs nanowires are used as the channel materials to produce high-performance metal-oxide-semiconductor field-effect transistors (MOSFET) with a high $I_{ON}/I_{OFF}$ ratio ($\sim 10^6$).

InAs nanowires were grown by MBE (VG system) based on a Ag-catalyzed nanowire growth method.[36] Commercial n-type Si (111) wafers were used as the substrates. Before loading the Si substrates into the MBE chamber, they were immersed in a diluted HF (2%) solution for 1 min to remove the surface contamination and native oxide. For catalyst deposition, we used a Ag effusion cell attached to the III−V growth chamber. This configuration enabled us to deposit the catalyst on a chemically clean surface and at the same time to control the substrate temperature and monitor the deposition process with reflection high-energy electron diffraction. All of the Ag layers (0.5−2 nm) were deposited at room temperature and then annealed in situ by using the substrate heater of the MBE system to generate Ag nanoparticles. In this work, two different catalyst annealing processes were used, and the resulting InAs nanowires were compared, which will be discussed in detail below. A range of growth parameters (growth temperature and V/III flux ratio) were explored for the Ag-catalyzed InAs nanowire growth, and optimum growth conditions were identified. We found that InAs nanowires can be grown over a temperature range from 380 to 530 °C (see Supporting Information, Figure S1). The nanowire density and the growth rate as well as their morphology vary with the changing V/III flux ratio. The density and the growth rate of the nanowires increase substantially with decreasing the V/III flux ratio from 80 to 10 (by keeping the As flux constant and increasing the In flux, see Supporting Information, Figure S2). In addition, a significant lateral growth of the nanowires can be observed when a low V/III flux ratio (≤20) is used. The optimum growth temperature and V/III ratio are 505 °C and 30, respectively. All of the InAs nanowires investigated below were grown under the optimum growth conditions for 40 min. Growth was terminated by switching off In supply while maintaining As supply until the substrate was cooled down below 300 °C. The morphologies of the InAs nanowires were investigated by a scanning electron microscope (SEM) (a Nova NanoSEM 650). The crystal structure of the nanowires was characterized by FEI Tecnai F20 and F30 transmission electron microscopes operated at 200 kV and 300 kV, respectively. For high-resolution transmission electron microscope (HRTEM) analysis, nanowires were removed from the growth substrate via sonication in ethanol and then drop-cast onto lacey carbon grids. The chemical composition of the nanowires and seed particles was evaluated by scanning TEM (STEM), operating in both the line scan and point analysis mode.

For the electrical characterization of the ultrathin nanowires, we fabricated back-gated field-effect transistors. The as-grown InAs nanowires were transferred onto a $p^+$-doped Si substrate covered by 300 nm thermally grown $SiO_2$. Nanowires with a diameter about 10 nm were identified and located using SEM. Then the samples were spin-coated with PMMA, and patterns of the contact electrodes were defined by electron beam lithography. Before depositing metal, the oxide layer covering the InAs nanowires was removed by etching the sample in a solution of $(NH_4)_2S_x$:$H_2O$ = 1:39 for 3 min followed by rinsing in water. A Cr/Au (15 nm/45 nm) film was then evaporated followed by lift-off in acetone. Finally, the samples were coated with 10 nm of $Al_2O_3$ by atomic layer deposition at 250 °C. The electrical properties of the FETs were measured on a probe station using a semiconductor parameter analyzer at room temperature.

InAs nanowires were first grown using the conventional one-step catalyst annealing process. As shown in Figure 1a, the Ag nanoparticles were generated by annealing a thin Ag film at a high temperature (600−650 °C) directly. From the SEM image of a pregrowth Si (111) substrate, onto which was deposited a Ag film of average thickness of 0.5 nm and subjected to the one-step annealing, the Ag droplets have a size distribution ranging from a few nanometers to about one hundred nanometer (Figure 1b) resulting from the Ostwald ripening.[37] The inset in Figure 1b shows the corresponding side-view SEM image of the Ag-catalyzed InAs nanowires. InAs nanowires with different diameters can be observed on the same sample due to the inhomogeneous size of the Ag droplets. Notably, those ultrathin wires grew perpendicularly to the substrate surface, that is, along the [111] direction, while the thick nanowires in our sample exhibited random growth directions. It is also worth noting that the density of ultrathin wires was very low, which was probably caused by the very low density of small Ag droplets (Figure 1b) owing to the Ostwald ripening, based on

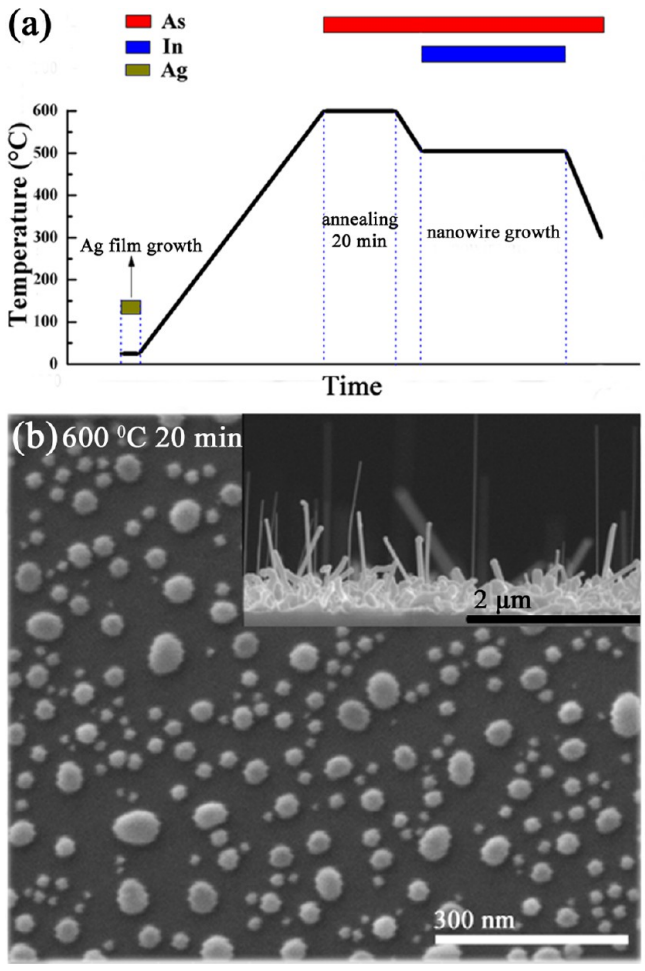


**Figure 1.** (a) Schematic illustrations of the temperature sequence for a one-step Ag annealing process and the subsequent InAs nanowire growth; (b) SEM image of the pregrowth Ag droplets distribution on a substrate with a starting Ag film of average thickness of 0.5 nm (top view). Inset shows corresponding SEM image of the InAs nanowires (side view).


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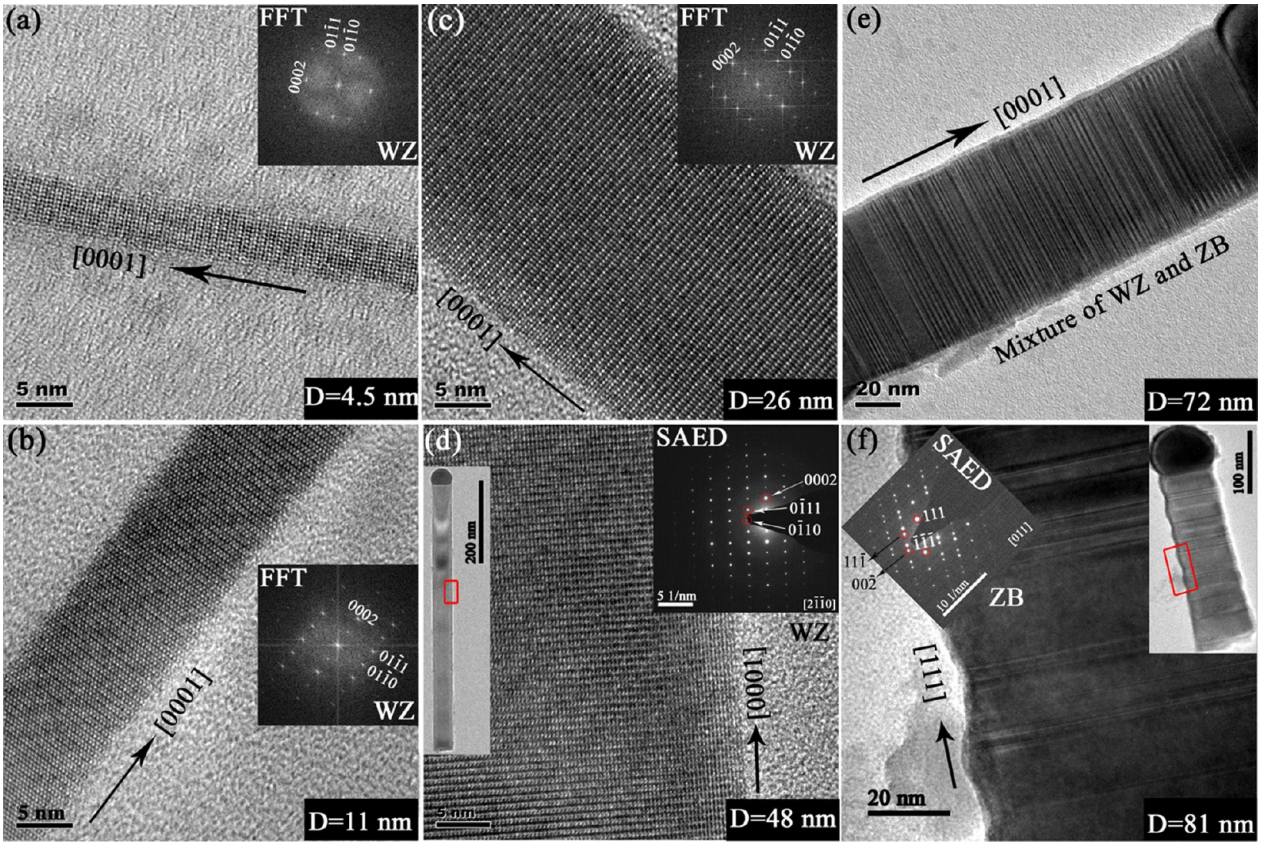


**Figure 2.** Evolution of the crystal structure (from WZ to ZB) with diameter of the Ag-catalyzed InAs nanowires grown on a substrate with Ag catalysts prepared by the one-step annealing process. (a) 4.5 nm; (b) 11 nm; (c) 26 nm; (d) 48 nm; (e) 72 nm; (d) 81 nm.

which the bigger droplets form by consuming smaller ones in the neighborhood. The length of the ultrathin nanowires in our sample varies from 1 to 3 $\mu$m, while those of the large diameter wires are shorter ($\leq$1 $\mu$m). Also, the density of the ultrathin nanowires decreases as the annealing temperature increases from 600 to 650 °C (not shown here). The size distribution of the InAs nanowires has no discernible differences. For the synthesized nanowires, both EDX line scans and point analysis indicate that the nanowire contains In and As and the catalyst particle is composed of Ag and In (see Supporting Information, Figure S3).

To determine the structural characteristics of the Ag-catalyzed InAs nanowires grown by means of the one-step catalyst annealing process, TEM measurements were performed on the wires grown along the [111] direction. Figure 2 shows TEM images of several InAs nanowires with diameters ranging from 4.5 to 81 nm. One can see from Figure 2a that the nanowire with a diameter of 4.5 nm has a pure WZ crystal phase with no stacking faults or other defects. To the best of our knowledge, this is the first report of successful growth of InAs nanowires with a diameter in the sub-5 nm range. Increasing the diameter slightly up to 11 nm (Figure 2b), 26 nm (Figure 2c), and until to 48 nm (Figure 2d), the structure remains pure WZ. For larger diameters (72 nm; Figure 2e), the structure is composed of a mixture of the WZ and ZB phases. Finally, for even larger diameters (81 nm, Figure 2f), a transition to ZB is observed. Our results are consistent with the theoretical work[38,39] and experimental results[25,26] on III−V substrates. That is, for small diameters, the InAs nanowires exhibit a pure WZ structure, and there is a crossover to the ZB structure when the diameter increases. In our experiment, we found pure WZ structure in the InAs nanowires with diameter up to 48 nm, and this value is larger than the values reported in the literature.[25,39] This may be attributable to the different growth method and growth parameters used, and the strong radius dependence of the WZ probability might be related to the difference of supersaturation during nanowire growth as reported in GaAs nanowires.[40] For those InAs nanowires grown along the non-[111] directions, pure WZ structured nanowires are observed with growth along [0−110] direction (see Supporting Information, Figure S4).

Although pure WZ InAs nanowires have been realized in our sample by the one-step catalyst annealing process, the diameter of the nanowires vary over a broad range. From previous studies[25,28] and the results mentioned above, it is clear that the nanowire diameter has a significant effect on its crystal structure and consequently could impact the electronic properties greatly.[41] Moreover, it is well-known that any well-controlled method to shrink the dimensions of nanoelectronic components could result in significant progress in the semiconductor microelectronics technology. Therefore, the ability to consistently grow ultrathin nanowires of uniform size, structure, and electronic properties is of great importance. However, it has been difficult to realize ultrathin InAs nanowires with a uniform morphology on a large scale, since the conventional annealing method is not well suited for preparation of a homogeneous catalyst film with a thickness less than one nanometer owing to Ostwald ripening. To address this issue, we developed a novel two-step catalyst annealing process to synthesize single-crystal ultrathin InAs nanowires. In the so-called two-step catalyst annealing process, the Ag film was first annealed at 200 °C for 10 h in the sample preparation chamber


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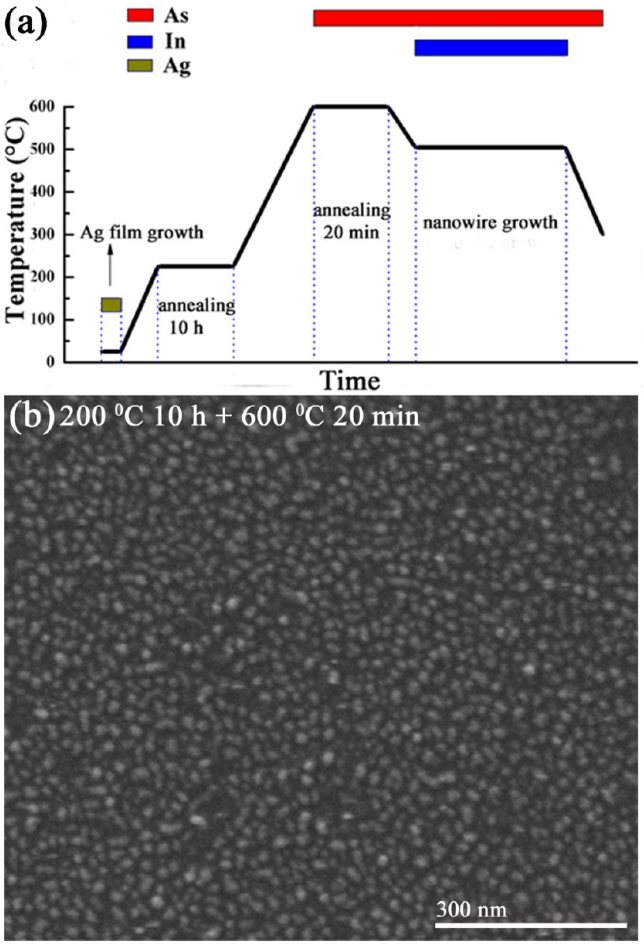


**Figure 3.** (a and b) Schematic illustrations of the temperature sequence for a two-step Ag annealing process and corresponding SEM images of the resulting pregrowth Ag droplets from a starting Ag film of an average thickness of 0.5 nm (top view), respectively.

and then annealed again at a higher temperature in the growth chamber to dewet the Ag film into nanoparticles (Figure 3a). Through this procedure, homogeneous Ag nanoparticles with small and uniform diameters were obtained, as shown in Figure 3b. We conjecture that the strain release of the thin Ag film during the low temperature annealing process is one of the possible reasons for the formation of small Ag nanoparticles, while the exact mechanism remains to be determined.

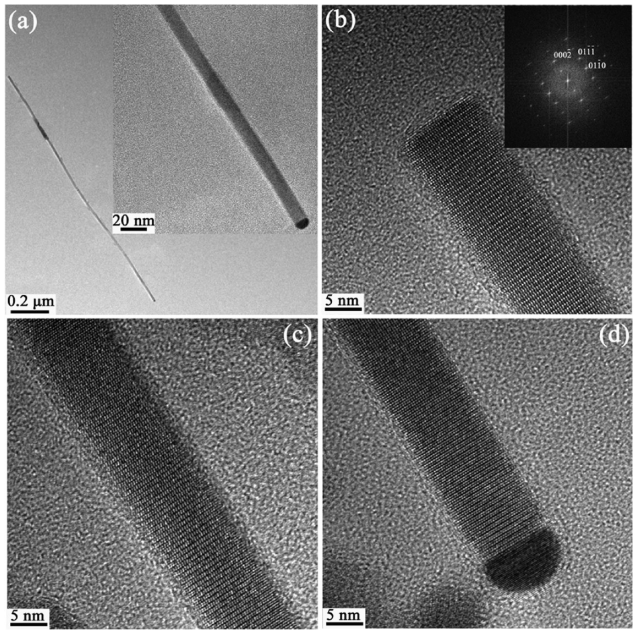


**Figure 5.** TEM images of a Ag-catalyzed ultrathin InAs nanowire. (a) A representative ultrathin InAs nanowire with the inset showing a magnified view of the catalyst region; (b, c, and d) HRTEM images taken from the bottom, center, and top of the nanowire, respectively. The inset is the fast Fourier transform of (b).

Figure 4 shows SEM images of ultrathin InAs nanowires grown with Ag-catalyst templates prepared via the two-step annealing process. The average deposited Ag thicknesses were 0.5−2 nm. Each template was first annealed at 200 °C for 10 h and then annealed at a different higher temperature for 20 min. As shown in Figure 4a−d, ultrathin InAs nanowires oriented perpendicular to the substrate surface were obtained with substrates of Ag film thicknesses from 0.5 to 2 nm and annealed at 600−650 °C. The resulting nanowires had an average diameter and height of ∼10 nm (ranging from 7 to 13 nm, see

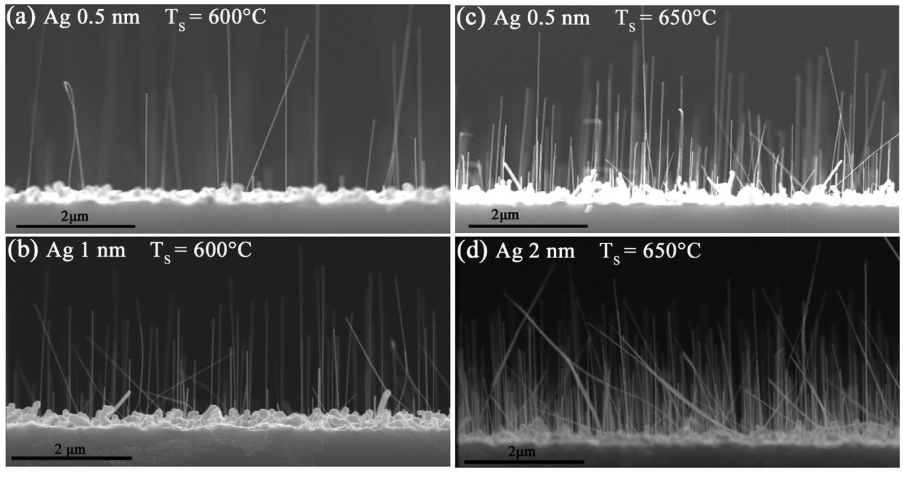


**Figure 4.** SEM images (side view) of Ag-catalyzed ultrathin InAs nanowires grown on substrates with starting Ag film thicknesses of 0.5−2 nm. The Ag films were first annealed at 200 °C for 10 h in the sample preparation chamber and then annealed at different temperatures for 20 min in the growth chamber. (a) Ag 0.5 nm, $T_{Annealing}$ ($T_A$) = 600 °C; (b) Ag 1 nm, $T_A$ = 600 °C; (c) Ag 0.5 nm, $T_A$ = 650 °C; (d) Ag 2 nm, $T_A$ = 650 °C.


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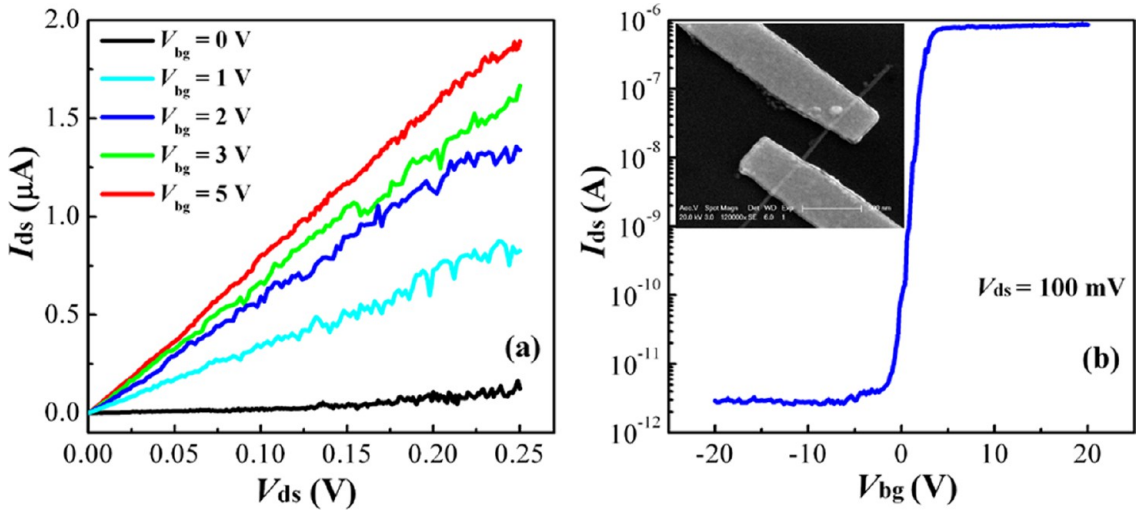


**Figure 6.** Output and transfer characteristics of an FET based an ultrathin InAs nanowire: (a) Current as a function of source-drain voltage for backgate voltages of 0, 1, 3, and 5 V. (b) Modulation of the current through the nanowire at a source−drain bias voltage $V_{ds}$ = 100 mV by the voltage applied to the backgate. The inset is an SEM image of the ultrathin InAs nanowire with Cr/Au source−drain contacts.

Supporting Information, Figure S5) and 2 $\mu$m (ranging from 1 to 3 $\mu$m), respectively. It is clear that the nanowire density can be controlled by the Ag film thickness and annealing temperature. When increasing the Ag film thickness from 0.5 nm (Figure 4a) to 1 nm (Figure 4b) or increasing the annealing temperature from 600 °C (Figure 4a) to 650 °C (Figure 4c), the InAs nanowire density increases significantly owing to the increased Ag nanoparticle density. Obviously, the higher annealing temperature is favorable to generating higher Ag nanoparticle density. However, when the annealing temperature exceeded 690 °C an opposite trend was observed: the density of the ultrathin wire decreased with increasing annealing temperature (see Supporting Information, Figure S6). Moreover, some self-assisted InAs nanowires with diameters over 50 nm appeared among the ultrathin InAs nanowires. A further increase in the annealing temperature to 750 °C leads to the disappearance of the ultrathin InAs nanowires, but a very high density of self-assisted InAs nanowires grew on the substrate. The decrease in the ultrathin InAs nanowire density at higher annealing temperatures is attributed to the vaporization of Ag nanoparticles. Although the melting and evaporation temperatures of bulk Ag are much higher than the annealing temperatures investigated, the melting and evaporation temperatures of Ag particles at nanoscale dimensions dramatically decrease with their size.[42,43] This phenomenon is also observed in Au-activated InAs nanowires.[15] From the above results, to obtain ultrathin InAs nanowires with a high density and over large scale, the optimum condition for the thickness of Ag film and annealing temperature are 2 nm and 650 °C, respectively (the SEM image for the larger scale ultrathin nanowires grown under this condition is shown in Supporting Information, Figure S7). We also found that some "bulk" material (i.e., InAs crystallites forming a discontinuous layer) is present on the substrate which is often observed in MBE InAs nanowire growth[19,44] and could be eliminated by further optimizing the growth parameters.

Self-assisted InAs nanowires show high density of stacking faults and twin defects as revealed in the TEM images (see Supporting Information, Figure S8), while for the ultrathin InAs nanowires, TEM micrographs once again demonstrate the high crystalline quality. The HRTEM images taken from the bottom, middle, and top of a typical ultrathin nanowire are presented in Figure 5b−d, respectively. Clearly, the nanowire is completely free of stacking faults and twin planes. The pure WZ crystal structure is confirmed by fast Fourier transform of the TEM image taken from the bottom of the nanowire (see inset of Figure 5b). Unlike the gold-catalyzed GaAs and InAs nanowires,[26,40] a change from WZ to ZB stacking was not observed at the tips of our InAs nanowires near the Ag droplets. Detailed TEM observation of a dozen such nanowires all revealed a perfect WZ crystal structure, free of stacking faults. Furthermore, almost all the ultrathin InAs nanowires showed a high aspect ratio (over 200) with uniform diameters along the growth direction.

Finally, we assess the electronic properties of the phase-pure ultrathin InAs nanowires. The inset in Figure 6b shows a top-view SEM image of an FET fabricated from a single ultrathin InAs nanowire. The gate length of this device, $L_G \approx 400$ nm, is determined by the separation between the source−drain contacts. Figure 6a and b show the output and transfer characteristics of the back-gated FET. The transistor functions as an n-type enhancement-mode MOSFET with a threshold voltage ($V_T$) of +1.84 V. A positive $V_T$, is extracted by a linear extrapolation from the maximum transconductance. In many applications, enhancement-mode devices are preferable to the depletion-mode counterparts because the power consumption is lower. Many previously reported InAs nanowire devices have negative threshold voltages. The positive threshold voltage in our devices is probably due to the small diameter of the nanowires, the lack of n-impurity doping in the nanowires, and the strong confinement effects of the surrounding dielectric/oxide layers. The on-state resistance of the device shown in Figure 6 is 3.9 Ω·mm, which is about 7 times larger than the typical value for modern HEMTs, where $R_{ON}$ = 0.5 Ω·mm.[45] The low on-state current could be attributed to two factors: (1) The surface scattering in the ultrathin nanowires is more severe than that in thicker nanowires;[46] (2) The present MBE-grown nanowires have very high purity in which carrier concentration might be lower than that in InAs nanowires fabricated by other methods. The $I_{ON}/I_{OFF}$ ratio, for $V_{DS}$ = 0.1 V, is almost $10^6$, which is much larger than that of previously reported lateral


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InAs nanowire FETs[47] and comparable to the highest value of InAs nanowire FETs demonstrated in a vertical surrounding-gate device.[48] We have fabricated and measured more than 30 FETs, and 90% of them show an $I_{ON}/I_{OFF}$ ratio around $10^6$. Figure S9a in the Supporting Information shows a transfer curve measured from another FET in the same batch of devices as that shown in Figure 6. Figure S9b shows the statistics for $I_{ON}/I_{OFF}$ ratio of the 30 back-gated devices based on nanowires with diameter 9 ± 2 nm. We believe that this high $I_{ON}/I_{OFF}$ ratio is likely due to the larger bandgap in thinner nanowires caused by quantum effects.[46,49,50]

In conclusion, we have realized controlled fabrication of defect-free InAs nanowires on Si (111) substrates by diminishing the diameter down to 10 nm. Combining a novel two-step catalyst annealing process with MBE growth, large scale production of InAs nanowires with an average diameter of 10 nm were realized. These ultrathin InAs nanowires have a pure WZ crystal structure, free of stacking faults and twin defects. Using individual ultrathin InAs nanowires as the channel material, we produced MOSFETs with $I_{ON}/I_{OFF}$ ratio as high as $\sim 10^6$. The ability to prepare pure WZ ultrathin InAs nanowires on Si substrates may provide new opportunities for studying their size-dependent physical properties and exploring potential nanodevice applications.

## ■ ASSOCIATED CONTENT

### Supporting Information

Typical growth temperature and V/III flux ratio dependence of InAs nanowire morphology, Ag deposition thickness dependence of InAs nanowire growth, post-growth EDX measurements of the seed particles and nanowires, TEM images of a non-[111] growth direction InAs nanowire, representative HRTEM images of ultrathin nanowires with different diameters, SEM images of Ag-catalyzed InAs nanowires, TEM images of self-assisted InAs nanowires, and electrical properties of ultrathin InAs nanowires. This material is available free of charge via the Internet at http://pubs.acs.org.

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### Notes

The authors declare no competing financial interest.

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## ■ REFERENCES

(1) Duan, X. F.; Huang, Y.; Agarwal, R.; Lieber, C. M. *Nature* **2003**, *421*, 241−245.
(2) Yan, R.; Gargas, D.; Yang, P. *Nat. Photonics* **2009**, *3*, 569−576.
(3) Lieber, C. M. *MRS Bull.* **2003**, *28*, 486−491.
(4) Wallentin, J.; Anttu, N.; Asoli, D.; Huffman, M.; Åberg, I.; Magnusson, M.; Siefer, G.; Kailuweit, P.; Dimrot, F.; Witzigmann, B.; Xu, H. Q.; Samuelson, L.; Deppert, K.; Borgström, M. *Science* **2013**, *339*, 1057−1060.
(5) Yu, X. Z.; Wang, H. L.; Pan, D.; Zhao, J. H.; Misuraca, J.; von Molnár, S.; Xiong, P. *Nano Lett.* **2013**, *13*, 1572−1577.
(6) Cui, Y.; Wei, Q.; Park, H.; Lieber, C. M. *Science* **2001**, *293*, 1289−1292.
(7) Thelander, C.; Mårtensson, T.; Björk, M. T.; Ohlsson, B. J.; Larsson, M. W.; Wallenberg, L. R.; Samuelson, L. *Appl. Phys. Lett.* **2003**, *83*, 2052−2054.
(8) Björk, M. T.; Ohlsson, B. J.; Thelander, C.; Persson, A. I.; Deppert, K.; Wallenberg, L. R.; Samuelson, L. *Appl. Phys. Lett.* **2002**, *81*, 4458−4460.
(9) Chuang, S.; Gao, Q.; Kapadia, R.; Ford, A. C.; Guo, J.; Javey, A. *Nano Lett.* **2013**, *13*, 555−558.
(10) Mandl, B.; StangI, J.; Mårtensson, T.; Mikkelsen, A.; Eriksson, J.; Karlsson, L.; Bauer, G.; Samuelson, L.; Seifert, W. *Nano Lett.* **2006**, *6*, 1817−1821.
(11) Dick, K. A.; Deppert, K.; Mårtensson, T.; Mandl, B.; Samuelson, L.; Seifert, W. *Nano Lett.* **2005**, *5*, 761−764.
(12) Heun, S.; Radha, B.; Ercolani, D.; Kulkarni, G. U.; Rossi, F.; Grillo, V.; Salviati, G.; Beltram, F.; Sorba, L. *Cryst. Growth Des.* **2010**, *10*, 4197−4220.
(13) Hong, Y. J.; Lee, W. H.; Wu, Y. P.; Ruoff, R. S.; Fukui, T. *Nano Lett.* **2012**, *12*, 1431−1436.
(14) Dayeh, S. A.; Aplin, D. P. R.; Zhou, X.; Yu, P. K. L.; Yu, E. T.; Wang, D. L. *Small* **2007**, *3*, 326−332.
(15) Ihn, S. G.; Song, G. I. *Nanotechnology* **2007**, *18*, 355603−355606.
(16) Tomioka, K.; Motohisa, J.; Hara, S.; Fukui, T. *Nano Lett.* **2008**, *8*, 3475−3480.
(17) Wei, W.; Bao, X. Y.; Soci, C.; Ding, Y.; Wang, Z. L.; Wang, D. L. *Nano Lett.* **2009**, *9*, 2926−2934.
(18) Hertenberger, S.; Rudolph, D.; Bolte, S.; Döblinger, M.; Bichler, M.; Spirkoska, D.; Finley, J. J.; Abstreiter, G.; Koblmüller, G. *Appl. Phys. Lett.* **2011**, *98*, 123114−123116.
(19) Dimakis, E.; Lähnemann, J.; Jahn, U.; Breuer, S.; Hilse, M.; Geelhaar, L.; Riechert, H. *Cryst. Growth Des.* **2011**, *11*, 4001−4008.
(20) Ghalamestani, S. G.; Johansson, S.; Borg, B. M.; Dick, K. A.; Wernersson, L. E. *Phys. Status Solidi C* **2012**, *9*, 206−209.
(21) Schroer, M. D.; Petta, J. R. *Nano Lett.* **2010**, *10*, 1618−1622.
(22) Stiles, M. D.; Hamann, D. R. *Phys. Rev. B* **1990**, *41*, 5280−8282.
(23) Stiles, M. D.; Hamann, D. R. *Phys. Rev. B* **1988**, *38*, 2021−2037.
(24) Joyce, H. J.; Leung, J.; Gao, Q.; Tan, H. H.; Jagadish, C. *Nano Lett.* **2010**, *10*, 908−915.
(25) Caroff, P.; Dick, K. A.; Johansson, J.; Messing, M. E.; Deppert, K.; Samuelson, L. *Nat. Nanotech.* **2009**, *4*, 50−55.
(26) Dick, K. A.; Caroff, P.; Bolinsson, J.; Messing, M. E.; Johansson, J.; Deppert, K.; Wallenberg, L. R.; Samuelson, L. *Semiconductor Sci. Technol.* **2010**, *25*, 024009−024019.
(27) Dick, K. A.; Thelander, C.; Samuelson, L.; Caroff, P. *Nano Lett.* **2010**, *10*, 3494−3499.
(28) Dick, K. A.; Bolinsson, J.; Messing, M. E.; Lehmann, S.; Johansson, J.; Caroff, P. *J. Vac. Sci. Technol. B* **2011**, *29*, 04D103−04D110.
(29) Lehmann, S.; Wallentin, J.; Jacobsson, D.; Deppert, K.; Dick, K. A. *Nano Lett.* **2013**, *13*, 4099−4105.
(30) Xu, H. Y.; Wang, Y.; Guo, Y. N.; Liao, Z. M.; Gao, Q.; Tan, H. H.; Jagadish, C.; Zou, J. *Nano Lett.* **2012**, *12*, 5744−5749.
(31) Zhang, Z.; Lu, Z. Y.; Chen, P. P.; Xu, H. Y.; Guo, Y. N.; Liao, Z. M.; Shi, S. X.; Lu, W.; Zou, J. *Appl. Phys. Lett.* **2013**, *103*, 073109−073113.
(32) Akiyama, T.; Sano, K.; Nakamura, K.; Ito, T. *Jpn J. Appl. Phys.* **2006**, *45*, L275−L278.
(33) Shtrikman, H.; Biro, R. P.; Kretinin, A.; Houben, L.; Heiblum, M.; Bukała, M.; Galicka, M.; Buczko, R.; Kacman, P. *Nano Lett.* **2009**, *9*, 1506−1510.
(34) Wu, Y.; Cui, Y.; Huynh, L.; Barrelet, C. J.; Bell, D. C.; Lieber, C. M. *Nano Lett.* **2004**, *4*, 433−436.
(35) Iwai, H. *Solid-State Electron.* **2004**, *48*, 497−503.

(36) Vogel, A. T.; de Boor, J.; Becker, M.; Wittemann, J. V.; Mensah, S. L.; Werner, P.; Schmid, V. *Nanotechnology* **2011**, *22*, 015605−015610.
(37) Xu, H. Y.; Guo, Y. N.; Sun, W.; Liao, Z. M.; Burgess, T.; Lu, H. F.; Gao, Q.; Tan, H. H.; Jagadish, C.; Zou, J. *Nanoscale Res. Lett.* **2012**, *7*, 589−594.
(38) Dubrovskii, V. G.; Sibirev, N. V. *Phys. Rev. B* **2008**, *77*, 035414−035421.
(39) Johansson, J.; Dick, K. A.; Caroff, P.; Messing, M. E.; Bolinsson, J.; Deppert, K.; Samuelson, L. *J. Phys. Chem. C* **2010**, *114*, 3837−3842.
(40) Shtrikman, H.; Popovitz-Biro, R.; Kretinin, A.; Heiblum, M. *Nano Lett.* **2009**, *9*, 215−219.
(41) Thelander, C.; Caroff, P.; Plissard, S.; Dey, A. W.; Dick, K. A. *Nano Lett.* **2011**, *11*, 2424−2429.
(42) Wautelet, M. *J. Phys. D: Appl. Phys.* **1991**, *24*, 343−346.
(43) Asoro, M. A.; Kovar, D.; Ferreira, J. P. *ACS Nano* **2013**, *7*, 7844−7852.
(44) Tchernycheva, M.; Travers, L.; Patriarche, G.; Glas, F.; Harmand, J. C.; Cirlin, G. E.; Dubrovskii, V. G. *J. Appl. Phys.* **2007**, *102*, 094313−094320.
(45) Kim, D. H.; Alamo, J. *IEEE Electron Device Lett.* **2010**, *31*, 806−808.
(46) Ford, A. C.; Ho, J. C.; Chueh, Y. L.; Tseng, Y. C.; Fan, Z. Y.; Guo, J.; Bokor, J.; Javey, A. *Nano Lett.* **2009**, *9*, 360−365.
(47) Dey, A. W.; Thelander, C.; Lind, E.; Dick, K. A.; Borg, B. M.; Borgström, M.; Nilsson, P.; Wernersson, L. E. *IEEE Electron Device Lett.* **2012**, *33*, 791−793.
(48) Thelander, C.; Rehnstedt, C.; Fröberg, L. E.; Lind, E.; Mårtensson, T.; Caroff, P.; Löwgren, T.; Ohlsson, B. J.; Lehmann, S.; Wernersson, L. E. *IEEE Trans. Electron. Devices* **2008**, *55*, 3030−3036.
(49) Zhao, Y. J.; Candebat, D.; Delker, C.; Zi, Y. L.; Janes, D.; Appenzeller, J.; Yang, C. *Nano Lett.* **2012**, *12*, 5331−5336.
(50) Lind, E.; Persson, M. P.; Niquet, Y. M.; Wernersson, L. E. *IEEE Trans. Electron Devices* **2009**, *56*, 201−205.