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Seebeck Coefficient of Nanowires Interconnected into Large Area Networks

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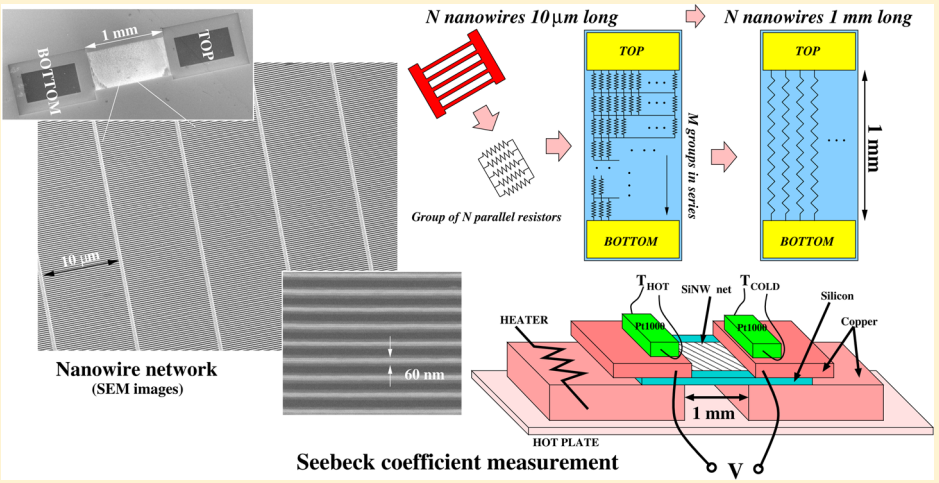

ABSTRACT: We measured the macroscopic Seebeck coefficient of silicon nanowires (SiNWs), organized in a highly interconnected networks on large areas (order of mm^2). The fabricated networks are very reliable with respect to random nanowire failure and are electrically and thermally equivalent to many SiNWs placed in parallel between the electrical contacts. The equivalent SiNWs have a macroscopic length of the order of millimeters and are very narrow (width smaller than 100 nm) so that they can be used to exploit thermoelectric properties at nanoscale for macroscopic electrical power generation and/or cooling. The measurement of the Seebeck coefficient S, facilitated by the macroscopic dimensions of the network, gives an insight into two questions, nanowire effective doping and carrier mobility, which are widely discussed in the literature. We found that the measured value of S is compatible with an effective doping that is higher than that of the original wafer. This higher doping is consistent with the value estimated from the measured electrical conductivity of the SiNWs with the assumption that the electron mobility inside the nanowire is equal to that of bulk silicon.

KEYWORDS: *Nanowires, thermoelectricity, Seebeck coefficient, carrier mobility*

Devices capable of direct conversion of heat into electrical power offer important opportunities for energy harvesting. For this reason, several research works focused on the development of materials with optimized thermoelectric properties[1,2] with the aim of increasing the conversion efficiency. In particular, the Seebeck coefficient S and the electrical conductivity σ must be both as high as possible, meanwhile the thermal conductivity k must be as small as possible so that the figure of merit $ZT = S^2\sigma/kT$ is increased and the efficiency of thermoelectric generators is high. In the research of materials for large scale application of thermoelectric generation, it is important to consider a trade-off between optimal thermal properties on one hand and technological aspects, material availability, cost, and sustainability on the other hand. In this respect, silicon could be an excellent material except for its high thermal conductivity (k = 148 W/mK), mainly due to phonon conduction. As it has been widely demonstrated, nanostructured materials, such as nanowires,[3−5] show a strong reduction of k due to surface scattering that reduces the phonon mean free path; k values as small as 1 W/mK for silicon have been found in rough nanowires.[6,7] This would offer a viable approach for the fabrication of silicon-based high-efficiency thermoelectric generator for energy harvesting that could exploit the large diffusion of advanced silicon technology and market. However, a single (or very few) nanowire(s) is (are) unsuitable for a significant production of energy due to obvious limitations in terms of maximum current. Furthermore, 100 nm wide nanowires can be fabricated with good reliability only with a reduced length, typically not exceeding 10−20 μm; consequently, there are noticeable problems for clamping the nanowire between the hot and

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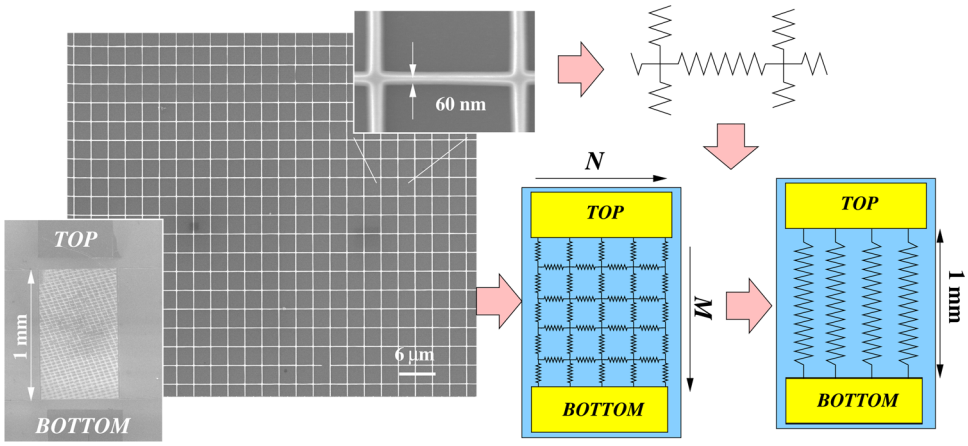

Figure 1. Composition of SEM images of interconnected nanowires, organized in a network. The overall network length is 1 mm, that is, the distance between the top and bottom contacts (see the SEM image in the bottom left inset). In the sketches, the electrical and/or thermal equivalent resistor network, made of $N \times M$ elementary resistors, is represented. The interconnected network behaves as many parallel silicon nanowires with a length of 1 mm.

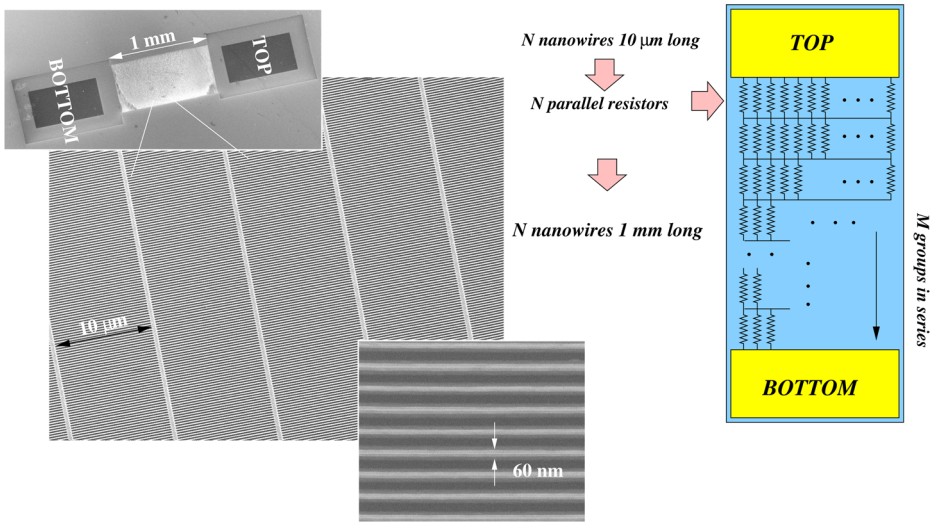

Figure 2. Composition of SEM images of a very dense nanowire network and its electrical/thermal equivalent net. The horizontal interconnections that increase the reliability of the network are ineffective both for the thermal and for the electrical behavior.

cold sources, which must be maintained at a suitable distance for good thermal insulation. For this reason, it is very important to develop solutions and techniques for the fabrication of nanostructures with macroscopic length. Recently, we proposed[8] top down fabrication of a large number of nanowires, each with a length in the micrometer range, organized in an interconnected network so that a macroscopic device of several millimeters can be obtained. The idea is that, at least in principle, the proposed macroscopic network continues to exhibit the interesting properties of the nanometric devices it is made of. In this work, we describe the results of measurements of both the Seebeck coefficient and electrical conductivity performed on nanowire networks. Note that the Seebeck coefficient measurement, performed with a purposely build apparatus, is considerably facilitated by the macroscopic dimensions of the samples. The consistency between the Seebeck coefficient and conductivity measurements is suggested by the fact that effective doping values estimated from both measurements are in good agreement. Interestingly, these estimates turned out to be much higher than the doping of the original silicon layer prior to nanowire fabrication. In order to confirm the actual potential of the proposed nanostructured material for thermoelectric generators, we have estimated the figure of merit of the network from previous thermal conductivity studies performed on single nanowires.

Nets of Top-down Silicon Nanowires. As it has been demonstrated in a previous work,[8] top down fabricated silicon nanowire networks are very reliable with respect to nanowire failure (breaking). In Figure 1, scanning electron microscopy (SEM) images of SiNW networks are shown. The main photo shows a net formed by nanowires, each with a length L_e ($L_{elementary}$) of 3 μm and diameter (width W_e) of 60 nm. The net has an overall area of $L \times W = 1 \times 0.6$ mm squares, and it is placed between a top and bottom aluminum contacts, both visible in the bottom left inset. A detail of a single nanowire composing the net ("elementary" nanowire) is shown in the SEM image of the top right inset; the nanowire is 60 nm wide and 3 μm long. Electrical conduction through the nanowire, as well as thermal conduction, can be represented by an elementary resistor. From the electrical point of view, let us indicate with R_0 the resistance of a single nanowire; if the

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nanowire is n-doped, $R_0 = (1/\sigma)(L_e/A)$, where σ is the electrical conductivity, $\sigma = q\mu_n n$ (q is the elementary charge, μ_n is the electron mobility in the nanowire and n is the electron concentration), and A is the nanowire cross section surface. As sketched in Figure 1, the overall nanowire net, made of $N \times M$ nanowires, can be represented with a $N \times M$ resistor network. In the case of an ideal network (no failures and homogeneous resistors) the horizontal branches are ineffective, and the vertical branches act as a long series of M elementary resistors. Similar considerations can be made for the thermal conductivity. In this way, the overall net is thermally and electrically equivalent to N parallel nanowires, each $M \times L_e$ long, that is, M times longer than each elementary nanowire; the length of the N parallel nanowires practically coincides with the top-to-bottom contact distance. The failure (breaking) of a nanowire can be schematized by removing the resistor from the net. The reliability of the network is very high due to the presence of both vertical and horizontal branches. Note that the latter actually affect the overall resistance of the network in the case of asymmetry due to failures and nonhomogeneous resistance distribution. As previously reported,[8] the network is very robust also with respect to nanowire width dispersion; the standard deviation of the top-to-bottom network resistance is within a few percent even if the standard deviation of elementary nanowire width W_e is over 50%.

Figure 2 shows SEM images of an improved SiNW network, based on a similar approach but with a different geometry that allows to achieve an higher nanowire density. In this way, the maximum current density (per unit of transversal width) is increased and consequently the required silicon area for a given current is reduced. Nanowires have an average width W_e of 60 nm, a pitch of 250 nm (see the SEM image of the bottom right inset) and a length L_e of 10 μm. The horizontal branches are very short (250 nm) and large (400 nm), if compared with SiNWs, so that their electrical and thermal resistances are negligible with respect to the nanowire ones. Therefore, they can be approximated by short circuits, as shown in the sketch on the right. Furthermore, horizontal branches have a very low probability of failure; in more than 10 fabricated samples, we have never detected a broken horizontal branch during SEM inspection.

The network is practically formed of a series of M groups, each made of the parallel of N nanowires, assuming that horizontal branches are short circuits. Let us indicate the probability of failure of a single nanowire with p; therefore, $(1 - p)$ is the probability that the SiNW is not broken. For very large values of N, the conductance of a group of N parallel silicon nanowires can be assumed to be equal to $N\,G_0(1 - p)$, where $G_0 = 1/R_0$. The resistance R of the overall network, made of M group in series is

$$R = \left[\frac{NG_0(1-p)}{M}\right]^{-1} = \frac{MR_0}{N(1-p)} \qquad (1)$$

The curves shown in Figure 3 represent the total top-to-bottom resistance of nets as a function of the SiNW probability of failure p. These curves have been obtained by simple Monte Carlo simulations: a random number r with uniform distribution in the interval [0,1] has been generated for each resistor, and the resistor has been removed from the net if $r < p$. For each random network obtained in this way, the overall top-to-bottom resistance has been calculated with standard circuit analysis. For each p, the procedure has been repeated 1000 times and the average value of the top-to-bottom resistance has been calculated. Note that the deviation with respect to the value for $p = 0$ can be considered as a measure of the network reliability. Curve **A** is relative to a net of nominally equal nanowires (uniform horizontal and vertical branches). The reliability is very good; the top-to-bottom resistance only doubles for a nanowire breaking probability of more than 20%, and it increases only of an order of magnitude for a nanowire breaking probability greater than 40% (almost a nanowire each two is broken). The average top-to-bottom resistance of the structure based on M series of groups ($M = 100$), each made up of N parallel nanowires (Figure 2), is shown by curves **B** (for $N = 10$), **C** (for $N = 100$), and **D** (for $N = 1000$). A further reliability improvement can be observed for this type of networks; as it can be reasonably expected, the reliability increases with N. For $N > 100$, the network resistance practically coincides with the ideal expression 1. In this case, the top-to-bottom resistance is within an order of magnitude of the nominal network resistance (no failures) even for breaking probabilities higher than 80%. For comparison, we have also reported the curve marked by **NH** (**N**o **H**orizontal interconnections), that shows the resistance as a function of the elementary nanowire breaking probability p for a net without horizontal interconnections. This net represents N parallel nanowires, each with a total length ML_e that can be decomposed into the series of M elementary nanowires. As expected, the top-to-bottom connection is interrupted even at very low values of p. This confirms that both configurations with horizontal branches show strong greater tolerance robustness to nanowire failure than millimeters long nanowires. In particular, the solution based on the M series of groups of N parallel nanowires is very robust, and furthermore a considerably low number N of parallel nanowires (100) is sufficient for good and reliable performances. So far, we have neglected the failure probability of horizontal branches. In order to provide a first order estimation for this probability, we

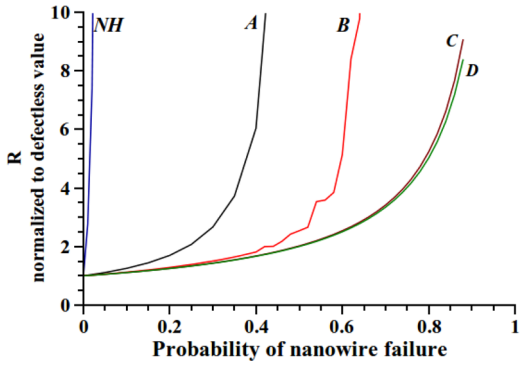

Figure 3. Top-to-bottom resistances R of resistor networks are reported as a function of nanowire failure probability (Monte Carlo simulations). The resistance values are normalized with respect to the ideal, defect-free (no nanowire breaking) network. **NH** shows R for a network without horizontal interconnection, that is, made of parallel nanowires 1 mm long. **A**: net of equal resistors, that represents a SiNW network as the one in Figure 1. **B** ($N = 10$), **C** ($N = 100$), **D** ($N = 1000$): nets made of the series of M groups, each made of of N parallel nanowires (resistors), that schematize SiNW networks as the one in Figure 2. With the increasing of N, the robustness with respect to nanowire failure increases. For N sufficiently high (greater than 100), the top-to-bottom resistance is within an order of magnitude of the nominal (defectless network) resistance, even for breaking probabilities higher than 80%.

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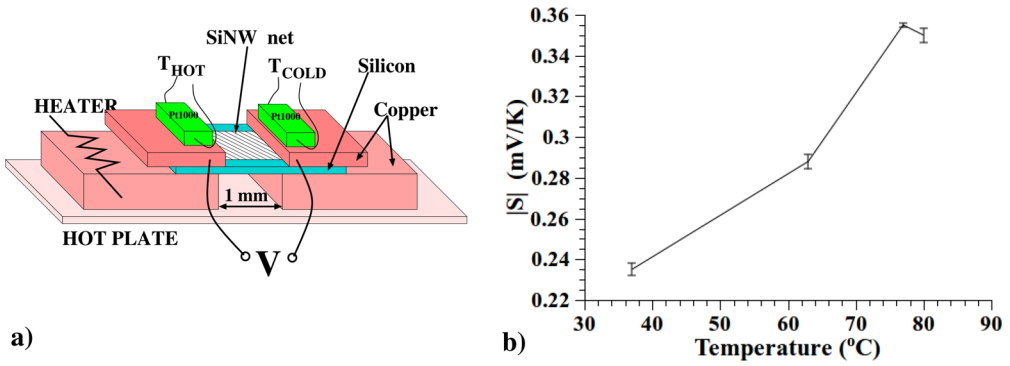

Figure 4. On the left (a) a sketch of the measurement apparatus for the Seebeck coefficient S is shown. On the right (b), the graph shows the measured Seebeck coefficient $S = \Delta V/\Delta T$ for different temperatures.

can consider an horizontal branch as the parallel of N_P nanowires, each one as wide as the vertical ones. Clearly, $N_P = W_{horizontal}/W_e$, where $W_{horizontal} = 400$ nm and $W_e = 60$ nm are the horizontal and vertical nanowire widths, respectively. Failure of an horizontal connection requires that all the N_P nanowires that form it are broken. In addition, if we neglect the case of multiple defects on the same wire, the probability failure of a single wire is proportional to its length. By these assumptions, the failure probability of an horizontal wire p_H is given by $p_H = p^{N_P} L_{horizontal}/L_e$, where $L_{horizontal} = 0.25$ μm and $L_e = 10$ μm are respectively the horizontal and vertical wire lengths. The result is that $p_H \ll p$, in agreement with the visual inspection of the fabricated samples.

Silicon Nanowire Net Fabrication and Measurement. We have fabricated the SiNW networks adapting and improving a top-down process already employed for the fabrication of devices based on a single SiNW.[9,10] We enhance this process for the simultaneous fabrication of a high number of nanostructures, with high density over large areas: the key point has been the development of the electron beam lithography step and, in particular, the correct calibration of the exposure dose. The details of the process have been described in our previous works.[9,10] In summary, the process is based on a Silicon On Insulator (SOI) wafer, with a 260 nm thick top silicon layer. A 50 nm thick silicon dioxide layer has been grown by means of thermal oxidation and patterned with electron beam lithography, followed by buffered HF (BHF) etching. The pattern has then been transferred to the top silicon layer with anisotropic (KOH) wet etching. The KOH etch defines nanowires with trapezoidal cross section that is suitable for a well controlled reduction by thermal oxidation. The mechanical stress, generated during the oxidation growth, limits the oxidation reaction rate making the process reliable and reproducible. The final cross section of the nanowire silicon core is triangular, as confirmed by SEM inspection. With this stress-controlled oxidation technique, very small widths can be obtained even starting from nanowires with an initial width greater than 100 nm, so that electron beam lithography is not mandatory; advanced optical lithography can be used in alternative. For this reason, the proposed SiNW networks are suitable, at least in principle, to be incorporated into microelectronic integrated circuits in order to provide on-chip thermoelectric power generation, temperature sensing or Peltier effect coolers.

Thermoelectric properties, and in particular the Seebeck coefficient, are strongly dependent on the material doping. Therefore, for the purpose of the present work, particular care has been dedicated to adjust the doping concentration of the top silicon layer, originally n-doped 10^{20} m^{-3}. We used a doping process based on phosphorus diffusion from solid ceramic source (FILMTRONICS), already employed for the selective doping of a silicon nanowire.[11] Before starting the silicon nanowire fabrication (lithography, etching, and oxidation), we cleaned the wafer by BHF, placed it onto the phosphorus-type ceramic source and performed a rapid thermal annealing at 800 °C for 10 min in N_2 atmosphere (predeposition). Once cooled down, we removed the ceramic source and performed another thermal treatment (drive-in) at 1150 °C for 10 min. For the first minute, an O_2 atmosphere has been used, so that the dopant species remain capped by a thin top SiO_2 layer; an N_2 atmosphere has been used for the remaining 9 min. As we found by numerical simulations, performed by Synopsys TCAD, the high-temperature drive-in step makes the top silicon layer uniformly n-doped in the whole thickness. We characterized the solid source doping process by means of a standard Hall technique. Predeposition time and temperature have been optimized so that the top silicon layer resulted n-doped 10^{23} m^{-3}. In order to confirm the doping uniformity, we etched the top silicon layer of test samples (after doping) with steps of 20 nm down to a remaining thickness of 100 nm, and we repeated the Hall measurement for each etch step: the same doping concentration $n = 10^{23}$ m^{-3} has always been measured.

We measured both the Seebeck coefficient $S = \Delta V/\Delta T$ and the overall resistance of the fabricated nanowire nets. From the total resistance, a value for SiNW electrical conductivity has been evaluated. This value resulted to be comparable to the ones previously obtained by means of four contact electrical measurements of single silicon nanowire devices, fabricated with the same process.[9,10] All the measured nets were 1 mm long (top-to-bottom distance). This macroscopic length allowed mechanical clamping of the nanowires between an "hot" and a "cold" source. Figure 4a shows a sketch of the experimental apparatus, where it is shown that the extremities of the nanowire net are clamped in an "hot" and "cold" heat sink made of a material (copper) with low thermal resistance. Temperatures at the net extremities are measured by means of two Pt 1000 resistors (temperature sensors), through high precision multimeters. The system is placed on a hot plate (70 W maximum) that heats uniformly the two sinks, meanwhile a smaller 5 W heater has been applied to the "hot" part, so that a temperature drop ΔT in the range 3−5 °C can be maintained between the extremities of the nanowire. The voltage difference ΔV is measured by means of a nanovoltmeter through metal (copper) connections applied to the top and bottom contacts.

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The measured Seebeck coefficient $S = \Delta V/\Delta T$ is negative, that is, the positive extremity is the "hot" one, in agreement with the fact the SiNWs are *n*-doped. The Seebeck coefficient of the metal used for the connections is of the order of few μV/K, and it has been neglected in these experiments. The graph of Figure 4b shows the absolute value of *S*, as a function of temperature, for a typical nanowire net formed by $N \times M = 190 \times 290$ nanowires 3 μm long. The measured Seebeck value is 0.24 mV/K at room temperature. This value is quite low if compared with the *S* value of *n*-doped bulk silicon 10^{23} m^{-3}, that is about 1 mV/K.[12] The value of $S = 0.24$ mV/K corresponds to a doping of 3×10^{25} m^{-3}.

This doping value can be compared with the electrical conductivity σ of the elementary SiNWs that compose the net. All the investigated samples (more than 10 nets of both types) showed a resistance value considerably lower than the expected one, that should be obtained given the original doping of the top silicon layer ($n = 10^{23}$ m^{-3}). The top-to-bottom net resistance *R* has been measured by recording *I*−*V* characteristics in the range (−5 to +5) V; the conduction resulted always in linear (ohmic) regime. As an example, Figure 5 shows the *I*−*V* characteristic of the typical SiNW net whose data for *S* have been shown in Figure 4, and the resistance is $R = 64$ kΩ. *R* can be used to determine the average resistance value R_0 of each elementary nanowire, knowing the percentage of failure *p*. Therefore, from R_0 the electrical conductivity σ can be determined knowing the geometrical parameter (elementary length L_e and width W_e) of the nanowire. We used SEM inspection to give an estimation of both *p* and average nanowire width W_e. We have chosen at least five selected zones on the same sample, each containing roughly 50 nanowires, and we counted the number of broken wires. In this way, a percentage of failure of roughly 10% has been estimated. During the same SEM inspection, we measured the nanowire width W_e for 5−8 nanowires in each zone and determined an average nanowire width of 70 nm. As pointed out in our previous work,[8] the overall resistance of the net is very robust with respect to nanowire width dispersion, so that the average width $W = 70$ nm can be used for the evaluation of σ; the average cross section area *A* can be evaluated as $A = W_e \times W_e\sqrt{2}/4$ because at the end of the reduction (by oxidation) the nanowire silicon core is triangular with the base width W_e and the height $W_e\sqrt{2}/2$ due to the anisotropic etching. Accordingly to graph *A* of Figure 3, a percentage of failure of 10% gives a top-to-bottom resistance value that is roughly 1.3 times higher than the nominal value $R = (290)/(190)R_0$ that would have been measured without nanowire failures. Thus, the resistance R_0 of an elementary nanowire is $R_0 = 32$ kΩ. From this data, we can estimate that the electrical conductivity inside our nanowires is $\sigma = 54128\ \Omega^{-1}\text{m}^{-1}$. Several experimental works[3,4] demonstrated that the thermal conductivity is reduced in nanowires narrower than 100 nm. Surface scattering strongly affects the phonon conductivity[6,7] because it reduces the phonon mean free path that is of the order of several tens of nanometers at room temperature. In particular, both Hochbaum et al.[6] and Boukay et al.[3] obtained thermal conductivities of the order of 1 W/mK. Using this value, a figure of merit ZT of about 0.9 at room temperature can be envisioned for our nanowire networks. Let us consider now the electron concentration and mobility in our nanowires. The product $\mu_n n = \sigma/q$ is 3.4×10^{23} V^{-1} s^{-1} m^{-1}. It must be pointed out that this is an average value on the nanowire cross section. In fact, thermal treatment during nanowire fabrication (such as oxidation) can generate a redistribution of the doping, and local modifications of the mobility. The electron mobility in a nanowire is still an open problem for nanowires narrower than 10 nm, when quantum effects begins to become important even at room temperature.[13,14] In our case, $W > 50$ nm so that at room temperatures we can exclude important quantum effect; modification of electron mobility can also derive from the surface scattering. Several works measured the SiNW electron mobility by different techniques.[15−18] Differently from the phonon behavior, the electron mobility in heavily doped, few tens of nanometer wide, nanowires is only weakly affected by surface scattering, as demonstrated by theoretical analysis.[19,20] The high doping level increases the impurity scattering, reducing the electron mean free path to few nanometers (2−5 nm, depending on doping). Therefore, electron scattering due to surfaces plays its effect only within few nanometers (that is, a distance comparable with the bulk mean free path) close to the surfaces.[21] For this reason, for a first order estimation of electron concentration *n* to be compared with the one obtained by the *S* value, we can assume here that the mobility is not very different from the one of *n*-doped bulk silicon. The empirical relationship between mobility and doping concentration in bulk silicon is[22]

$$\mu_n = 65 + \frac{1265}{1.0 + \left(\frac{n}{8.510^{22}}\right)^{0.72}} \qquad (2)$$

From relation 2 and from the experimental value of $\mu_n n = 3.4 \times 10^{23}$ V^{-1} s^{-1} m^{-1}, we find for the mobility $\mu_n = 0.0079$ m^2/(V s), and for the doping concentration $n = 4 \times 10^{25}$ m^{-3}. This high value of doping is consistent with that obtained from the measured value of the Seebeck coefficient *S* (*S* is weakly affected by μ_n[23,24]). The consistency between *S* and σ indicates that the nanowire is heavily *n*-doped, despite the initial moderated doping of the top silicon layer (10^{23} m^{-3}), and on the other hand it suggests that the hypothesis of considering the electron mobility in the nanowire equal to that of bulk silicon is correct. This would imply that in our nanowires the surface scattering has a negligible effect on the electrical conduction.

The reason of this final high-doping value of nanowires, obtained by an initial uniform doping of 10^{23} m^{-3}, can be ascribed to the surface segregation of doping species, occurring during the oxidation process used for the nanowire width reduction. It has been demonstrated[25,26] that during oxidation phosphorus segregates near the Si/SiO$_2$ interface, accumulating into the silicon side. This fact has been recently demonstrated

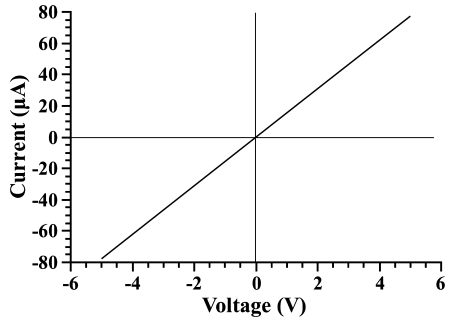

Figure 5. *I*−*V* characteristic of a typical SiNW network. The conduction is linear and, in this case, the top-to-bottom resistance is 64 kΩ.

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also at nanoscale, by experimental[27] and theoretical[28] investigation on silicon nanowires. However, segregation alone is not sufficient to justify the high value of nanowire doping (4×10^{25} m^{-3}), which is more than 2 orders of magnitude greater than the original doping of 10^{23} m^{-3}. Surface states, generated at the Si/SiO_2 interface during the oxide reduction process, and SiO_2 oxide charges, due to sodium impurities, could also provide an important contribution to the electron generation.

Conclusions. In this article, we demonstrate for the first time that it is possible to exploit the high equivalent length of a nanostructured interconnected network for a macroscopic measurement of the Seebeck coefficient *S* in nanowires. The demonstrated high reliability of the proposed networks even in presence of high nanowire failures, represents an important step toward practical employment of silicon based, regularly nanostructured materials.

Furthermore, we present an experimental evaluation of the SiNW effective doping, estimated both from the Seebeck coefficient measurement and from the nanowire electrical conductivity, showing that there is a substantial agreement between *S* and the unusually low values of the overall network resistance. This suggests that straightforward extrapolations of both the Seebeck coefficient and electrical conductivity of nanowires from the doping level of the original bulk silicon layer is not correct. In terms of practical applications in the field of thermoelectric power generation and/or sensing, much work has clearly to be done. A method to free the network from the highly conductive supporting substrate should be developed. This would also allow measurement of the macroscopic thermal conductivity of the networks, completing the set of physical parameters required to determine the actual thermoelectric efficiency of the proposed devices.

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Notes

The authors declare no competing financial interest.

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