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Electrical Properties of Self-Assembled Branched InAs Nanowire Junctions

Dmitry B. Suyatin,[†] Jie Sun,[†] Andreas Fuhrer,[†] Daniel Wallin,[†] Linus E. Fröberg,[†] Lisa S. Karlsson,[‡] Ivan Maximov,[†] L. Reine Wallenberg,[‡] Lars Samuelson,[†] and H. Q. Xu*,[†]

Division of Solid State Physics and The Nanometre Structure Consortium, Lund University, Box 118, S-221 00 Lund, Sweden, and Polymer & Materials Chemistry/ nCHREM, Lund University, Box 124, S-221 00 Lund, Sweden

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ABSTRACT

We investigate electrical properties of self-assembled branched InAs nanowires. The branched nanowires are catalytically grown using chemical beam epitaxy, and three-terminal nanoelectronic devices are fabricated from the branched nanowires using electron-beam lithography. We demonstrate that, in difference from conventional macroscopic junctions, the fabricated self-assembled nanowire junction devices exhibit tunable nonlinear electrical characteristics and a signature of ballistic electron transport. As an example of applications, we demonstrate that the self-assembled three-terminal nanowire junctions can be used to implement the functions of frequency mixing, multiplication, and phase-difference detection of input electrical signals at room temperature. Our results suggest a wide range of potential applications of branched semiconductor nanostructures in nanoelectronics.

Nanoelectronic elements made from self-assembled semiconductor nanowires are considered nowadays as one of the most promising alternatives to conventional electronic elements fabricated using lithography methods and techniques.[1–3] Recently, growth of branched nanowires has been demonstrated in different semiconductor material systems.[4–20] However, electrical properties of these self-assembled branched nanowires have rarely been studied.[11] Here we report on a study of the electrical properties of three-terminal junction devices made from self-assembled branched InAs nanowires. We show that the self-assembled nanoscale junctions exhibit tunable nonlinear electrical characteristics and a signature of ballistic electron transport. Thus, the branched nanowire junctions can provide a variety of applications in future nanoelectronics. As an example, we demonstrate in this work that the self-assembled three-terminal nanowire junctions can be used to implement the functions of frequency mixing, multiplication, and phase-difference detection in nanoelectronic circuits at room temperature.

The branched self-assembled nanowires were catalytically grown using chemical beam epitaxy (CBE) in two steps.[21,22] The first step was the growth of vertical InAs nanowire trunks. For this step of growth, gold seed particles with diameters of about 70 nm were produced with an aerosol method[23] and deposited on an InAs (111) B substrate with a deposition density of 0.5 particles/μm^2. The nanowire growth was carried out at 435 °C. Trimethylindium (TMIn) and tertiarybutylarsine (TBAs) were used as the growth sources. The source pressures in lines before the inlet valves during the growth were $p_{As} = 200$ Pa for TBAs and $p_{In} = 15$ Pa for TMIn. The lengths of the grown nanowire trunks were about 1.7 μm, and the diameters of the trunks, determined by the aerosol catalyst particle sizes, were found to be about 80 nm. After a second isotropic aerosol Au particle deposition, InAs nanowire branches were grown on the trunks. For this second growth step, aerosol particles with diameters of about 40 nm were deposited with a deposition density of 1 particle/μm^2 on the substrates with the grown trunks. Nanowire branches were grown on the trunks for 25 min under a similar condition as for the growth of the trunks. The grown nanowire branches had a diameter of about 55 nm, and typically they grew faster at the base section of the trunks than on the top. Figure 1a shows a transmission electron microscope (TEM) image of some typical InAs nanowire junctions grown for this work. Figure 1b shows a high-resolution TEM image of the junction region of a branched nanowire. The image indicates that the grown branched InAs nanowire junctions had a wurtzite crystalline structure with some occasions of thin cubic sections or stacking faults. The nanowire trunks were grown in the [000–1] direction, while the branches were grown perpendicularly to the trunks in ⟨1120⟩ directions.

After growth, branched nanowires were mechanically transferred onto the surface of a highly doped Si substrate

* Corresponding author. E-mail: Hongqi.Xu@ftf.lth.se.
† Solid State Physics.
‡ Polymer & Materials Chemistry/nCHREM.

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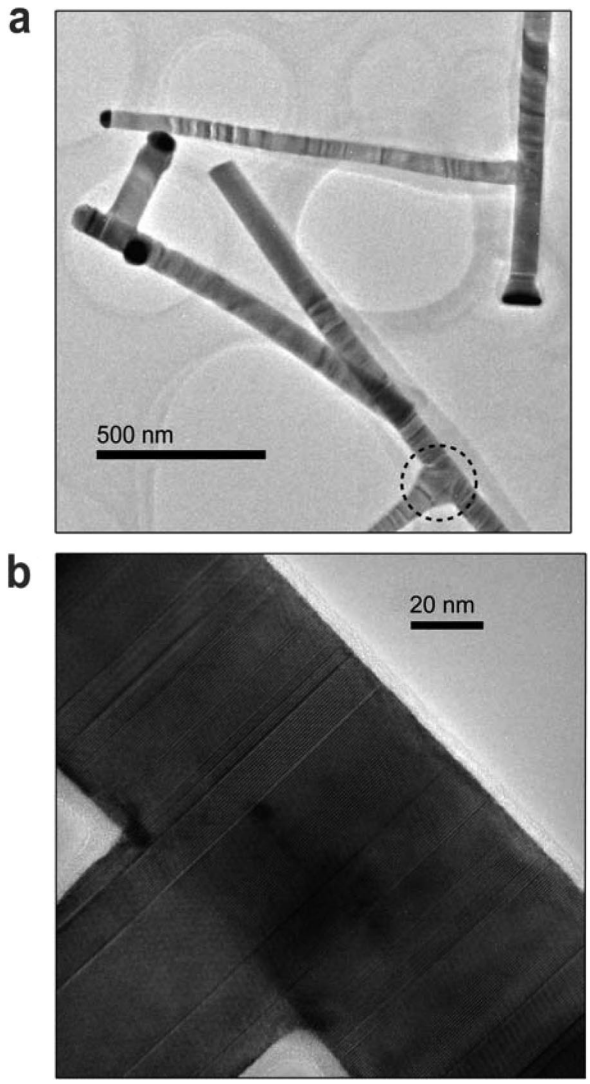

Figure 1. (a) Low- and (b) high-resolution TEM images of some InAs branched nanowires grown by CBE. The InAs branched nanowires had a wurtzite structure. The nanowire trunks were grown in the [000–1] direction, and the nanowire branches were grown perpendicularly to the trunks in ⟨1120⟩ directions. The diameters of the nanowire trunks and branches were controlled by the sizes of Au seed particles produced by an aerosol technique, and the nanowire trunks were thicker than the nanowire branches. In some cases, a broadening around the base of a nanowire branch was observed as can be seen in the region marked with a dashed circle in (a), and thin cubic sections or stacking faults occurred in the branched nanowires, as can be seen as straight stripe sections perpendicular to the trunk in (b).

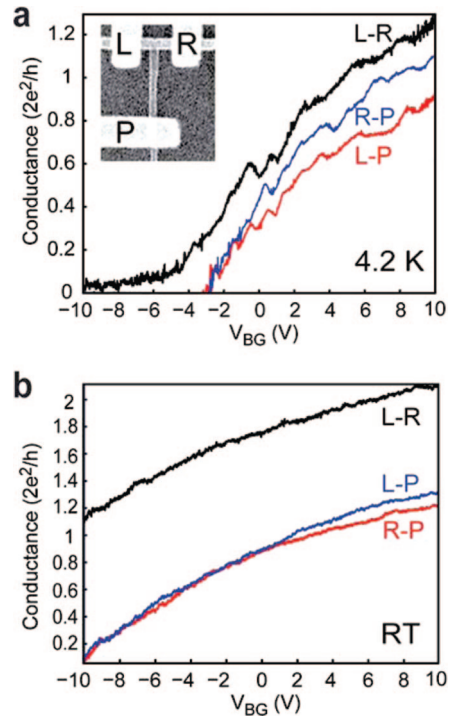

Figure 2. Measured conductances of a three-terminal InAs nanowire junction device. (a) Conductances measured between any two terminals of a nanowire junction device, with the third terminal left floating, as a function of V_{BG} at 4.2 K in the linear response regime. The inset shows an SEM image of the measured device. In the device, the nanowire junction had a trunk diameter of about 90 nm and a varying branch diameter of about 80 nm at the base side and about 70 nm at the contact side, and the separation between the left and right metal contacts to the trunk was about 240 nm. The device was slightly asymmetric with respect to the central branch; the distance between the center of the nanowire branch and the left contact was about 110 nm. (b) The same conductance measurements for the device but carried out at room temperature.

capped with a thermally grown 100 nm thick silicon dioxide layer. Electrical contacts (NiAu metal electrodes) to branched nanowires were fabricated by electron beam lithography (EBL), metal evaporation, and lift-off. Further details about the device fabrication can be found elsewhere.[24,25] Scanning electron microscope (SEM) images of some fabricated three-terminal nanowire junction devices are shown in the insets of Figures 2a and 3a. The fabricated nanowire junction devices were characterized by the conductance measurements between any two terminals in the linear response regime with the third terminal left floating. Figure 2 shows the results of the measurements for the device shown in the inset of Figure 2a as a function of voltage V_{BG} applied to the gate on the backside of the Si substrate. For these measurements, we used the lock-in technique at an excitation voltage of 100 μV (root mean square). The measured gate dependences of the conductances indicated that conduction carriers in the branched nanowire were n-type.

Functional, nonlinear electrical properties of the three-terminal nanowire junction devices were studied by measuring the voltage output at the branch terminal, V_P, as a function of voltages V_L and V_R applied to the left and right contacts of the nanowire trunk (cf. the inset in Figure 3a). In the following, we refer to measurements with antisymmetrically applied voltages, $V_L = -V_R$, as *push–pull* measurements and measurements where one contact to the trunk is kept grounded while sweeping of the voltage applied to the other contact as *push−fix* measurements. We find that the nanowire junction devices exhibit rich electrical characteristics. Parts a and b of Figure 3 depict the results of the push−fix and push–pull measurements at 4.2 K at different values of V_{BG} for the device shown in the inset of Figure 3a, respectively. In the push−fix measurements we find that for positive values of V_{BG} the curves show an up-bending behavior [see, e.g., the inset (+) of Figure 3a], and as V_{BG} is tuned toward

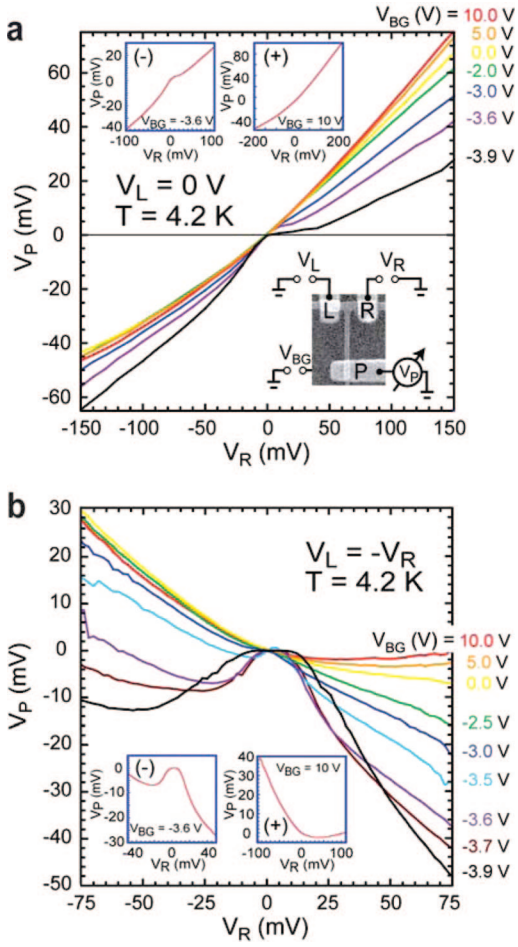

Figure 3. Low-temperature electrical properties of a three-terminal InAs nanowire junction device. (a) Measured voltage output V_P from the central branch terminal of a three-terminal InAs nanowire junction device as a function of the voltage V_R applied to the right terminal in the push−fix configuration (i.e., with $V_L = 0$) at different values of the voltage V_{BG} applied to the backside of the Si substrate at 4.2 K. The upper-left and upper-right insets highlight the results of the measurements at $V_{BG} = -3.6$ V and $V_{BG} = 10$ V, respectively. The lower inset shows an SEM image of the measured device and a schematic of the electrical circuit setup for the measurements. In this device, the nanowire trunk had a diameter of 90 nm, the nanowire branch had a diameter of 50 nm, the separation between the left and right metal contacts to the trunk was about 200 nm, and the distance between the center of the nanowire branch and the left metal contact was about 80 nm. (b) Measured voltage output V_P from the central branch of the device as a function of V_R applied to the right terminal in the push–pull configuration (i.e., with $V_L = -V_R$) at different values of V_{BG} at 4.2 K. The insets highlight the results of the measurements at $V_{BG} = -3.6$ V and $V_{BG} = 10$ V, respectively.

negative values a down-bending region develops around $V_R = 0$ mV [see, e.g., the inset (−) of Figure 3a]. Similarly, the push–pull measurements show a down-bending behavior around $V_R = V_L = 0$ mV in a large range of values of V_{BG} [see, e.g., the inset (−) of Figure 3b], while at sufficiently large positive values of V_{BG} the measured curves show an up-bending behavior [see, e.g., the inset (+) of Figure 3b]. Here we note that the asymmetry seen in the measured curves in Figure 3b is due to an inevitable structural asymmetry in the fabricated device.

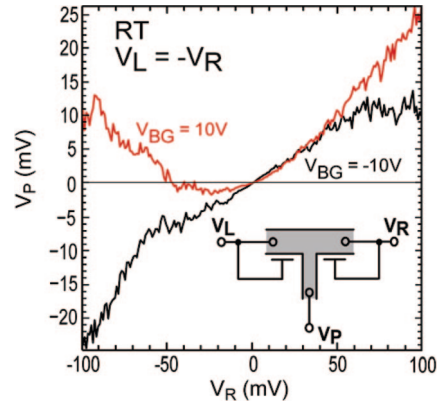

Figure 4. Electrical properties of a three-terminal InAs nanowire junction device at room temperature. Measured voltage output V_P from the central branch terminal of the InAs nanowire junction device as shown in the inset of Figure 2a as a function of the voltage V_R applied to the right terminal in the push–pull configuration (i.e., with $V_L = -V_R$) at the voltages of $V_{BG} = -10$ V and $V_{BG} = 10$ V applied to the backside of the Si substrate at room temperature. The inset is a schematic representation of an equivalent circuit for the self-gating effect observed in this work.

The rich gate-voltage-dependent electrical characteristics of the branched nanowire junction devices reflect tunable signatures of the carrier transport in three different regimes: (i) diffusive regime where the electron mean free path l_{mfp} is much smaller than the junction dimension l_{jcn} (the length between the source and drain contact pads on the trunk), i.e., $l_{mfp} \ll l_{jcn}$; (ii) ballistic regime where l_{mfp} is comparable to l_{jcn} or $l_{mfp} > l_{jcn}$; and (iii) a self-gating regime in which electric field emanating from the contact pads causes carrier depletion or accumulation in the nanowire regions close to the contacts (see the inset in Figure 4 for a schematic). In the fully diffusive regime the device can simply be modeled as a resistor network, and V_P depends linearly on V_L and V_R. In the ballistic regime of carrier transport,[26] we can expect a down-bending behavior in the measured curves of V_P (V_L,V_R) in both push–pull and push−fix configurations.[27–34] The curvature of the down-bending curves is larger for lower carrier density in the junction.[27–29] On the other hand, the self-gating effect (in the case of an n-type nanowire device) leads to a local resistance increase in the nanowire region close to a more negatively biased metal contact and a resistance decrease in the region close to a more positively biased contact. Thus, the probe voltage V_P shows an up-bending behavior in both the push–pull and the push−fix measurements.

At very negative back-gate voltages ($V_{BG} < -4$ V), the carriers in the nanowire branch were completely depleted; no reliable electrical measurements were possible. When the back-gate voltage was increased to be just above $V_{BG} = -4$ V, the electrical conduction in the nanowire junction became possible. However, at this rather low carrier density, the electrical properties of the device at small bias voltages of V_L and V_R were dominantly determined by diffusive transport (see, e.g., the middle flat section of the curve measured at $V_{BG} = -3.9$ V in Figure 3b and ref 35 for further discussion about the measured curve). As the voltage V_{BG} was further increased, the carrier density in the nanowire became high

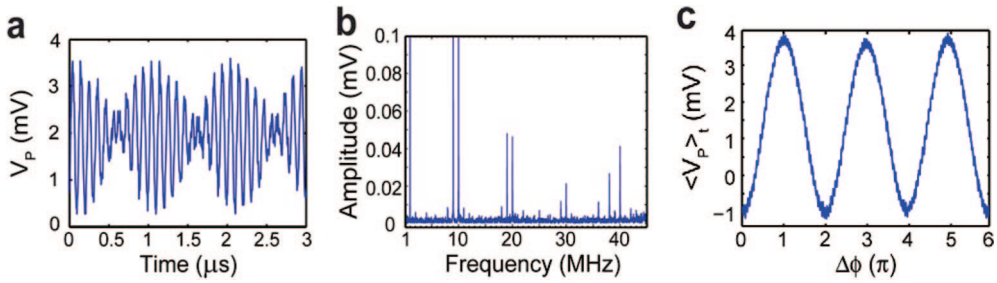

Figure 5. Measured frequency mixing and phase detection functionalities of a three-terminal InAs nanowire junction device at room temperature. Panels a and b show the results of frequency mixing measurements for the device shown in the inset of Figure 2a. The measured output voltages V_P from the central branch of the device are plotted in (a) time and (b) frequency domains for two sinusoidal input signals of the same amplitude (100 mV) but different frequencies (9 and 10 MHz) applied to the left and right terminals of the device. The measured signal strengths at 1, 9, and 10 MHz were about 0.14, 0.71, and 0.83 mV, respectively, and were truncated in (b). Panel c shows the results of phase detection measurements for the same device. In the measurements, two sinusoidal input signals of the same amplitude (100 mV) and frequency (1 MHz) were applied to the left and right terminals of the nanowire junction device, and the output voltage $\langle V_P \rangle_t$ from the central branch terminal, averaged with an integration time of 10 μs, was recorded as a function of the phase difference $\Delta\phi$ of the two input signals. In all the measurements for the results shown in this figure, a voltage of $V_{BG} = 10$ V was applied to the back gate.

enough to screen carrier scattering from impurities, defects, surface damages, etc. Thus, the carrier mean free path in the junction was increased, and the device showed the signature of ballistic transport in the small applied bias region (see the curves measured at -3.9 V $< V_{BG} < 0$ V in Figure 3). When the voltage V_{BG} became sufficiently high (see the curves measured at $V_{BG} > 0$ V in Figure 3), the measured V_P showed an up-bending behavior, indicating that the self-gating effect starts to play a dominant role in the determination of the electrical properties of the nanowire junction device. Here we would like to note that the nature of ballistic transport was still present in the device in this high back-gate voltage range. However, the effect, which would lead to a down-bending curve of V_P vs V_L and V_R, could not be directly seen in Figure 3 in this back-gate voltage range. This is because a higher back-gate voltage should give a larger carrier concentration and thus a smaller curvature in the ballistic down-bending curve.[27–29] Thus, the ballistic down-bending behavior was much weaker than the up-bending behavior arising from the self-gating effect in this high back-gate voltage range. As a consequence, one could only observe in Figure 3 an overall up-bending behavior in the measured curve of V_P vs V_L and V_R in this high back-gate voltage range.

In the region where large bias voltages of $|V_L - V_R|$ were applied between the left and right contacts of the nanowire junction, the ballistic nature of electron transport in the device was suppressed, and the electrical properties of the device were dominantly determined by diffusive electron transport and the self-gating effect (see the transitions from the down-bending behavior at low bias voltages to a linear behavior at high bias voltages or an overall up-bending behavior in Figure 3a,b). This occurs as a result of electron transfer into high-energy valleys by intervalley scattering in the nanowire junction. It is known that the electron transfer occurs at a threshold field of ~1.7 kV/cm in bulk InAs.[36] In our measured branched nanowire junction devices, the separation between the source and drain contacts to the trunk was about 200 nm. The electric field at $|V_R| = 40$ mV was then about 2 kV/cm in the junction region of the trunk for the push–pull measurements, and therefore the electron transfer to high-energy valleys could be expected at these conditions. However, it should be noted that the intervalley scattering does not block electrons from their forward motion completely. Thus, at sufficiently large bias voltages, it is possible to see a residual signature of ballistic electron transport.

Measurements at room temperature showed similar gate-dependent electrical characteristics (see Figure 4). However, the electron mean free path is known to be much shorter at room temperature due to electron–phonon scattering, which results in weaker ballistic effects and, hence, less pronounced down-bending behaviors.

The tunable nonlinear electrical characteristics of the three-terminal branched nanowire junctions can be put in use for the realization of functional devices.[30,31,37–41] Here we will demonstrate that the three-terminal nanowire junctions can be used for frequency mixing, frequency multiplication, and detection of phase difference between input signals. Generally, the measured voltage V_P can be expanded into a Taylor series: $V_P(V_L,V_R) = a_{00} + a_{10}V_L + a_{01}V_R + a_{20}V_L^2 + a_{11}V_LV_R + a_{02}V_R^2 + \ldots$. The nonlinear terms in the expansion imply that for inputs, $V_L = A_L \sin(2\pi f_L t)$ and $V_R = A_R \sin(2\pi f_R t + \Delta\phi_{LR})$, the nanowire junction can work as a frequency mixer and a frequency multiplier. Figure 5a,b shows the probe voltage V_P, measured at room temperature and $V_{BG} = 10$ V, in time and frequency domains when two sinusoidal signals with amplitudes $A_L = A_R = 100$ mV and frequencies $f_L = 9$ MHz and $f_R = 10$ MHz were applied as inputs. As expected, strong peaks in the power spectrum of V_P occurred at mixed frequencies of $f_R - f_L = 1$ MHz and $f_L + f_R = 19$ MHz. Peaks at the input frequencies and their multiple frequencies are also visible in the power spectrum shown in Figure 5b. The same nonlinear behavior can be used for determining the relative phase between two input periodic signals since, for two input signals with the same frequency $f_L = f_R$, the cross term V_LV_R contains information about the relative phase $\Delta\phi_{LR}$ between the two inputs. Assuming again that the two inputs were sinusoidal signals, the time-averaged voltage can be expressed as $\langle V_P \rangle_t = \text{const} + A_LA_R(a_{11}/2)\cos(\Delta\phi_{LR})$. Figure 5c shows the measured relation between $\langle V_P \rangle_t$ and

$\Delta\phi_{LR}$ at room temperature and $V_{BG} = 10$ V for two sinusoidal input signals with amplitudes $A_L = A_R = 100$ mV and frequencies $f_L = f_R = 1$ MHz. The results show that the nanowire junction can be used as a good phase-difference detector at megahertz or higher frequencies.

In summary, nanoscale three-terminal junction devices have been realized with self-assembled branched InAs nanowires and the electrical properties of the devices have been studied. It has been shown that these nanowire junction devices exhibit rich, tunable nonlinear electrical properties. These rich nonlinear properties arise from interplay of electron transport in diffusive, ballistic, and self-gating regimes. Our study should stimulate the efforts worldwide toward the realization of complex functional nanoelectronic devices and circuits with bottom-up approach.

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