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Toward Atomic-Scale Device Fabrication in Silicon Using Scanning Probe Microscopy

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ABSTRACT

We present a complete fabrication process for the creation of robust nano-and atomic-scale devices in silicon using a scanning tunneling microscope (STM). In particular we develop registration markers which, in combination with a custom-designed STM-scanning electron microscope (SEM) system, solve one of the key fabrication problems – connecting the STM-patterned buried phosphorus-doped devices, fabricated in the ultrahigh vacuum environment, to the outside world. The first devices demonstrate the feasibility of this technology and confirm the presence of quantum confinement in devices as electron propagation is laterally constricted by STM patterning.

It is well established that the scanning tunneling microscope cannot only image surfaces but can also be used to manipulate matter at the atomic scale as demonstrated by the seminal work of Eigler et al.[1] Since this time many researchers have become interested in using a STM to fabricate nano- and atomic-scale semiconductor devices,[2−5] where recent results have shown it is possible to pattern donors into silicon with atomic precision.[6] The key obstacle to making functional semiconductor devices with a STM is connecting leads to the device once it is removed from the ultrahigh vacuum (UHV) environment. Since the STM essentially creates an atomically perfect device, there is little contrast between the STM-patterned dopants and their environment, making the device invisible to optical and electron beam microscopes. As a consequence, it is necessary to register the device to some sort of feature or marker on the silicon surface that can be used to align macroscopic contacts from the outside world to the buried device to perform electrical measurements. The challenge is to develop registration markers that survive all the high temperature and UHV−STM fabrication steps, without contaminating the atomically flat surface required for STM imaging and lithography.

Over the past five years many groups have tried to connect to STM-patterned devices once they are removed from the ultrahigh vacuum environment using different techniques to either relocate a STM-patterned structure or prepattern the starting surface with metallic contacts. However, patterning of the surface requires the use of a resist. It is therefore necessary to completely remove any trace of the resist to avoid contamination of the surface before the high-temperature sample preparation step which is required to achieve atomic resolution. Whatever registration process is developed must therefore survive these cleaning and high-temperature steps before it is possible to pattern the device using the STM and connect to it ex-situ.[7−9] Some success has been achieved by making large-scale ohmic contacts in the silicon substrate before STM patterning using either dopant diffusion[10] or ion implantation of interdigitated contacts for the creation of an Aharonov-Bohm ring.[11] While these approaches circumvent the problem, they do not provide an absolute method of registration. In this paper we demonstrate a novel strategy for the realization of nano- and atomic-scale devices in silicon which uses a combination of etched registration markers (Figure 1a) and a custom designed STM-SEM/molecular beam epitaxy (MBE) system to overcome the registration problem. This strategy has several advantages: (i) by relocating and imaging the same area using the STM, each stage of the fabrication process can be inspected as the devices are made; (ii) it is possible to connect multiple voltage and current leads to each device, allowing full four-terminal electrical measurements; (iii) it is possible to register nanoscale surface electrodes to the active region of the buried device; (iv) we are able to produce many different devices on the same chip and contact them individually using conventional optical lithography; and (v)

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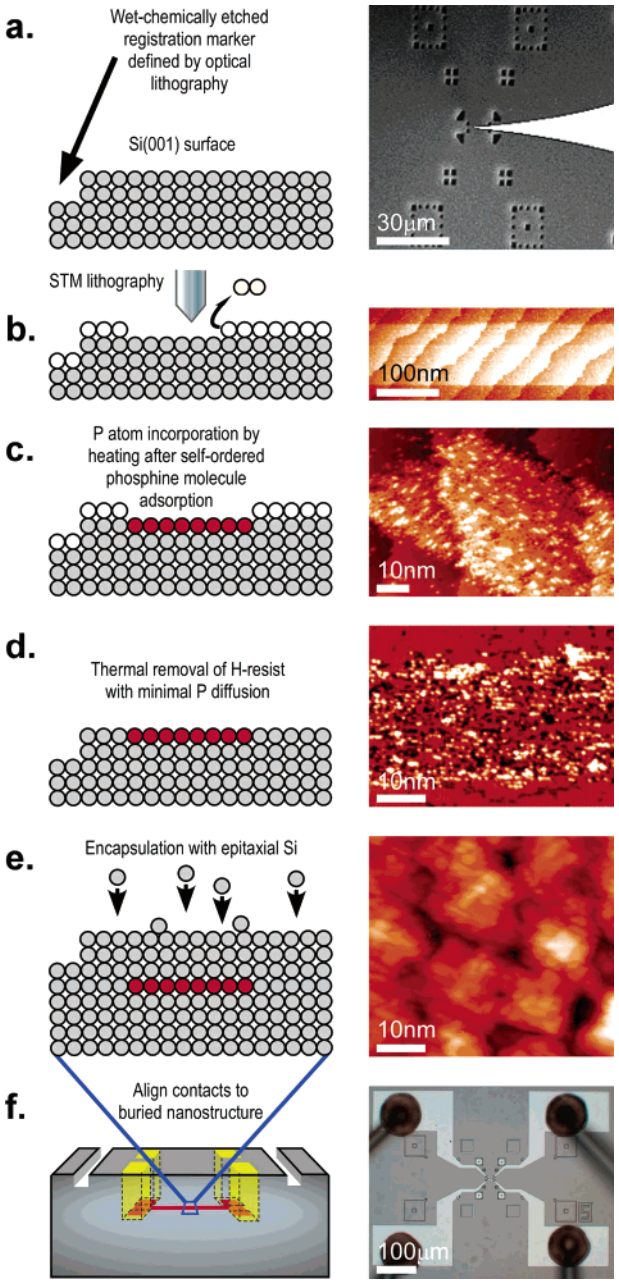

Figure 1. Novel device fabrication strategy for the creation of Si:P nanoscale devices using scanning probe microscopy. (Left) (a−e) Cross-sectional schematics of essential fabrication steps and (f) 3D sketch of final device. (Right) Corresponding (a) SEM image of STM tip (white) aligned to registration markers, (b) STM image of lithographically patterned wire, STM images of P incorporated wires, before (c) and after (d) hydrogen resist removal, and (e) 25 nm MBE Si overgrowth; concluded by an optical microscope image of the final device with contact wires (f).

this strategy allows multilevel STM patterning combined with MBE growth, giving atomic-scale resolution in all three spatial dimensions to form truly 3D atomic-scale devices.

To use etched registration markers and still achieve atomic resolution lithography we have custom-designed, in collaboration with Omicron Nanotechnology, a combined STM-SEM/MBE system that has several unique features. The STM chamber has a scanning electron microscope (SEM) to allow us to position the delicate STM tip a known distance from the registration markers. In addition, to ensure the STM-patterned samples are compatible with clean room processing (optical and/or electron beam lithography) the STM-SEM/MBE system has been designed to achieve atomic resolution on large 1×1 cm^2 silicon samples. Such large sample sizes make it difficult to use direct current heating to achieve atomic resolution imaging, and we therefore heat the backside of the sample using an electron beam to reconstruct the surface. We can precisely and reproducibly reposition the STM stage system with sub-100 nm accuracy using a laser interferometer so that it is possible to return to the same area of the sample after each processing step. Finally, extreme antivibration measures have been taken to decouple the STM chamber from the MBE system and its associated pumps.

The overall fabrication strategy is outlined in Figure 1, showing the key milestones in the creation of silicon based atomic-scale devices. Optimization of STM-based hydrogen lithography[12] (Figure 1b) at the atomic scale allows the selective adsorption of single phosphine (PH_3) molecules at specific sites on the silicon surface.[5] A critical anneal incorporates individual phosphorus dopant atoms (Figure 1c) from the PH_3 molecules into the silicon surface in the nanostructured region before thermal removal of the hydrogen resist (Figure 1d). Note that this incorporation process has been achieved with atomic precision.[6] We have also shown that a sheet of phosphorus atoms can be encapsulated using silicon MBE (Figure 1e) at low temperatures[13,14] minimizing the possibility of dopant diffusion and segregation out of the STM-patterned regions. Importantly, we have been able to achieve each of these process steps on large 1×1 cm^2 samples. However, it is the final and arguably most difficult step to connect the STM-patterned device to the outside world (Figure 1f); that is the key to the work reported here.

We have fabricated three devices on the same chip, each with four registered ohmic contacts: a 90×900 nm^2 quantum wire device (Figure 2a,d), an unpatterned control device (Figure 2b), and a 4×4 μm^2 phosphorus δ-doped square (Figure 2c). For all devices a set of registration markers of both square and triangular geometry are prepatterned into the silicon substrate using conventional dark-field mask optical lithography. The pattern is then transferred to an accuracy below ~50 nm into a 1×1 cm^2 Si(001) substrate using a tetramethylammonium hydroxide (TMAH) anisotropic wet chemical etch. Features are etched to a depth of ~300 nm and vary in size from 1×1 μm^2 for alignment of STM-patterned regions to 50×50 μm^2 for the alignment of ohmic contacts by optical lithography. Following etching, a thorough cleaning process is undertaken to remove the optical resist from the silicon surface. The sample is then loaded into the STM-SEM/MBE system and the silicon surface undergoes a high-temperature preparation step (approximately 1050 °C for 10 s using an electron beam heater) to desorb remaining adsorbants from the surface. This is the most severe process step that the registration markers have to survive. The heating step is necessary to achieve the highest possible surface quality for STM lithography on the atomic scale, although a recent paper has reported a low

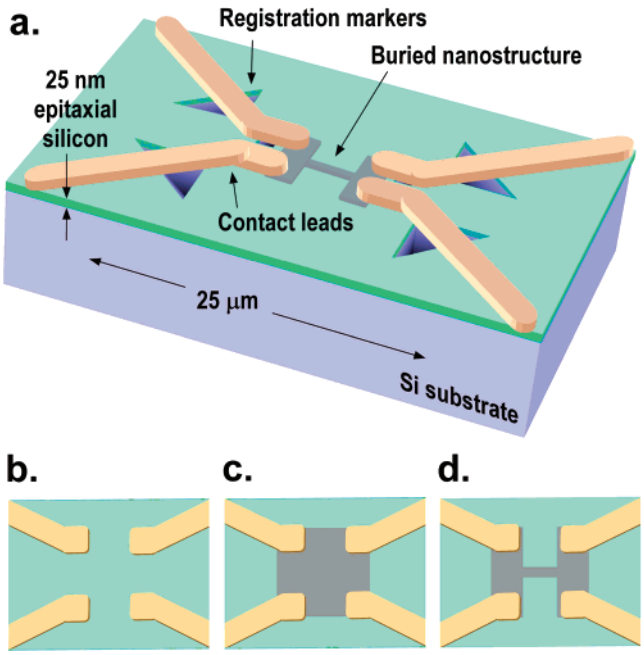

Figure 2. Device schematics. (a) A 90 × 900 nm^2 quantum wire patterned by STM showing triangular registration markers etched into the silicon substrate. Aluminum ohmic contacts (shown in yellow) were fabricated by optical lithography after removing the sample from the STM-MBE system. (b−d) 2D schematics of the three fabricated devices with contact leads. The gray areas mark lithographically defined regions using STM−a control device (b), a 4 × 4 μm^2 P-doped square (c), and a 90 × 900 nm^2 quantum wire (d).

temperature cleaning process compatible with ion implanted markers.[15] SEM imaging of the registration markers shows little change in their contrast and shape before and after the heating step, or during the entire device fabrication process.

After the sample is exposed to atomic hydrogen to form a monohydride resist layer, the STM tip is placed with respect to the registration markers for STM lithography using both the SEM and a laser-based STM stage positioning system. The STM is then used to selectively desorb the hydrogen resist by applying a bias voltage of 6 V and a tunneling current of 4 nA to form the desired pattern. Exposing the surface to a saturation dose of PH_3 gas at a pressure of 1.1×10^{-9} mbar for 15 min selectively adsorbs PH_3 molecules on the reactive, exposed silicon area of the patterned surface. The surrounding, nonreactive H-terminated surface blocks PH_3 adsorption.[5] The silicon sample is then controllably heated to 470 °C for 60 s, which initially incorporates the phosphorus atoms from the PH_3 molecules into the top Si layer (at ∼350 °C) and subsequently removes the hydrogen resist layer. This process preserves the carefully created STM-patterned phosphorus-doped structure and provides a high quality surface for subsequent epitaxial overgrowth.[16]

Finally, the patterned phosphorus device structure is encapsulated with 25 nm of epitaxially grown silicon at 250 °C, since this has been found to give full electrical activation with minimal segregation.[14] The sample is then removed from the UHV system and four aluminum terminals are aligned to the registration markers using optical lithography. After metallization, the sample is annealed at 350 °C for 15 min, in which time the aluminum diffuses down to the buried STM-fabricated contact pads to form an ohmic contact.[17] An optical microscope image of the final device structure after gold wire bonding is shown in Figure 1f. Currently we achieve alignment accuracies between the STM-fabricated nanostructure and the registration markers on the order of 100 nm and an instrument-limited accuracy of ∼500 nm in the optical lithography process for the formation of metal contacts. It is possible to achieve higher alignment accuracy by using electron beam lithography instead of optical lithography, which is expected to improve alignment accuracies between metal contacts and STM-fabricated nanostructures to below ∼100 nm. However, we emphasize that the creation of nano- or atomic-scale devices using this registration strategy does not require such accurate alignment, as the STM can also be used to define large buried contact pads connected to the device that can be readily contacted with standard optical lithography techniques, as demonstrated here.

Four terminal magnetoresistance measurements of the three devices were performed at 0.05−4 K to confirm the success of the fabrication strategy. Initially the device with no STM patterning (see Figure 2b) was tested. This device underwent all the processing steps of the other two devices, except that the STM was not used to remove the hydrogen resist in the active region between the contacts. Consequently, no PH_3 molecules adhere to the silicon surface and there should be no dopant incorporation or conduction between the ohmic contacts. Measurements at 4 K on this device showed that applying ±2.5 V across the contacts resulted in no current flow (I < 10 pA), equivalent to a resistance in excess of 2.5×10^{11} Ω. This confirms the effectiveness of the hydrogen resist at blocking the adsorption of phosphine gas to the silicon surface.

Figure 3a shows the magnetoresistance of the 4 × 4 μm^2 phosphorus-doped square device both at 4 K and 50 mK. This device allows us to determine how efficient the STM is at removing hydrogen from the surface. Hall measurements of the square device at 4 K gave an electron density of $1.79 \pm 0.05 \times 10^{14}$ cm^{-2}, in excellent agreement with $2.0 \pm 0.4 \times 10^{14}$ cm^{-2} obtained from previous studies of P δ-doped layers in Si formed by PH_3 saturation dosing of the bare silicon surface.[14] This result confirms that the hydrogen resist was removed with close to 100% efficiency by STM lithography. We can also extract information about the quality of the epitaxial overgrowth by measuring the electron mobility and phase coherence length. The electron mobility of the square device is ∼21 cm^2/Vs, comparable to that obtained in recent studies of high quality P δ-doped layers,[18] demonstrating that the fabrication process we have developed has not adversely affected the device quality.

Further examination of the magnetoresistance of the square device in Figure 3a at 4 K shows a peak centered around $B = 0$ (blue trace) that becomes more pronounced as the sample is cooled to 50 mK (red trace). This temperature-dependent magnetoresistance is a characteristic signature of weak localization arising from coherent backscattering of

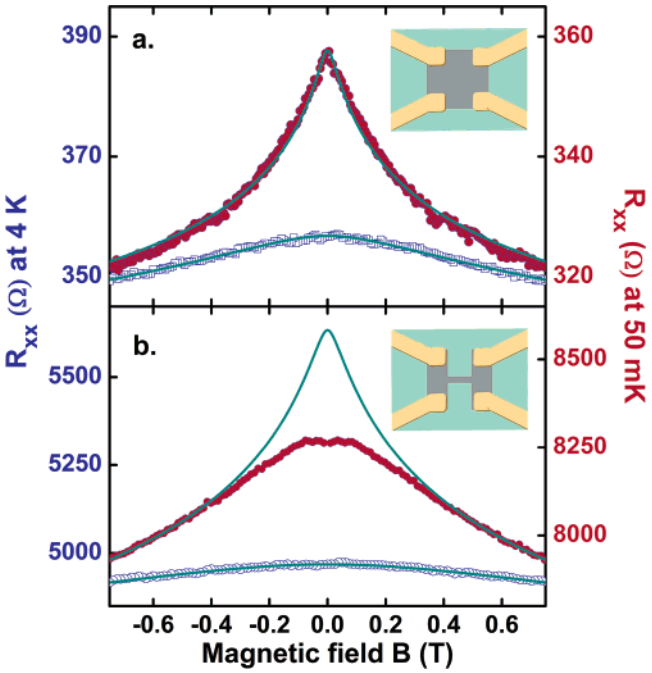

Figure 3. Electrical measurements showing the magnetoresistance of the 4 × 4 μm^2 square device (a) and of the 90 × 900 nm^2 wire (b) at 4 K (blue circles) and 50 mK (red circles). The green lines show fits to 2D weak localization theory. Insets show schematics of the device geometries.

forward and time-reversed electron waves around a loop as electrons diffuse through the sample.[19] The application of a magnetic field breaks the time reversal symmetry in these loops, suppressing the coherent backscattering, and resulting in a drop in the magnetoresistance. As the temperature is lowered the phase coherence length increases, leading to the formation of more and longer phase coherent loops, further increasing the resistance of the sample at $B = 0$ and producing a more pronounced drop in the magnetoresistance. Note that the overall resistivity is similar at both temperatures, as expected for a highly doped 2D system.

We can extract the phase coherence length l_ϕ of the electrons by fitting the magnetoresistance to the Hikami[20] expression for weak localization (see green line in Figure 3a). At 4 K we find $l_\phi = 39$ nm, which increases to $l_\phi = 136$ nm as the temperature is reduced to 50 mK. Therefore, to observe signatures of quantum confinement in an STM-patterned device we would need to make a device with widths w below ~130 nm.

In Figure 3b we present the magnetoresistance of the 90 nm-wide quantum wire device processed on the same chip. We can see that the overall resistance of the wire is much higher than for the square device, as expected from the sample geometry. At 4 K (blue trace) the resistance of the wire device shows a similar peak in the magnetoresistance around $B = 0$ with an extracted phase coherence length $l_\varphi = 32$ nm. Therefore, electron transport in the wire at 4 K is essentially two-dimensional, as electrons are unable to distinguish if they are traveling through a 4 μm-wide square or a 90 nm-wide wire. As the temperature is reduced to 50 mK, l_φ becomes larger than the wire width, and the lateral confinement of the wire limits the maximum size of electron loops that can contribute to weak localization. Thus, although the negative magnetoresistance starts to become stronger as T is reduced (red trace in Figure 3b), it does not produce such a pronounced peak around $B = 0$. This is further highlighted if we consider the 2D Hikami fit applied to the wire (green line in Figure 3b), which gives a phase coherence length $l_\varphi = 135$ nm. Here we can clearly see a suppression of the 2D weak localization around $B = 0$ due to a crossover from two-dimensional to one-dimensional electron transport.

We can use the suppression of the 2D weak localization to independently measure the width of the quantum wire. Constructive interference is destroyed when a magnetic flux quantum threads a loop of radius r, i.e., when $r^2 = \hbar/(eB) = l_B^2$. When the magnetic length l_B is much larger than the wire width w, the magnetic field has relatively little effect, which results in the plateau around $B = 0$. As the magnetic field increases the size of the constructively interfering loops becomes smaller, so that it is B, and not the wire width, that determines the magnitude of the weak localization effect. Thus the wire approaches two-dimensional behavior when $2l_B \sim w$. From Figure 3b we see that the measured data merges with the green line of the 2D theory at $|B| \sim 0.3$ T, giving a wire width of ~90 nm, in excellent agreement with the STM-defined geometry. It is worth noting that a wire width of 90 nm was chosen as the ideal geometry, dictated by the phase coherence length, to observe the crossover from one-dimensional to two-dimensional electron transport in this highly doped Si:P system. However the true power of this approach is the capability of STM to make structures down to the atomic level by using exactly the same fabrication process as we have described here.

In summary, we have demonstrated a novel strategy for fabricating nanoscale devices in silicon using a unique combination of STM-based lithography, phosphorus-doping, MBE crystal growth, and conventional optical lithography. We demonstrate that registration markers patterned into the substrate surface by conventional optical lithography can be used to align surface ohmic contacts to buried dopant structures patterned by STM lithography. Electrical transport measurements confirm both full electrical activation of the buried phosphorus atoms and integrity of the nanoscale device geometry defined by STM lithography. Using this technology we have been able to observe the crossover from 2D to 1D behavior in a buried dopant device by confining the electrons to a 90 nm-wide quantum wire.

It is important to add that the fabrication strategy we have developed shows promise for the realization of sophisticated atomic-scale devices in silicon such as single electron transistors (SETs),[21] quantum cellular automata,[22] and a Si-based solid-state quantum computer.[23]

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