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Self-Aligned Ballistic n-Type Single-Walled Carbon Nanotube Field-Effect Transistors with Adjustable Threshold Voltage

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ABSTRACT

Near ballistic n-type single-walled carbon nanotube field-effect transistors (SWCNT FETs) have been fabricated with a novel self-aligned gate structure and a channel length of about 120 nm on a SWCNT with a diameter of 1.5 nm. The device shows excellent on- and off-state performance, including high transconductance of up to 25 μS, small subthreshold swing of 100 mV/dec, and gate delay time of 0.86 ps, suggesting that the device can potentially work at THz regime. Quantitative analysis on the electrical characteristics of a long channel device fabricated on the same SWCNT reveals that the SWCNT has a mean-free-path of 191 nm, and the electron mobility of the device reaches 4650 cm^2/Vs. When benchmarked by the metric CV/*I* vs I_{on}/I_{off}, the n-type SWCNT FETs show significantly better off-state leakage than that of the Si-based n-type FETs with similar channel length. An important advantage of this self-aligned gate structure is that any suitable gate materials can be used, and in particular it is shown that the threshold voltage of the self-aligned n-type FETs can be adjusted by selecting gate metals with different work functions.

Carbon nanotube (CNT) has been considered as one of the most promising building blocks for future nanoelectronics due to its unique one-dimensional (1D) structure and superior physical properties.[1] Field-effect transistors (FETs) based on semiconducting single wall CNTs (SWCNTs) have been actively developed in the past ten years,[2,3] and both p-type and n-type high performance ballistic SWCNT FETs have been fabricated[4−6] showing significant improvements on several key device metrics over the corresponding state-of-the-art Si-based metal-oxide-semiconductor (MOS) FETs.[7−9] Basic logic gate circuits, including inverter, NOR, NAND, and ring oscillators have been realized using SWCNT FETs,[10−12] and a CNT-based doping-free complementary MOS (CMOS) circuit was recently demonstrated.[5] A major remaining challenge for realizing more complex high performance CNT-based CMOS circuits is how to make CNT-based high performance FETs smaller but reliable while retaining tight control of the properties of these devices, in particular their threshold voltage.

In the state-of-the-art silicon CMOS technology[13] a self-aligned structure is used to ensure the accuracy of the entire fabrication process. As the size of the device becomes smaller and smaller there is a need for a more precise and reliable way to fabricate MOS FETs automatically, and the self-aligned structure ensures that the edges of the source (S), drain (D), and gate (G) electrodes are precisely and automatically positioned such that no overlapping or significant gaps exist between these electrodes. The use of self-aligned gates is one of the many innovations that has enabled computing power to increase steadily over the last 40 years.[13] A self-aligned structure is therefore necessary for massive fabricating of high performance CNT FETs and for the construction of CNT based CMOS integrated circuits.

A self-aligned structure which utilizes the existence of native oxide on the surfaces of certain metals, such as Al_2O_3 on Al, has been developed and used to fabricate near ballistic p-type CNT FETs with near ideal performance.[14] While this structure works well for aligning gates for p-type CNT FETs, where reactive metals with low work function (such as Al) may be used as the gate materials, it is not suitable for fabricating high performance self-aligned n-type CNT FETs;

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for enhanced n-type FETs, inert metals with high work function (such as Pd, Au and Pt) must be used. In a previous work,[9] we demonstrated that high-performance n-type CNT FETs can be fabricated by integrating the devices with Sc contacts and atom layer deposition (ALD) grown HfO_2 gate insulator. However the devices so fabricated without self-aligned gate structures cannot be pushed to their performance limit due to the large parasitical capacitances and leakage current induced by large overlapping between gate and source (drain) electrodes. In this communication, we report a novel self-aligned gate structure which is suitable for fabricating both n- and p-type CNT FETs with desired threshold voltage, and indeed for any FETs based on 1D nanomaterials. Both near ballistic (with a channel length $L \sim 120$ nm) and long channel (with $L \sim 2$ μm) n-type CNT FETs are fabricated with this structure on a single SWCNT with a diameter of ~1.5 nm. Quantitative fitting of the electric characteristics of the long channel FETs reveals a high electron mobility of over 4650 cm^2/Vs and a mean-free path $l_0 = 191$ nm. A careful evaluation of the 120 nm devices shows that the self-aligned gate can effectively control the channel yielding a very small gate delay time of 0.86 ps and a large room temperature I_{on}/I_{off} ratio of over 10^4. We demonstrate that by using this simple self-aligned structure we can readily adjust the threshold voltage of the FET by freely selecting gate material with suitable work function.

The threshold voltage V_{th} is one of the most important device parameters which must be considered carefully when FETs are being integrated into a complex CMOS circuit. In principle the threshold voltage of a FET may be adjusted by controlling the doping of its conduction channel,[15] but this method is not suitable for implementing CNT-based doing-free CMOS technology.[5] Alternatively gate metal with suitable work function may be utilized to control the threshold of the device, and this is the method we used in the doping-free fabrication of CNT-based CMOS circuits.

The fabrication of our self-aligned n-type CNT FETs is illustrated in the process flow shown in Figure 1. Windows for S and D electrodes were first patterned via electron beam lithography (Figure 1a), Sc film of 60 nm was then deposited by e-beam evaporation (Figure 1b) followed by lift-off to finish the S and D electrodes with steep sidewalls on top of the SWCNT (Figure 1c). The gate window was then patterned via electron beam lithography (Figure 1d), and a 15 nm HfO_2 film with dielectric constant of about 15 was grown by ALD at 90 °C (Figure 1e) followed by 5 nm Ti film deposition by e-beam evaporation (Figure 1f). The standard lift-off process was then used to form the HfO_2/Ti gate stack (Figure 1g) and a top view scanning electron microscopy (SEM) image of the final device is shown in Figure 1h. In this self-aligned structure, we take the advantage of the different grown mechanisms of HfO_2 and Ti films. While the ALD grown HfO_2 film is continuous with excellent thickness uniformity and step coverage, that is, uniform film presents even on the sidewalls of the S and D electrodes[16] (Figure 1e) which effectively insulates G from S and D, the Ti film grown via e-beam evaporation is basically two-dimensional and does not present on the

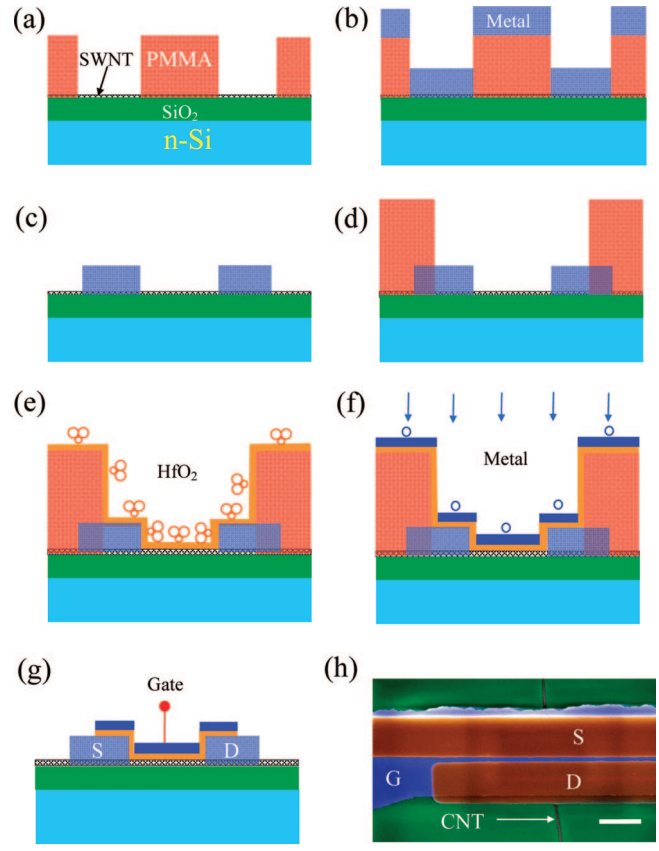

Figure 1. Process flow for the fabrication of self-aligned CNT FETs. (a) The source (S) and drain (D) patterns are defined by e-beam lithography on photoresist PMMA. (b) Metal (Sc) film of 60 nm is deposited by e-beam evaporation. (c) A standard lift-off process is used to form the S and D electrodes. (d) The gate (G) pattern is defined by e-beam lithography. (e) HfO_2 film of 15 nm is grown via ALD, followed by (f) Ti film (about 5−10 nm) via e-beam evaporation. (g) A standard lift-off process is used to form the G electrode. (h) SEM image showing the top view of a final device; the scale bar is 1 um.

sidewalls of the S and D electrodes (Figure 1f) so that the part of Ti film between S and D is disconnected from that on top of the S and D or on top of PMMA which defines the gate window (Figure 1f). The so fabricated final structure (Figure 1g) shows that the edges of the S, D, and G electrodes are precisely positioned. CNT FETs with channel length of about 120 nm were fabricated with this self-aligned structure. For these 120 nm devices and 15nm HfO_2 gate dielectric, the gate length $L_g = 120 - (2 \times 15) = 90$ nm, giving excellent control on the conductance of the 120 nm SWCNT segment between S and D. Moreover since there are no overlaps between G, S, and D, the parasitical capacitances between G, S, and D are also minimized.

Figure 2a shows the field transfer characteristics of a typical 120 nm device fabricated on a 1.5 nm SWCNT. The four curves in this figure correspond respectively to $V_{ds} =$ 0.1 V (blue), 0.3 V (green), 0.5 V (red), and 1.0 V (black), showing that the device is an n-type FET having its ON state at positive gate voltage. Notably for a fixed bias V_{ds} the device shows hardly any hystereis in its transfer characteristic (see Figure 2b) when scanning the gate V_{gs} from −2 to 2 V and from 2 to −2 V, suggesting that there exist effectively

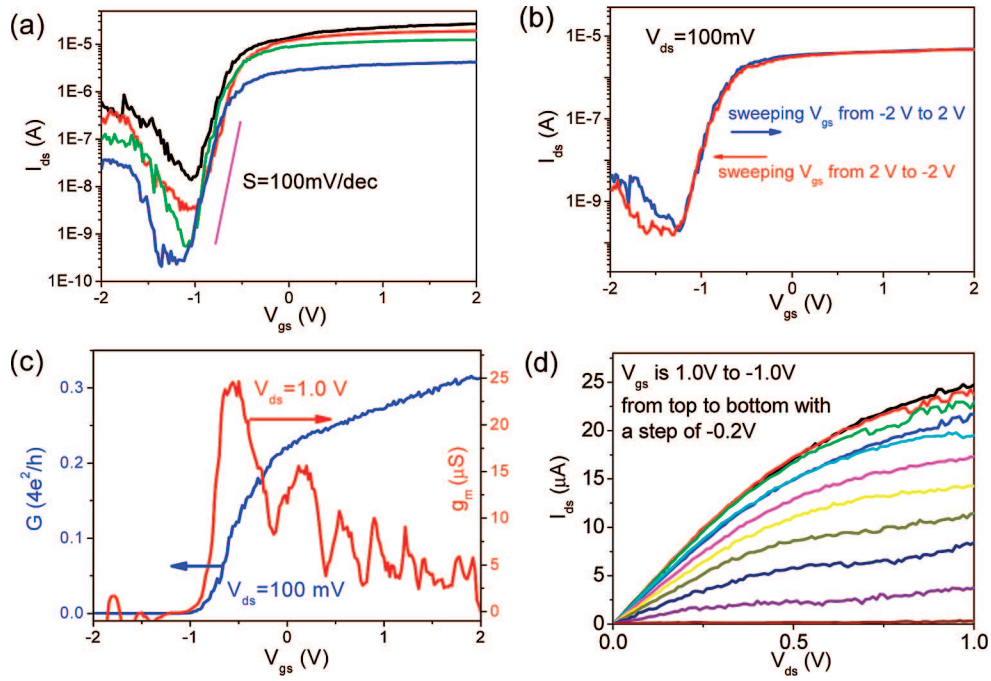

Figure 2. Self-aligned SWNT-FETs. (a) Transfer characteristics of a self-aligned n-type SWCNT FET (with a channel length $L = 120$ nm and a SWCNT diameter $d = 1.5$ nm) for V_{ds}=1.0, 0.5, 0.3, and 0.1 V, respectively, from top to bottom. (b) Two $I_{ds}-V_{gs}$ curves obtained using the same $V_{ds} = 0.1$ V but with different V_{gs} scanning direction. (c) Gate voltage dependence conductance (G) (blue curve, left) and transconductance (g_m) under $V_{ds} = 1.0$ V. (d) Output characteristics of the device in which V_{gs} is varied from 1.0 V (top) to −1.0 V (bottom) with a step of −0.2 V.

few charge traps around SWCNT in this device. The hystereis-free transfer characteristics are resulted from three improvements. First, oxygen-related defect traps such as water molecules are isolated from the SWCNT which is fully covered by HfO_2 in our self-aligned structure.[17] Second, the growth condition is so chosen that there are only few charge traps in our ALD grown HfO_2 dielectric. Third, gate electrode film is deposited immediately after the growth of HfO_2 film, so the interface between the gate dielectric and metal electrode is very clean.

The 120 nm n-type CNT FET exhibits a high peak transconductance g_m of up to 25 μS at about $V_{gs} = -0.5$ V and approaches its On-state at $V_{gs} > 2$ V with a conductance G_{on} of $\sim 0.32 \times 4e^2/h$ (Figure 2c). This device also has a large saturation current I_{sat} of about 25 μA as shown in Figure 2d. The current ON/OFF ratio for this FET (with a diameter $d \sim 1.5$ nm) is larger than 10^4 at $V_{ds} = 0.3$ V and larger than 10^3 at $V_{ds} = 1.0$ V, and the subthreshold swing S is about 100 mV/decade (see Figure 2a). The excellent transconductance and threshold swing suggest that the SWCNT channel of our FET is indeed effectively controlled by the self-aligned gate.

The performance of the CNT FETs can be benchmarked against that of the state-of-the-art Si MOSFET devices using the device metrics proposed by Chau et al..[18,19] The metric that is used to describe the intrinsic speed of the FET is the intrinsic gate delay $\tau = CV/I$, in which C is the total gate capacitance, $V = V_{dd}$ is the applied voltage and $I = I_{on}$ is the On-state current as defined in Figure 3a.[18] The intrinsic gate delay is considered as an indication of how fast a transistor operates. For our 120 nm FET, the SWCNT channel has a diameter $d = 1.5$ nm and the gate dielectric HfO_2 thin film has a thickness $t = 15$ nm and $\varepsilon_r = 15$, we have $C = 1.43$ pF/cm. The threshold voltage V_{th} is extracted from the peak transconductance method[18] to be −0.67 V (Figure 2c). By constructing a V_{dd} window as shown in Figure 3a at V_{th}, we have then $I = I_{on} = 7.6$ μA and $V = V_{dd} = 0.5$ V. The device with $L_g = 90$ nm thus has a small intrinsic delay time $\tau = CV/I = 0.86$ ps, suggesting 1 THz switching speed is potentially possible with this CNT device, and this delay time is comparable with that of the silicon NMOS devices with $L_g = 40$ nm.[18,20] Another important metric describing switching energy is the energy-delay product ($CV{\cdot}I/CV^2$) per unit device width. For our 120 nm device this product is about 6.0×10^{-28} Js/μm, and this value is also comparable to that of the 40 nm (L_g) Si NMOS device.[18] In Table 1 we give a comparison of the key device parameters between our n-type CNT FETs and that of the best p-type devices.[8,14] Although some ON-state device parameters such as g_m and G_{on} are slightly smaller than that of the best p-type CNT FET (p-type II)[14] due to the longer channel length and smaller diameter of our device, our self-aligned n-type FET outperforms in some important aspects the p-type FETs, in particular the intrinsic gate delay per unit length τ/L of our device is much smaller and I_{on}/I_{off} ratio is larger than that of the p-type devices.

We have already demonstrated that the Sc-contacted top gate n-type CNT FETs exhibit better length dependent intrinsic speed (CV/I) and energy-delay product ($CV{\cdot}I/CV^2$) than that of the state-of-the-art silicon NMOS devices.[9] Another important performance metric is CV/I versus I_{on}/I_{off} which describes the transistor OFF-state leakage I_{off}. This

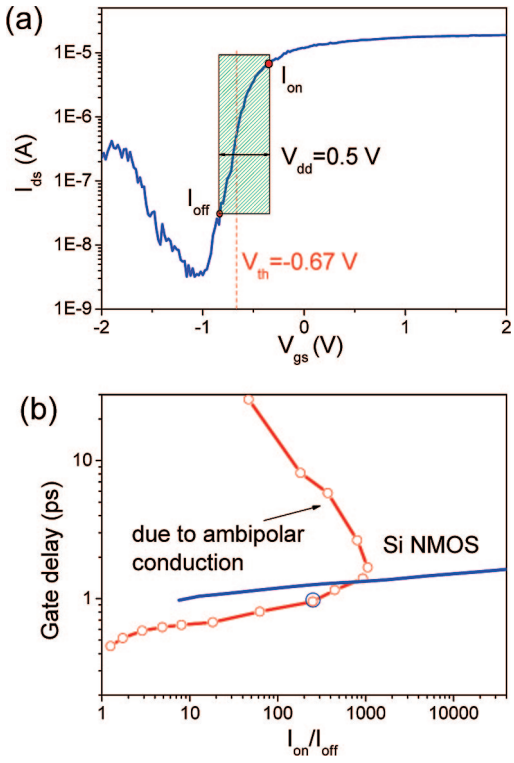

Figure 3. (a) $I_{ds}-V_{gs}$ data for the same device as shown in Figure 1 at bias $V_{ds} = 0.5$ V. The shaded area defines a 0.5 V gate voltage window used to obtain I_{on} and I_{off}, where V_{th} is determined using the standard peak transconductance method. (b) Intrinsic delay versus I_{on}/I_{off} ratio for the n-type CNT FET comparing to that of a Si NMOS FET with similar channel length of $L = 130$ nm but large applied voltage $V_{dd} = 1.0$ V. The blue circled point indicates the value of intrinsic delay used in Figure 3a. The data for Si NMOS is adopted from Figure 7a of ref 21.

metric is particularly important for CNT-based devices since typically a CNT has a smaller bandgap than that of Si.[18] Figure 3b shows *CV/I* versus I_{on}/I_{off} curve for our 120 nm ($L_g = 90$ nm) n-type CNT FET, together with that for the Si NMOS FETs with similar $L = 130$ nm ($L_g = 70$ nm).[21] The curve is obtained by rigidly moving the V_{dd} window in Figure 3a along the V_{gs} axis and calculating corresponding *CV/I* and I_{on}/I_{off} values for each V_{gs}. The I_{on}/I_{off} ratio decreases as we move the V_{dd} window away from the OFF-state at about $V_{gs} = -1.0$ V to the ON-state at large positive V_{gs}, and the gate delay (*CV/I*) decreases smoothly with reducing I_{on}/I_{off} ratio. This is because for smaller I_{on}/I_{off} ratio we have larger ON-state current which reduces *CV/I* but increases significantly the OFF-state leakage current I_{off}. The I_{on}/I_{off} ratio reaches its maximum value of about 1000 at the valley of the field transfer curve of Figure 3a, and decreases again as the V_{dd} window moves into the p-type region with $V_{gs} < -1.0$ V where I_{off} current increases while I_{on} decreases in moving along the negative V_{gs} axis, resulting in a rapidly increasing *CV/I*. Figure 3b also shows that the n-type CNT FET has significantly reduced gate delay than that of the Si NMOS FETs for all I_{on}/I_{off} ratios that are smaller than 1000, and this has been attributed to the higher carrier mobility and lower supplied power V_{dd} used here. An important point to note is that although the highest achievable I_{on}/I_{off} ratio in a CNT FET is limited by the ambipolar conduction of the CNT, a I_{on}/I_{off} ratio between 100 to 1000 may already satisfy the criterion for certain high-performance applications.[22]

To estimate the electron mobility of our n-type CNT FETs, a long channel (with $L = 2.0$ μm) device was fabricated using the same self-aligned structure and on the same SWCNT on which the short channel 120 nm device was fabricated. The field transfer and output characteristic are shown in Figure 4 and fitted with a modified diffusive conductance model.[23] The perfect agreement between the experimental (circles) and simulated (solid line) data shows clearly that our Sc-contacted long channel device can be described quantitatively using this diffusive model. In its simplest form, the conductance of a diffusive device is given by

$$G = (4e^2/h)(l_{mfp}/L) \quad (1)$$

in which the mean free path of the electron $l_{mfp} = \tau\nu$, with τ^{-1} being the scattering rate and ν being the electron velocity. It is the general property of a 1D system that the scattering rate τ^{-1} is proportional to the density of state (g) of the system. For the conduction band of a CNT $g = 8/h\nu$, we therefore have $\tau^{-1}\nu = \tau_0{}^{-1}\nu_0 =$ constant with $\tau_0{}^{-1}$ being the scattering rate and $\nu_0 = 8.7 \times 10^5$m/s being the electron velocity at large gate voltage or when E_f is in the linear dispersion regime. Substituting these relations into eq 1 yields

$$G = (4e^2/h)(l_0/L)(\nu/\nu_0)^2 \quad (2)$$

where $l_0 = \tau_0\nu_0$ is the electron mean free path at large V_g. The above equation shows that G depends on V_{gs} implicitly via the electron velocity $\nu(E_f)$. Quantitative fitting of the experimental data shown in Figure 4 yields $l_0 = 191$ nm, confirming that our 120 nm short channel device fabricated on the same SWCNT (Figure 2) is indeed a ballistic device having its channel length much smaller than $l_0 = 191$ nm. The electron field-effect mobility μ_e for the long channel CNT FET can be calculated using the relation

$$\mu_e = (L/C)[d(G/dV_{gs})] \quad (3)$$

At the conduction band edge the electron velocity $\nu = 0$, but it increases rapidly with increasing E_f ($\propto V_{gs} - V_{th}$) when the channel is opened from $V_{gs} \sim V_{th}$ and approaches its saturation value ν_0 at large V_{gs} when E_f is moved into the linear dispersion regime of the conduction band of the CNT. Equation 2 shows that the conductance $G = I_{ds}/V_{ds}$ follows V_{gs} via its $G \propto \nu^2$ dependence, and the electron mobility as a function of V_{gs} can be calculated using $G(V_{gs})$ via eq 3. Figure 4a shows that the electron mobility is very small when the device is near its OFF-state ($V_{gs} \sim V_{th}$) or when E_f is near the conduction band edge. But μ_e increases rapidly with increasing V_{gs} and reaches a peak value 4650 cm^2/Vs at $V_{gs} = -0.2$ V. This rapidly increase in the electron mobility is largely due to the fact that the velocity of the electron in a semiconducting CNT increases dramatically from zero when V_{gs} is at the threshold or when E_f is at the bottom of its conduction band. But the rate of increase of $\nu(E_f)$ slows down at $V_{gs} > -0.2$ V and the velocity saturates eventually to ν_0 at large V_{gs}, leading to a peaked mobility followed by a slow decaying tail down to a very low electron mobility. This decreasing trend in the electron mobility is a result of the quantum constrain on the conductance of the CNT, limiting

Table 1. Comparison of Key Parameters Between p-Type and n-Type CNT FETs[a]

	D nm	L nm	I_{sat} μA	g_m μS	S mV/dec	G_{on} $4e^2/h$	ON/OFF (V_{ds})	τ/L ps/μm
p-type I	1.8	600	18	12.5	140	<0.1	10^5(0.3V)	19
p-type II	1.7	50	25	30	110	0.5	10^3(0.3V)	28
n-type (this work)	1.5	120	25	25	100	0.32	>10^4(0.3V) >10^3(1.0 V)	7.2

[a] In this table, data for p-type device I are taken from ref 8 and for device II from ref 14.

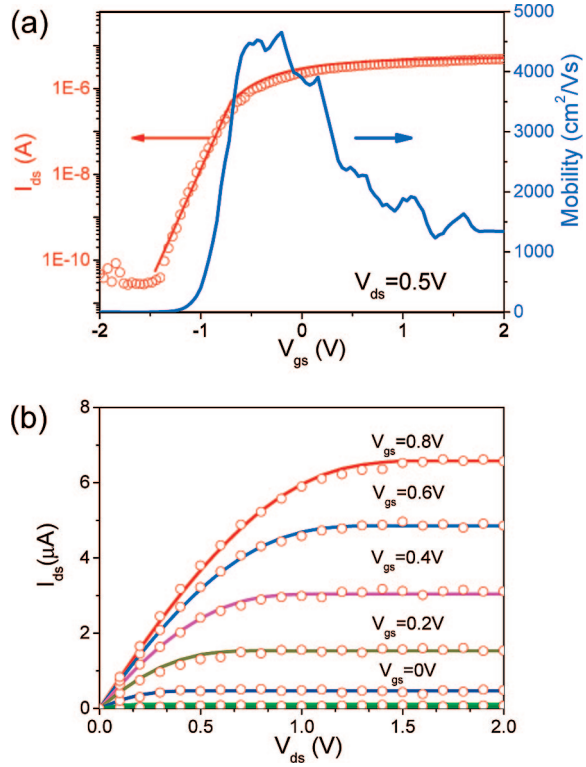

Figure 4. Electrical transport characteristics of a long channel (L = 2 μm) CNT FET which is fabricated on the same SWCNT as the 120 nm device shown in in Figure 2. (a) Transfer characteristic of the FET at V_{ds} = 0.5 V (red curve) and V_{gs} dependent electron mobility (blue curve). (b) Output characteristics of the same device in which V_{gs} is varied from 0.8 to −0.4 V in step of −0.2 V from top to bottom. Symbols are experimental data and solid lines are simulated data using a diffusive FET model.

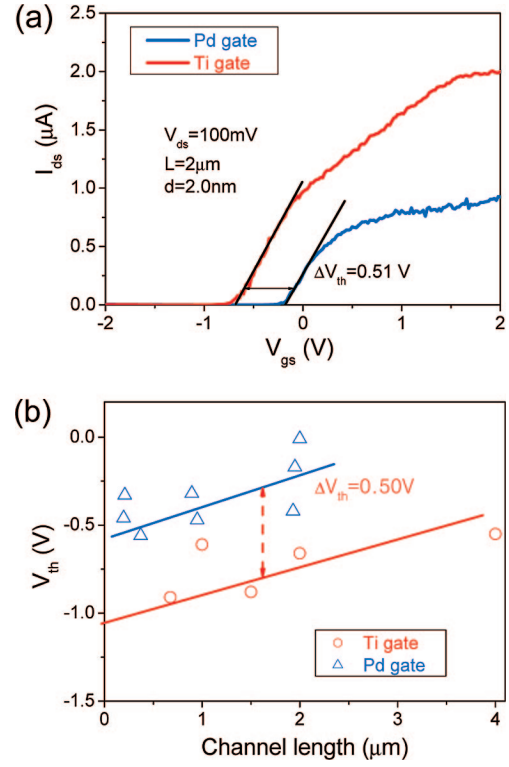

Figure 5. Adjustment of threshold voltage of CNT FETs via selecting gate metal. (a) Transfer characteristics for two FETs on the same SWCNT with L = 2.0 um and d = 2.0 nm. The red (green) curve corresponds to the device with a Ti (Pd) gate and a bias V_{ds} = 100 mV. (b) Channel length dependence of V_{th} for 13 FETs with different top gate electrodes. All the FETs are fabricated on the same CNT as used in (a) with Ti (green) and Pd (blue) top gate electrodes.

the maximum conductance of a SWCNT to be less than the quantum conductance $G_0 = 4e^2/h$. Although at large V_{gs}, when E_f is in the linear dispersion regime, more electrons are being added into the CNT, this increase in the electron density is perfectly compensated by a decrease in the electron mobility leading to a limited constant conductance at larger V_{gs}. The nonmonotonic gate voltage dependent electron mobility behaves similar to the hole mobility in a p-type FET.[24−26] It should be noted that the peak mobility of 4650 cm^2/Vs achieved here is of the same order of magnitude as the best hole mobility reported for the p-type CNT with similar diameter.[25] The high electron mobility achieved here suggests that the deposition of high-κ gate dielectric HfO_2 film on top of the SWCNT does not degrade significantly its electrical transport property.

The main advantage of our self-aligned gate structure is that it can be applied to use any gate material with desired property. In particular this structure allows us to adjust the threshold voltage of the FET by choosing suitable gate metal with desired work function to meet the requirement of the circuit design. Two self-aligned FETs with the same channel length were fabricated on the same SWCNT with a diameter of 2.0 nm. The only difference between the two devices is that one FET used Ti as gate electrode and the other used Pd. The transfer characteristics of the two devices are given in Figure 5a, showing clearly that the threshold voltage V_{th} of the device with Pd gate has been shifted by about 0.51 V along positive V_{gs} axis with respect to the device fabricated using Ti gate. This shift is found to be channel length dependent as shown in Figure 5b where results from 13 devices with different channel lengths but on the same CNT are shown. Among the 13 devices, 5 devices were fabricated using Ti gate and 8 using Pd gate. The V_{th} of each device is extracted using the standard peak transconductance method under the bias of 0.1 V. The L dependence of V_{th} might result from the fact that the electric property of the FETs varies from channel dominated to contact dominated as the channel length decreases from diffusive regime toward ballistic regime.[27] The V_{th} values for these FETs with Pd gate are obvious separated from that with Ti gate. For simplicity, two

parallel lines are used to fit the data of the two types of FETs, and the V_{th} shift between these two lines is fount to be 0.50 V. This value is much smaller than the work function difference of ~0.8 V between Pd (5.1 eV) and Ti (4.3 eV), and this large discrepancy is largely due to the fact that the work function of a metal on a high-κ dielectric is different from that in vacuum.[28] The effective work function for Ti/ HfO_2 is 4.47 eV and for Pd/ HfO_2 is 4.90 eV,[28] and the work function difference between these two gate metals becomes smaller on a dielectric.[28] This reduction in the work function difference is described in term of a S parameter which accounts for dielectric screening and depends on the electronic component of the dielectric constant. For HfO_2 thin film $S = 0.52$,[28] the effective work function difference between Pd and Ti is then $\Delta W_{eff} = S(5.1 - 4.3) = 0.43$ eV, which is smaller but close to the experimental V_{th} shift $\Delta V_{th} = 0.50$ V. It should be noted that the gate HfO_2 dielectric we used here is not perfect, having a dielectric constant of about 15 (which is much smaller than that of an ideal HfO_2 with $\kappa \sim 25$). Since the S factor is smaller for larger dielectric screening, effective S factor for our nonperfect HfO_2 dielectric is therefore expected to be larger than the ideal value of 0.52 (for a perfect HfO_2), resulting in a larger ΔV_{th}. Nevertheless the results shown in Figure 5 demonstrate clearly that it is possible to tune V_{th} for desired applications via choosing suitable gate (metal) materials and dielectrics.

In conclusion, near ballistic n-type CNT FETs are pushed almost to their performance limit by using Sc contacts and a novel self-aligned metal gate with high-κ gate dielectric HfO_2, and the threshold voltage of these n-type CNT FETs is demonstrated to be adjustable by using suitable gate metal with desired work function. The overall performance of the Sc-contacted n-type CNT FETs are shown to be comparable to that of the best Pd-contacted p-type CNT FETs, suggesting that ideal CMOS circuits composed of perfectly matching n- and p-type FETs could be made on CNTs.

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