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Graphene-Based Atomic-Scale Switches

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ABSTRACT

Graphene's remarkable mechanical and electrical properties, combined with its compatibility with existing planar silicon-based technology, make it an attractive material for novel computing devices. We report the development of a nonvolatile memory element based on graphene break junctions. Our devices have demonstrated thousands of writing cycles and long retention times. We propose a model for device operation based on the formation and breaking of carbon atomic chains that bridge the junctions. We demonstrate information storage based on the concept of rank coding, in which information is stored in the relative conductance of graphene switches in a memory cell.

The ultimate limit for the miniaturization of electronics is the atomic scale. Reaching this limit will require novel materials as well as new paradigms for device operation and architecture. Graphene is a one-atom-thick conductor that has rapidly emerged as an exceedingly promising novel electronic material[1−4] for scaling beyond complementary metal oxide semiconductor (CMOS) circuitry and architecture. Compared to silicon, graphene has far superior mobility,[1,3,5−8] thermal conductivity,[9] and current-carrying capabilities[10] and may support room temperature ballistic transport;[2] yet like silicon, it has a planar geometry that enables multilayer device architecture and simplifies future integration with CMOS technology. However, the absence of a band gap poses a major challenge for graphene electronics, as this limits the ON/OFF ratio of digital devices. Recent progress has been made toward fabrication of graphene nanoribbon field effect transistors with high ON/OFF ratios;[11−13] nevertheless, this approach presents several additional challenges such as precision control of the ribbon width and the atomic structure of the graphene edges. Switching behavior with high ON/OFF ratio may also be promoted via chemical modification of graphene, though improvement in cycling capability remains to be developed.[14]

In this Letter, we demonstrate fabrication and operation of graphene switches and their application for nonvolatile information storage. We interpret their behavior using a model of electric-field-driven motion of atomic chains of carbon. These switches are fabricated by creating nanoscale gaps using electrical breakdown of graphene sheets—a reliable self-limiting process that avoids the need for advanced lithographic techniques, similar to that employed in metallic wires.[15,16] Applying appropriate bias voltage pulses switches the gap conductance between high (ON) or low (OFF) conductance states. Remarkably, these switches are extremely robust; we have operated them for many thousands of cycles without degradation, with the conductance state easily persisting for >24 h and perhaps indefinitely. As an example of potential applications, we demonstrate information storage based on the combination of two or more switches using rank coding, in which information is stored by the relative magnitudes of device conductance in a memory cell. Such nonvolatile, robust, atomic switches based on graphene, which are suitable for integration with CMOS as well as monolithic integration with graphene electronics, are extremely promising as components for atomic-scale devices.

Two-terminal graphene devices are fabricated using standard techniques.[17] Briefly, graphene sheets are transferred from a high-quality graphite source to a heavily doped silicon substrate with a 290 nm layer of thermally grown oxide. One- or two-layer graphene sheets are identified by color interference using optical microscopy, and metallic leads are attached to these sheets using electron beam lithography and thermal evaporation. The left panel of Figure 1a shows a scanning electron microscope (SEM) image of a completed device. The devices are placed within a vacuum chamber for transport measurements, which is then evacuated to 10^{-7} Torr. We find that the high vacuum is crucial to the breakdown process, presumably because this prevents atmospheric gases from reacting with the graphene.

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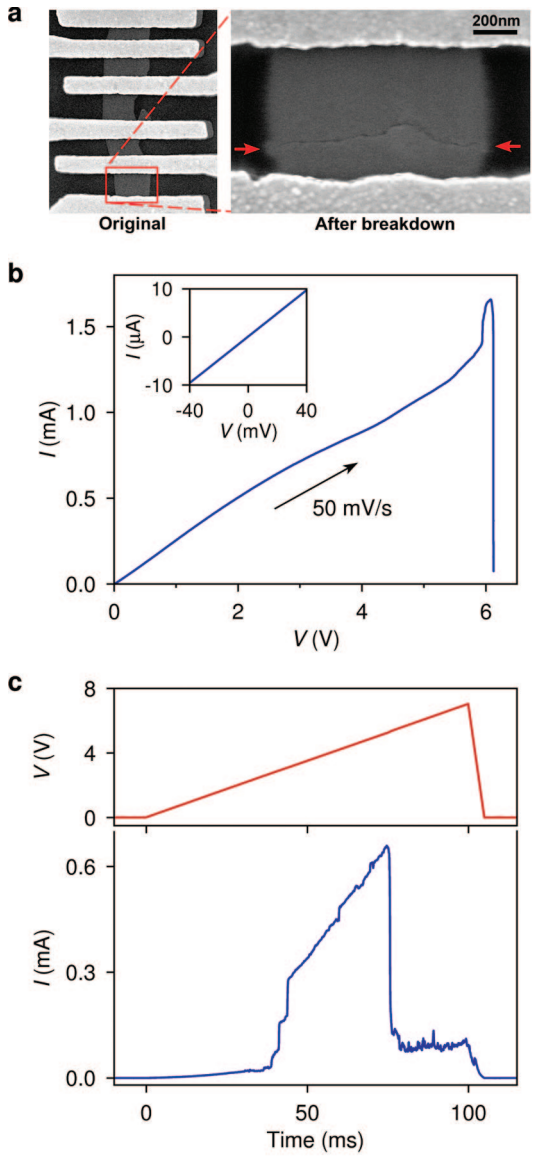

Figure 1. Sample preparation, nanogap formation via electrical breakdown, and switching behavior for a single representative graphene device. (a) SEM image of the device before (left panel) and after breakdown (right panel). The arrows indicate the edges of the nanoscale gap. (b) Current vs voltage during the breakdown process. Inset: Low bias current−voltage characteristic prior to breakdown. (c) Upper panel: Voltage vs time applied to the junction. Lower panel: Current response of the junction showing conductance recovery and subsequent reduction.

For each device, we first measure a baseline current−voltage (*IV*) characteristic up to a bias of 0.1 V. As shown in Figure 1b, inset, the typical conductance of a device before breakdown is ∼250 μS. We then gradually ramp up the bias voltage while monitoring the current. At a critical sheet current density of approximately 1.6 mA/ μm, the measured current drops precipitously, indicating breakdown of the graphene sheet (Figure 1b). Atomic force microscopy (AFM) imaging shows that a physical gap forms within graphene; at the closest approach of graphene edges, the gap's width is typically <10 nm. The right panel of Figure 1a shows an SEM image from a representative device after breakdown.

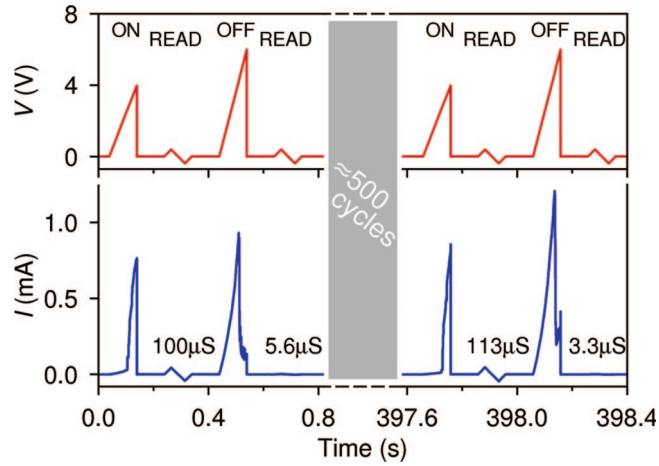

Figure 2. Repeatable programming over hundreds of cycles. Upper left panel: Voltage applied to the junction vs time. A ramp with a peak value of ∼4 V corresponds to an ON pulse, while a ramp with a peak value of ∼6 V corresponds to an OFF pulse. A small sawtooth-shaped read-out pulse is applied after each write to determine the junction conductance. Lower left panel: Current flow through the junction, with the low-bias conductance labeled above each read-out pulse. Right panels: Similar data taken after approximately 500 intervening cycles, demonstrating the reproducibility of the switching behavior.

Following the breakdown step, the low-bias device conductance is much lower, ranging from ∼0.1 nS to ∼20 μS. Remarkably, this conductance can be reproducibly increased or decreased using appropriate biases. Figure 1c illustrates a single switching cycle. The upper panel displays the applied source−drain bias V that quickly ramps up as a function of time, and the lower panel displays the current response. When $V < 2$ V, the current is very low; when it reaches ∼2.5−4 V, the current abruptly increases, reaching a maximum of 0.65 mA up to ∼5 V. At still larger voltages, the device returns to its initial low-conductance state. The conductance exhibits little or no gate voltage dependence in either state. Thus, by applying voltages of different magnitudes, the graphene devices can be switched into ON and OFF states, thereby functioning as voltage-programmable bistable switches or memory elements.

Similar conductance switching has been observed in a number of systems, such as molecules,[18] titanium oxides,[19] and Ag/Ag_2S nanowires.[20] What sets our graphene switches apart are their unique combination of reproducibility, nonvolatility, and integrability with graphene electronics. The conductance state has been cycled up to 10^5 times without degradation. Once the devices switch, they remain in either ON or OFF states for >24 h at room temperature, without external maintenance voltages. Although a systematic study of continuous monitoring for longer time periods has yet to be performed, we have observed devices after several weeks having conductance values similar to their last written states.

Figure 2 demonstrates the repeated operation of our devices. The upper left panel shows the programming and read-out voltage versus time. A ramped pulse that reaches 4 V corresponds to an ON pulse that increases the device conductance, while a pulse with a maximum of 6 V corresponds to an OFF pulse that decreases the device

conductance. In between the ON and OFF pulses, low-bias readout pulses are applied. The lower left panel shows the current response to the applied voltage versus time. Note that a large difference in current is observed during the readout pulses of the ON and OFF states, although similar current levels flow during the writing process. The ON state conductance is typically ~100 μS, while the OFF state conductance is typically ~5 μS. The upper right and lower right panels show similar data taken after ~500 switching cycles. The device behavior is virtually identical to that shown in the left panels, demonstrating its exceptional reproducibility.

The observed switching behavior of graphene devices that have been electrically broken down is quite surprising, especially given the robustness and reproducibility of this phenomenon. One possibility for the switching mechanism is dielectric breakdown and conduction through the substrate. However, such a process is not expected to be cycleable, as the conductance usually continues to increase upon further electrical stress, and the ON state conductance is far too large to be accounted for by current flow though stressed oxide. Another possibility is that the conductance occurs along a small graphene ribbon that bridges the contacts. However, small ribbons are expected to have a band gap,[11−13] with a strong gate voltage dependence in conductance, which is not observed. The absence of a gate voltage effect also excludes switching mechanisms arising from the storage of charge in traps in the oxide layer or from the formation of a small metallic island that may function as a quantum dot.

To gain further insight into the switching mechanism, we investigated the time-resolved behavior of the switching from the OFF to ON states, shown in Figure 3a. The conductance I/V shows well-defined steps, with magnitude ~G_Q (the characteristic step sizes, which include a series resistance from the graphene sheets, can vary by a factor of order unity from device to device). Here $G_Q = 2e^2/h$, the conductance quantum, where e is the electron charge, and h is Planck's constant. Since G_Q is the conductance of a spin-degenerate one-dimensional conductor, e.g., a linear chain of gold atoms,[21] observation of the conductance steps suggests that the device conductance states are likely multiples of highly transmitting quantum channels. To further investigate this phenomenon, we produce a histogram of the conductance by assembling data from 1000 cycles, as shown in Figure 3b. The histogram exhibits two main peaks, separated by ~$2e^2/h$. These well-defined peaks, as well as the conductance steps, strongly resemble those found in the breaking process of mechanically controlled break junctions,[21] in which a linear chain of atoms forms between two closely spaced metallic electrodes. These results strongly suggest that the conducting pathway bridging the graphene edges is atomic in scale.

Additional information about the switching mechanism is provided by the voltage dependence of the switching rate. We apply a square pulse with a given voltage magnitude to the device in the OFF state and measure the lapse in time t until the first sharp increase in conductance. Because of the

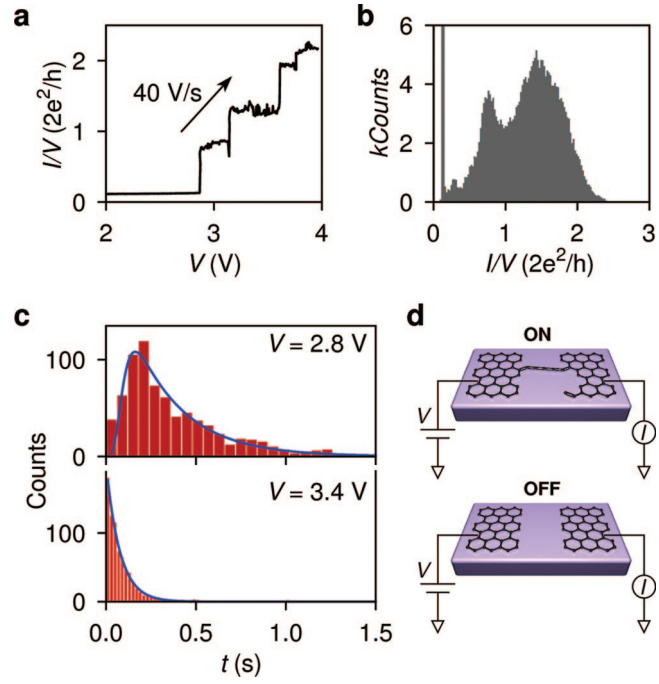

Figure 3. Conductance steps and histogram of conductance during switching, statistical analysis of the switching dynamics, and device schematic of ON and OFF states. (a) Conductance I/V taken while the device switches from the OFF to ON states. A sequence of steps of magnitude ~$2e^2/h$ is observed. (b) Histogram of conductance values showing two major peaks at approximately integer multiples of $2e^2/h$. (c) Histograms of waiting times for the first conductance-increase step for two different bias voltages. (d) Proposed schematic atomic configurations in the ON and OFF states.

stochastic nature of the switching, t follows a statistical distribution. Data from approximately 800 switching cycles are complied into histograms. The upper panel in Figure 3c shows a histogram of the measured t at $V = 2.8$ V. The peak at $t \sim 200$ ms indicates the most probable time scale at which switching occurs. The lower panel shows similar data, but with a larger bias $V = 3.4$ V. The peak in probability distribution visibly shifts toward zero, indicating the high probability of switching at relatively short time scales. Moreover, these observed switching rates are found to be strongly temperature dependent, increasing by a factor of ~3 for every 10 K increase in temperature.

The strong temperature and voltage dependence indicates a thermally activated process. In the simplest picture, such a process can be described by a single rate

$$\Gamma = \nu \exp[-\Delta(V)/k_B T] \quad (1)$$

where $\Delta(V)$ is the bias-dependent energy barrier, k_B is Boltzmann's constant, T is the temperature, and ν is an attempt frequency. At fixed temperature and bias, the rate is a constant, hence the waiting time would follow Poisson statistics, yielding a waiting probability per unit time $P(t) = \Gamma \exp[-\Gamma t]$. While this could account for the behavior shown in the lower panel, it cannot account for the maximum observed at finite waiting time in the upper panel.

We propose, therefore, that the conductance switching occurs by formation of linear chains of carbon atoms that bridge the gap under a strong electric field (Figure 3d). The

formation of such chains was reported earlier to account for the strong field emission current from the open end of multiwalled nanotubes,[22] and the associated unraveling process was studied theoretically.[23] Theoretical calculations predict that these chains are metallic without significant Pierls distortion and have the cumulene structure where each carbon atom in the chain is double bonded to its neighbor.[24] Their expected conductance is $\sim 2e^2/h$.[25] If multiple chains bridge the gap as the ON pulses are applied, this would be expected to produce $\sim 2e^2/h$ steps in the conductance, as observed. Moreover, calculations show[25,26] that the conductance of these wires is expected to be approximately independent of the Fermi level, therefore accounting for the lack of an observed gate voltage effect. Finally, the voltage dependence of the distribution in t can be readily explained if we consider a two-step process—the first step consists of n unlinking events, each of which corresponds to a carbon atom being "unzipped" from the graphene sheet, and has a rate Γ_1; the second step is the binding of the chain which extends all the way across the gap, with rate Γ_2. Both these rates should have a similar form to eq 1. The distribution $P(t)$ for the total waiting time would then be given by the convolution of the waiting time for an n-step Poisson process with rate Γ_1, known as the Erlang distribution, and a Poisson process with rate Γ_2. We find

$$P(t) = \frac{{\Gamma_1}^n \Gamma_2}{(\Gamma_1 - \Gamma_2)^n} e^{-\Gamma_2 t} - \sum_{m=1}^{n} \frac{{\Gamma_1}^n \Gamma_2}{(m-1)!} t^{m-1} e^{-\Gamma_1 t} \frac{1}{(\Gamma_1 - \Gamma_2)^{n-m+1}} \tag{2}$$

Fitting eq 2 to the data shown in Figure 3c gives $\Gamma_1 = 51$ s^{-1}, $\Gamma_2 = 3.6$ s^{-1} for the upper panel, and $\Gamma_1 = 4300$ s^{-1}, $\Gamma_2 = 13$ s^{-1} for the lower panel. On the basis of the nanometer-scale gaps observed, we have assumed $n = 5$, which corresponds to a $\sim$1 nm long carbon chain. The quality of the fit was not sensitive to the precise value of n, which indicates considerable uncertainty in the value of Γ_1. Nevertheless, the time constants observed are consistent with electonvolt-scale energy barriers.

This model of extending carbon chains coherently and comprehensively accounts for all the experimental observations: the lack of gate dependence on conductance, the $2e^2/h$ conductance steps, as well as the voltage and temperature dependence of waiting time distribution. Taken together, our results strongly suggest that the devices switch by the formation and breaking of chains of carbon atoms; the conductance state of the device therefore changes by the motion of atoms rather than by electric charge.

The device properties of these junctions can be exploited to make logic gates and store information. However, one potential obstacle is the relatively modest ON/OFF ratio, $\sim$50−100, while 10^5−10^6 is typically achieved in CMOS devices. Here we demonstrate a novel concept for a memory cell that we call rank coding.[27] A bit is stored not by the absolute value of the device conductance but by the comparison of the conductance of 2 or more devices in a cell. The information capacity for an N device cell is therefore $\log_2 N!$ bits. Note that for large N, the capacity even exceeds that of a conventional memory cell.

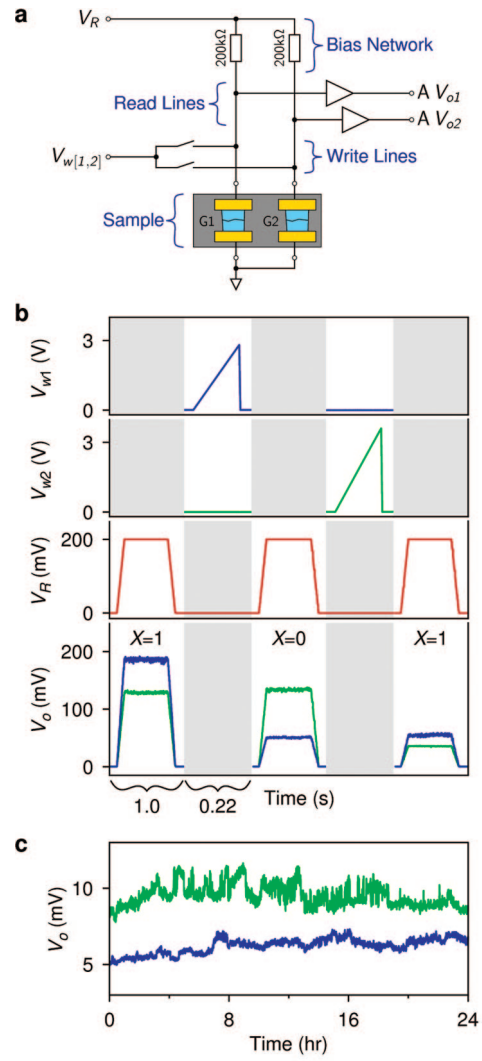

Figure 4. Demonstration of rank coding cell writing and retention time. (a) Schematic diagram for a two-device rank coding cell. (b) First and second panels: Voltage applied to the write line of device G1 and G2, respectively. Third panel: Voltage applied to readout line vs time. Fourth panel: Voltages from the output of device G1 and G2 vs time. The logic state X is indicated above each readout. (c) Conductance vs time over a 24 h period with no write voltages applied.

As a first demonstration of this concept, we have realized a rank coding cell (RCC) using $N = 2$ graphene devices to store one bit. A schematic of the device circuit is shown in Figure 4a. The two graphene devices, G1 and G2, are each connected in series to a 200 kΩ bias resistor. A single readout voltage V_R is applied to both lines in parallel, and two write voltages, V_{w1} and V_{w2}, are applied between the resistors and the devices. The outputs of this RCC are V_{o1} and V_{o2}, which may be sent to a comparator to produce digital logic voltages. Figure 4b shows the operation of the memory cell. The top three panels plot the voltages versus time for V_{w1}, V_{w2}, and V_R, respectively. The bottom panel shows the two voltages read at the output with V_{o1} in blue and V_{o2} in green: if $V_{o1} > V_{o2}$, the output is a logical 1, and zero otherwise. Hence, in the sequence shown, the logic state is switched from 1 to 0 and back to 1 again. In principle, the sequence could be continued indefinitely by applying OFF write pulses to return

G1 and G2 to their original low conductance states and then repeating the cycle shown. The stability of the stored information is demonstrated in Figure 4c, which shows the voltage on the two outputs read continuously for 24 h, without external bias on the write lines. The voltage rank is maintained during the observation time, indicating the stability of the stored bit for extended time periods.

Our work opens the door for a number of directions of future research. Apart from forming the basis for nonvolatile, robust, and CMOS compatible memory devices, reconfigurable circuits, and logic gates, our devices may enable detailed transport studies of individual carbon atomic chains. More generally, we have demonstrated a simple bottom-up way to realize a novel nanoscale system: the graphene nanogap, which may be useful for a variety of scientific studies such as making single molecule transistors[28] or combined transport and scanned probe experiments. Although our graphene switches' writing speed is presently relatively slow (~100 ms), we found dramatic increase in switching speed at elevated temperatures, indicating substantial potential for improvement. Furthermore, the devices could in principle be imprinted in dense arrays that are suitable for read-out by scanned probe arrays,[29] yielding a basis for large-capacity long-term information storage.

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