NANO LETTERS

pubs.acs.org/NanoLett

Graphene Field-Effect Transistors with High On/Off Current Ratio and Large Transport Band Gap at Room Temperature

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ABSTRACT Graphene is considered to be a promising candidate for future nanoelectronics due to its exceptional electronic properties. Unfortunately, the graphene field-effect transistors (FETs) cannot be turned off effectively due to the absence of a band gap, leading to an on/off current ratio typically around 5 in top-gated graphene FETs. On the other hand, theoretical investigations and optical measurements suggest that a band gap up to a few hundred millielectronvolts can be created by the perpendicular E-field in bilayer graphenes. Although previous carrier transport measurements in bilayer graphene transistors did indicate a gate-induced insulating state at temperatures below 1 K, the electrical (or transport) band gap was estimated to be a few millielectronvolts, and the room temperature on/off current ratio in bilayer graphene FETs remains similar to those in single-layer graphene FETs. Here, for the first time, we report an on/off current ratio of around 100 and 2000 at room temperature and 20 K, respectively, in our dual-gate bilayer graphene FETs. We also measured an electrical band gap of >130 and 80 meV at average electric displacements of 2.2 and 1.3 V nm^{-1}, respectively. This demonstration reveals the great potential of bilayer graphene in applications such as digital electronics, pseudospintronics, terahertz technology, and infrared nanophotonics.

KEYWORDS Graphene, field-effect transistors, on/off current ratio, transport band gap, digital electronics

Recently, graphene attracts enormous attention due to its unique electronic properties.[1−3] Creating a band gap in graphene is probably one of the most important and tantalizing research topics in graphene community since it may ultimately enable new applications in digital electronics, pseudospintronics,[4] terahertz technology,[5] and infrared nanophotonics.[6−9] A number of approaches have been proposed or implemented to create a band gap in single or bilayer graphenes already, such as using uniaxial strain,[10,11] graphene−substrate interaction,[12] lateral confinement,[13−17] and breaking the inversion symmetry in bilayer graphenes.[6,18−23] Graphene nanoribbon field-effect transistors exhibit an electrical band gap up to a few hundred millielectronvolts and very large current on/off ratio even at room temperature.[15−17] However, currently there is no reliable method to produce nanoribbons with desirable nanometer scale width. Moreover, carrier mobility in ultranarrow graphene nanoribbons is usually not as high as that in large area graphene.[16]

On the other hand, theoretical investigations predict a sizable band gap opening up to 300 meV in Bernal-stacking bilayer graphene using a perpendicular E-filed to render the A1 and B2 sites (see Figure 1a) nonequivalent.[18−20] Optical measurements did confirm a band gap in bilayer graphenes with broken inversion symmetry.[6,21,23] However, previous carrier transport measurements were not able to find such a large band gap. Therefore, whether a considerable electrical (or transport) band gap exists in biased bilayer graphene remains an unsolved problem in graphene research. In our work, we recognized the importance of preserving the intrinsic properties of bilayer graphene and introduced an important step in the bilayer graphene FET fabrication, which allowed us to observe a large electrical band gap (>130 meV) in biased bilayer graphene.

Figure 1b depicts a three-dimensional schematic view of our dual-gate bilayer graphene transistor, and the layer structure within the channel region of such a device is shown in Figure 1c. The bilayer graphene channel is sandwiched completely between top and bottom gates. The bottom gate SiO_2 film is 300 nm thick. The top gate dielectric stack consists of first 9 ± 3 nm of an organic seed layer made from a derivative of polyhydroxystyrene (the polymer NFC 1400-3CP manufactured by JSR Micro, Inc.) followed by a 10 ± 1 nm film of HfO_2 deposited by atomic layer deposition (ALD). Details of the fabrication processes are presented in the Fabrication of the Dual-Gate Bilayer Graphene FETs section at the end of the main text and in ref 24. This approach to FET fabrication allows us to probe the intrinsic properties of the biased bilayer graphene and to observe a large electrical band gap. The introduction of the organic seed layer before HfO_2 ALD not only facilitates the high-k gate HfO_2 deposition through methyl and hydroxyl groups contained within the polymer on the otherwise inert graphene surface but also preserves the high mobility and intrinsic properties of the active graphene layer by reducing remote phonon and Coulomb scattering.[24]

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Received for review: 11/27/2009
Published on Web: 01/21/2010

DOI: 10.1021/nl9039636 | *Nano Lett.* **2010,** *10,* 715-718

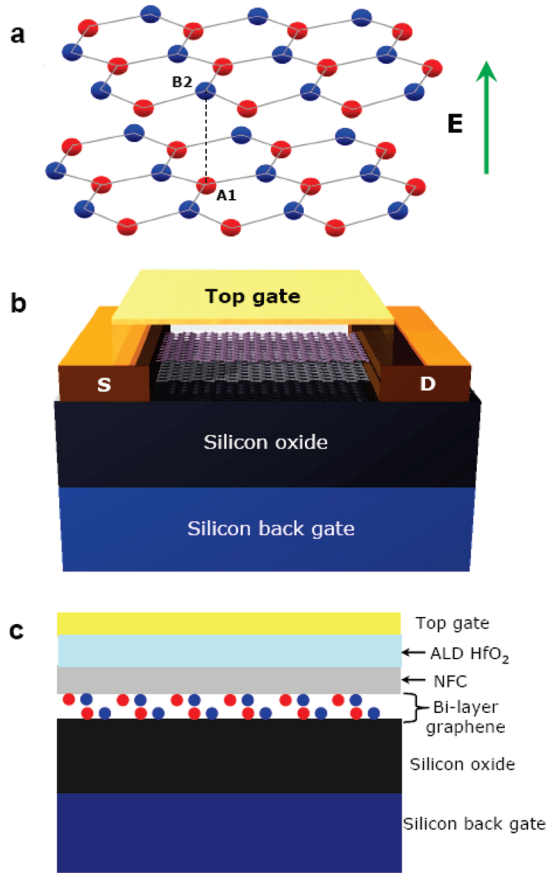

FIGURE 1. Structure of the bilayer graphene FET. (a) A schematic view of bilayer graphene in Bernal stacking. A1 and B2 are equivalent without vertical E field shown by the green arrow; hence the system possess inversion symmetry. This symmetry is broken under E-field. (b) A three-dimensional schematic view of the dual-gate bilayer graphene FET. (c) The layer structure within this bilayer graphene FET channel. From top to bottom are: top metal gate, HfO_2 deposited using ALD, organic polymer NFC 1400-3CP as ALD seeding layer, bilayer graphene, bottom gate oxide, and silicon back gate. Red and blue dots denote carbon atoms. The thickness of the layers is not drawn to scale.

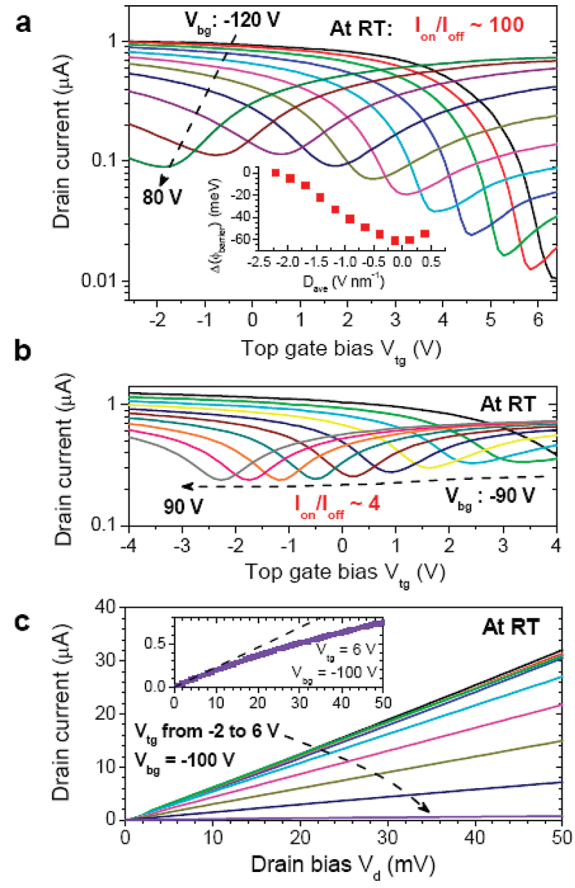

FIGURE 2. Transport characteristics of a bilayer graphene FET at room temperature, (a) The room temperature transfer characteristics of a dual-gate bilayer graphene FET. V_{bg} is varied from −120 to 80 V at steps of 20 V. Inset: variation of the Schottky barrier height, $\Delta(\phi_{barrier})$, as a function of the average electrical displacement, D_{ave}, inferred from the off currents at the charge-neutrality point. (b) The room temperature transfer characteristics of a similar dual-gate, single-layer graphene FET for comparison purpose. V_{bg} is varied from −90 to 90 V at steps of 20 V. In this device, an on/off current ratio of 4 is obtained, 25-fold smaller if compared with that in dual-gate bilayer graphene FET as shown in (a). (c) The room temperature output characteristics of the bilayer graphene FET in (a) at $V_{bg} = -100$ V and V_{tg} from −2 to 6 V. Inset: enlarged view of the output characteristics at $V_{bg} = -100$ V and $V_{tg} = 6$ V. The horizontal and vertical axes are identical to those in the main figure.

We first investigated the switching behavior of our dual-gated bilayer graphene FETs at room temperature. Figure 2a shows the transfer characteristics of a bilayer graphene FET with a channel 1.6 μm wide by 3 μm long. In each curve, the back gate bias (V_{bg}) is fixed and the top gate bias (V_{tg}) is scanned from −2.6 to 6.4 V. V_{bg} is varied from −120 to 80 V at steps of 20 V as shown by the black dashed arrow in Figure 2a. The source is grounded, and a drain bias of 1 mV is applied to the device. Here, both "on" and "off" currents are defined at a specific back gate bias. At different back gate biases, both on and off currents are different. However, we defined the device on/off current ratio to be the maximum current modulation factor possible at the optimum back gate bias (−120 V in this device) when modulating the top gate bias. A minimum off current of around 10 nA is realized at V_{bg} and V_{tg} of −120 and 6.4 V, respectively, as shown by the black curve in Figure 2a, corresponding to a device on/off current ratio of about 100 at room temperature. In comparison, an on/off current ratio of about 4 is observed in a single-layer graphene FET with similar device structure as shown in Figure 2b. Hence the on/off current ratio in our bilayer graphene FET is enhanced by a factor of 25 when compared with that of a single layer graphene FET. Moreover, the decrease of the off-current in our bilayer graphene FET does not seem to cease at V_{bg} and V_{tg} of −120 and 6.4 V, respectively as shown by Figure 2a. Further enhancing the top and back gate biases would result in even smaller off-current. However, in our current devices, this was not possible due to the limited strength of our gate dielectric stacks.

Scanning of the top gate bias not only modulates the doping of the bilayer graphene but also changes the induced band gap.[6,21] In each curve, at the minimum conductance

DOI: 10.1021/nl9039636 | Nano Lett. 2010, 10, 715-718

the graphene sheet is approximately at the charge-neutrality condition. If an appreciable band gap exists at this condition, the off current would be dominated by the thermionic emission of carriers through the metal−graphene Schottky barrier. Hence the off current, I_{off}, would be proportional to $\exp(-q\phi_{barrier}/kT)$, where q is the electron charge, $\phi_{barrier}$ is the Schottky barrier height, k is the Boltzmann constant, and T is the temperature. A maximum Schottky barrier height, $\phi^0_{barrier}$, is attained at the charge-neutrality point when the top and back gate biases are −120 and 6.4 V, respectively. The variation of the Schottky barrier

$$\Delta(\phi_{barrier}) = \phi_{barrier} - \phi^0_{barrier}$$

can be inferred using the off-current at each charge-neutrality condition in each curve. The results are plotted in the inset of Figure 2a as a function of the average electrical displacement, D_{ave}.[6] At the charge-neutrality condition, $D \approx \varepsilon_{SiO_2}(V_{bg} - V_{bg0})/d_{SiO_2}$, where ε_{SiO_2} (∼3.9) is the dielectric constant of the back gate oxide, V_{bg0} is the Dirac offset voltage (50 V in this device), and d_{SiO_2} (300 nm) is the thickness of the back gate oxide. This approach is reliable when the Schottky barrier height is much larger than kT. When the barrier height is smaller or comparable with kT, the off current is no longer limited by thermionic emission but also significantly affected by the metal−graphene contact and graphene channel resistances, leading to a reduced off current. Therefore, the inset of Figure 2a represents a lower limit to the Schottky barrier height created in the bilayer graphene device. We can therefore conclude that in this bilayer graphene, at an average electrical displacement of 2.2 V nm^{-1}, the electrical band gap is >130 meV, assuming the Schottky barrier height is about half of the electrical band gap. At a similar bias condition, the optical measurements indicated an optical band gap of around 200 meV.[6,21]

The room temperature output characteristics of the same bilayer graphene device in Figure 2a are shown in Figure 2c. In this measurement, the back gate bias (V_{bg}) is fixed at −100 V. The top gate bias (V_{tg}) is varied from −2 to 6 V at steps of 1 V. The inset of Figure 2c depicts an enlarged view of the output characteristics at $V_{bg} = -100$ V and $V_{tg} = 6$ V. Current saturation is observed only in this curve, which shows a typical rectifying behavior of a metal−semiconductor junction[25] and implies again an appreciable band gap opening in graphene at this biasing condition. By contrast, other curves in Figure 2c show a completely linear behavior, which is typical for metal-zero-gap-semiconductor (graphene) junctions as reported in many previous publications.

We have also performed transfer characteristic measurements on graphene FETs as a function of temperature. Figure 3a shows the transfer characteristics of another of these devices with a channel geometry 1.2 μm wide by 1.5 μm long at 20 K. V_{bg} is varied from 0 to 120 V at steps of 20 V as shown by the black dashed arrow in the inset of Figure 3a. A device on/off current ratio of about 2000 is achieved at a fixed back gate bias of 120 V as shown by the black curve in Figure 3a. At the minimum conductance ($V_{bg} = 120$ V and $V_{tg} = -3.5$ V), the D_{ave} is 1.3 V nm^{-1} since V_{bg0} in this device is about 20 V. Figure 3b shows the device on/off current ratio measured at 10 different temperatures with off currents all taken at D_{ave} of around 1.3 V nm^{-1}. The improvement in device on/off current ratio at low temperature is due to the reduction in off current. The off current, I_{off}, for thermionic injection is proportional to $\exp(-q\phi_{barrier}/kT)$ as discussed above; thus we may expect that $\ln(I_{on}/I_{off})$ vs $1/T$ would yield a straight line with a slope of $q\phi_{barrier}/k$.[13] In fact, the dashed line in Figure 3b obtained from the on/off ratios from 295 to 100 K leads to a Schottky barrier height of 40 meV, corresponding to a electrical band gap of 80 meV, if we assume the barrier height is about half of the gap. This barrier is smaller than the optical gap of ∼130 meV measured with optical techniques at a similar bias.[6,21] Moreover, we observe that at temperatures below about 100 K, the on/off current ratio does not improve as fast as indicated by the dashed line, most likely due to the presence of tunneling through defect states, i.e., tails in the density of states.[13,26] This phenomenon has been observed in both carbon nanotube[26] and graphene nanoribbon[13] transistors. The optical measurements[6,21] on the other hand reflect the peak in the joint density of states. Therefore, differences in electrical and optical band gaps should not be surprising.

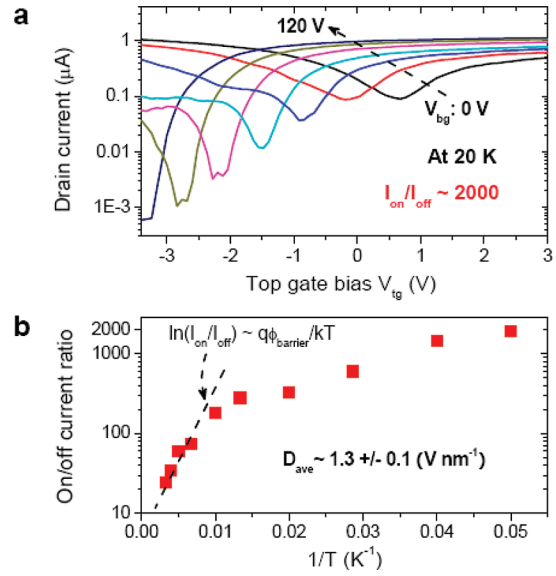

FIGURE 3. Transfer characteristics of a bilayer graphene FET at 10 different temperatures. (a) The transfer characteristics of another bilayer graphene FET at 20 K. (b) The device on/off current ratio vs temperature at D_{ave} of 1.3 V nm^{-1}. The dashed line denotes the estimated on/off ratio vs temperature for a Schottky barrier height of 40 meV, which corresponds to an electrical band gap of 80 meV.

Finally, we note that in our current devices, the large conducting plate (back gate) underneath the bilayer graphene will decrease the operational speed of the device. For realistic applications, local bottom gates should be introduced to minimize such parasitic capacitances. Moreover, the on current of the graphene transistors can be further enhanced by reducing the graphene−metal contact resis-

DOI: 10.1021/nl9039636 | *Nano Lett.* **2010,** *10,* 715-718

tance and optimizing the device geometry. The off current can be further suppressed by improving the overall gate dielectric strength (or overall gate dielectric constant) and the purity of bilayer graphene. Hence, room temperature on/off current ratio of 100 is by no means the upper limit of the graphene FET.

In summary, we demonstrated a bilayer graphene transistor with an on/off current ratio of around 100 at room temperature. The transport measurement indicates a Schottky barrier height >65 meV at D_{ave} of 2.2 V nm^{-1}, corresponding to an electrical (transport) band gap of >130 meV. At 20 K, a device on/off current ratio of about 2000 is demonstrated at D_{ave} of 1.3 V nm^{-1}. Revealing of the large electrical band gap in bilayer graphene may enable a number of novel nanoelectronic and nanophotonic applications.

Fabrication of the Dual-Gate Bilayer Graphene FETs. The fabrication steps of the dual-gate bilayer graphene field effect transistor (FET) are described as follows:

1. Identification of bilayer graphene flakes using optical approach and Raman spectroscopy. The bilayer graphene flakes in this experiment were purchased from Graphene Industries, Inc.

2. First e-beam lithography and source/drain metallization (Ti/Pd/Au/Ti: 0.5/20/20/5 nm).

3. Second e-beam lithography and patterning of the bilayer graphene channel.

4. Spin coating of the organic seed layer made from a derivative of polyhydroxystyrene (the polymer NFC 1400-3CP manufactured by JSR Micro, Inc.) for atomic layer deposition (ALD). The layer thickness can be adjusted by spin speed. The dielectric constant of this material is about 2.5.[24]

5. Atomic layer deposition of top gate oxide (HfO_2) at $T <$ 200 °C.

6. Third e-beam lithography and top gate metallization (Ti/Au: 5/25 nm).

Poly(methyl methacrylate) (PMMA) was used as the e-beam resist in all the processing steps mentioned above. Removal of PMMA was realized using acetone and usually was followed by isopropanol rinse. No specific surface cleaning steps were involved in the processing.

Acknowledgment. The authors are grateful to B. Ek and J. Bucchignano for help in technical assistance. F.X. is indebted to C. Y. Sung for his encouragement.

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DOI: 10.1021/nl9039636 | *Nano Lett.* **2010,** *10,* 715-718