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ARTICLE *in* JOURNAL OF APPLIED PHYSICS · MAY 2001

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Probing diffusion barrier integrity on porous silica low-*k* thin films using positron annihilation lifetime spectroscopy

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(Received 13 November 2000; accepted for publication 6 February 2001)

The technique of positron annihilation lifetime spectroscopy (PALS) has been used to investigate the continuity and thermal stability of thin barrier layers designed to prevent Cu atom diffusion into porous silica, low-dielectric constant (*k*) films. Nanoglass™ K2.2-A10C (A10C), a porous organosilicate film, is determined to have interconnected pores with an average tubular-pore diameter of (6.9 ± 0.4) nm. Cu deposited directly on the A10C films is observed to diffuse into the porous structure. The minimum necessary barrier thickness for stable continuity of Ta and TaN layers deposited on A10C is determined by detecting the signal of positronium (Ps) escaping into vacuum. It is found that the 25 nm thick layers do not form continuous barriers. This is confirmed by the presence of holes observed in such films using a transmission electron microscope. Although 35 nm and 45 nm Ta and TaN layers perform effectively at room temperature as Ps barriers, only the Ta-capped samples are able to withstand heat treatments up to 500 °C without breakdown or penetration into the porous film. TaN interdiffusion into the silica pores is indicated by the reduction of the Ps lifetime after high annealing temperatures. The validity of using Ps diffusion to test barrier layers designed to inhibit Cu diffusion is discussed. The procedures to standardize the testing of barrier layer integrity and thermal stability using PALS are proposed. Extension to probing barrier layers in realistic vias and trenches should be straightforward. © *2001 American Institute of Physics.* [DOI: 10.1063/1.1360704]

I. INTRODUCTION

As the feature size of integrated circuits continues to shrink below 0.18 μm, the interconnect RC (wire resistance *R* and capacitance *C*) delay becomes the major factor limiting the device performance.[1] The need to introduce advanced interconnect and dielectric materials becomes essential to limit the number of metal levels and die size, and reduce the RC delay in ultralarge-scale integrated circuits. Cu technology has been developed to replace aluminum as interconnect lines since it can lower the resistance and improve the electromigration reliability. In addition, materials with low dielectric constant (*k*) are being extensively investigated as interlayer dielectric (ILD) to reduce the capacitance. Lowering the density by increasing the free volume and/or by introducing porosity is the dominant strategy as the microelectronics industry targets to achieve future-generation ultralow-*k* (*k* less than 2.2) ILD materials. The promising porous dielectric candidates[2] mainly include porous silica, porous silsesquioxane, and porous polymers.

The integration of Cu with porous, low-*k* ILDs has attracted significant interest since the combination will lead to additional performance improvement and potential cost reduction using the recently developed damascene fabrication process. However, the successful integration of Cu /low-*k* systems is very challenging. Cu is known to have high diffusivity in silica, and thus it is necessary to isolate the Cu interconnect lines from the surrounding ILDs by thin, low diffusivity barrier layers. Refractory metals and their compounds, such as Ta and TaN, have recently drawn attention as candidates for barrier materials. Many studies have investigated the barrier reliability between Cu and silica,[3,4] polymer,[4–6] or Si.[7] Unfortunately, there is little work on the study of actual barrier layer performance (layer continuity and thermal stability) on porous low-*k* dielectrics.[8]

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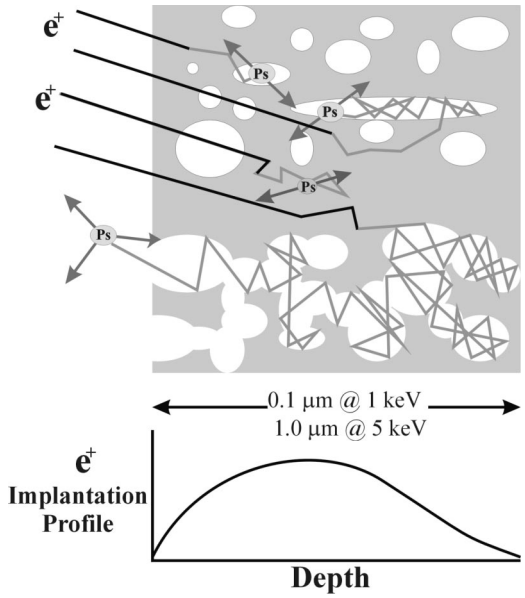

FIG. 1. Positronium behavior in two types of porous materials; (upper) closed pores, and (lower) connected pores. The shape of a typical positron implantation profile is depicted in the bottom panel.

The porous structure of the ultralow-*k* dielectrics definitely highlights the necessity of barrier layers, especially in highly interconnected pore networks such as that detected in porous silica,[9–11] since metal diffusion could be more pronounced. To perform effectively, the barrier layers must at least be continuous (no pinholes) in order to prevent Cu interdiffusion. In addition, they are required to be thin enough to retain the advantage of low effective resistance. Hence, determining the minimum ''critical'' barrier layer thickness is essential to optimize device performance and reliability. In this article, beam-positron annihilation lifetime spectroscopy (PALS), a promising tool for studying the void volumes in thin insulating films,[9,12–14] is used to investigate the pore structure and the barrier layer integrity of porous silica film.

In using PALS with thin films, a focussed beam of several keV positrons forms positronium (Ps, the electron bound state with its antiparticle, the positron) over a distribution of depths that depends on the beam energy as indicated in the lower panel of Fig. 1. Ps inherently localizes in the pores where its vacuum lifetime about 140 ns is reduced by annihilation with bound electrons during collisions with the pore surfaces. The collisionally reduced Ps lifetime is correlated with void size,[9,15–19] thus forming the basis of the PALS technique. It is sensitive to pore diameters in the range of 0.1 to 100 nm.

The behavior of Ps in porous media is illustrated in Fig. 1 and depends on the pore morphology. After being implanted, a positron will begin to thermalize and can capture an electron to form Ps within the film.[12] The Ps tends to localize in voids where its binding energy is not reduced by the dielectric constant of the solid. If the pores are closed (as depicted in the upper part of Fig. 1), then Ps should be trapped in a pore with no further diffusion occurring. A distribution of Ps lifetimes may result if there is a distribution of pore sizes.[14,18] Indeed, the technique of deconvolving a pore-size distribution from a Ps lifetime distribution has been developed for porous methylsilsesquioxane samples.[18] In interconnected pores, instead of being trapped in one pore, Ps may diffuse throughout the pore network over distances that can be much larger than the film thickness as illustrated in Fig. 1. As a result, Ps can easily diffuse out of the film and into the surrounding vacuum and annihilate with the vacuum lifetime (~140 ns), producing an unusually high intensity of this component.[9] This observable feature enables PALS to determine the pore interconnectivity and to probe barrier layer integrity.[19] An effective capping layer/diffusion barrier will prevent Ps from diffusing into the vacuum, thereby enabling the measurement of an *average* pore size[9,19] corresponding to the observation of a single, *average* lifetime of Ps diffusing within the porous network.

In this work, we focus on using PALS to probe the continuity and thermal stability of diffusion barrier layers on porous silica films. The minimum critical thicknesses of Ta and TaN barrier layers are determined, and the thermal stability of such barriers is studied. The films utilized are mainly blanket (featureless) samples with barriers deposited uniformly on the top surface of the low-*k* dielectrics. However, one patterned sample was analyzed to check its barrier layer effectiveness in an actual integrated circuit test vehicle fabricated using copper damascene technology. In patterned circuits, the ability to achieve the uniformity and continuity of barrier layers on trench sidewalls is made difficult by a combination of outgassing problems, subquarter micron trenches and vias with high aspect ratios, and surface roughness along the etched sidewall of the porous low-*k* film. We will discuss the feasibility of extending the PALS technique to directly probing the sidewall continuity of patterned samples and propose a standardized PALS testing procedure to define barrier layer integrity and thermal stability.

II. EXPERIMENTAL METHODS

The particular low-*k* ILD examined is a porous silica film, Nanoglass A10C (400 nm), on a silicon substrate, supplied by SEMATECH. One film was capped with 100 nm of silicon oxide to permit the measurement of average pore size in A10C films. This thick, oxide-capped film also served as a control sample for the tests' diffusion barrier integrity and thermal stability. Another sample with 27.5 nm of Cu deposited on top of A10C was used for the purpose of verifying Cu interdiffusion. A Novellus Systems Inova physical vapor deposition system was used for the deposition of all films on the porous silica.

Beam-PALS experiments were performed on the oxide- and Cu-capped samples at room temperature and the spectra are plotted in Fig. 2 along with that of an uncapped A10C film for comparison. The uncapped sample has a fitted Ps lifetime very near the vacuum value of 140 ns and a relative Ps intensity around 35% (i.e., 35% of the positrons form long-lived Ps). This indicates that the porosity is highly *interconnected* and effectively all the Ps formed in the dielectric film is able to diffuse into the surrounding vacuum and annihilate with the vacuum lifetime. With 100 nm of oxide blocking the diffusive escape of Ps this oxide-capped sample

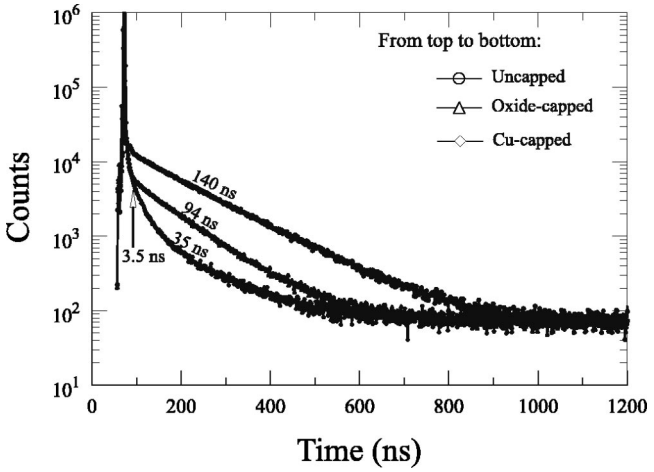

FIG. 2. PALS spectra of uncapped, 100 nm oxide-capped, and 27.5 nm Cu-capped Nanoglass A10C silica films. Two Ps lifetimes, 3.5 ns and 35 ns, are fitted for the Cu-capped film.

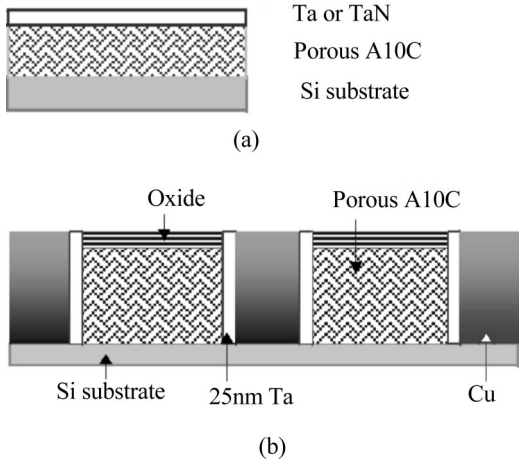

FIG. 3. Sample configuration for barrier layer integrity test; (a) represents the blanket sample and (b) represents the patterned sample.

presents a spectrum consisting of only one intermediate Ps lifetime component with average lifetime of (94 ± 2) ns. This indicates that the highly mobile Ps atoms all sample the same average pore dimension in the *interconnected* voids of porous silica films.[9] This value is considered to be the *inherent* lifetime of Ps *confined* to A10C silica film. The mean free path corresponding to this lifetime is determined to be (6.9 ± 4) nm, which then corresponds to the diameter of a long, cylindrical pore (see Refs. 9 and 19 for details).

The Cu-capped A10C film, however, presents two Ps lifetime components of 35 ns and 3.5 ns instead of the single 94 ns component, which suggests that all the Ps formed has faster collisional wall annihilation than expected. This reduction of the Ps lifetime must almost certainly be due to Cu metal coating on the inner pore surfaces where Ps annihilation would be enhanced by the high density of free electrons in Cu. Some of the pores are apparently closed off by large-scale Cu interdiffusion during the deposition process and present a very short, trapped-Ps lifetime of only 3.5 ns. On the other hand, some deeper-lying pores may have thinly diffused metal in them and are still interconnected to the remainder of the pure porous silica. Ps can diffuse back and forth between this region of high annihilation and normal, uncoated A10C and produce, on average, a shortened lifetime of 35 ns. Thus, the interface between the Cu-capping layer and the porous silica does not appear to be sharply defined. There appears to be significant Cu metal interdiffusion into the silica pore surfaces. These results are not surprising as the need for diffusion barriers with Cu metalization on porous silica is an accepted fact.

As discussed, Cu easily diffuses into the porous silica structure and its presence is readily observed in PALS spectra. We can detect similar phenomena in Al-capped porous silica films depending on the deposition process.[19] Therefore, it is crucial to have diffusion barriers between metals and porous silica low-*k* ILDs. The question then to be addressed is: what is the minimum thickness required of a barrier layer in order to prevent Cu diffusion over a range of elevated temperatures encountered in device processing? To assess the performance of several candidate materials, we have studied a series of Ta- and TaN-capped A10C films deposited on silicon substrates (Fig. 3). The thicknesses of the capping layers tested are 25, 35, and 45 nm for each of the two barrier materials. PALS spectra were collected at room temperature and the films were depth profiled by changing the positron beam implantation energy from 1.1 to 6.0 keV. The samples that are determined to have a continuous barrier layer at room temperature were thermally annealed for 1 h in the high vacuum system at progressively elevated temperatures up to 500 °C. PALS spectra were acquired after the samples cooled down back to room temperature to investigate the thermal stability of the barrier. A transmission electron microscope (TEM) was used to study the continuity of the 25 nm Ta-capped A10C film and the heated (500 °C) 45 nm Ta-capped A10C. A specially prepared patterned sample [see illustration in Fig. 3(b)] with a 25 nm Ta barrier between porous silica A10C and Cu lines was examined by PALS and TEM. An optical microscope was used to check the surface of the samples.

III. RESULTS AND DISCUSSION

A. Minimum barrier thickness

A simple method to directly probe the continuity of barrier layers is illustrated in the top panel of Fig. 4. Positrons are injected into the dielectric film and form Ps that diffuses rapidly throughout the interconnected pores. Despite *many* collisions with the barrier, a continuous overlayer should prevent Ps from escaping into vacuum. Hence, detection of Ps in vacuum through its telltale 140 ns vacuum lifetime clearly indicates leakage through pinholes or discontinuities in the barrier. In so doing, one must also account for a second source of Ps in vacuum related to positrons backscattering from the incident beam. Whenever a positron beam impinges on a surface, backscattered positrons will form vacuum Ps by electron capture near the surface.[20] The intensity of this so-called backscattered Ps component depends on the implantation energy (E), empirically found to be an inverse relationship with E. This ubiquitous systematic effect can be effectively removed by depth profiling through the

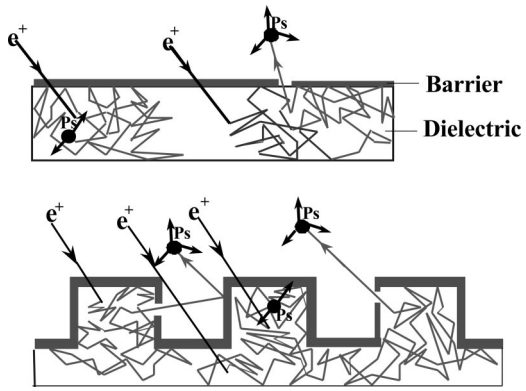

FIG. 4. Illustration of Ps diffusion barrier testing in blanket (upper) and patterned (lower) samples. The patterned sample has trenches but they are not filled with Cu.

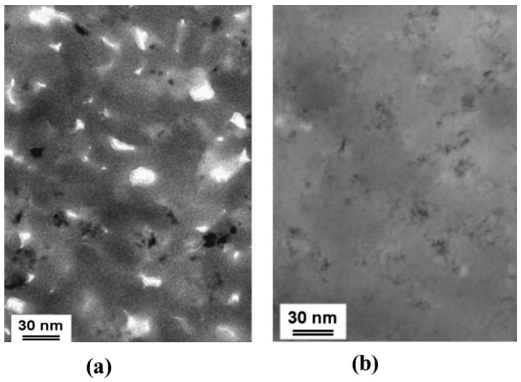

FIG. 6. TEM images of (a) 25 nm, (b) 45 nm Ta (annealed at 500 °C for 1 h) on A10C.

sample and these results are shown for all six barrier layers in Fig. 5. The intensity of Ps detected in vacuum at low beam energies are all similar since all the positrons implant in the barrier layer (see Fig. 1) and the intensity of the 140 ns component is entirely due to backscattered Ps. At high beam implantation energies, however, Fig. 5 shows the clear trend that far too much Ps is escaping into vacuum from the two films with 25 nm thick barriers. Backscattered Ps, as shown in thicker films, cannot account for such high intensities. (The reduced intensity of Ps in vacuum for the thicker barriers in Fig. 5 is not the result of low Ps formation in the dielectric. The majority of beam positrons can penetrate the thicker barriers and form Ps in the porous silica.) Our only explanation is that the 25 nm barriers on A10C do not form a continuous layer so that some of the Ps formed in the film is able to diffuse out through barrier imperfections into the vacuum system, as illustrated in Fig. 4.

How imperfect is the 25 nm barrier? With a mean free path (pore diameter) of $\sim$ 7 nm and a typical Ps lifetime within the pores of $\sim$ 80 ns, thermal Ps can make about a million collisions with the pore walls and hence make many attempts to probe the barrier layer. With a diffusion length on the order of several microns, Ps can therefore probe a lateral region across the barrier of roughly 1 μm. Nominally, one open 7 nm diameter pore in this 1 μm diameter region (an area ratio of 5×10^{-5}) would permit roughly 50% of the diffusing Ps to escape. We crudely estimate this to be the case for 25 nm TaN barrier (see Fig. 5) whereas the 25 nm Ta barrier displays nearly 100% escape into vacuum. Although we cannot determine the degree of discontinuity in the 25 nm Ta films, it may indeed be so small as to be challenging to detect with other techniques. In this case, we took this particular sample and carefully milled down the supporting wafer to permit TEM analysis. The TEM results in Fig. 6(a) clearly show the presence of numerous pinholes, which indicates that 25 nm Ta does not form a continuous barrier layer on A10C and thus cannot perform effectively in preventing Ps leakage into vacuum. The TEM image substantiates the PALS interpretation.

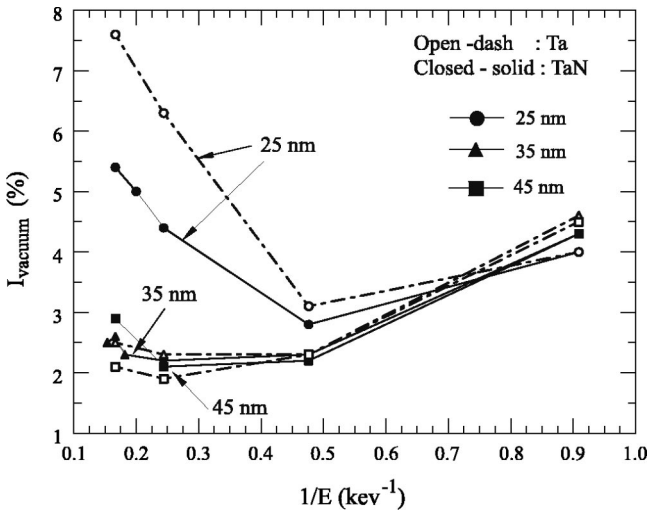

FIG. 5. Intensity of Ps vacuum component in Ta and TaN-capped Nanoglass A10C silica samples.

The results for 35 nm and 45 nm Ta- and TaN-capped samples are substantially similar to each other. The similarity of these two sets of films in Fig. 5 underscores the difference of the 25 nm films. If both barrier materials at all three thicknesses were completely continuous then Fig. 5 would simply be a measure of backscattered Ps and all six curves would be the same. Clearly, the 25 nm curves are very different. The thicker Ta and TaN capping layers (35 nm and 45 nm) seem to form a continuous Ps barrier, however, the fitted lifetime is still slightly lower than expected, about 72–80 ns rather than 94 ns. This might be significant if this shortened Ps lifetime indicates that there is significant metal interdiffused into the silica from the barrier deposition process. Such a possibility is suggested in a TEM micrograph on A10B (an earlier generation of A10C and quite similar under PALS analysis) as shown in Fig. 7. The blurring of the interface between the dielectric and a Ta barrier layer in the micrograph indicates interdiffusion of either the barrier material or Cu from the trench. The shortened Ps lifetime could instead be an indication of trapped or adsorbed pore contaminants generated during the layer deposition process. Thus, an emerging issue from these studies is that one needs to untangle possible contamination effects in the barrier deposition process from subsequent metal interdiffusion effects; both of which could produce shortened Ps lifetimes in the capped sample. Prior to any heat treatment, we conclude that

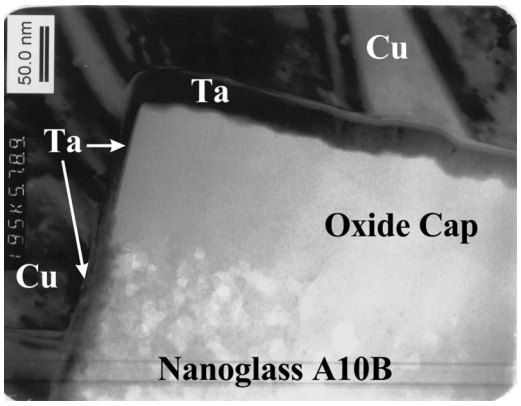

FIG. 7. A TEM image of Cu-filled 350 nm trench in A10B. This image shows the Ta barrier layer and the oxide hardmask at the top of the trench.

35 nm Ta or TaN is able to perform effectively as a continuous barrier on A10C and the minimum critical thickness is greater than 25 nm using the current SEMATECH deposition process. This result does not seem unreasonable given the 7 nm pore size of A10C coupled with a nominal dielectric film surface roughness of comparable size scale.

B. Thermal stability

The Ta and TaN barriers with thickness of 35 nm and 45 nm are found to be continuous barrier layers at room temperature. These samples, as well as the oxide-capped control sample, were then progressively annealed in vacuum up to 500 °C in order to test their thermal stability. The PALS temperature-dependent results for the lifetimes of the Ps trapped and annihilating in the mesopores are plotted in Fig. 8. The intensity of the escaping 140 ns Ps vacuum component is plotted in Fig. 9. This component is the sum of any Ps escaping through the barrier plus the ever-present Ps formed by backscattered positrons from the incident beam.

As can be seen from Fig. 8, oxide-capped A10C stays thermally stable at all temperatures through 500 °C. The fitted lifetime is stable around 90 ns and the intensity of trapped Ps is found to slightly increase with heat treatment. This sample acts as a control sample in that it indicates that

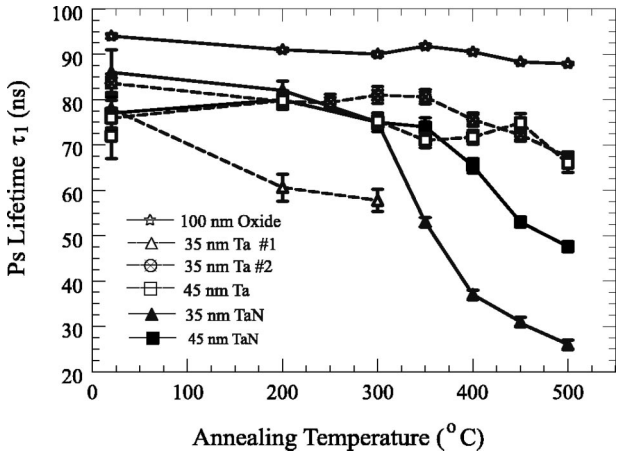

FIG. 8. The lifetimes of Ps annihilating in the pores of annealed Ta- or TaN-capped A10C films.

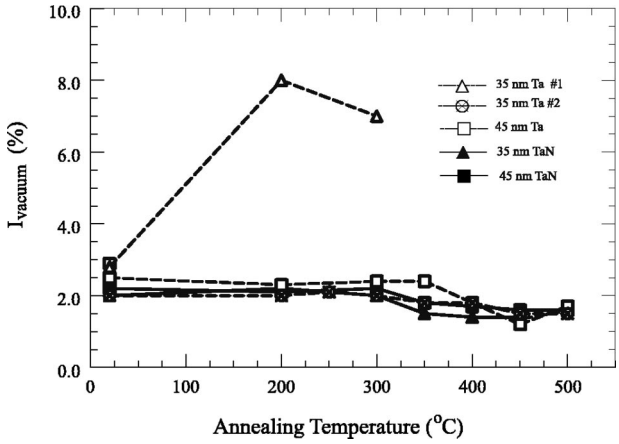

FIG. 9. The intensity of Ps escaping into vacuum after thermal annealing. The first 35 nm Ta-capped sample clearly has too much Ps annihilation in vacuum.

nothing fundamental happens to the pore morphology of the A10C film up through temperatures of 500 °C.

The 35 nm and 45 nm TaN barrier layers remain continuous even after annealing to 500 °C since no Ps leakage through the barriers is observed during the whole process (as indicated by the low intensity of the Ps vacuum component in Fig. 9). However, the Ps lifetime (and to a lesser extent the intensity of this trapped Ps) in the mesopores started to decrease at 350 °C as shown in Fig. 8. The lifetime drop above 350 °C is particularly sharp, even though this occurs with no breakdown of capping effectiveness. Something is promoting annihilation of Ps in the porous silica after elevated heat treatment temperatures and the best explanation would be that something is interdiffusing into the pores of the A10C. One possible explanation is that TaN, or a contaminant, is thermally activated to interdiffuse into the mesopores, which results in the shortened Ps lifetime and reduced intensity. This property of releasing an interdiffusing species into the pores seems to be specific to TaN barriers as we do not see this effect in films with Ta barriers, as discussed in the following session.

Results on the Ta-capped films are quite different. Two samples of 35 nm Ta-capped films were studied. The first sample failed as a Ps barrier layer after heating only to 200 °C, as indicated by the high intensity of Ps escaping into vacuum as shown in Fig. 9. However, we found that the surface at the center of this sample became *visibly* very rough after the thermal treatment, as can be seen in Fig. 10, in contrast to the visibly much smoother surface before it was put into the vacuum system. A region of about 2 mm wide full of visible, tiny cracks was observed near the sample center, where the beam was implanted. There is little doubt that this rough surface with visible cracking produced the observed Ps leakage. Systematic tests have eliminated the possibility that the positron beam irradiation and the vacuum exposure caused such damage.[21] The damage to the sample, which might be due to existence of impurities, stress mismatch, or mechanical damage triggered by the heat treatment, is believed to be associated with the observed Ps results, suggesting the films are still quite fragile. To further

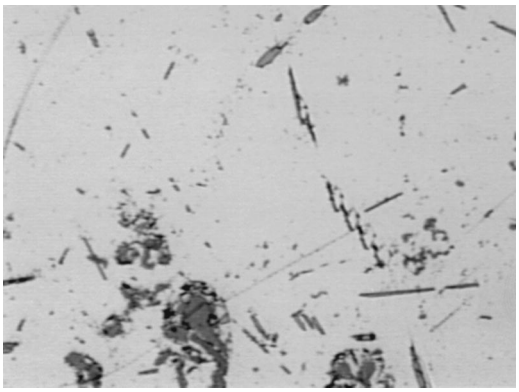

FIG. 10. Optical microscope image of surface of the 35 nm Ta-capped A10C after annealing at 300 °C for 1 h.

test our interpretation, we studied a second sample cut from the same wafer, with 35 nm Ta on the top of A10C. This second sample was found to retain its diffusion barrier property through 500 °C and shows only the slightest hint of a Ps lifetime decrease at the highest temperature of 500 °C (Fig. 8). The sample retained its smooth, undamaged appearance after PALS analysis. These results indicate that PALS can be very sensitive to changes in the barrier integrity. The 45 nm Ta capping layer shows results similar to that of the second 35 nm Ta barrier layer, being able to survive high temperature annealing. The continuity of this sample was also confirmed by TEM analysis after milling down of the supporting wafer [see Fig. 6(b)]. Thus, the TEM micrographs in Fig. 6 confirm the PALS analysis that a 25 nm barrier on A10C is too thin to be continuous and that the heated 45 nm barrier is indeed continuous. We conclude that of all the barriers studied, *the 35 nm and the 45 nm Ta-capped* A10C films are stable and benign throughout the full range of heat treatment temperature. 25 nm of either material is below the minimum critical barrier thickness and the TaN films (35–45 nm) strongly curtailed the Ps lifetime at heat treatment temperature above 300–350 °C due to penetration into the pores of something from the barrier materials.

C. Ps diffusion and Cu diffusion

In this study, we have used PALS to determine barrier layer integrity based on Ps diffusion. How indicative then is Ps diffusion of Cu diffusion? Indeed, we have observed that Cu diffusion and Ps diffusion are correlated in a patterned sample (Fig. 3) that had 25 nm of Ta deposited onto the sidewalls of Cu-filled trenches in A10C. PALS results show a reduced Ps lifetime of only 65 ns (instead of 94 ns) in the dielectric, which is consistent with TEM results[22] that show that Cu interdiffusion does occur in this sample. This result had been correctly predicted by the PALS analysis of blanket films in showing that 25 nm Ta does not form a continuous barrier layer. Thus, *in general*, will the failure of a barrier layer in preventing Ps diffusion definitely forecast breakdown for Cu diffusion? We can address this issue by comparing Ps and Cu in several ways. First, Ps is a bound state of a positron - electron pair, similar to the hydrogen atom except it is about a thousand times lighter. The radius of Ps particle is about 0.5 A, slightly smaller than that of a Cu atom (1.3 A). However, it has at most only 140 ns to diffuse through the barrier layers, while Cu atoms have effectively infinite time to diffuse. Moreover, within the electric field of the application environment, the Cu atoms could lose electrons and exist in the ionic form. The drift of Cu ions with reduced size (0.9 A) will be facilitated by bias voltage and temperature, which has not been considered in the Ps diffusion test at all. Therefore, it is very likely that the small pinholes in the barrier that permit Ps diffusive escape could also allow Cu atoms or ions to penetrate into the dielectric. Thus, it is presumably safe to assert that it should be *necessary* for a candidate diffusion barrier to pass the Ps testing phase. On the other hand, passing such tests may not be *sufficient* to fully certify a material as a Cu diffusion barrier since there may be specific effects such as grain boundary diffusion that Ps is not sensitive to. To absolutely determine the barrier layer integrity, we need to combine PALS with some other techniques, such as bias-temperature stress and electrical properties test. Compared to other techniques, PALS should allow one to quickly narrow the field of candidate materials and barrier thicknesses in order to facilitate direct testing of Cu diffusion.

D. Standard test procedure

Once we better understand how representative Ps diffusion is of Cu diffusion, the failure of diffusion barriers in such Ps tests may be sufficient to rule out the possibility of candidate barriers in preventing Cu diffusion. Indeed, the existence of numerous combinations of low-*k* candidates and barrier materials highlight the need for a simple technique capable of quickly narrowing down the possible combinations of barrier/thickness/processing and enable barrier deposition process optimization. Our studies on barrier integrity have successfully demonstrated the ability of PALS to detect the diffusion barrier integrity so far as Ps diffusion is concerned. The test procedures utilized herein can be *standardized*. To qualify as a diffusion barrier for Ps, a candidate barrier layer must not allow any Ps to escape through it into the vacuum (escape is readily manifested by a 140 ns component in the fitted PALS spectrum). An elevated temperature at which the barrier-dielectric combination must be able to withstand prolonged exposure can be selected. Beam-PALS spectra will be acquired before the annealing and after the sample has cooled to room temperature. To pass the Ps diffusion test, firstly, there must be no indication before or after heat treatment of any Ps breaching/diffusing through the barrier. This is easily determined by the intensity of the Ps vacuum component in the fitted PALS spectrum as demonstrated in Figs. 5 and 9. Secondly, there must be no significant change in the fitted Ps lifetime in the dielectric's mesopores, an indication that the diffusion barrier material has not contaminated the porous film in any way.

This testing can be performed quickly if one is only interested in whether a barrier can pass inspection at one temperature. We methodically investigated herein the *onset* of capping failure in the Ta and TaN layers, but only two spectra are really needed: one at room temperature and one

after the specified heat treatment. With this testing procedure, we can quickly determine the minimum critical thickness for a particular diffusion barrier on a particular low-*k* film. This approach should be most useful in future research on advanced barrier materials for use on ultralow-*k* films.

E. Extension to testing deposition methods on real trenches

A more realistic test of the efficacy of a diffusion barrier is to test its barrier properties after deposition into the trenches of a patterned low-*k* sample device. This test is illustrated in the lower panel of Fig. 4. PALS on patterned samples are no more difficult to perform than on the blanket films used in this study. In fact, comparison of a *patterned* test sample with that of a *blanket* sample will distinguish whether any observed breakdown is occurring at the trench sidewalls or at the horizontal surfaces. This could be an important diagnostic research tool in setting up the necessary deposition technique and/or it simply becomes a part of the standardized testing procedure, namely the two criteria above must be met for a specifically patterned low-*k* material with diffusion barrier deposited therein.

IV. CONCLUSION

PALS is a unique method for characterizing the underlying pore structure and studying the effectiveness of barrier layers on interconnected porous low-*k* thin films. It is sensitive to Cu metal interdiffusion as indicated by the reduction of Ps lifetime. The barrier integrity is determined by the Ps vacuum annihilation signal. It has been found that layers of 25 nm Ta and TaN deposited using the SEMATECH baseline deposition process do not form continuous barrier layers on Nanoglass A10C films and result in both Ps diffusion and Cu diffusion leakage on Nanoglass A10C film. The minimum critical thickness for Ta and TaN barriers is determined to be between 25 and 35 nm. TaN films fail as barrier layers after thermal annealing above 300 °C since TaN outgassing or diffusion into the mesopores was observed. A 35 nm Ta layer remains to be a continuous barrier after thermal annealing up to 500 °C without breakdown or penetration. This study demonstrates that PALS is capable of exploring Ps diffusion through candidate barrier layers and thus probing Cu interdiffusion as well. This establishes the possibility of using a standardized PALS technique to quickly narrow down the potential field of candidate barrier material/thickness/processing combinations. Extension of this technique to probe patterned samples with realistic trenches or vias to address the attendant problems associated with trench/via sidewall deposition appears to be straightforward.

ACKNOWLEDGMENTS

The authors would like to thank Huagen Peng and other members of the Michigan Positron Group for helpful discussions. This research is supported by the National Science Foundation and by the Low-K Dielectrics Program at SEMATECH.

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