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Electrically Controlled Giant Piezoresistance in Silicon Nanowires

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ABSTRACT Herein we demonstrate giant piezoresistance in silicon nanowires (NWs) by the modulation of an electric field-induced with an external electrical bias. Positive bias for a p-type device (negative for an n-type) partially depleted the NWs forming a pinch-off region, which resembled a funnel through which the electrical current squeezed. This region determined the total current flowing through the NWs. In this report, we combined the electrical biasing with the application of mechanical stress, which impacts the charge carriers' concentration, to achieve an electrically controlled giant piezoresistance in nanowires. This phenomenon was used to create a stress-gated field-effect transistor, exhibiting a maximum gauge factor of 5000, 2 orders of magnitude increase over bulk value. Giant piezoresistance can be tailored to create highly sensitive mechanical sensors operating in a discrete mode such as nanoelectromechanical switches.

KEYWORDS Giant piezoresistivity, silicon nanowires, electromechanical property

Nanomaterials offer considerable opportunities due to their exceptional physical properties.[1,2] For example, carbon nanotubes show the highest Young's modulus known so far.[3] Semiconductor nanowires have also attracted significant research efforts and were found to have very unusual thermoelectric[4,5] and electromechanical properties.[6,7] As with these unique features, giant piezoresistance is only known to arise in nanostructured materials. It is caused by carrier depletion within the semiconductor due to mechanical stress.[8] Here we show that the carrier depletion can be modulated electrically enabling the control of the giant piezoresistive effect in NWs.

To investigate piezoresistive properties as a function of transverse electric field, we have designed and fabricated silicon dioxide (SiO_2) cantilevers with embedded silicon NWs above an electrically conductive substrate (see Figure 1a,b). The electromechanical characterization of NWs has always been a challenging task due to their small dimensions.[9] They are typically measured in conjunction with direct force loading by an atomic force microscope (AFM)[10,11] or indirectly by a bulge test[12] or four-point bending.[6,7,13] As long as the NWs are naked with their surface unprotected, direct AFM contact or environment can modify their surface properties and thus influence the measurement.[2,6] Embedding the nanowires within the cantilever eliminated this problem. Specific stress profiles were induced in the NWs by poking the free end of the cantilever with a nanoindentation stylus. This platform enabled to measure the electrical conductance of the NWs under controlled mechanical load while modulating the transverse electric field.

The NWs were fabricated using conventional integrated circuit technology with silicon-on-insulator (SOI) wafers as starting substrates. Silicon nanowires (NWs) oriented in the ⟨110⟩ direction with a width of 100 nm and a length of 5 μm were lithographically defined on 200 mm silicon-on-insulator (SOI) wafers with 100 nm thick top silicon and 145 nm thick buried SiO_2.[14] Once the silicon layer was patterned, the NW line width was trimmed by oxidation. Subsequently the NWs were doped by ion implantation of BF_2^+ at 1×10^{12} ion/cm^2. The silicon was covered with 0.5 μm thick SiO_2 layer deposited by plasma-enhanced chemical vapor deposition (PECVD). Contact holes were opened, implanted with BF_2^+ at 1×10^{15} ion/cm^2 to form nonrectifying contacts. After impurities activation by rapid thermal processing (RTP), an Al4 % Cu1 % Si layer was sputtered, patterned, and sintered in a forming gas (5 % H_2 in N_2) for 20 min at 450 °C to provide electrical connection between the NWs and the bonding pads. Eighteen micrometers deep and 1 μm wide trenches were etched into the silicon substrate to form mechanical stiffeners. A second layer of PECVD SiO_2 was deposited to fill the trenches and provide a passivation of the aluminum layer. Microcantilevers 8 μm wide, 2.6 μm thick, and 80 μm long were defined with the NWs located next to the cantilever anchor. A pair of NWs was located close to the cantilever bottom, (1.2 μm from the neutral axis of the cantilever) to maximize the stress amplitude on the nanostructures. As a last step, the cantilevers were released by removing the silicon substrate underneath by XeF_2 vapor (see Figure 1b). The transmission electron microscope (TEM) image of a NW cross-section illustrates its dimension of 100 $\times$ 100 nm^2 (see inset in Figure 1b). The NW is sandwiched

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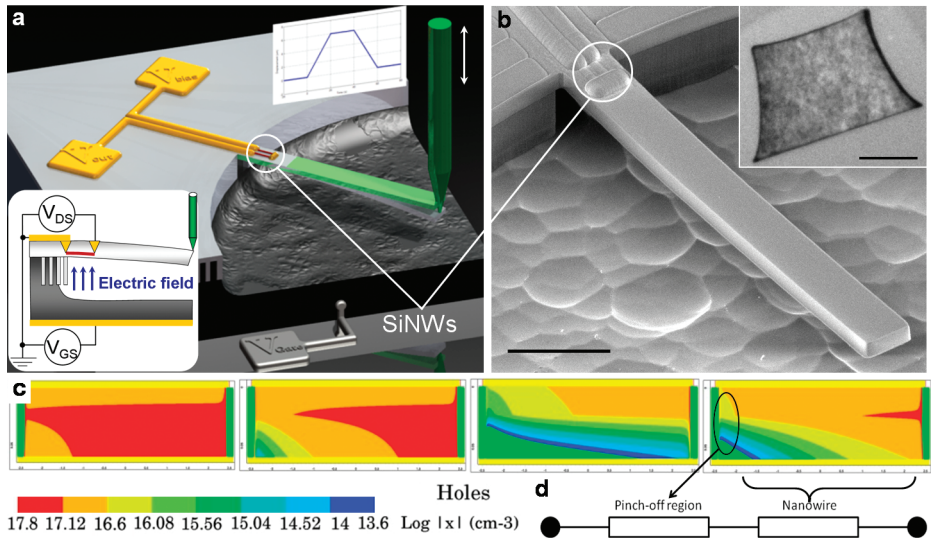

FIGURE 1. Device structure. (a) Schematic of the test setup, showing the 5 μm long NWs (red) embedded next to the anchor of the SiO_2 cantilever, the aluminum lines, the source and drain pads (gold), the mechanical stylus (green) contacting the cantilever (transparent green) and deflecting it (gray) the cantilever (transparent green). The passivation SiO_2 after metallization as well as the capping SiO_2 for the cantilever were not shown in the schematic. Biasing the substrate electrode (silver) creates a transverse electric field that controls the carriers' concentration within the NWs. (b) SEM image of the released cantilever. The NWs embedded within the cantilever are sandwiched between a bottom 0.15 μm thick thermal SiO_2 and a top 2.45 μm thick of PECVD SiO_2, which is responsible for the relief on the top of the cantilever. Scale bar, 20 μm. Inset: TEM image of a NW cross-section. Scale bar, 50 nm. (c) Holes concentration in the NW as function of V_{GS} (left to right: 0 to 7.5 V, step 2.5 V) with 0 V on source (right terminal) and 5 V on drain (left terminal) as simulated by MEDICI device simulator. These results demonstrated that V_{GS} can deplete carriers within the NW creating a pinch-off region. (d) The NW structure can be then represented as two resistors in series, the "funnel" (pinch-off) and "bulk". Small modulation of the funnel size (resistance) controls the current flowing through the NW.

between a bottom 150 nm thick thermal SiO_2 and a top 2.45 μm thick of PECVD SiO_2.

The NW device taken together with the conductive substrate resembled a metal-oxide-semiconductor field effect transistor (MOSFET). Hence, in the rest of the text we will call the two NW terminals "source" and "drain", while the substrate will be called "gate". Using the process simulator SUPREM IV and the device simulator Medici (both by TMA, Inc.), we confirmed that the substrate (gate) voltage strongly influences the device performance and can even fully deplete the entire silicon layer (Figure 1c for a p-type ⟨110⟩-oriented NW). As demonstrated by the holes concentration distribution in Figure 1c, the drain current along the NW is determined by properties of a tiny pinch-off region next to the source contact. Illustratively, current flowing through this pinch-off region is squeezed like a liquid passing through a funnel. The current amplitude in the NW is then defined by the "size" of the funnel aperture, that is, properties of the pinch-off region (see Figure 1d). To demonstrate this phenomenon, we have measured the electrical properties of the unstrained NWs, which showed a behavior similar to a MOSFET device.[15] Complete current versus voltage ($I-V$) characteristics with substrate voltage as parameter are presented in Figure S1 Supporting Information. Modulating the carrier's concentration by stress in a pinch-off region will have great influence on the total resistance of the device.

Electrical characterization of the NW was conducted on a HP 4156A Semiconductor Parameter Analyzer (Agilent, Inc.) connected to a RBL6100 probe station (Cascade Microtech, Inc.). The source of the NW was grounded (0 V) and the drain was connected to 5 V. Substrate (gate) bias was applied at the silicon backside via the wafer holder. The gate voltage V_{GS} was swept from −10 to +5 V with mechanical load as parameter. The absolute value of the V_{GS} increment was 25 mV. In addition, we investigated the capacitive nature of unstrained NWs by sweeping V_{GS} from −10 to + 5 V and back with a double sweep mode from the Semiconductor Parameter Analyzer. Figure S2a (see Supporting Information) shows that the capacitive effect of the NW becomes significant for I_D below 10 pA. All the measurements were conducted at 24 °C in darkness and I_D below 1 pA were ignored. Ambient light has usually very little influence on piezoresistivity measurements but here the devices were deliberately depleted and photocurrents had an impact on the residual drain current in the device.

The impact of stress on the NW properties was studied by poking the free end of the released cantilever with a stylus in either discrete or continuous waveform displacements (see Figure 1a). A lead zirconate titanate (PZT)-based nanopositioning system (Physik Instrumente GmbH & Co. KG) was mounted vertically on a DCM 210 micromanipulator (Cascade Microtech, Inc.). A stylus was attached to the PZT and positioned above the end of the cantilever. The vertical position of the stylus was controlled with 10 nm precision. The stylus was moved down until the drain current I_D change indicated the first contact. Then the stylus was

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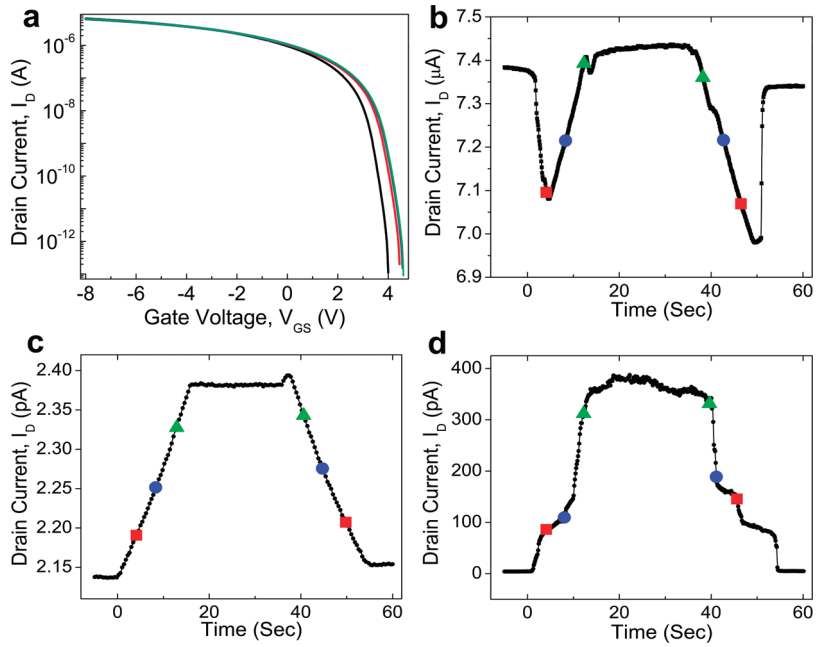

FIGURE 2. Electrically controlled piezoresistance of p+ ⟨110⟩ oriented silicon NWs. (a) Steady-state behavior of drain current I_D as a function of substrate bias V_{GS} from −10 to +5 V with tip displacement as parameter, keeping the drain-source voltage V_{DS} fixed at 5 V. Unstressed NW (black) and compressively stressed NW by displacing the cantilever tip by 1 μm (red), 2 μm (blue), and 3 μm (green). All experiments were conducted at 24 °C in dark conditions. Real-time electromechanical measurements of I_D in NWs as function of mechanical stress. The stress was controlled by lowering the PZT-held tip at 250 nm/s for 3 μm. The tip was then stopped for 20 s and disengaged at the same speed. Stylus displacement at 1 μm (squares), 2 μm (circles), and 3 μm (triangles) are indicated in the plots. (b) Unless the pinch-off region is formed, the NW has conventional piezoresistive properties resembling bulk, regardless of the bias applied, as shown for small relative I_D change for V_{GS} of −10 V and (c) V_{GS} of −2 V. (d) Once the pinch-off region is formed at V_{GS} of 4 V, the I_D changes by 2 orders of magnitude revealing impressive piezoresistive properties of NWs.

moved further down in 1 μm increments while the I_D versus V_{GS} electrical characteristics were captured (Figure 2a). Alternatively, the stylus was moved down at a speed of 250 nm/s for a displacement of 3 μm, dwelled for 20 s, and retracted with the same speed, while I_D was captured as function of time.

The stress induced to the NWs was then easily extracted from the amplitude of the cantilever's tip deflection, its mechanical properties and the NWs vertical location within the cantilever. However, anchorage undercutting during the cantilever release resulted in uncertainty in the actual cantilever length, which in turn tainted the precision of location of the NWs. The unknown cantilever length makes precise stress determination a challenging task. To remedy this issue, we minimized the undercut by adding mechanical stiffeners made from SiO_2-filled 18 μm deep trenches by adapting a method used previously to prevent buckling of a SiO_2 membrane.[16] Location of the NW close to the cantilever bottom resulted in the creation of a compressive stress in the NW when a vertical load was applied. Here we assumed that the pair of NWs embedded at the anchor of the SiO_2 cantilever beam has insignificant contribution to the mechanical properties of the cantilever. This can be explained by considering the "rule of mixture" for composite material,[17] where the effective Young's modulus E of a composite is a function of the components' volume ratio and respective E. Because of their minute size (0.1% of area ratio of cantilever), they do not mechanically influence the SiO_2 cantilever beam, despite the fact that NWs (silicon) Young's modulus is three times higher than that of SiO_2.

The electrical response of the NW under stress to the substrate bias was affected by the air gap formed underneath the cantilever. For distances ranging from 0 μm (prior to release) to 50 μm, measurements confirmed that the voltage required to deplete the NW is proportional to the air gap, as the bias is distributed between the air gap and the SiO_2 in the reverse ratio of their capacitances. We measured the drain current I_D across the NW as a function of the substrate bias (gate-source voltage V_{GS}) with the cantilever tip vertical displacement as parameter (see Figure 2a). This schematic applied a constant strain on the NWs and allowed us to decouple the dynamic effects of the mechanical strain from the electrical measurements. Under compressive stress, the conductance across the NW varied nonlinearly with the applied V_{GS}. I_D increased by 2 orders of magnitude from 4 to 360 pA at V_{GS} of 4 V. Although highly depleted NWs (I_D < 10 pA) exhibited hysteresis during the double sweep I_D versus V_{GS} measurements, the hysteresis in the NW's I_D is only 1.3 times (see Figure S2b in Supporting Information) compared to a factor of 90 times increase with mechanical strain.

Electromechanical responses of materials can be subjected to hysteresis or time lag.[18] Real-time measurements of I_D as a function of stress with V_{GS} as parameter did not

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reveal such behaviors. However the application of V_{GS} −10 V (Figure 2b) exposed an unexpected discrete step change (spiking) upon the initial contact between the probe tip and the cantilever. This step was sharp and could be considered as a discrete change as no displacement amplitude was able to stabilize the I_D between the baseline at the beginning of the experiment and the change observed after the contact. It should be further investigated and may be linked to a similar phenomenon recently published relating it to the plasticity of nanostructured materials.[19] The electromechanical response at V_{GS} of −2 V (see Figure 2c) resembled that of a typical bulk piezoresistor.[20] Further increase of V_{GS} to 4 V (Figure 2d) depleted the carriers in the NWs resulting in a huge increase in I_D (2 orders of magnitude).

The piezoresistive properties of a material are usually characterized by their gauge factor (GF), which is the ratio of the normalized change of the electrical conductance of the material ($\Delta\sigma/\sigma_o$) to the applied compressive stress (ε).[6] As V_{DS} is fixed, the drain current I_D is proportional to the conductance of the NW. The GF of the NW can then be

$$\mathrm{GF} = \frac{\mathrm{d}I}{I_o\,\mathrm{d}\varepsilon} \tag{1}$$

when the stylus deflects the tip of the cantilever, I_D changes with time. I_o is the current selected at the origin of a linear electromechanical response. The gradient of the current I_D versus the time t in Figure 2b−d is proportional to the ratio of dI to the change in the cantilever tip deflection dδ

$$\frac{\mathrm{d}I}{I_o\,\mathrm{d}t} = \frac{v}{I_o}\frac{\mathrm{d}I}{\mathrm{d}\delta} \tag{2}$$

where v is the poking speed of the stylus. The gradient with R-square greater than 0.9 was chosen for the analysis of the NW's GF. The induced mechanical strain in the NW is determined from the cantilever beam deflection formula.[17] The relationship between the tip deflection of a rectangular cantilever to the average induced strain ε_{ave} in NWs is given by

$$\delta = \frac{3(L - l/2)c\varepsilon_{ave}}{L^3} \tag{3}$$

where L is the length of the cantilever, l is the length of NW, and c is the vertical location of the NW from its neutral axis. Derivation for ε_{ave} as a function of δ is provided in Supporting Information. Extracted GF for the NW device with V_{GS} as parameter are plotted in Figure 3. The maximum GF of 5400 was achieved at V_{GS} of 3.75 V corresponding to an increase

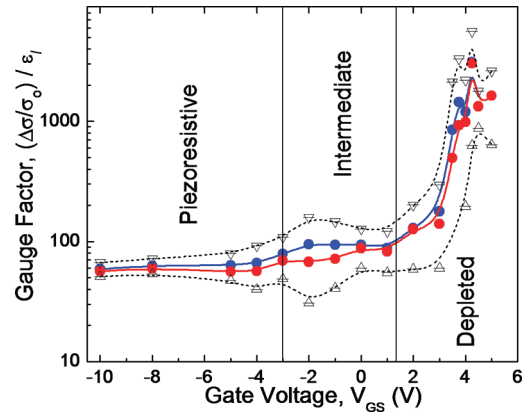

FIGURE 3. Extracted gauge factor (GF) as a function of gate voltage. For V_{GS} from −10 to −3 V, the device behaved as conventional piezoresistor with GF of 50. For V_{GS} between −3 and 1 V, the device was in an intermediate state, where the combination of piezoresistance and carrier depletion allowed the I_D control; the *GF* increased to almost 300. Further V_{GS} increase resulted in a *GF* of up to 5000 at 3.75 V when the pinch-off region had the strongest influence on the device behavior. At a V_{GS} above 4 V, the NW structure was fully depleted and only leakage current was detected decreasing the GF. Results from 8 pairs of NWs are shown; (blue trace) mean, (red trace) median, (inverting triangle) positive standard deviation, and (triangle) negative standard deviation.

of 2 orders of magnitude. For higher V_{GS}, the NWs were fully depleted, independently of the applied stress.

It has been reported that (de)population of dielectric trap and interface states during high voltage stressing can result in time-dependent-dielectric breakdown.[21] The consequent discharge of these traps when subjected to high V_{DS} can become an additional source of gating for the conducting channel. Inevitably, the amplitude of V_{DS} has become the limiting factor for the investigation of the effect of transverse electrical fields on NW's GF. To study the contribution of V_{DS} on the piezoresistance in depleted NWs, we recorded I_D versus V_{GS} with compressive strain and V_{DS} as parameter (see Figure S3 in Supporting Information). A NW with V_{DS} of 5 V exhibited similar of order magnitude change (from GF ∼610 at intermediate state to a GF of >5000 in highly depleted NW) in I_D when operated in depleted region as one with a V_{DS} of 0.5 V (a low bias voltage). This shows that the contribution of induced gating from a 5 V V_{DS} is minimal with regards to the mechanical gating.

We have demonstrated that the piezoresistivity in silicon NW could be controlled by an external electric field perpendicular to the current flow within the NW. Optimizing NW doping and biasing conditions could lead to the formation of a virtual funnel (pinch-off region) within the NW, which determines the overall NW resistance. Mechanical stress applied on the NW caused an increase of the charge carriers' concentration. By combining the formation of the pinch-off region with mechanical stress, we achieved a modulation of the GF by 2 orders of magnitude from 50 to 5000, creating electrically controlled giant piezoresistance in nanowires. This device may be the first seed of a foreseeable new family of sensors with externally controlled sensitivity, tunable for

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specific application. Low gain devices can be used as conventional piezoresistive sensors while high gain devices will be powerful force-activated NEMS mechanical switches or mechanical/electrical comparators.

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Supporting Information Available. Details of I_D-V_{DS} plots for unstrained silicon nanowires, I_D-V_{GS} measurements with mechanical stress, and V_{DS} as parameters and strain analysis. This material is available free of charge via the Internet at http://pubs.acs.org.

REFERENCES AND NOTES

(1) Kong, J.; Franklin, N. R.; Zhou, C. W.; Chapline, M. G.; Peng, S.; Cho, K. J.; Dai, H. J. *Science* **2000**, *287* (5453), 622–625.
(2) Cui, Y.; Wei, Q. Q.; Park, H. K.; Lieber, C. M. *Science* **2001**, *293* (5533), 1289–1292.
(3) Poncharal, P.; Wang, Z. L.; Ugarte, D.; de Heer, W. A. *Science* **1999**, *283* (5407), 1513–1516.
(4) Boukai, A. I.; Bunimovich, Y.; Tahir-Kheli, J.; Yu, J. K.; Goddard, W. A.; Heath, J. R. *Nature* **2008**, *451* (7175), 168–171.
(5) Hochbaum, A. I.; Chen, R. K.; Delgado, R. D.; Liang, W. J.; Garnett, E. C.; Najarian, M.; Majumdar, A.; Yang, P. D. *Nature* **2008**, *451* (7175), 163–U5.
(6) He, R. R.; Yang, P. D. *Nat. Nanotechnol.* **2006**, *1* (1), 42–46.
(7) Toriyama, T.; Funai, D.; Sugiyama, S. *J. Appl. Phys.* **2003**, *93* (1), 561–565.
(8) Rowe, A. C. H. *Nat. Nanotechnol.* **2008**, *3* (6), 311–312.
(9) Wong, E. W.; Sheehan, P. E.; Lieber, C. M. *Science* **1997**, *277* (5334), 1971–1975.
(10) Cao, J.; Wang, Q.; Dai, H. J. *Phys. Rev. Lett.* **2003**, *90* (15), 4.
(11) Stampfer, C.; Jungen, A.; Linderman, R.; Obergfell, D.; Roth, S.; Hierold, C. *Nano Lett.* **2006**, *6* (7), 1449–1453.
(12) Stampfer, C.; Helbling, T.; Obergfell, D.; Schoberle, B.; Tripp, M. K.; Jungen, A.; Roth, S.; Bright, V. M.; Hierold, C. *Nano Lett.* **2006**, *6* (2), 233–237.
(13) Richter, J.; Arnoldus, M. B.; Hansen, O.; Thomsen, E. V. *Rev. Sci. Instrum.* **2008**, *79* (4), 10.
(14) Singh, N.; Agarwal, A.; Bera, L. K.; Liow, T. Y.; Yang, R.; Rustagi, S. C.; Tung, C. H.; Kumar, R.; Lo, G. Q.; Balasubramanian, N.; Kwong, D. L. *IEEE Electron Device Lett.* **2006**, *27* (5), 383–386.
(15) Sze, S. M.; Ng, K. K. *Physics of Semiconductor Devices*, 3rd ed.; Wiley: New York, 2006.
(16) Neuzil, P.; Liu, Y.; Feng, H. H.; Zeng, W. J. *IEEE Electron Device Lett.* **2005**, *26* (5), 320–322.
(17) Young, W. C.; Budynas, R. G. *Roark's Formulas for Stress and Strain*, 7th ed.; McGraw-Hill: New York, 2002.
(18) Zhou, J.; Gu, Y. D.; Fei, P.; Mai, W. J.; Gao, Y. F.; Yang, R. S.; Bao, G.; Wang, Z. L. *Nano Lett.* **2008**, *8* (9), 3035–3040.
(19) Nowak, R.; Chrobak, D.; Nagao, S.; Vodnick, D.; Berg, M.; Tukiainen, A.; Pessa, M. *Nat. Nanotechnol.* **2009**, *4* (5), 287–291.
(20) Smith, C. S. *Phys. Rev.* **1954**, *94* (1), 42.
(21) Scott, R. S.; Dumin, N. A.; Hughes, T. W.; Dumin, D. J.; Moore, B. T. *IEEE Trans. Electron Devices* **1996**, *43* (7), 1133–1143.

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