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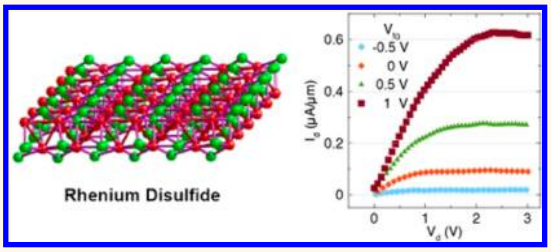
Field Effect Transistors with Current Saturation and Voltage Gain in Ultrathin ReS_2

Chris M. Corbet,[†] Connor McClellan,[†] Amritesh Rai, Sushant Sudam Sonde, Emanuel Tutuc, and Sanjay K. Banerjee*

Department of Electrical Engineering, The University of Texas at Austin, Austin, Texas 78712, United States. [†]These authors (C.M.C. and C.M.) contributed equally to this work.

ABSTRACT We report the fabrication and device characteristics of exfoliated, few-layer, dual-gated ReS_2 field effect transistors (FETs). The ReS_2 FETs display n-type behavior with a room temperature I_{on}/I_{off} of 10^5. Many devices were studied with a maximum intrinsic mobility of 12 $cm^2 \cdot V^{-1} \cdot s^{-1}$ at room temperature and 26 $cm^2 \cdot V^{-1} \cdot s^{-1}$ at 77 K. The Cr/Au-ReS_2 contact resistance determined using the transfer length method is gate-bias dependent and ranges from 175 $k\Omega \cdot \mu m$ to 5 $k\Omega \cdot \mu m$, and shows an exponential dependence on back-gate voltage indicating Schottky barriers at the source and drain contacts. Dual-gated ReS_2 FETs demonstrate current saturation, voltage gain, and a subthreshold swing of 148 mV/decade.



KEYWORDS: rhenium disulfide · transistor · TMD · gain · saturation · mobility

In the past decade, two-dimensional (2D) materials have been intensely researched for their potential use in solid-state device technology beyond silicon.[1−3] Atomically thin, 2D materials are potentially ideal for eliminating short-channel effects, such as drain-induced barrier lowering (DIBL) in today's state-of-the-art metal−oxide−semiconductor field-effect transistors (MOSFETs).[3] The atomically smooth surfaces have no dangling bonds, which is potentially beneficial for lowering interface state densities and reducing surface roughness scattering.[3] In recent years, a class of materials known as transition metal dichalcogenides (TMDs) has been extensively studied because of unique monolayer and few-layer electronic properties.[2]

TMDs are compounds of the form MX_2, where M is a transition metal and X is a chalcogen. The bulk material is a stack of individual molecular layers held together by weak van der Waals forces, whereas strong covalent bonding exists between the atoms of each individual layer. These TMDs display semiconducting, metallic, or superconducting behavior depending upon their constituent elements.[2,4] Mechanical exfoliation[5] is used to reduce bulk TMDs and isolate 2D molecular layers that exhibit large bandgaps. Having a bandgap gives TMDs an advantage over gapless graphene for use in logic transistors, as a sizable bandgap is required to achieve high I_{on}/I_{off}.[6]

Because a wide range of TMDs exists, many still await a thorough theoretical and experimental exploration by the scientific community. Semiconducting TMDs generally have different electronic properties between their bulk and monolayer forms,[7] the most common manifestation of this effect being the transition from indirect to direct bandgap as the number of layers decreases.[8,9] ReS_2 has recently gained attention for having a bulk form that behaves optically like its individual monolayers resulting from charge decoupling from an extra valence electron in the Re atoms that causes ReS_2 to take a distorted 1T crystal structure.[10] Thus, ReS_2 has a direct bandgap in both its bulk (E_g = 1.5 eV), and monolayer (E_g = 1.58 eV) forms. This is different from most TMDs whose bandgap changes from indirect to direct while decreasing in thickness such as MoS_2,[8] $MoSe_2$,[11] WS_2,[12] and WSe_2.[12] While a direct bandgap is not necessary for logic transistors, optoelectronics and interband tunnel FETs (TFETs) require

* Address correspondence to banerjee@ece.utexas.edu.

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a direct bandgap for efficient photon absorption/emission and electron transmission, respectively. We also note the anisotropic crystal structure of ReS_2, allowing for possible novel high efficiency photodetectors as has been implemented with $ReSe_2$ and GaS.[13,14] Therefore, ReS_2 may provide a seamless platform for combining logic FETs and optoelectronic devices in a monolayer/multilayer platform, using processes such as chemical vapor deposition.[2,15]

Using high-*k* dielectrics and top-gates in TMDs devices has been shown to improve FET mobilities by means of dielectric screening and increase channel control using the top-gate.[16] Here, we report the FET properties of ReS_2 by fabricating and characterizing dual-gated transistors made from two to seven layers of exfoliated ReS_2, with Al_2O_3 as the high-*k* top-gate dielectric and thick SiO_2 as the back gate dielectric.

RESULTS AND DISCUSSION

As ReS_2 is a comparatively less studied TMD material, an effort was made to ensure the composition and quality of the ReS_2 crystals used in this study. X-ray photoelectron spectroscopy (XPS) was employed to confirm the ratios of Re and S in the crystal. Figure 1a shows the number of electrons collected *versus* the binding energy of the electrons around the Re 4f bond states. There are two distinct peaks at 42.58 and 45.00 eV representing the Re 4f 5/2 and Re 4f 7/2 states. Similarly, Figure 1b shows two peaks at 163.03 and 163.40 eV representing the S 2p 3/2 and S 2p 1/2 states. Compositional analyses of these peaks show the crystal to contain ~34 atom % Re and ~66 atom % S. To confirm these results energy-dispersive X-ray spectroscopy (EDS) was also conducted on the parent ReS_2 crystal. Figure 1c shows the number of X-rays detected *versus* the energy of the excited X-rays in the crystal. The two major peaks detected at 1.84 and 2.31 keV are associated with Re (M_α) and S (K_α). Compositional analysis of the EDS spectrum gives ~34 atom % Re and ~66 atom % S, confirming the XPS data and the high quality of the source ReS_2 crystal.

Next, we created a set of dual-gated ReS_2 FETs by isolating few-layer areas *via* mechanical exfoliation.[5] As with graphene, solely optical confirmation of the number of layers in the isolated films can be quite difficult. A combination of atomic force microscopy (AFM), photoluminescence (PL), and Raman spectroscopy were used to characterize the flakes and determine the number of layers in our devices. Figure 2a shows an AFM image of a ReS_2 FET after Cr/Au deposition, and Figure 2b gives an optical micrograph of the device after completion of the top-gate. Since monolayer ReS_2 is approximately 0.7 nm thick,[10,17] and the sample shown is 1.4 nm thick, we estimate this ReS_2 FET channel to be two layers thick. Unlike many TMDs the bandgap in ReS_2 remains constant for samples thicker than a monolayer, and an accurate determination of layer

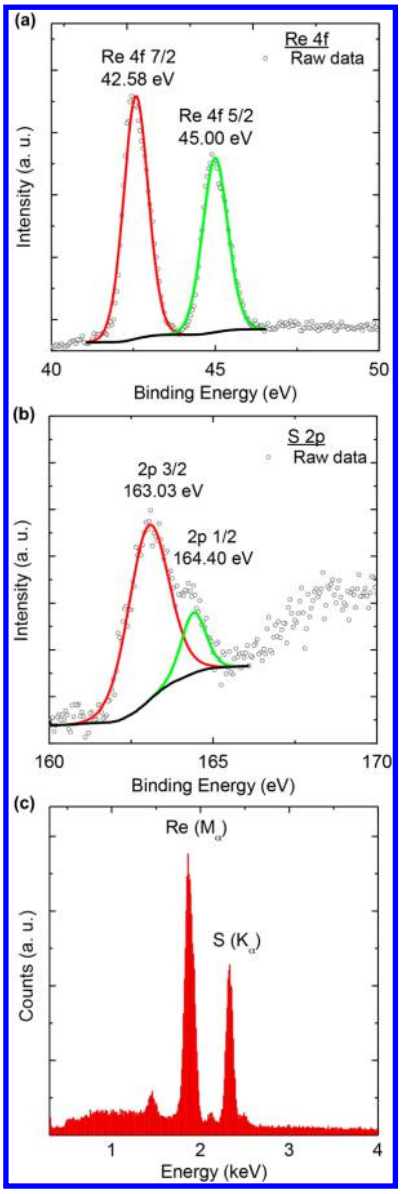

Figure 1. Elemental composition: (a) XPS spectra of the Re 4f state; (b) XPS spectra of the S 2p state; (c) EDS measurement of the ReS_2 crystal. Both XPS and EDS confirm a composition 34 atom % Re and 66 atom % S.

number is difficult using techniques other than AFM. Figure 2c displays PL measurements on bulk, few-layer, and monolayer unprocessed ReS_2 flakes. The bulk and four-to-five layer data show a PL intensity peak at 1.50 eV, and a monolayer PL intensity peak at 1.58 eV is observed. These intensity peaks are consistent with previous ReS_2 studies[10,17] and are attributed to the layer-number-independent direct bandgap in ReS_2. Recent studies have shown that the optical bandgap probed *via* PL measurements of few-layer TMDs can be substantially different from their electrical bandgap.[18] This difference occurs because the lowest exciton binding energy is smaller than the electrical bandgap of the material. It is unknown if this holds true with few-layer ReS_2 as the only reported exciton binding

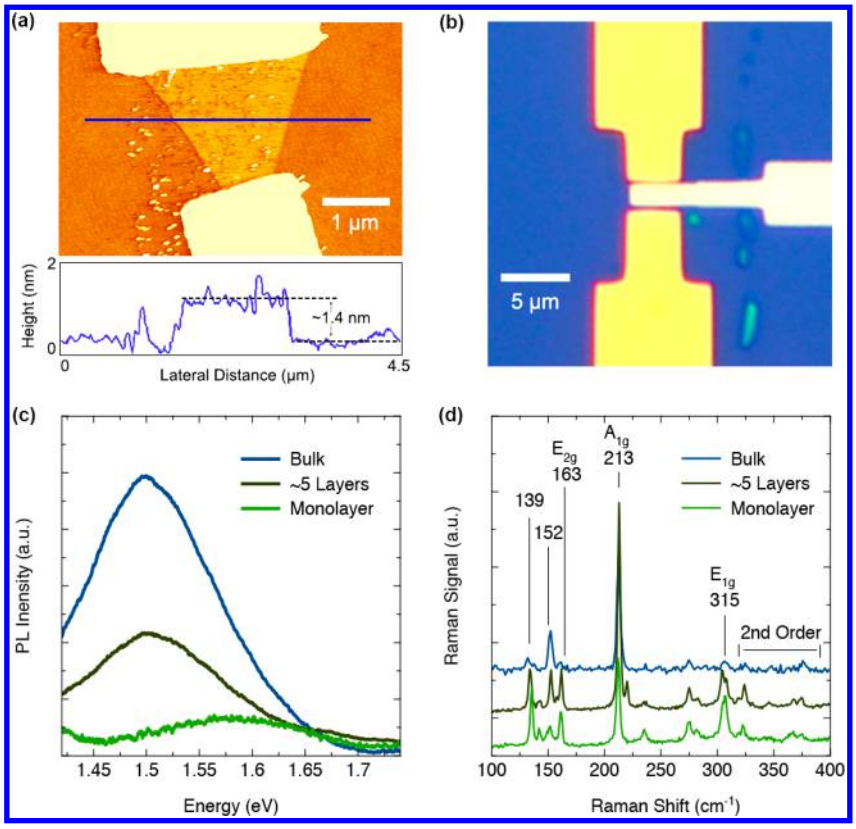

Figure 2. Isolation of few layer ReS_2 flakes. (a) AFM image of a ReS_2 FET after contact deposition but before depositing Al_2O_3 and Ni top-gate. The figure below gives the height of the ReS_2 flake along the line scan shown above. (b) Optical micrograph of completed ReS_2 FET. (c) PL measurements of unprocessed ReS_2 bulk, few-layer, and monolayer flakes. The direct bandgap shift is observed as flake is scaled from multiple layers to monolayer form. (d) Raman spectroscopy measurements of monolayer, multilayer, and bulk ReS_2 flakes.

energies for this material are 1.55 and 1.58 eV measured in a bulk crystal.[19] Figure 2d displays the Raman spectrum of unprocessed ReS_2 flakes with different thicknesses. The peaks at 211 and 164 cm^{-1} can be attributed to the out-of-plane (A_g), and in-plane (E_{2g}) vibrational modes of ReS_2, and are consistent with previous few-layer ReS_2 measurements.[10] A more thorough study is required to determine if Raman spectroscopy could be used to accurately determine the number of layers in a ReS_2 crystal. All devices in this study were chosen to have a two-to-seven layer thick ReS_2 channel.

We provide an initial assessment of ReS_2 FETs by extracting the device I_{on}/I_{off}, subthreshold swing, metal/semiconductor contact resistance, and carrier mobility. For measuring the electrical characteristics of our devices, we used a high-vacuum probe station with a base pressure of $3 \cdot 10^{-5}$ Torr in order to desorb contaminants that might affect the electrical characteristics. All measurements were performed in the dark at either 300 or 77 K. The source contact (V_s) was grounded and the drain contact (V_d) was biased while using the Si substrate as the back-gate (V_{bg}) electrode. Figure 2 shows the transfer and output characteristics of one device ($L = 7\ \mu m$, $W = 1.4\ \mu m$, $H = 3$ nm) at room temperature (300 K) and low temperature (77 K) before the addition of a top-gate. Figure 3a shows drain current (I_d) normalized by the channel width as a function of V_d for different positive V_{bg} values at 300 K. Similar I_d-V_d results were obtained at different V_{bg} with switched source and drain contacts, indicating symmetric contacts. The I_d-V_d data in Figure 3 reveal that ReS_2 exhibits n-type behavior with increasing conductance as V_{bg} increases. At room temperature (Figure 3a), the Cr contacts appear to be forming Ohmic contacts with the ReS_2 flakes given by the linear I_d-V_d relationship and symmetric I_d measurements when source and drain contacts are switched. However, once the devices are cooled to 77 K, the I_d-V_d dependence (Figure 3b), becomes slightly superlinear indicating the Schottky nature of the metal/ReS_2 interface as is typical with metal contacts to TMD materials reported in literature.[20] Thermal excitation at room temperature allows the electrons to more readily overcome the Schottky barrier that results in an apparent Ohmic contact.

Figure 3c shows I_d as a function of V_{bg} with $V_d = 1$ V for a device at 300 and 77 K to illuminate the differences in transfer characteristics of the same device at different temperatures. There is a positive shift in the threshold voltage (V_{th}) as temperature decreases from 300 K to 77 K. This shift is expected as the channel

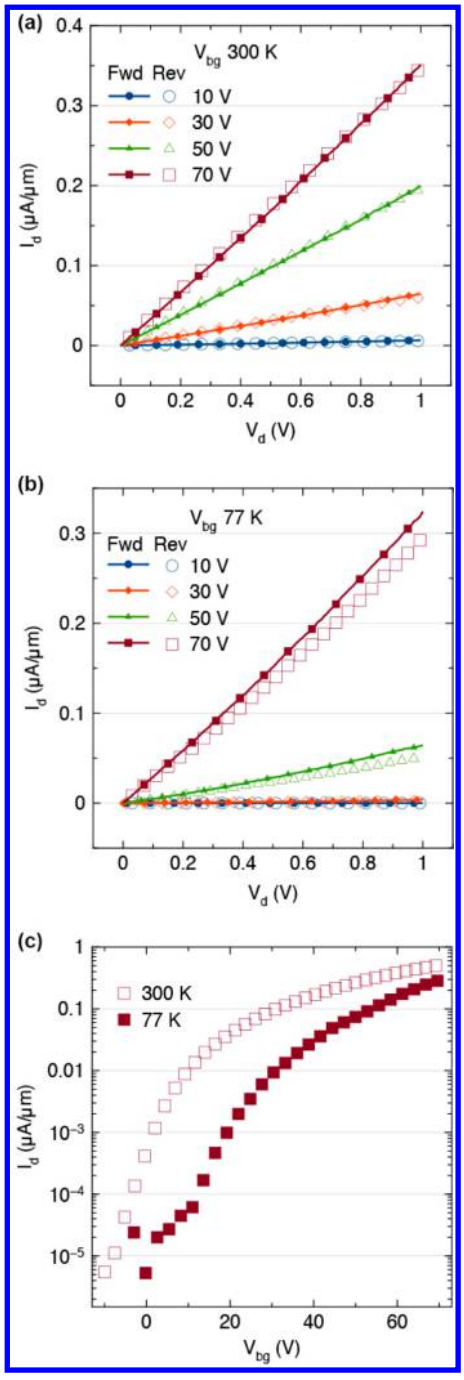

Figure 3. Examination of Schottky contacts. (a) I_d-V_d output characteristics for different V_{bg} at room temperature (300 K)). (b) I_d-V_d characteristics at low temperature (77 K). Similar drain currents with source and drain contacts reversed (solid and open) and linear I_d-V_d relationship at 300 K suggest symmetric S/D contacts, but the slightly superlinear I_d-V_d relationship at 77 K may indicate that the S/D contacts actually have a small Schottky barrier. (c) I_d-V_{bg} with V_d at 1 V at 300 and 77 K. Shift in V_{th} due to reduced carrier concentrations or Schottky barrier widening at low temperature. High I_{on}/I_{off} is the result of a high bandgap (E_g = 1.5 eV).

carrier concentration decreases with temperature causing the semiconducting channel to become less doped.[21] Also the shift may be due to an increase in the bandgap, and corresponding shifts in the flatband voltage, as in other semiconductors. Moreover, at 77 K, the electrons have less energy to overcome the Schottky barrier at the source contact, which reduces the thermionic component of the current and V_{th} increases. Additionally we extract the subthreshold swing (S) and I_{on}/I_{off} ratio from the I_d-V_{bg} data in Figure 3c. By taking the inverse of the slope in the subthreshold region, we calculate S = 1.2 V/decade in our back-gated devices and $I_{on}/I_{off} = 10^5$. These values are characteristic of TMD devices,[16,22] and larger than the required $I_{on}/I_{off} = 10^4$ for CMOS logic devices.[6]

When comparing the I_d-V_d data of different devices at 77 K, we observed a slight variation in the superlinear behavior of the drain current demonstrating the variability the Schottky barriers formed at the TMD/metal interface. While Fermi level pinning[20] close to the conduction band edge of ReS_2 results in n-type behavior, the exact energy at which this pinning occurs varies from device to device, yielding differing degrees of superlinear I_d-V_d relationships across the devices at 77 K. Additionally, we fabricated devices with Ti/Au contacts and observed Schottky behavior at 300 K despite Ti having a lower work function than Cr, indicating that the Ti may be oxidizing, forming a tunnel barrier,[23] and causing poor electrical contact at the interface.

To further explore the contact resistance (R_c) in our devices, we use the transfer length method (TLM) to quantify the R_c between the Cr contacts and ReS_2, and the sheet resistance of the ReS_2 channel. Using an exfoliated ReS_2 flake with uniform thickness and width, we created different channel lengths using a set of contacts placed at different spacings along the flake. Measuring the I_d-V_{bg} relationship at low V_d values, the total resistance (R_T) of different channel lengths at different V_{bg} values can be calculated using V_d, I_d, and Ohm's law. The following TLM equation gives a relationship between R_T and R_c:

$$R_T = \rho_{sh}\cdot\frac{L}{W} + 2R_C \qquad (1)$$

Here, ρ_{sh} is the sheet resistance of the channel, L is the channel length, W is the channel width, and R_c is the contact resistance. R_c includes the resistance at the source/drain−ReS_2 interface, and the resistance of the ReS_2 under the contact.[24,25] Figure 4a shows R_T *versus* L at different V_{bg} values ranging from −20 to 70 V in 10 V increments and the linear regression line of best fit for each set of V_{bg}. The slope of the line is ρ_{sh}/W and the y-axis intercept is $2R_c$. The slope decreases with increasing V_{bg} as expected for an n-type FET as the ρ_{sh} decreases as the channel has more electrons and becomes more conductive. Figure 4b shows R_c versus V_{bg}. The R_c value is approximately 175 kΩ·μm at V_{bg} of −20 V and decreases to 5 kΩ·μm at V_{bg} of 70 V, and shows a strong dependence on V_{bg}, consistent with the presence of a Schottky barrier at the Cr−ReS_2 interface.

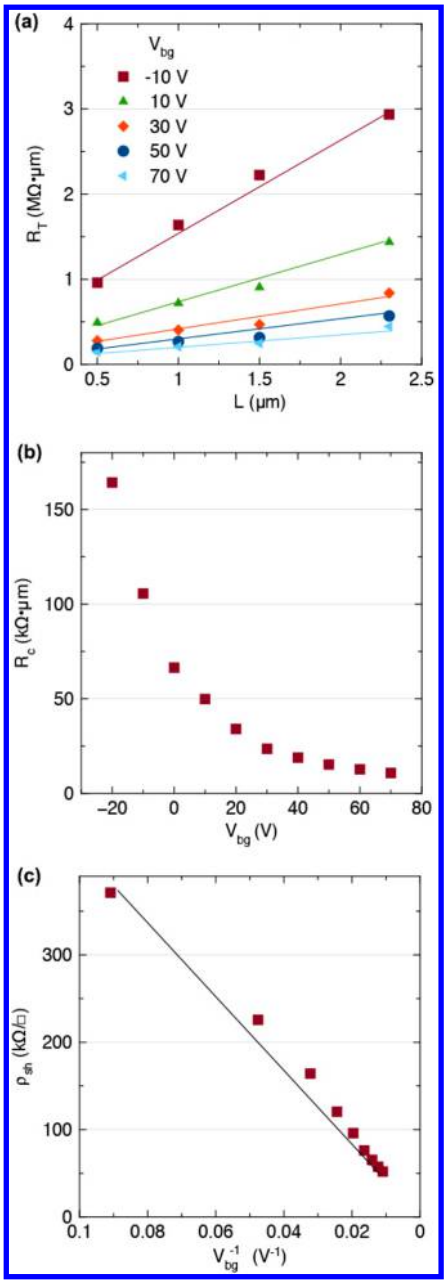

Figure 4. Transfer length method data analysis. (a) Channel length (L) *vs* total resistance (R_T) data at different back gate voltages with trend lines used to determine the sheet and contact resistances. (b) Contact resistance (R_c) *vs* back gate voltage (V_{bg}). The exponential decrease in contact resistance as V_{bg} increases indicates Schottky contacts. (c) Sheet resistance (ρ_{sh}) *vs* inverse back-gate voltage (V_{bg}^{-1}). Linear fit represents intrinsic carrier mobility.

Similar R_c values have been reported in $MoSe_2$ FETs.[22] Future studies may explore various doping schemes or metal contacts for reducing R_c.[20,26]

The measurement of the Schottky barrier at the metal/TMD interface has been shown to vary, depending on the methods and materials used. In the case of MoS_2, Das *et al.*[20] extracted the Schottky barrier height of Ti to be 50 meV using thermionic emission theory, while Kwak *et al.*[27] found the height to be 400 meV using thermionic field emission theory. McDonnell *et al.*[28] suggested that this difference stems from the density of the point defects in the MoS_2 channel, which can cause variable Fermi level pinning up to 400 meV and an apparent lowering of the Schottky barrier. While the Schottky barrier height at the metal−TMD interface remains an important topic to be addressed, we note that the intrinsic mobility values discussed below are not affected by the presence or magnitude of the Schottky barrier height at the metal−ReS_2 interface.

A natural extension at this point is to calculate the intrinsic ReS_2 mobility (μ_i) using the ρ_{sh} values extracted from eq 1 and

$$\rho_{sh} = \frac{1}{C_{ox} \cdot (V_{bg} - V_{th}) \cdot \mu_i} \tag{2}$$

In eq 2, $C_{ox} = 12$ nF/cm^2 is the capacitance per unit area of the 285 nm thick SiO_2 gate dielectric, and V_{th} is the threshold voltage corresponding to the onset of electrons populating the channel. Figure 4c shows ρ_{sh} as a function of V_{bg}^{-1} for the TLM structure. The linear dependence of ρ_{sh} on V_{bg}^{-1} allows us to extract a μ_i of 8.4 cm^2 V^{-1} s^{-1}. To confirm this mobility value, four-point probe conductance measurements were conducted as a function of V_{bg}. These four-point probe, gate-dependent measurements on the TLM structure yielded mobility values ranging from 8.1 to 8.7 cm^2 V^{-1} s^{-1}.

It is interesting to study the difference in μ_i and the field effect mobility (μ_e). To determine μ_e we measured I_d as a function of V_{bg} in the linear regime and used the equation:

$$\mu_e = \frac{\partial I_d}{\partial V_{bg}} \cdot \frac{L}{W} \cdot \frac{1}{C_{ox} V_d} \tag{3}$$

where L and W are the channel length and width, respectively. Note that this method assumes that the source/drain resistances are small compared the channel resistance. The TLM measurements revealed the variation in μ_e in the presence of Schottky contacts. At room temperature and across all variations of adjacent probe combinations μ_e ranges from 0.5 to 11.6 cm^2 V^{-1} s^{-1} and values were dependent on the bias magnitude and orientation of the source and drain contacts during electrical measurement. The highest intrinsic mobility found in the set of fabricated transistors was 12 cm^2 V^{-1} s^{-1} at 300 K which increased to 26 cm^2 V^{-1} s^{-1} at 77 K; however, most of our devices were in the 1 to 10 cm^2 V^{-1} s^{-1} range at 300 K, which is typical of back-gated TMD FETs.[29]

We used Al_2O_3 as a high-k dielectric to fabricate dual-gated ReS_2 devices. The transfer and output characteristics probed in one dual-gated FET (L = 3.6 μm, W = 1 μm, H = 3 nm) are displayed in Figure 5. After the deposition of the high-k dielectric the hysteresis in the I_d−V_{bg} characteristics increased from 0.8 to 1.4 V suggesting an increase in carrier trapping

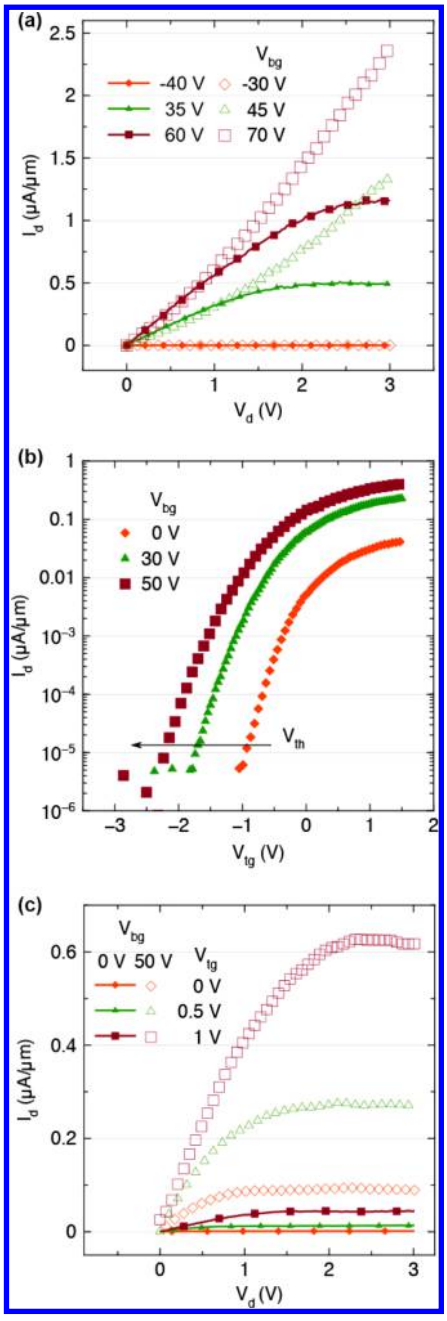

Figure 5. Output and subthreshold characteristics. (a) I_d-V_d data for different V_{bg} before (open) and after (solid) deposition of Al_2O_3 and top-gate. Current saturation is observed after top-gate deposition. (b) I_d-V_{tg} with V_d at 1 V and V_{bg}= 0, 30, and 50 V. I_d-V_{tg} data demonstrates good channel conductance modulation using a nickel top gate. A negative shift in V_{th} is observed as V_{bg} increases due to thinning of the S/D Schottky barrier and an increase in channel carrier concentration. (c) I_d-V_d data with V_{bg} at 0 V (open) and V_{bg} at 50 V (line) while varying the top gate bias, demonstrating current saturation.

originating in the deposited Al_2O_3.[30] After top gate stack deposition we achieved current saturation, which is required for most circuits. Figure 5a shows the I_d-V_d characteristics of the transistor at various V_{bg} values before and after top-gate deposition. The data acquired after top gate deposition are measured at V_{tg} = 0 V. Current saturation was not observed in any back-gated ReS_2 FETs, with or without top dielectric. Figure 5b shows I_d-V_{tg} with V_{bg} set to 0, 30, and 50 V, which causes a shift in V_{th} and increase in I_{on}/I_{off} from 10^4 to 10^5 with V_{bg} at 0 and 50 V, respectively. Additionally, the hysteresis in the I_d-V_{tg} data increases from 0.21 V at V_{bg} = 0 V, to 0.42 V at V_{bg} = 50 V. Better performance at higher V_{bg} results from decreasing the contact resistance in the Schottky contacts, as discussed previously. The μ_e of this top-gated FET derived from I_d-V_{tg} data probed at V_{bg} = 50 V is found to be 1.2 $cm^2\ V^{-1}\ s^{-1}$, similar to the back-gated mobility measurement for this device.

The observation of current saturation after the formation of the top-gate can be explained using the "pinch off" mechanism in the FET model.[21] This is indicated in Figure 5c which shows saturation of I_d *versus* V_d with V_{bg} at 0 and 50 V, and V_{tg} at 0, 0.5, and 1 V. The top-gate dielectric yields better electrostatic control over the ReS_2 channel resulting in a lower V_{th} value, roughly 500 mV with V_{bg} at 50 V. Thus, lower V_d values will satisfy $V_d > V_{tg} - V_t$, the condition which controls the FET current saturation regime. Furthermore, our top gate does not overlap the source/drain Schottky contacts, unlike the bottom gate which overlaps both contacts, and modulating V_{tg} is not expected to affect the drain and source Schottky barriers. Increasing V_{bg} from 0 to 50 V effectively "thins down" both the drain and source Schottky barriers to a greater extent, increasing saturation currents. Also it may be noted that current saturation occurs when R_c is low (V_{bg} = 50 V) and high (V_{bg} = 0 V), indicating that the effect is not a result of large contact resistances, as has been attributed for short channel saturation in MoS_2 FETs.[31] This analysis is confirmed by the quadratic dependence of the current saturation (I_{dsat}) on gate voltage (V_g), as per the long channel current saturation equation:[21] $I_{dsat} \approx (V_g - V_{th})^2$. Finally, the estimated transconductance (g_m) at V_d = 1 V and output conductance (g_d) at V_{tg} = 1 V from Figure 5c with V_{bg} = 50 V are 190 nS and 15 nS, respectively. Since g_m/g_d = 13, these devices show voltage gain, which is critical for circuits.

CONCLUSION

Here, we have demonstrated FET behavior in the TMD material ReS_2 for the first time. We measured the transfer and output characteristics, carrier mobility, I_{on}/I_{off}, subthreshold swing, and metal/semiconductor contact resistance. We demonstrated current saturation and voltage gain in these n-channel FETs with a high-*k* dielectric and top-gate, which is important for most circuits. The n-type FET behavior could complement recently reported $ReSe_2$ FETs exhibiting p-type conduction with Cr contacts.[32] One could potentially combine ReS_2 and $ReSe_2$ in a CMOS layout where the same contact metal could yield n and p type behavior with ReS_2 and $ReSe_2$, respectively. Using substitutional

chalcogen doping techniques,[33,34] it may be possible to construct rhenium-based CMOS architecture using top gates to achieve current saturation. Examining ReS_2 FETs' optoelectronic responses using an electrically induced p−n junction[35] could also be interesting for future optoelectronic applications.

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MATERIALS AND METHODS

ReS_2 Crystals and Characterization. Single crystal ReS_2 (rhenium disulfide) was purchased commercially from 2D Semiconductors, Inc. EDS measurements were taken from the EDAX Apollo X Silicon Drift Detector and Genesis software mounted on a Zeiss Neon 40 scanning electron microscope. XPS was performed in a MULTIPORBE system from Omicron NanoTechnology GmbH.

Few Layer ReS_2 Isolation and Characterization. Optical investigation was conducted with the Olympus BX51 M and their proprietary Stream Essentials analysis software. Raman spectroscopy measurements were taken with a Renishaw inVia micro-Raman system. Samples were exposed for 3 s to a 1 mW incident beam with an excitation wavelength of 532 nm. A 3000 l/mm grating was used for <0.5 cm^{-1} resolution. Atomic force microscopy images were taken with a Veeco Nanoscope 5 in tapping mode. Photoluminescence measurements were taken with a Renishaw inVia micro-Raman system configured for photoluminescence measurements with specialized optics. Samples were exposed for 30 s to a 5 mW incident beam with an excitation wavelength of 532 nm. Photoluminescence measurements were taken with a 1200 l/mm grating to obtain high energy peaks.

Transistor Fabrication. We mechanically exfoliated synthetic ReS_2 crystals onto a heavily N^+ doped silicon wafer with 285 nm of thermally grown SiO_2, which allows for the optical contrast necessary to distinguish between flakes of varying thicknesses. To remove the residual tape adhesive from the flakes after exfoliation, the samples were annealed at 275 °C for 8 h in an ultra-high-vacuum (UHV) annealing chamber at 2×10^{-9} Torr. Electron beam lithography (EBL) followed by 10 nm Cr and 50 nm Au deposition were used to define the metal contacts. Devices were again annealed in the UHV chamber at 350 °C for 8 h to remove residual resist. Subsequently, 27 nm of Al_2O_3 was deposited on top of our devices using physical vapor deposition (PVD). EBL and metallization was used to deposit 50 nm of nickel to serve as the top-gate electrode. We calculate the top-gate capacitance to be 298 nF/cm^2 using a method we previously employed in calculating the top-gate capacitance of AlO_x in graphene FETs.[36]

Electrical Characterization. All electrical measurements were taken in a Lake Shore Cryotronics cryogenic probe station. All samples were measured in vacuum below 5×10^{-5} Torr and cooled with liquid nitrogen to achieve 77 K where stated. Data were taken with an Agilent B1500 semiconductor parameter analyzer.

Conflict of Interest: The authors declare no competing financial interest.

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