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ARTICLE *in* ACS NANO · APRIL 2012

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Remote Doping and Schottky Barrier Formation in Strongly Quantum Confined Single PbSe Nanowire Field-Effect Transistors

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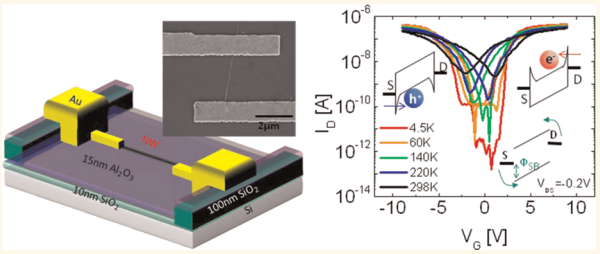
ABSTRACT



We report studies of charge injection and transport in ambipolar, predominantly n-type, and unipolar p-type single, strongly quantum confined PbSe nanowire (NW) field effect transistors (FETs). The PbSe NW FETs operate as Schottky barrier FETs in which the Fermi level is pinned near midgap, consistent with the low ionicity of PbSe, and is nearly invariant with semiconductor doping. Electron and hole mobilities increase monotonically with decreasing temperature, dominated at high temperature by electron—phonon scattering with no evidence of scattering at low temperatures. Transport in NWs is consistent with their single crystalline nature. Surface oxygen used to dope the NWs acts remotely, providing a promising route to dope nanostructures.

KEYWORDS: colloidal nanowires · Schottky barrier · field effect transistor · band transport · remote doping

PbSe is a particularly interesting semiconductor to study in one-dimension. It has a large Bohr exciton radius (46 nm) and large and equal electron and hole Bohr radii (23 nm),[1] and therefore allows the regime of strong quantum confinement to be readily accessed in semiconducting nanowires (NWs). PbSe NWs are also technologically of great promise and have potential in field-effect transistors (FETs),[2] thermoelectrics,[3,4] and photodetectors[5] arising from large and similar carrier mobilities, reduced phonon scattering, and low thermal conductivity. In FETs, PbSe NWs have been shown to switch the polarity of charge transport between ambipolar, n-type, and p-type characteristics depending on the chemistry of surface ligating compounds,[6] the presence of surface oxygen,[7] the surrounding gas,[8] and stoichiometric imbalance,[9] but little is understood about the fundamental physics of charge injection and transport in these strongly quantum confined NWs and single PbSe NW FETs have been limitedly explored.

Here, we report temperature-dependent electrical measurements used to uncover the physics of charge injection and charge transport in ambipolar, predominantly n-type ambipolar, and unipolar p-type strongly quantum confined PbSe single nanowire (SNW) FETs. We demonstrate that PbSe SNW FETs behave as Schottky Barrier (SB) FETs in which the *OFF* current is limited by the SB and decreases as temperature decreases, while the *ON* current is achieved by gate thinning of the SB and increases as temperature decreases. In the *OFF* state, the sum of the electron and hole SB heights is similar to the bandgap of PbSe NWs and the Fermi level is pinned consistent with the low ionicity of PbSe. In the *ON* states, we show that electron and hole mobilities increase monotonically as temperature decreases consistent with the single crystalline nature of PbSe NWs and in contrast to most PbSe thin films[10,11] and PbSe nanocrystal (NC) arrays[12] which are dominated at low temperature by scattering at defects, dislocations, and grain boundaries, and by thermally activated hopping transport. Finally, we introduce surface oxygen and show that remote dopants form high mobility PbSe NWs. We suggest that remote dopants are a promising route to dope nanostructures without leading to Coulomb scattering.

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Received for review March 1, 2012 and accepted April 18, 2012.

Published online April 18, 2012
10.1021/nn3009382

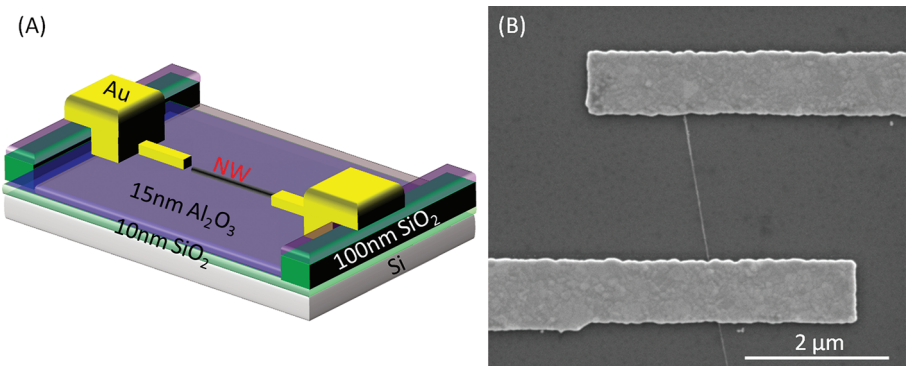

Figure 1. (A) Schematic of PbSe single nanowire (SNW), FET device, and (B) SEM image of single NW device.

A single PbSe NW FET is depicted in Figure 1A. FETs were fabricated on heavily n-doped silicon wafers with dielectric stacks of 10 nm thermally grown SiO_2 serving as the back gate and part of the gate dielectric stack, respectively. The 100 nm SiO_2 layer was patterned by photolithography to reduce gate leakage between subsequently deposited large area contact pads and the gate electrode, and 15 nm Al_2O_3 was deposited using atomic layer deposition to reduce further leakage and hysteresis. Photolithography and electron beam lithography were used to define metal pads. Single-crystalline, straight, 10 nm diameter PbSe NWs were synthesized by wet-chemical methods, as reported previously.[7,13] A 5 μL aliquot of the NW solution in octane/chloroform was dropcast between contacts, and its location was recorded using optical microscopy. Top contact electrodes were defined by e-beam lithography and deposited by e-beam evaporation to contact the ends of the NWs with the bridging electrodes previously fabricated on the Si wafer. Rigorous air-free conditions were used from synthesis, device fabrication, and characterization to prevent unintentional oxidation of the NWs.[7,15] These electrostatically well-scaled devices allow the study of SNW transport properties without short channel effects. An SEM image of the channel region of a representative PbSe SNW device is shown in Figure 1B.

RESULTS AND DISCUSSION

As-fabricated, PbSe SNW FETs are p-type with I_{ON}/I_{OFF} of 10^3 and hole saturation mobility of ~30 (±5) $cm^2/(V \cdot s)$ (Supporting Information, Figure S1). The mobility was calculated in the saturation regime using the cylinder-on-plate model[14]

$$\mu = \left(\frac{d(I_D)^{0.5}}{dV_G}\right)^2 \frac{2L}{C_{OX}} \quad (1)$$

$$C_{ox} = \frac{2\pi\varepsilon\varepsilon_0 L}{\cosh\left(\frac{r+t_{ox}}{r}\right)} \quad (2)$$

where L is the length and r is the radius of the NW and ε is the dielectric constant and t_{ox} is the thickness of the oxide layer. Annealing the NW FETs at 180 °C for 5 min desorbs surface bound oxygen that acts to p-dope[15−18] the NWs and increases the electron current, forming FETs showing ambipolar behavior. Previously we have shown that annealing and evacuating PbSe NW FETs desorbs surface-bound oxygen,[15] which creates acceptor states in PbSe,[7,15,19−21] resulting in the polarity switching from p-type to ambipolar predominantly n-type behavior arising from a stoichiometric Pb excess introduced in synthesis.[15,22,23] It should be noted that devices annealed for longer times show predominant n-type conductivity, but if the device is not kept under vacuum the conductivity type again switched from predominantly n-type to ambipolar, and eventually to predominantly p-type again due to oxygen doping, even at the <1 ppm O_2 levels in the inert environment of a nitrogen glovebox. The SNW FET shows balanced electron and hole transport as seen in Figure 2 in the output characteristics in the (A) hole and (B) electron accumulation regimes and in (C) the transfer characteristics. The device was kept under

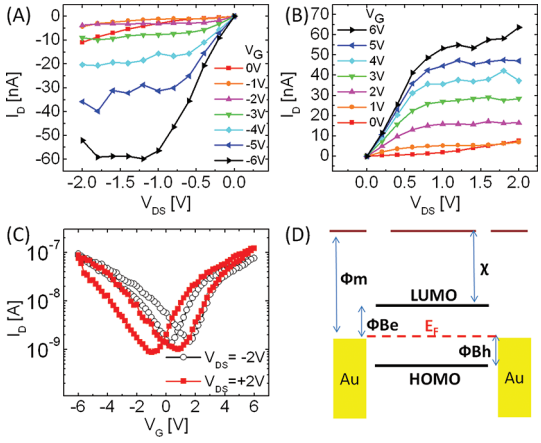

Figure 2. Output characteristics in the (A) hole and (B) electron accumulation regimes and (C) transfer characteristics at (black) $V_{DS} = -2$ V and (red) $V_{DS} = +2$ V of an ambipolar, PbSe SNW FET. (D) Schematic band diagram of an ambipolar SNW FET. LUMO is the lowest unoccupied molecular orbital, HOMO is the highest occupied molecular orbital, E_F is the Fermi energy, Φ_m is the work function of metal, Φ_{Be} is the electron barrier height, Φ_{Bh} is the hole barrier height, χ is the electron affinity of the PbSe NW.

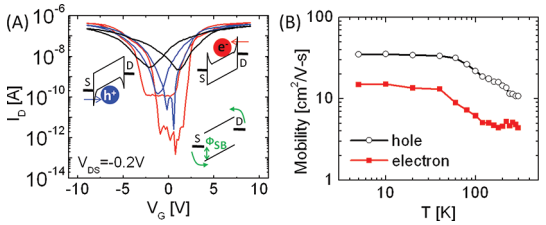

Figure 3. Ambipolar PbSe SNW FET (A) transfer characteristics at 4.5 K (red), 140 K (blue), and 298 K (black) and (inset) schematic band diagrams as a function of V_G and (B) electron mobility and hole mobility as a function of temperature.

vacuum after annealing. The threshold voltage shifted slightly further toward negative voltages, consistent with further oxygen desorption, and then the ambipolar behavior remained stable as studied for more than a few weeks under vacuum.

There were noticeable changes observed before and after annealing. As the electron current increased with annealing, the hole current decreased, and the I_{ON}/I_{OFF} was limited to $\sim 10^2$. Statistics extracted from the I_D-V_G characteristics of tens of SNW FETs show electron and hole saturation mobilities of $6(\pm 2)$ cm^2/(V·s) and $9(\pm 2)$ cm^2/(V·s), respectively. The change in electron and hole current levels are consistent with a shift in the Fermi energy toward midgap as oxygen acceptors are removed and the NW is dedoped.[15] Given the simplified electronic structure of PbSe and the similar bulk effective masses[24] and carrier mobilities, the ambipolar characteristics suggest the barriers to electron and hole injection are comparable (Figure 2D). As the NW FETs are annealed to become ambipolar, the I_D-V_{DS} characteristics show greater nonlinear behavior and are more closely spaced at low-voltages, consistent with current crowding and increased barriers to carrier injection.

Representative temperature-dependent transfer characteristics between 4.5 and 298 K for ambipolar SNW FETs are shown for a subset of measured temperatures in Figure 3 and for the full range of collected temperatures in the Supporting Information, Figure S2. At room temperature, the device I_{ON}/I_{OFF} is *ca.* 10^2-10^3 while at 4.5 K I_{ON}/I_{OFF} is $>10^6$. A noticeable phenomenon is that the device shows a different dependence of current on temperature when the FET is in the *ON* state as opposed to in the *OFF* state (Figure 3A). The current level increases as the temperature decreases in the *ON* state (both at high positive V_G in electron accumulation and at high negative V_G in hole accumulation), while the current level decreases as temperature decreases in the *OFF* state at low $|V_G|$. We model the behavior by a SB FET[25] where the total current is controlled by charge injection, which is limited by the metal-semiconductor barrier, as well as charge transport through the NW. In the *ON* state, particularly for FETs with thin gate dielectrics, high applied gate fields thin the SB at the

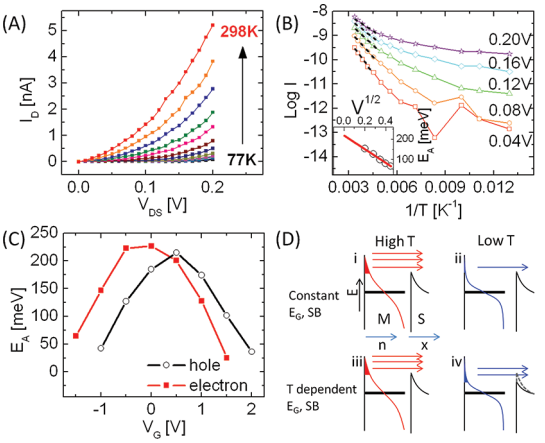

Figure 4. (A) I_D-V_{DS} curves at V_G = 0.2 V at temperatures between 77 and 298 K. (B) Arrhenius plot of I_D at different V_{DS} and (inset) the activation energy as a function of $V_{DS}^{1/2}$. (C) Calculated barrier heights as a function of V_G. (D) Schematic band diagrams of the metal−semiconductor interface representing charge injection for constant energy gap materials at (i) high and (ii) low temperature and for materials with a positive dE_G/dT at (iii) high and (iv) low temperature. M is metal, S is semiconductor, E is energy, n is number of electrons, and x is distance. Red and blue lines indicate the electron distribution[35] versus energy at high temperature and low temperature, respectively, and the arrows indicate the amplitude of electron injection from metal to semiconductor.

metal−semiconductor interface, removing the barriers to charge injection. As seen in the inset of Figure 3A, high negative (positive) gate voltage pulls the bands up (down), narrowing the barrier to allow the tunneling of holes (electrons). In this ON state, drain current is controlled by charge transport through the NW. The ON current increases as temperature decreases, which indicates band conduction transport where carrier scattering dominates, as commonly seen in inorganic semiconductors[26] and single crystalline PbSe.[10,27]

However, in the *OFF* state the current level at low temperature is lower than that at high temperature. The decrease in the current in the *OFF* state is attributed to limited charge injection from the SB.[28] In the absence of a high gate bias, the barrier is not thin enough for tunneling to occur and thus carrier injection is limited by the SB. For example, at low negative gate bias, the hole current is blocked by the SB at the source as shown in the inset of Figure 3A. In this regime, thermionic emission over the barrier is the limiting step to reduce the drain current. The same behavior can be seen in an earlier work by Liang *et al.*,[4] although it was not described in detail, and we propose that it is attributed to SB control. It should also be mentioned that the temperature-dependent PbSe NW FET behavior is different from that of PbSe NC FETs.[12] In reported temperature-dependent charge transport studies of ethanedithiol-treated PbSe NC thin films by Kang *et al.*, currents in both the *ON* state and *OFF* state decrease with decreasing temperature as conduction is controlled by thermally activated hopping

between NCs. In the single crystalline PbSe NWs reported here, carriers are transported through the bands of the NWs, and the role of SB can be easily separated. Since the SBs limit charge injection, linear electron and hole mobilities cannot be extracted. Therefore, electron and hole mobilities were calculated in the saturation regime (*ON* state). As temperature decreases from 298 to 4.5 K, for ambipolar SNW PbSe FETs saturation mobilities of electrons and holes increase monotonically from 6(±2) to 15(±2) $cm^2/(V \cdot s)$ and from 9(±2) to 40(±4) $cm^2/(V \cdot s)$, respectively (Figure 3B). It should be noted that the carrier mobilities in PbSe NWs are lower than those found in Hall measurements of bulk PbSe. The measured and calculated PbSe NW carrier mobilities are effective mobilities rather than true mobilities since they may be limited by (i) charge injection due to the metal−semiconductor SB, and (ii) the cylinder-on plate model eq 1[29] which is reported to provide a lower bound in extracting carrier mobility. The mobilities may also be limited by (iii) surface scattering in these high surface-to-volume materials.

The I_D-V_{DS} curves at different temperatures in the electron and hole accumulation regimes show the nonlinear, Schottky behavior (Figure 4A and Supporting Information, Figure S3). The SB height can be extracted from the equation for thermionic emission[30]

$$I = A^{**}T^2 \exp[-q(\phi_B - (qE/4\pi\varepsilon_s)^{0.5}/k_BT)] \quad (3)$$

where A^{**} is the effective Richardson's constant, k_B is Boltzmann's constant, q is electric charge, ϕ_B is the Schottky barrier height, and E is the electric field. Figure 4B is the Arrhenius plot of the data obtained from Figure 4A. The actual barrier height was calculated from the extrapolation of the plot inset in Figure 4B since activation energy, E_A, is proportional to $V_{DS}^{1/2}$ due to image force lowering.[26,30] The electron and hole barrier heights depend on the gate bias, as the gate bias acts to pull down the barrier at the metal−semiconductor interface [Figure 4C]. The barrier height attains its maximum value around $V_G = 0$. As the gate bias deviates from $V_G = 0$, the effective barrier height decreases to zero and goes to negative values as it thins to where carrier tunneling through the barrier starts to dominate.[31] The electron and hole barrier heights, independently calculated from the data in the Arrhenius plots, were found to be 225 and 215 meV, respectively. The sum of the barrier heights is similar to the 0.44 eV bandgap of these 10 nm diameter PbSe NWs measured from their optical absorption spectrum[7] [Supporting Information, Figure S4], as we expect ($E_g = \phi_{Be} + \phi_{Bh}$)[26] and is illustrated in the schematic band diagram (Figure 2D). The band alignment and SB formation is consistent with the balanced electron and hole current levels and similar carrier mobilities. We previously reported cyclic

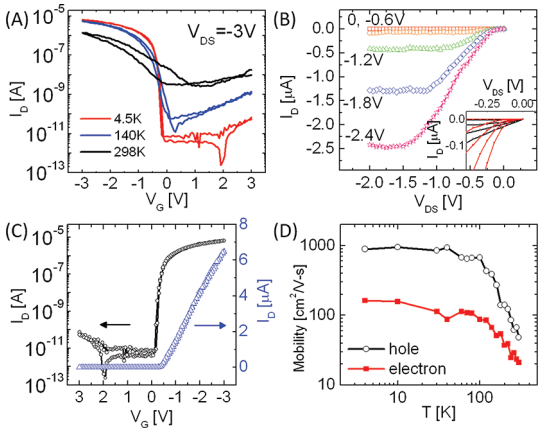

Figure 5. p-Type PbSe SNW FET (A) transfer characteristics at 4.5 K (red), 140 K (blue), and 298 K (black); (B) output characteristics at 4.5 K. Inset magnifies the low voltage region of the I_D-V_{DS} characteristics at 4.5 (red) and 298 K (black). (C) Transfer characteristics at 4.5 K. (D) Saturation mobility as a function of temperature for holes in a unipolar p-type and electrons in a predominantly n-type PbSe SNW FET.

voltammetry measurements to characterize the energies of the HOMO and LUMO levels of PbSe NWs. The HOMO and LUMO levels of predominantly p-type NWs, as-synthesized and washed with ethanol to remove surface bound ligands, are 4.62 and 4.17 eV, respectively; whereas surface treatment with hydrazine converts NW devices to predominantly n-type and shifts the energy levels to 5.01 and 4.56 eV, respectively.[7] The estimated 5.1 eV work function of Au for these top-contact single PbSe NW FETs is well below that of the energy levels of the NWs and suggests that the origin of SB is Fermi level pinning. The Schottky barrier may arise from defects introduced by metal deposition in top contact devices.[26,32] In addition, for compound semiconductors with small electronegativity differences (where ΔX is the difference in electronegativities of the elements), as is the case for PbSe with ionicity $\Delta X = 0.22$ well lower than the characteristic $\Delta X < 1$,[26] barrier height is known to be weakly dependent on metal work function due to surface effects or pinning of the surface Fermi level. The observed SB is also consistent with the study of Luther *et al.*[33] on PbSe NCs which show weak dependence on metal work function and surface Fermi Level pinning that follows the Schottky model. In Figure 4B, the slope of the Arrhenius plot decreases as temperature decreases, suggesting the SB height also decreases. It is accordant with the work of Boercker *et al.*[34] that the band gap of PbSe NWs decreases as temperature decreases. The temperature-dependent slope can be understood by a thermionic emission model with a temperature-dependent SB height. In materials with a temperature independent bandgap and SB height, as the temperature decreases from (i) high to (ii) low temperature (Figure 4D), the amount of injected electrons only depends on the electron distribution according to the Fermi Dirac

distribution,[35] resulting in a linear slope in the Arrhenius plot. In contrast, PbSe NWs with a large positive dE_G/dT,[34] are expected to show a different behavior. As the temperature decreases from (iii) high to (iv) low temperature, (Figure 4D) the SB height is reduced (iv) and therefore more carriers have sufficient energy to overcome the barrier, giving rise to the nonlinear slope in the Arrhenius plot. Despite the reduced SB height, however, current injection is limited at low temperature by the low carrier concentration.[35] While we report that PbSe NWs show SB behavior, it should be noted that SBs were not observed in bulk PbSe with Au contacts. We attribute this difference to the smaller bandgap and higher carrier concentration of bulk PbSe.[9,11]

Using this PbSe SNW FET platform, we explored charge injection and transport in the NWs as a function of doping. Figure 5A shows the temperature-dependent transfer characteristics of a representative p-type PbSe SNW FET which was obtained by oxygen doping *via* 30s of UV−ozone exposure.[7,36] The complete set of temperature-dependent transfer characteristics collected between 4.5 and 298 K are shown in Supporting Information, Figure S5. Similar to ambipolar NWs, p-type NWs also behave as SB FETs. The more severe "current crowding" behavior at low temperature (inset Figure 5B) reflects larger barriers to charge injection. Using temperature-dependent I_D-V_{DS} characteristics, we extract the SB for holes as 185 meV, smaller than the SB for holes found for the ambipolar SNW FETs. At 4.5 K a higher I_{ON}/I_{OFF} of $\sim 10^7$ and lower subthreshold swing of ~40 mV/dec than at room temperature (Figure 5C) are attributed to these SB FET characteristics and band conduction transport. At low temperature, the SB height limits the current at low V_G in the OFF state and as V_G increases the SB becomes thinned in the ON state, allowing hole tunneling and giving rise to a dramatic increase in current. At low temperature (<100 K), all hysteresis is eliminated, indicating that trap sites[15] are frozen out. The maximum current for a single NW is ~10 μA, corresponding to 1−2 orders higher current density of 10MA/cm^2 than previously reported for PbSe NWs.[3] The hole mobility of p-type PbSe NWs, calculated in the saturation regime, is plotted as a function of temperature in Figure 5D. The hole mobility increased monotonically with decreasing temperature from 65(±10) cm^2/(V·s) at room temperature to 1000(±100) cm^2/(V·s) at 30 K where it starts to saturate. The mobility increase between 200 and 300 K shows a $\sim T^{-2.2}$ power law dependence akin to the power law dependence of $\sim T^{-2.1-2.5}$ for bulk PbSe.[9,11] Similarly, ambipolar predominantly n-type FETs are prepared by annealing the SNW PbSe FETs at 200 °C for 10 min and immediately transferring (see Method section) them to the vacuum chamber to avoid oxygen exposure. Output characteristics and temperature-dependent transfer characteristics are shown in Supporting Information, Figure S6. The electron mobility of predominantly n-type FETs as a function of temperature is shown in Figure 5D and the SB height for the electrons and holes are extracted as 190 and 230 meV, respectively. The observed trend in SB height for p-type, ambipolar, and predominantly n-type PbSe NW FETs shows a weak decrease in barrier height for the majority carrier and corresponding increase in barrier height for the minority carrier height as the NW doping is tailored.

In ambipolar, predominantly n-type, and unipolar p-type PbSe SNW devices, electron and hole mobilities increased monotonically with decreasing temperature and saturated at temperatures less than ~30 K. There were no signatures of impurity scattering observed which commonly limits carrier mobilities at low temperatures in substitutionally doped NWs while other NWs[37,38] show higher impurity scattering at low temperature. While mobility decreases as temperature decreases in the case of most PbSe thin films and PbSe NCs mainly due to grain boundaries,[17,39] dislocations,[9] defects,[11,17] and thermally activated hopping mechanisms,[12] our data shows that the mobility of PbSe NWs increases monotonically as temperature decreases, which is limited at high temperatures by phonon scattering. To the best of our knowledge, this is the first report to show that nanoscale lead chalcogenides behave like single crystals without showing the effects of defects or grain boundaries. We also show that stoichiometric imbalance, which gives rise to the predominantly n-type characteristics, in which excess Pb acts as an ionized impurity,[15,27] does not contribute to scattering down to ~30 K, in accordance with bulk lead salts.[9] Moreover, we found that the introduction of surface oxygen which dopes PbSe NWs p-type[8,15] acts as a remote dopant, leaving the PbSe NW channel free of impurities with no evidence of scattering to limit carrier mobility. Remote doping by introducing surface species is akin to "modulation doping" in modulation-doped FETs (MODFET)[26] where charge maybe transferred without introducing impurities.

CONCLUSIONS

We have studied the physics of charge injection and charge transport using p-type, predominantly n-type, and ambipolar, 10 nm diameter single PbSe NW FETs, which is one of the most strongly confined systems that has been studied, particularly in 1D. Using temperature-dependent electrical measurements of single NW FETs, we show for the first time that PbSe NW FETs operate as SB FETs. PbSe NWs behave as single crystals without defects which have not been reported previously in nanostructured lead chalcogenides. We show that remote doping in nanostructured lead chalcogenides promises an attractive route to apply

more broadly in achieving high mobility n- and p-type materials without suffering from impurity scattering. Engineering the metal-semiconductor interface to lower the barriers to charge injection and reduced scattering through charge transport in remotely doped, single crystalline nanostructures are essential for the application of PbSe NWs in thermoelectrics and near-infrared photodetectors.

METHODS SECTION

Materials for Nanowire Synthesis. All manipulations were carried out using standard Schlenk-line techniques under dry nitrogen. Tri-*n*-octylphosphine (further referred to as TOP, Aldrich, 90%), diphenyl ether (Aldrich, 99%), oleic acid (OA, Aldrich, 90%), amorphous selenium pellets (Aldrich, 99.999%), lead acetate trihydrate (Fisher Scientific Co.), and *n*-tetradecylphosphonic acid (TDPA, Strem, 97%) were used as purchased without further purification. Anhydrous chloroform and hexane were bought from Aldrich. To prepare a 0.167 M stock solution of trioctylphosphine selenide (TOPSe), 1.32 g of selenium was dissolved in 100 mL of TOP with overnight continuous stirring.

Synthesis. The synthesis is based on a previous report.[7,13] A 0.76 g portion of lead acetate trihydrate was dissolved in 10 mL of diphenyl ether and 2 mL of OA. The solution was then heated to 150 °C for 30 min under nitrogen flow to form a lead−oleate complex. After the mixture was cooled to 60 °C, 4 mL of 0.167 M TOPSe solution was slowly added to prevent premature nucleation of PbSe. The mixed lead−oleate/TOPSe solution was quickly injected under stirring into a hot (250 °C) growth solution containing 0.2 g of TDPA dissolved in 15 mL of diphenyl ether. After ∼60 s of being heated, the reaction mixture was cooled to room temperature using a water bath. Once cooled, the reaction vessel (still under N_2) was transferred to a glovebox, where the crude solution was mixed with equal amounts of hexane, and the nanowires (NWs) were isolated by centrifugation at 4000 rpm for 5 min. The resulting NW precipitate was then redispersed in chloroform for further characterization.

Device Fabrication. FETs were fabricated on heavily n-doped silicon wafers with 15 nm thermally grown SiO_2. A 100 nm SiO_2 layer was defined by photolithography and deposited by e-beam evaporation to reduce the gate leakage between subsequently deposited large area contact pads and the gate electrode. To reduce hysteresis[15] and further minimize gate leakage, 10 nm Al_2O_3 was deposited uniformly across the wafer using atomic layer deposition. Photolithography and electron beam lithography were employed, respectively, to pattern large metal contact pads (5 nm Ti/145 nm Au) and electrodes (1 nm Ti/19 nm Au) bridging the large contact pads and source and drain electrodes, described below. Devices were cleaned with acetone, isopropyl alcohol, and deionized water and further treated with oxygen plasma. Straight PbSe NWs were dispersed in octane/chloroform (1:3 vol/vol) mixture, and several drops of 10 wt % solution of hexadecene-graft-polyvinylpyrrolidone copolymer in nonane was added to improve the NW dispersibility. A 5 μL aliquot of the NW dispersion was dropcast between contacts. To remove excess ligands, devices were washed with ethanol and chloroform.[7] Devices were soaked in 2 M hydrazine (Aldrich, 98%) in acetonitrile (Aldrich, anhydrous, 99.8%) (*NOTE: hydrazine is toxic by vapor inhalation and skin absorption*) for 1 h and evacuated for 1 h. Poly(methyl)methacrylate (PMMA from Microchem) was spincast on the devices, and the location of the NW was recorded using an optical microscope. Top contact, 30 nm Au source, and drain electrodes separated by 2−5 μm channel lengths were defined by e-beam lithography and deposited by e-beam evaporation to contact the ends of the NWs with the bridging electrodes previously fabricated on the Si wafer, followed by lift-off with anhydrous solvents in a glovebox. The capacitance of the gate dielectric stack was measured to be 215(±4) nF/cm^2 by HP 4276A LCZ meter.

FET Characterization. Device characterization was carried out on a model 4156C semiconductor parameter analyzer (Agilent) in combination with a Karl Suss PM5 probe station mounted in the nitrogen glovebox. Temperature-dependent device characteristics were measured in a Lakeshore Cryotonics (formerly Desert Cryogenics) probe station equipped with a model 4156C semiconductor parameter analyzer. Sample were sealed with a glass coverslip using epoxy (ITW Devcon) and transferred to the Lakeshore Cryotonics vacuum, cryogenic probe station. Once under high vacuum, the epoxy seal was broken upon cooling to low temperature (at ∼200 K) and the sample was kept under vacuum for all reported measurements. Measurements were performed under high vacuum (∼10^{-6} Torr) and at varying temperatures between 4.5 and 298 K by introducing liquid helium.

Conflict of Interest: The authors declare no competing financial interest.

Acknowledgment. S.J.O. and C.R.K. acknowledge support by the U.S. Department of Energy, Office of Basic Energy Sciences, Division of Materials Sciences and Engineering (Award DE-SC0002158) and D.K.K. and C.R.K. acknowledge support from the NSF (NSF DMR-0805155).

Supporting Information Available: Detailed and output characteristics and transfer characteristics of pristine p-type and predominantly n-type PbSe NW FETs. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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