Y-Contacted High-Performance n-Type Single-Walled Carbon Nanotube Field-Effect Transistors: Scaling and Comparison with Sc-Contacted Devices

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ABSTRACT

While it has been shown that scandium (Sc) can be used for making high-quality Ohmic contact to the conduction band of a carbon nanotube (CNT) and thus for fabricating high-performance n-type CNT field effect transistors (FETs), the cost for metal Sc is currently five times more expensive than that for gold and one thousand times more expensive than for yttrium (Y) which in many ways resembles Sc. In this Letter we show that near perfect contacts can be fabricated on single-walled CNTs (SWCNTs) using Y, and the Y-contacted CNT FETs outperform the Sc-contacted CNT FETs in many important aspects. Low-temperature measurements on Y-contacted devices reveal that linear output characteristics persist down to 4.3 K, suggesting that Y makes a perfect Ohmic contact with the conduction band of the CNT. Self-aligned top-gate devices have been fabricated, showing high performance approaching the theoretical limit of CNT-based devices. In particular a room temperature conductance of about $0.55G_0$ (with $G_0 = 4e^2/h$ being the quantum conductance limit of the SWCNT), threshold swing of 73 mV/decade, electron mobility of 5100 cm^2/V·s, and mean free length of up to 0.639 μm have been achieved. Gate length scaling behavior of the Y-contacted CNT FETs is also investigated, revealing a more favorable energy consumption and faster intrinsic speed scaling than that of the Si-based devices.

One of the crucial issues in the development of large scale integrated (LSI) circuits is the fabrication of Ohmic contacts that are used by the millions in integrated circuits to contact sources and drains of metal-on-semiconductor (MOS) field-effect transistors (FETs).[1] Ohmic contacts serve the purpose of carrying electrical current into and out of the semiconductor, ideally with no parasitic resistance. Since the RC time constant associated with the contact resistance can limit the frequency response of the devices, low resistivity Ohmic contacts are essential for high-frequency operation. In theory it seems that an Ohmic contact to an n-type (or p-type) semiconductor can be made by simply using a metal with a work function close to or smaller (larger) than the band edge of the conduction (valence) band of the semiconductor. But this has never been realized for both the valence and conduction bands in bulk semiconductor. Fermi pinning induced by charge traps at the metal/semiconductor interface typically results in a Schottky barrier regardless of the Fermi energy alignment between metal and semiconductor.[2] In practice the only way to make an Ohmic contact is to use a heavily doped (degenerated) semiconductor. Fortunately, in carbon nanotube[3] (CNT) based nanoelectronics,[4-6] it has been found that Pd can make a barrier-free contact to the valence band of the CNT (with a moderately large diameter of d >1.5 nm) to make p-type CNT FETs,[6-8] and Sc can make perfect Ohmic contact to the conduction band to make n-type CNT FETs.[9-12] For both p- and n-type FETs, near perfect performance approaching theoretical limit has been realized.

While resources of Sc are abundant, Sc is rarely concentrated in nature because of its lack of affinity to combine with the common ore-forming anions and has been produced exclusively as a byproduct during processing of various ores. According to the Commodity Statistics and Information published by the U.S Geological Survey Minerals Information Team[13] scandium ingot metal costs $152.00 per gram,
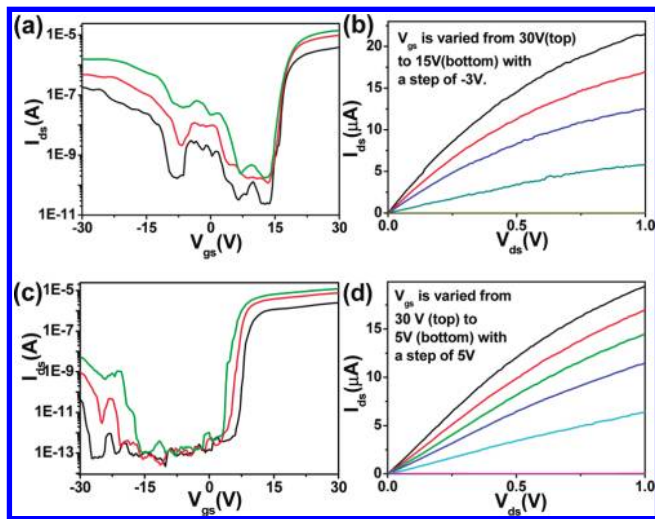
Figure 1. Performance of Y-contacted n-type bottom-gate CNT-FET (based on a CNT with a diameter of about 2 nm and a channel length $L_g \sim 2$ μm). Room temperature (a) transfer characteristics of the device for $V_{ds} = 0.5$, 0.3, and 0.1 V, respectively, from top to bottom. (b) Output characteristics of the device for V_{gs} varying from 30 (top, black) to 15 V (bottom, dark yellow) with a step of -3 V. Low temperature (4.3 K). (c) Transfer characteristics of the device for $V_{ds} = 0.5$, 0.3, and 0.1 V, respectively, from top to bottom at 4.3 K. (d) Output characteristics of the device for V_{gs} varying from 30 V (top, black) to 5 V (bottom, dark yellow) with a step of -5 V.

which is about five times more expensive than gold ($\sim$\$30.00) and 1000 times more expensive than yttrium metal, which in many ways resembles scandium.[14] Among other things, metal Sc (atomic number $Z = 21$) and Y ($Z = 39$) are in the same group IIIB (lanthanon elements), and both have the same crystal structure and similar low work function (3.3 eV for Sc and 3.1 eV for Y). In this Letter we show that Y can also be used most effectively for making Ohmic contact to the conduction band of the CNT, and in many ways the Y-contacted CNT FETs outperform the best n-type CNT devices.[10]

The carbon nanotubes used in this work are ultralong single-walled carbon nanotubes (SWCNTs) of a few hundred micrometers in length, which were directionally grown on heavily n-doped silicon substrate covered with a layer of insulating SiO_2 (500 nm) via catalytic chemical vapor deposition.[15] Y-contacted back-gate CNT FETs were fabricated based on these SWCNTs, and a typical transmission electron microscopy (TEM) image of a Y-coated SWCNT and a scanning electron microscopy (SEM) image of a back-gated CNT FET are shown in Figure S1 of Supporting Information. The basic room-temperature device characteristics are shown in parts a and b of Figure 1 for a CNT FET, which is based on a SWCNT with a diameter $d \sim 2$ μm and a channel length $L_g \sim 2$ μm. The transfer characteristics of the device (Figure 1a) were measured by sweeping V_{gs} from 30 to -30 V and at different V_{ds} (from top (green) to bottom (black), V_{ds} values are 0.5, 0.3, and 0.1 V, respectively), showing clearly that the Y-contacted CNT device is n-type FET which may be turned on by applying a large positive gate voltage, e.g., $V_{gs} = 30$ V, and turned off by reducing the gate voltage below 15 V. The current increases linearly

with V_{ds} at low bias (Figure 1b). The large saturation current of up to 20 μA in the output characteristic shows that the Y electrode forms an Ohmic contact with the conduction band of the CNT, and electrons may be injected into the CNT barrier freely at room temperature from the source Y electrode. Similar measurements were also carried out at low temperature (4.3 K), and these measurements show that the I_{on}/I_{off} ratio of the device was increased significantly from about $\sim 10^4 - 10^5$ at room temperature (Figure 1a) to become $\sim 10^7$ (Figure 1c) and that the linear output characteristic persists from room temperature (Figure 1b) down to 4.3 K (Figure 1d), suggesting that at low temperature ($\sim$4.3 K) electron injection from the Y electrode into the conductance band of the CNT is barrier-free and Y electrode forms an Ohmic contact with the conduction band of the CNT. The slight degradation of saturation current at 4.3 K compared to that at room temperature may be attributed to the weak localization due to defects which are unavoidable in CNT.[7] In additional to a long channel length ($\sim$2 μm) device, we also fabricated a short channel length device (with $L_g \sim 400$ nm) on the same CNT. The electrical properties are shown in Figure S2 of the Supporting Information. These device characteristics show clearly that at room temperature the device is an n-type FET with excellent I_{on}/I_{off} ratio of about $10^5 - 10^6$, the current I_{ds} increases linearly with increasing V_{ds} at low bias region and reaches about 24 μA at moderately high bias ($V_{ds} = 0.4$ V), and the on state conductance of the short channel device reaches $0.55G_0$ (with $G_0 = 4e^2/h$ being the quantum conductance limit of a SWCNT) suggesting near-ballistic transport of the Y-contacted short channel FET.

Figure 2a compares directly the device performance of a Sc- and Y-contacted CNT FETs. The two FETs were fabricated adjacent to each other on the same SWCNT with $d \sim 2.4$ nm and $L_g \sim 2$ μm. It is obvious that the transfer characteristics of these two kinds of devices are almost the same, including nearly the same subthreshold swing S, I_{on}/I_{off} ratio and on state current (actually the Y-contacted device has a slightly higher on state current than that of Sc-contacted device). Good air stability between metal/CNT contacts is desirous for further processes to fabricate high-performance top-gate devices and IC applications, especially for n-type FETs in which the reactive contact metal with low work function is needed.[9] The effects of environment on the Y-contacted n-type CNT FETs were investigated, and results for a typical device are shown in Figure 2b. The transfer characteristic of the device was measured in vacuum (about 10^{-8} Torr) immediately after the device was fabricated (blue curve). The device was kept in air without any passivation treatment for 1 week and was then measured in vacuum (green curve). The characteristic of the air-exposed device (Figure 2b) shows again typical n-type behavior without obvious performance degradation.

In general the ON-state current of a CNT FET depends on the diameter of the CNT. This is because the height of the Schottky barrier between metal and CNT depends on the diameter d of the CNT.[16,17] For a semiconducting CNT with $d > \sim 1.6$ nm, p-type Ohmic contacts can be made through contact with Pd or Rh metal,[7,16] and n-type Ohmic
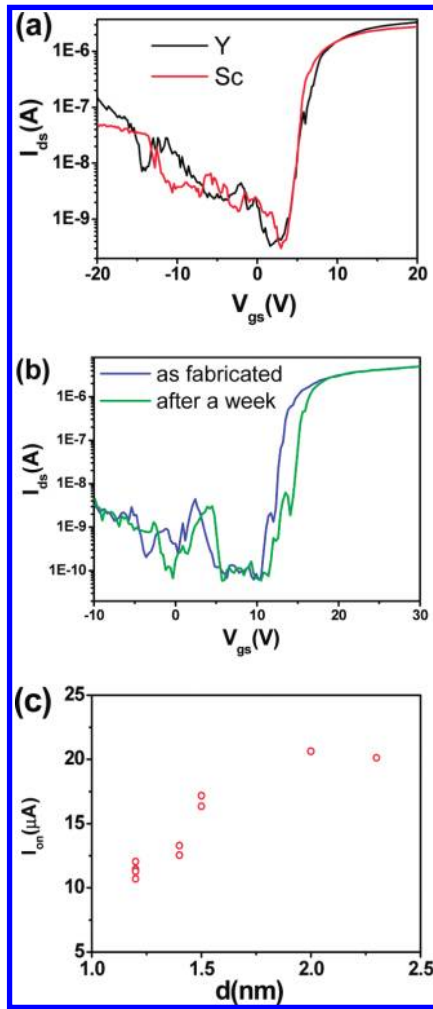
Figure 2. Transfer characteristics, stability, and diameter dependency of Y-contacted CNT FETs. (a) Transfer characteristics of Y-contacted (black curve) and Sc-contacted (red curve) FETs fabricated on the same CNT with $L_g = 2$ μm and $d \sim 2.4$ nm for $V_{ds} = 0.1$ V. (b) Transfer characteristics for another Y-contacted CNT FET with $d \sim 2.0$ nm and $L_g = 2$ μm for $V_{ds} = 0.1$ V. The blue curve was measured immediately after device fabrication. The device was then exposed in air for 1 week without any passivation treatment and protection. The green curve was measured a week later. (c) Dependence of on-state current I_{on} vs d for Y-contact CNT FETs with different diameters but same channel length of 0.5 μm. I_{on} values were all taken at $V_{ds} = 1.0$ V and $V_{gs} - V_{th} = 20$ V. The diameter of CNTs was measured by AFM.

contacts can be obtained through Sc contact.[9] But a Schottky barrier develops for smaller CNTs. Figure 2c shows the dependence of the ON-state current I_{on} for Y-contacted CNT FETs with different diameters d but the same channel length of 0.5 μm. The I_{on} hereon is defined as the current I_{ds} measured at $V_{ds} = 1.0$ V and $V_{gs} - V_{th} = 20$ V (V_{th} being the threshold voltage) and used as an indicator of the contact quality.[16] Figure 2c shows clearly that for CNTs with $d \geq$ 1.5 nm, the Y-contacted CNT FET has an ON-state current of about 20 μA suggesting zero or negligible Schottky barrier for the electron injection into the conduction band of the CNT. On the other hand, for CNTs with $d < 1.5$ nm, the ON-state current begins to degrade with decreasing diameter. Considering the measurement error associated with the CNT diameter d using atomic force microscopy (AFM), we
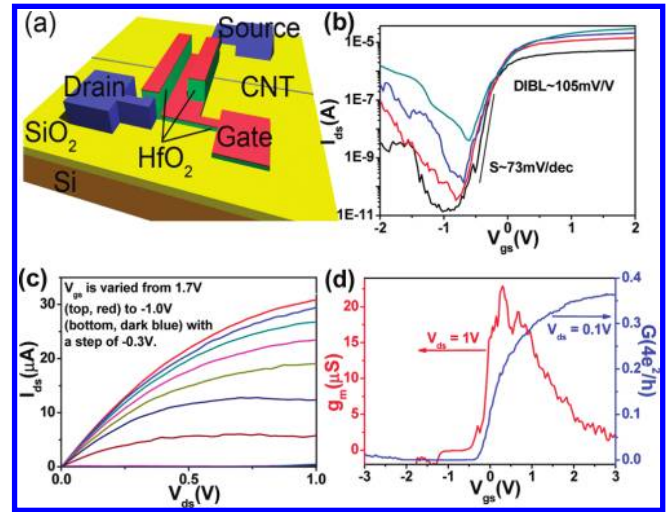

Figure 3. Performance of a Y-contacted top-gate CNT-FET device. (a) Depicted structure of the self-aligned top-gate CNT-FET device. (b) Transfer characteristics of an n-type CNT-FET with a channel length L about 800 nm for $V_{ds} = 1.0, 0.5, 0.3, 0.1$ V, respectively, from top to bottom. (c) Output characteristics of the device in which V_{gs} is varied from 1.7 (top, red) to -1.0 V (bottom, dark blue) with a step of -0.3 V. (d) Gate voltage-dependent conductance (G) (blue curve, right) and transconductance (g_m) under $V_{ds} = 1.0$ V (red curve, left).

conclude that the contact quality for Y/CNT is at least as good as that for Sc and Pd.[9,16,17]

A good FET should have a high on state current I_{on}, a low off state current I_{off}, and rapid transition between the on and off states (measured by the subthreshold swing S). While a bottom-gate FET (e.g., Figure 1) with a thick SiO_2 gate oxide can deliver high I_{on} and low I_{off}, it cannot rapidly switch between the on and off states, i.e., it usually has a rather large value of S (~ 400 mV/decade). To improve this situation, top-gate CNT FET devices were fabricated via the self-aligned process we developed earlier.[11] Briefly, this process takes advantage of the different grown mechanisms of gate oxide (conformal growth of HfO_2, via atom layer deposition (ALD)) and metal gate (direct deposition of Ti, via electron beam evaporation). While the ALD grown HfO_2 film presents even on the sidewalls of the Source (S) and Drain (D) electrodes (green colored regions, Figure 3a) which effectively insulates G (gate) from S and D, the Ti metal film grown via e-beam evaporation does not present on the sidewalls of the S and D electrodes so that the part of Ti film (red colored regions, Figure 3a) between S and D is disconnected from that on top of the S and D. Shown in parts b and c of Figure 3 are transfer and output characteristics of a so fabricated top-gate device which is based on a SWCNT (with $d \sim 2.3$ nm and $L_g \sim 0.8$ μm) and a gate oxide HfO_2 (with thickness $t \sim 15$ nm and $\kappa \sim 15$). The four transfer characteristics of Figure 3b correspond to V_{ds} = 0.1 V (black), 0.3 V (red), 0.5 V (blue), and 1 V (dark green), respectively. The subthreshold swing $S = \partial V_{gs}/\partial \log(I_{ds})$, which is the gate voltage necessary to change the drain current by a factor of 10, is about 73 mV/decade (when $V_{ds} = 0.1$ V), suggesting a near theoretical limit (~ 60 mV/ decade) rapid transition between the on and off states. In the sub- and near-threshold region, the $I_{ds} - V_{gs}$ character-
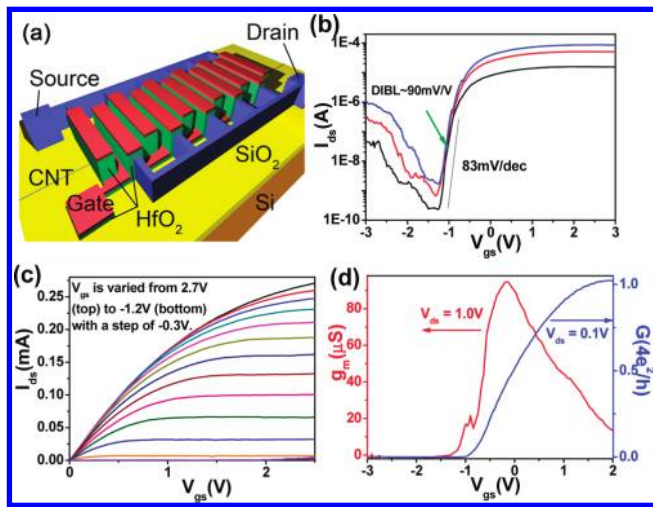
Figure 4. Performance of a finger-structured n-type CNT-FET device. The device is based on a CNT with a diameter of $d \sim 2.3$ nm, and the gate length for all channels is about 2 μm. (a) Depicted structure of the self-aligned top-gate finger-structured FET device. (b) Transfer characteristics of the device for $V_{ds} = 0.5, 0.3, 0.1$ V, respectively, from top (blue) to bottom (black). (c) Output characteristics of the device for V_{gs} varying from 2.7 V (top) to -1.2 V (bottom) with a step of -0.3 V. (d) Gate voltage-dependent conductance (G) (blue curve, right) and transconductance (g_m) under $V_{ds} = 1.0$ V (red curve, left).

istics are translated horizontally for different V_{ds}. This translation is caused by drain-induced barrier lowering (DIBL)[18] and is characterized by the number of millivolts of translation per volt of change in V_{ds}. The characteristics of Figure 3b show DIBL = 105 mV/V, suggesting that the device is a well-behaved FET in which the drain current I_{ds} is hardly affected by the drain voltage V_{ds}. The I_{on}/I_{off} ratio for a top-gate device is typically not better than that for a bottom gate device due to the thinner tunneling Schottky barrier for holes under large negative gate voltage. Nevertheless, Figure 3b shows that for this top-gate device, typical I_{on}/I_{off} ratio is more than 10^4 and at small bias value of 0.1 V this ratio indeed exceeds 10^5. The $I_{ds} - V_{ds}$ characteristics of Figure 3c show that at low bias the drain current I_{ds} increases linearly with increasing bias V_{ds} and reaches about 30 μA under $V_{gs} = 1.7$ V and that the channel conductance (the slop of the $I_{ds} - V_{ds}$ curve, see Figure 3d) increases monotonically with increasing gate voltage V_{gs} and approaches $0.37G_0$ at room temperature. Also shown in Figure 3d is the transconductance $g_m = \partial I_{ds}/\partial V_{gs}$, which has a high peak transconductance g_m of ~ 23 μS at $V_{gs} = 0.3$ V and $V_{ds} = 1.0$ V. The near theoretical limit performance of the top-gated CNT FETs shows that the fabrication process of the Y-contacted CNT FET is compatible to that of the ALD-grown high-κ HfO$_2$ gate insulator.

Finger-structured FETs can deliver large on state current and are widely investigated for rf power amplifications. Figure 4a depicts a multifinger CNT FET, which is composed of an array of 10 CNT FETs with a channel length of 2 μm on a single CNT. On one side of the CNT all electrodes are linked together as Source (Drain) while on the other side all electrodes are linked together as Drain (Source). Self-aligned gate structure is used, with a 15 nm thick gate oxide HfO$_2$

and 8 nm metal Ti gate.[11] In this device structure (Figure 4a), multiple top-gate Y-contacted n-type CNT FETs are connected in parallel to deliver a larger current than that which can be delivered by a single FET. The transfer characteristics of the devices are shown in Figure 4b for three $V_{ds} = 0.1$ V (black), 0.3 V (red), and 0.5 V (blue). The main advantage of this finger device is that it can deliver large on state current (over 250 μA, Figure 4c), while Figure 4b shows that its off state current is also very low ($\sim 10^{-10}$A) yielding a large I_{on}/I_{off} ratio of about 10^5 for $V_{ds} = 0.1$ V. The subthreshold swing S of about 83 mV/decade is slightly higher than that of a single device (Figure 3b), but the DIBL of 90 mV/V is much lower than that shown in Figure 3b due to the cooperation of 10 FETs. The on state conductance of the finger device reaches $1.022G_0$ at room temperature when $V_{gs} = 2.0$ V, and the peaks transconductance g_m is up to 95 μS at $V_{gs} = -0.15$ V under bias of 1.0 V.

The ultimate performance of the CNT FETs is reflected in the scaling behavior of the devices, especially on the gate length scaling. We fabricated Y-contacted top-gate CNT-FETs of different channel lengths (with $L_g = 50, 20, 10, 5, 2, 0.7, 0.5, 0.3$ μm) on the same CNT with $d \sim 2.3$ nm (an optical image showing the layout of these devices before the top-gate fabrication is shown in Figure S1c in Supporting Information) in order to understand how the performance of our CNT devices scales down as the gate length shrinks from 50 μm down to 0.3 μm. The transfer characteristics of five devices among these devices are shown in Figure 5a for simplicity. The field-dependent mobility may be calculated for a typical device (e.g., the one with $L_g = 5$ μm) using the experimental transfer characteristics via the relation[19] $\mu_{FE} = (L/C)\partial G/\partial V_{gs}$, and the result is shown in Figure 5b. The peak mobility value of up to 5100 cm^2/V·s is larger than all the published electron mobility values of n-type CNT FETs at room temperature, demonstrating the high quality of Ohmic contacts and ALD grown gate oxide. We define the on state resistance $R_{on} = V_{ds}/I_{ds}$ under low bias and at 3 V above the threshold voltage, i.e., at $V_{gs} = V_{th} + 3$ V. For a long channel device (e.g., for $L \geq 2$ μm, see the five right data points of Figure 5c), where the transport is in diffusive regime, the on state resistance R_{on} is expected to increase linearly with the channel length L_g. On the other hand, for a very short channel device (when the channel length is much smaller than the electron mean free path L_m), electron transport in the channel becomes a ballistic one and the channel resistance becomes independent of its length. In general the on state channel resistance of a CNT device can be described by[20]

$$R_{on}(L) = (h/4e^2)(L/L_m + 1) + R_{nc}$$

where h and e are the Plank constant and electron charge, R_{nc} is nontransparent contact resistance of the device. Normally the measured resistance contains two components: intrinsic resistance of carbon nanotube, contact resistance (R_c) consisting of quantum resistance $R_Q = h/4e^2$ and nontransparent resistance R_{nc}. In an ideal situation, the contact resistance is dominated by quantum resistance, namely, $R_c \sim R_Q = 6.5$ kΩ, and $R_{nc} \sim 0$. Figure 5c shows that all
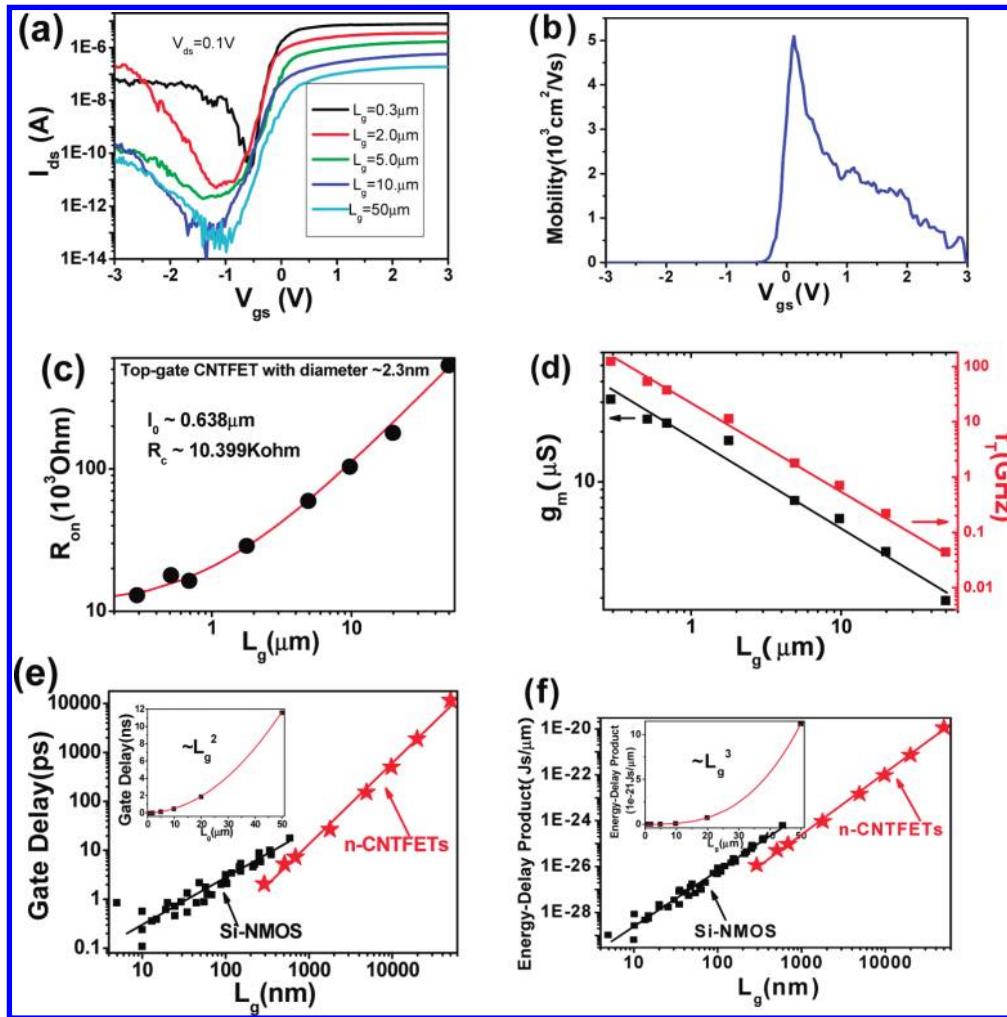
Figure 5. Scaling property of Y-contacted top-gate CNT-FETs. (a) Transfer characteristics of n-type CNT FETs fabricated on the same CNT ($d = 2.3$ nm) with different L_g. (b) A typical field-dependent mobility for the CNT FET with $L_g = 5.0$ μm in Figure 1a. (c) On-state resistance graph of different top-gate devices with different channel lengths. (d) Scaling property of transconductance (g_m) and cutoff frequency (f_T). (e) Scaling property of n-CNTFETs gate delay and comparison with that of Si-NMOS, inset is polynomial fitting of gate delay property in linear scale. (f) Scaling property of n-CNTFETs energy-delay product and comparison with that of Si-NMOS, inset is polynomial fitting of energy-delay product property in linear scale..

experimental data points can be modeled very well via this simple formula, yielding an electron mean free path $L_m = 0.638$ μm, a nontransparent resistance $R_{nc} = 5.6$ kΩ, and resistivity of the CNT $\rho = R_Q/L_m = 10.3 \pm 0.32$ kΩ/μm. These results show that among the eight devices investigated the one with the shortest channel length of 0.3 μm is clearly a ballistic device, while those with $L_g \gg L_m = 0.638$ μm are diffusive ones.

The transconductance $g_m = \partial I_{ds}/\partial V_{gs}$ of a device is closely related to its cutoff frequency $f_T = g_m/(2\pi C)$.[21] For estimating the ultimate performance of the CNT device, here we consider only the intrinsic gate capacitance C neglecting parasitic and other capacitances. The intrinsic C is the device capacitance including gate to CNT capacitance and quantum capacitance of CNT in series and is directly proportional to the channel length L_g, i.e., $C = cL_g$, with c being the unit capacitance. Since CNT has an extremely small capacitance C, the cutoff frequency f_T (Figure 5d) increases rapidly with decreasing channel length and reaches 123 GHz for $L_g \sim 0.3$ μm. It is expected that for a device with a channel less

than 100 nm, f_T could exceed terahertz.[21] A high f_T of up to 30 GHz has been revealed in high-frequency measurements.[22]

Two of the most important device metrics charactering the performance of a FET are gate delay and energy-delay product.[23] Gate delay reflects the intrinsic speed of a FET and may be estimated via $\tau = C*V/I_{on}$, while energy-delay product is closely related to the switching energy and is defined as τCV^2. These two metrics for our CNT FETs are shown in parts e and f of Figure 5, together with that of Si-based n-type FETs. All the data points are seen to fall very well on certain straight lines, revealing a clear channel length scaling trend. Parts e and f of Figure 5 show that while the energy-delay product for CNT devices decreases with channel length with a similar rate as that of the Si-based devices (Figure 5f), the gate delay of CNT devices decreases much more rapidly with decreasing channel length than that of the Si-based device (Figure 5e). For the shortest channel (with $L_g \sim 300$ nm) device investigated here, the gate delay is 2.06 ps and the energy-delay product is $1.16e^{-26}$ J s/μm. Continuing with this trend, it is expected that a 30 nm CNT

device could deliver a gate delay of $\sim$100 fs, which is among the shortest gate delay that has ever been achieved by a Si-based device for a channel length of less than 10 nm. For long channel devices, the gate delay scales with the channel length as $\sim L_g^2$, and the energy-delay product as $\sim L_g^3$. The inserts in parts c and d of Figure 5 are polynomial fittings of the gate delay and energy-delay product, showing that these quantities do scale with the gate length as expected.

In conclusion, almost perfect n-type CNT FETs have been fabricated using metal yttrium as the contacting metal electrode. While short channel devices exhibit ballistic transport with room temperature conductance of $0.55G_0$ (with $G_0 = 4\ e^2/h$) and linear input−output $I_{ds} - V_{ds}$ characteristic persisting down to 4.3 K, long channel devices show a gate length scaling that compares more favorably and decreases more rapidly for the gate delay metric with decreasing gate length than that for the Si-based devices, and the device characteristics are consistent with a mean free path of about 638 nm and an electron mobility of up to 5100 cm^2/V·s. The performance of the Y-contacted CNT FET is compared directly with that of the Sc-contacted CNT FET being fabricated on the same SWCNT adjacent to each other, and it is found that the Y-contacted CNT FETs outperform in many ways that of the Sc-contacted CNT FETs. Since yttrium is extremely cost-effective and widely used in industry, it is expected that the Y-contacted devices could be more suitable for fabricating large scale integrated nanoelectronics circuits.

Supporting Information Available: Typical TEM image of a Y-coated SWCNT and a SEM image of a back-gated CNT FET and figures showing the electrical properties of the CNT FET. This material is available free of charge via the Internet at http://pubs.acs.org.

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