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Coulomb blockade oscillations in ultrathin gate oxide silicon single-electron transistors

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Ultrathin oxide-gated (thickness ~6 nm) point-contact junctions have been fabricated to explore single-electron charging effects in strongly gate-dot-coupled polycrystallinesilicon transistors. Current–voltage (*I–V*) measurements show periodic current oscillations near room temperature. Analysis of the energy-level spacing relates the electron charging energy to a quantum dot of size ~8 nm, and also suggests electron tunneling is via the first excited state. These low-power ~30 pW and low-cost devices can be useful for the next generation nanoelectronics. © *2005 American Institute of Physics*. [DOI: 10.1063/1.1921335]

The realization of room-temperature quantum dot single-electron transistors (SETs) by utilizing the Coulomb blockade effects in nanostructures has attracted much research attention during the past decades. Its objective is to enable next generation low-power electronics. Tremendous success has been achieved to minimize the dot size down to ~sub-10 nm by developing various nanostructures such as point-contact junctions,[1] abacus bead-shaped constrictions,[2,3] and as well as straight nanowires[4] based on metal-oxide-semiconductor devices on silicon-on-insulator (SOI) wafers. These devices, in particular, have led to the observations of single-electron charging and switching at high temperatures.

Besides the criticalness of the quantum dot, another key factor, which generally is overlooked, that can trigger quantum oscillations is the gate-dot coupling strength α. This parameter basically controls the efficiency of converting electrical voltage on the gate into quantum excitation in the dot, thereby switching the transistor on and off. Determination of this factor is important in order to correlate the charging energy to the dot size. Technically, it is controlled by the thickness of a very thin oxide layer in between the dot and the gate electrode. For devices that have been fabricated and reported in the literature, the thickness has been found ranging from 50 nm (Ref. 1) to 25 nm (Refs. 2 and 3), yielding $0.05 \leqslant \alpha \leqslant 0.08$. As a result of the relatively large thickness compared to the dot size of ~10 nm, one always finds that most observations of the oscillations in *I–V* characteristics are claimed at high gate bias. The inability to control the manifestation of quantum excitation at low bias definitely impedes their applications in the package of high density. Hence, it is necessary to have the gate oxide as thin as possible while maintaining its high quality. Accordingly, in this study we try to explore a more sophisticated SET with oxide thickness down to sub-10 nm. Our experimental data shows very promising results, thus highlights the importance of using thin oxide in these devices for room-temperature operation.

Our transistors, as shown in Fig. 1(a), were fabricated on *p*-type (100) silicon wafers by using the technique of *e*-beam lithography that was reported earlier.[5] First, a thin polycrystallinesilicon layer of ~25 nm thick was deposited in low-pressure chemical vapor deposition (LPCVD) system in a

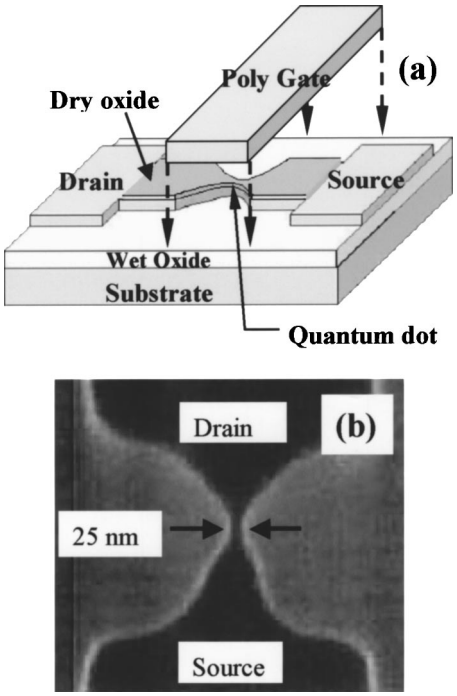

FIG. 1. (a) Schematic drawing of the point-contact transistor with a thin gate oxide. The device is built on a thick wet oxide layer over a dummy wafer. The thin oxide layer ~6 nm serves to effectively couple the gate energy to a quantum dot in the junction. (b) A scanning electron microscope (SEM) picture of the junction after chemical etching but before oxidation. Note that the junction width is found to be ~25 nm.

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mixed gas of SiH_4 and PH_3 onto a 200-nm-thick wet oxide. The sheet resistance of this layer was characterized at $\sim 30\ \Omega/\square$ reflecting a low doping level of $\sim 1\times 10^{17}\ cm^{-3}$. Nanojunctions, as shown in a microscopic view in Fig. 1(b), can be consistently created by proximity effect and reactive ion etching (RIE). The typical junction after etch was controlled to the size of ~40 nm long and ~25 nm wide. After that, a high-quality silicon dioxide layer of ~6 nm thick was then grown out of the layer using dry oxidation in rapid thermal annealing (RTA) at ~925 °C for 150 sec. Because of the importance of the gate oxide, its thickness was carefully examined by an ellipsometer with a resolution of 0.5 nm. This oxidation procedure can further reduce the junction width down to ~15 nm. A top-gate electrode of polycrystallinesilicon (50-nm thickness) was then applied, with its width controlled at ~200 nm. Finally, the passivation of a silicon glass layer of 200 nm from tetraethylorthosilicate (TEOS), drilling of contact holes, and metalization of Al pads were implemented.

Electron-transport measurements were conducted at temperatures from 300 to 100 K. Devices were loaded in a probe station and pumped down to a low pressure of 100 mtorr. The sample stage was cooled in a helium bath and the device temperature was monitored with a carbon-glass thermometer over the range of 300–40 K. Device temperatures were stabilized electronically with a heater, and in this range, the absolute measurement accuracy was 0.5 K. The equipment used for current–voltage measurements was a three-terminal Keithley 4200 with a 1-μV absolute voltage resolution and 100-fA current resolutions.

Granular silicon is known to be very sensitive to the conditions of doping levels and thermal treatments during fabrication. Therefore, prior to more advanced *I–V* measurements, our SETs were checked to meet the following criterions: the junction width must be <30 nm and the drain-source current I_d falls in the range $0.5\ nA < I_d < 10\ nA$, under the condition that $V_g = 1$ V and $V_{ds} = 10$ mV were applied. We found that over several hundreds piece of devices tested, only few showed good consistency and the data presented was chosen from these high-quality samples. It should be noted that although the thin oxide obviously provides an advantage to explore low bias charging, care must be taken in order to avoid excess charge breakdown, which was found at about 2 V.

In Fig. 2, the *I–V* characteristics of a high-quality SET taken at high temperatures clearly exhibit periodic staircases and oscillations. The most outstanding feature found here is the collapse of the many peak's maximums at different temperatures, which strongly implies electrons tunnel through a quantum dot in sequence in the junction.[2,6,7] To specify the dot size, one has to find out the energy spacing $\Delta E = \alpha e \Delta V_g$ and the α in the first place. According to the linear-response theory of Coulomb blockade,[8] α is a reciprocal function of the peak's full width at half maximum (FWHM), i.e, $FWHM = 3.5K_BT/(\alpha e)$, where K_B is the Boltzman constant, T is temperature, and e is the free-electron charge. As shown in Fig 3, we find a linear dependence of the FWHM and the slope yields an $\alpha \sim 0.6$. This value is impressive and very large compared to most values reported previously.

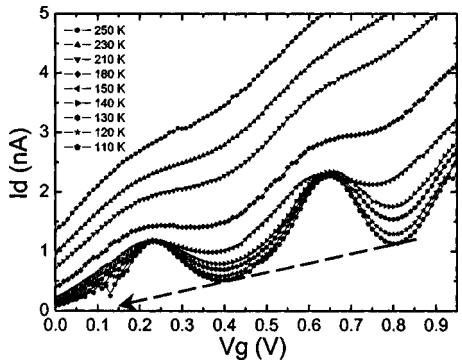

FIG. 2. Dependence of the drain current I_d on gate voltage V_g for a drain-source bias at 10 mV. The temperature is reduced from 250 to 110 K. The abrupt drain current jumps at 110 K is the random telegraph noise.

When the temperature is further reduced, we find that $\alpha(T)$ becomes nonlinear and the effects of multiple grains dominate, suggesting a much stronger intergrain coupling, to be discussed in detail elsewhere. Given the peak separation $\Delta V_g \sim 0.4\ V$ and the $\alpha \sim 0.6$, ΔE is therefore derived of ~240 meV.

It is also known that ΔE includes both the Coulomb charging energy ($E_C = e^2/2C_g$) and the quantum confinement energy E_Q, as expressed in Eq. (1), where $C_g = 4\pi\varepsilon d(1+\beta)$ is the capacitance of the dot sitting above a grounded substrate,[9] in which d is the dot radius, $\varepsilon = 1/36\pi \times 10^{-9}$, $\beta = d/2l$, and $l = 200$ nm being the distance between the dot and the substrate. The second term is the quantization of energy of a single particle in a three-dimensional potential well sized $2d$ and the ground state is [1,1,1]. Assuming that the charge tunneling process is via the first excited state of [1,1,2], $n_z = 2$ is in the direction of charge tunneling. Under the assumption, we can simplify ΔE as $740/d + 93(n_x^2 + n_y^2 + n_z^2)/d^2$ by substituting all the parameters into Eq. (1) in units of meV and d is in nanometer. By matching the value of 240 meV to the formula $\Delta E(1,1,2)$, d is determined of ~4 nm; so does the C_g of ~1 aF.

$$E(n_x, n_y, n_z) = \frac{\pi^2\hbar^2}{8md^2}(n_x^2 + n_y^2 + n_z^2). \tag{1}$$

The drain and source capacitances, C_d and C_s, of the dot can be probed as well with the voltage applied on the drain.

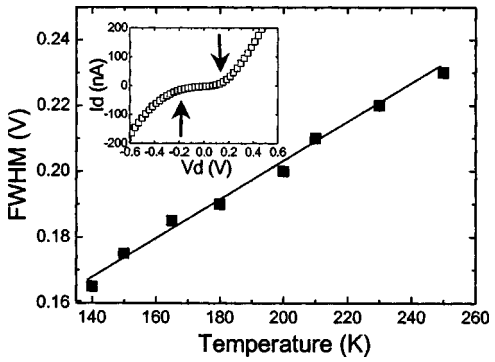

FIG. 3. Temperature dependence of the FWHM of the second peak derived from the data in Fig. 2 and a linear curve fit. Inset shows the data of I_d–V_d, and the Coulomb thresholds marked by arrows.

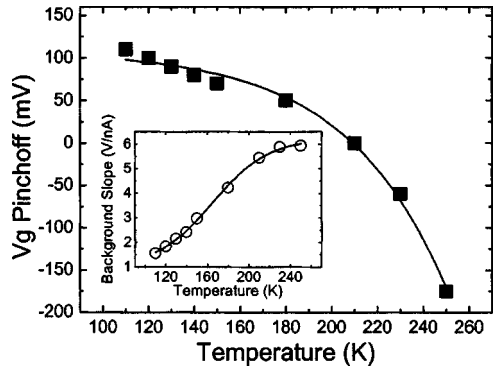

FIG. 4. Temperature dependence of the gate pinch-off voltage. The solid squares represent the data and the line is a square-root best fit. The power law behavior at $T<180$ K is believed to be related to the effectiveness of tunnel barriers as discussed in Ref. 12. The inset depicts the background slopes and the solid line is a visual guide.

In the inset of Fig. 3, two nearly symmetric and sharp onsets are clearly observed near the null voltage. The $\sim\pm0.16$-V thresholds, which correspond to the major gap in the Coulomb diamond, imply that $V_dC_d=e/2$ and $V_dC_s=e/2$. Hence, the capacitance of C_d and C_s are decided to be 0.5 aF and the total capacitance $C_\Sigma=C_s+C_d+C_g$ is ~2 aF. The dominance of C_g in the C_Σ, i.e, $C_g=\alpha C_\Sigma$, clearly favors the single-dot picture in high-temperature regime. This result also coincides with the study of Ono *et al.*[10] They found that the C_g can be made equally large to the C_Σ as long as the gate-dot coupling strength is high enough, and such effect is indeed evidenced in our analysis.

Comparison of our data to the results in a modeling study by Joyez *et al.*[7] and Grabert and Devoret[11] enables us to estimate the density of state, $\rho\sim1/\Delta E_Q$, in the dot. Notice that the points near the onset of the collapse provide a good means, at T=180 K, $K_BT/\Delta E_Q=5\times10^{-3}$ leads to $\Delta E_Q\sim0.31$ meV and in a similar manner, $K_BT/\Delta E_Q=2\times10^{-3}$ at 150 K results into 0.65 meV. The averaged 0.48 ± 0.15 meV is much smaller than the energy ~35 mV of the first excited state in quantum excitation, thus suggesting that there are many off-tunneling states participating in the process of electron tunneling. The existence of such many states seems to suggest the importance of degeneracy that has not yet been well understood. The cause for the existence of the quantum dot is believed to be associated with intrinsic crystalline grains, presumably resulting from inhomogeneous oxygen concentrations during thermal nucleation, as examined by the transmission electron microscope (TEM) in a previous study.[12]

Having convincingly demonstrated that a quantum dot is responsible for the Coulomb oscillations in the junction, the high offsets in the peak valleys may have useful meanings. In Fig. 2 of each I_d–V_g curve, the points at the valleys can be linked into straight lines (as represented by the dashed line). The current extrapolated to zero marks the transistor's pinch-off voltage V_g for the particular temperature. The overall pinch offs showns in Fig. 4 clearly suggest that there is a parallel but resistive network in the junction. The cause for such resistive network as discussed in detail in a previous study[13] might be related to the atomic segregation during oxidation. Nevertheless, in terms of engineering circuitry, the junction can be seen as a quantum dot coupled to a resistor in parallel. In the end, we emphasize that the low doping of phosphorus at $\sim1\times10^{17}$ cm^{-3} definitely contributes to the low background signal (see inset of Fig. 4). Since the volume of the active junction is about $\sim5\times10^3$ nm^3 ($20\times15\times15$ nm^3), its dopant number estimated is about $\sim10^{-1}$.[13,14] Such low value certainly can limit the number of charge carriers excited thermally in the channel and therefore reduces the background conductance.

In summary, we have fabricated low-power ~30 pW polycrystallinesilicon SETs on cheap dummy silicon wafers, instead of using expensive SOI counterparts. Coulomb blockade oscillations have also been observed with gate bias less than 1 V near room temperature. Realization of such devices is mainly relied on *e*-beam lithographically-defined point-contact junctions, as well as the control growth of a sub-10-nm gate oxide layer. It is believed that this breakthrough can help to speed up the fulfillment of very large-scale integration (VLSI)-compatible nanoelectronics.

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