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Increase of mobility in dual gate amorphous-$InGaZnO_4$ thin-film transistors by pseudo-doping

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Dual gate amorphous-$InGaZnO_4$ (a-IGZO) thin-film transistors (TFTs) with a bottom gate that covers the whole channel and a top gate that covers only a small portion of the channel are investigated. It is shown that if the larger gate (bottom gate) is held at constant positive bias, while the smaller gate (top gate) drives the TFT, not only does the V_{TH} shift negatively but the on-current also increases, resulting in dramatic increase in field-effect mobility (μ_{FE}). The μ_{FE} reaches $\sim 70\,cm^2/V{\cdot}s$ with a bottom gate potential of 15 V—confirming that the carrier mobility of a-IGZO TFTs can be significantly increased by electron doping in the channel. In such a configuration, the larger bottom gate acts as an electron supplier—effectively raising the conductivity of the a-IGZO layer (pseudo-doping). The smaller one works in the usual way, which is to either deplete of or accumulate the channel with carriers. © *2013 AIP Publishing LLC*.
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Amorphous–indium-gallium-zinc-oxide (a-IGZO) thin-film transistors (TFTs) are being broadly investigated as an alternative for silicon-based TFTs in active matrix displays (AMDs).[1] Advantages of a-IGZO TFTs include: (1) optical transparency in the visible light range because the band gap of the a-IGZO semiconductor is >3 eV; (2) high carrier mobility, even when the a-IGZO semiconductor is the amorphous phase, because carrier transport is through overlapping metal s-orbitals, whose overlap distance is insensitive to bond angle distortion of the amorphous network; and (3) the ability to be fabricated on flexible or large-area substrates, since a-IGZO can be deposited through sputtering and at low temperatures.[2,3]

There are, however, drawbacks associated with a-IGZO TFTs. Two major drawbacks are stability under electrical and/or light stress and the lack of p-type operation. As a result of the numerous studies devoted to the subject, stability of the a-IGZO TFTs has significantly improved over the past few years,[4–9] but the lack of p-type operation remains unsolvable. The a-IGZO semiconductor is intrinsically n-type and the reason for that is not fully understood but often attributed to oxygen vacancies, as in the case of ZnO.[10–12] Kamiya *et al*. reported a large density of states (DOS) ($\sim 10^{20}\,cm^{-3}$) above the valence band of the a-IGZO material, which makes it very difficult to invert the a-IGZO TFTs to p-type operation because of Fermi-level pinning.[1,2] Lack of p-type a-IGZO TFTs limits the realization of complementary metal oxide semiconductor (CMOS) circuits. This has therefore led to the development of n-type Pseudo-CMOS circuits, in which the n-type TFTs are either operated in the depletion or enhancement mode by controlling their threshold voltage (V_{TH}). Several techniques such as active-layer or gate insulator thickness variation have been used to control the TFT's V_{TH}.[13–15] More recently, secondary gates in the so-called dual gate structures are now being implemented and application of constant voltage to these secondary gates, while sweeping the primary gates, has resulted in precise control the TFT's V_{TH}.[16–21]

In inverted staggered dual-gate TFTs, the primary gate is the bottom gate (BG) and the secondary gate is the top gate (TG). Until now, TGs that are equal in length to the BGs or at least cover the whole channel region have been implemented and biasing them with constant voltage shifts the TFT's V_{TH}, without significant changes in other TFT parameters such as the field-effect mobility (μ_{FE}).[16–21] Here we investigate dual gate a-IGZO TFTs with BGs that cover the whole channel and TGs that cover only a small portion of the channel. We show that if constant positive bias is applied to the BG, while sweeping TG, not only does the V_{TH} shift negatively but the on-current (I_{ON}) also increases, resulting in dramatic increase in μ_{FE}. The increase in mobility is explained by a pseudo-doping effect induced by the BG.

The schematic cross-section of the TFTs used in this study is depicted in Fig. 1(a). Fig. 1(b) shows the TFT's optical image after fabrication. The detailed fabrication process is described elsewhere.[21] All metal electrodes are sputtered molybdenum (Mo) and all dielectrics (gate-insulator, etch-stopper, and passivation) are plasma enhanced chemical vapor (PECVD) deposited silicon-dioxide (SiO_2). The a-IGZO is sputter deposited at 200 °C in an Ar and O_2 environment. The gate-insulator, a-IGZO, and etch-stopper are deposited consecutively without breaking vacuum. The a-IGZO is, therefore, passivated immediately after deposition without being exposed to air. The a-IGZO TFTs studied herein are, therefore, very stable and reproducible, which ensures the detection of intrinsic characteristics rather than process-related variations. Another passivation layer is used after source and drain formation, which, combined with the etch-stopper, acts as the gate-insulator for the TG. The channel width (W) and channel length (L) of the TFTs are both 20 μm but the length of the TG is only 2 μm (Fig. 1(b)).

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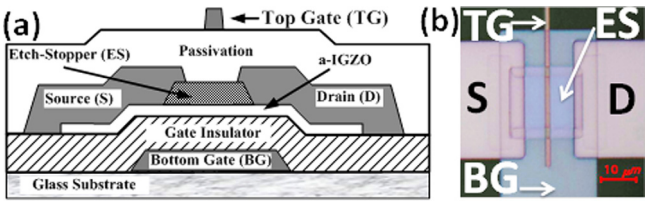

FIG. 1. (a) Schematic cross-sectional and (b) optical image of the fabricated dual gate a-IGZO TFTs. Channel Width (W) and channel Length (L) are determined respectively by the width and length of the etch-stopper (ES) and are both 20 μm. The length of the bottom gate (BG) is 26 μm, whereas that of the TG is only 2 μm.

TFT characteristics were extracted for two cases: By (1) holding a constant bias to the TG, while sweeping the BG and (2) holding a constant bias to the BG, sweeping the TG. In all cases, a drain voltage $V_{DS} = 0.1$ V was used. μ_{FE} was derived from transconductance $(g_M) = \partial I_{DS}/\partial V_{GS}$ as

$$\mu_{FE} = \frac{\partial V_{DS}}{\partial V_{GS}} \frac{1}{C_{OX}(W/L)V_{DS}}, \quad (1)$$

where C_{OX} is either the bottom or top gate oxide capacitance per unit area and V_{GS} is the voltage that is applied to either the TG (V_{TG}) or BG (V_{BG}). V_{TH} was estimated from constant current to be the V_{GS} corresponding to a drain current $I_{DS} = W/L*10$ pA. The subthreshold swing (SS) was taken as $(d \log (I_{DS})/d V_{BG})^{-1}$ of the range $10\,pA \le I_{DS} \le 100\,pA$, with $V_{DS} = 0.1$ V.

Fig. 2 shows (a) transfer characteristics and (b) μ_{FE} curves obtained by sweeping the BG while holding the TG at a constant bias (V_{TG}). V_{TG} was varied from 0 to 15 V. Application of a positive V_{TG} induces a small negative V_{TH} shift (ΔV_{TH}) (Fig. 2(a)) and small increase in μ_{FE} (Fig. 2(b))—consistent with the weak influence of a 2-μm-long TG. However, if the functions of the two gates are switched, i.e., if the BG is held at a constant bias, while sweeping the TG, ΔV_{TH} is 4-times larger (Fig. 3(a)), and μ_{FE} dramatically increases with increasing positive V_{BG} (Fig. 3(b)). In contrast to the previous case (Fig. 2(a)) on-current (I_{ON}) also increases with increasing V_{TG}, which is also consistent with the increase in μ_{FE}.

Fig. 4 summarizes TFT parameters as a function of V_{BG}. Note here that application of negative V_{BG} results in massive reduction in on-current (I_{ON}), where I_{ON} is taken as the I_{DS}

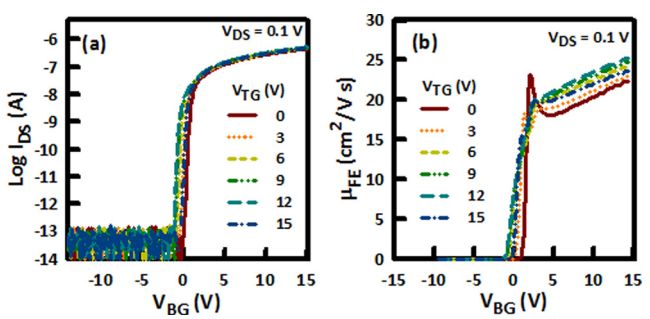

FIG. 2. (a) Transfer curves and (b) μ_{FE} curves obtained by sweeping the bottom gate (BG), while applying constant voltage to the TG. The voltages applied to the bottom gate and top gate are denoted V_{BG} and V_{TG}, respectively. V_{TG} is varied from 0 to 15 V. The length of the bottom gate (L_{BG}) is 26 μm and length of the top gate (L_{TG}) is 2 μm. W = L = 20 μm.

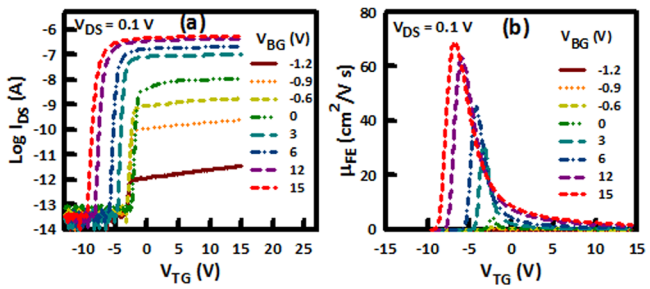

FIG. 3. (a) Transfer curves and (b) μ_{FE} curves obtained by sweeping the TG, while applying constant voltage to the BG. The voltages applied to the bottom gate and top gate are denoted V_{BG} and V_{TG}, respectively. V_{BG} is varied from −1.2 to 15 V. The length of the bottom gate (L_{BG}) is 26 μm and length of the top gate (L_{TG}) is 2 μm. W = L = 20 μm.

induced by $V_{TG} = 10$ V for each V_{BG}. μ_{FE_MAX} is the maximum (peak) μ_{FE}, which goes up to ~70 cm^2/V·s when $V_{BG} = 15$ V. The mechanism responsible for the increase in μ_{FE} with increasing V_{BG} is depicted in Fig. 5. The larger gate (BG) acts as an electron supplier, while the smaller gate (TG) either depletes the channel of or induces the accumulation of carriers. Note that when the top-gate is the primary gate (i.e., when the top-gate is swept from −15 to 15 V, while holding the bottom gate at constant voltage) the TFT can be regarded as a drain and source offset TFT with respect to the top channel. Although L = 20 μm, the length of the top gate is only 2 μm, which gives 9-μm-long offsets on each side of the channel. Since the bottom gate covers the whole channel region, it controls the Fermi level of the offset regions by either supplying them with or depleting them of electrons. The μ_{FE} of a dual gate TFT with bottom and top gates that are equal in length (symmetric gate length) does not increase as much as that of dual gate TFT with an asymmetric gate length because the top gate of the former modulates the whole channel, whereas the latter modulates only 10% of the channel. As a result, when V_{BG} is high (e.g., 15 V) there is always a large supply of carriers in the channel of the latter, regardless of polarity or magnitude of V_{TG}, whereas in the former, the top gate either depletes the whole channel of carriers or enhances the accumulation layer. The movement of the E_F when the top gate is swept from −15 to 15 V, while the bottom gate is held at 15 V is depicted in Fig. 5 for (a) symmetric gate length and (b) asymmetric gate

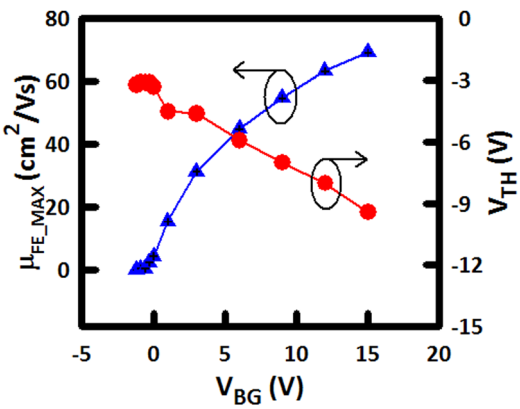

FIG. 4. TFT parameters achieved by sweeping the TG, while applying constant voltage to the BG. The parameters are plotted as a function of the constant voltage applied to the BG (V_{BG}). μ_{FE_MAX} is the maximum (peak) μ_{FE}.

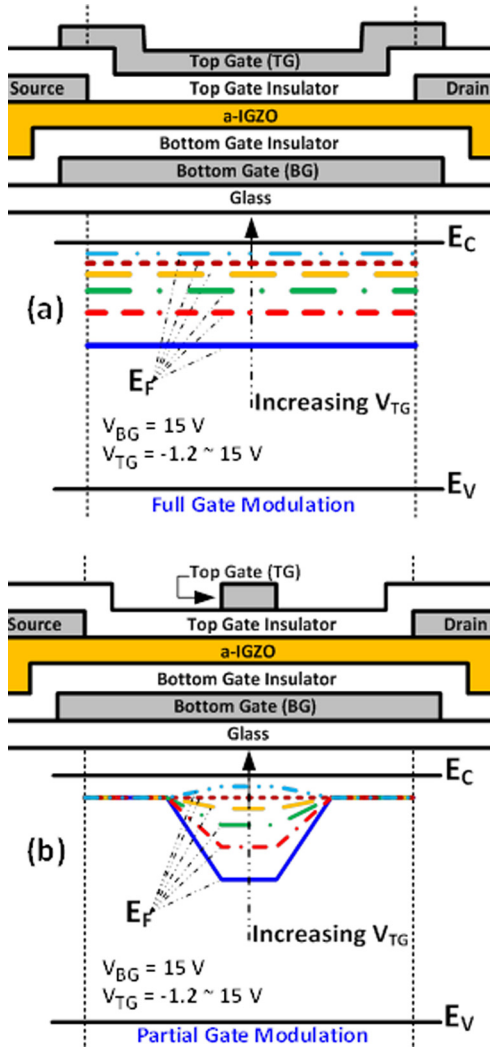

FIG. 5. Mechanism responsible for the increase in on-current (I_{ON}) and μ_{FE}. When biased positively, the larger gate (bottom gate) acts as an electron supplier, effectively raising the conductivity of the a-IGZO layer (pseudo-doping).

length. The partial gate modulation in the asymmetric gate length results in very high mobilities.

Channel resistance (R_{CH}) extracted as a function of the top-gate voltage (V_{TG}) is presented in Fig. 6 for each bottom gate voltage (V_{BG}). R_{CH} as a function of V_{TG} is given by

$$R_{CH}(V_{TG}) = R_{TOT}(V_{TG}) - R_{PAR}, \tag{2}$$

where R_{TOT} and R_{PAR} are respectively the TFT's total and parasitic resistances. $R_{TOT}(V_{TG})$ is given by

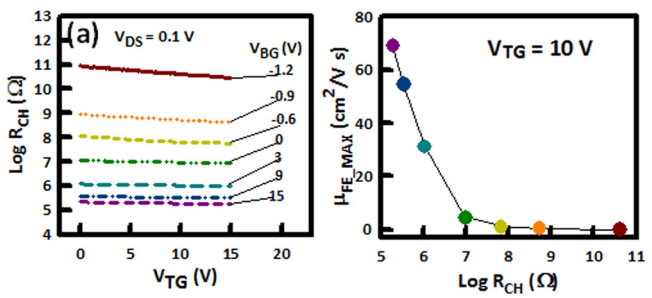

FIG. 6. (a) Channel resistance as a function of top gate voltage (V_{TG}) for varying bottom gate voltages (V_{BG}). (b) Maximum field-effect mobility (μ_{FE_MAX}) as a function of channel resistance.

$$R_{TOT}(V_{TG}) = \frac{V_{DS}}{I_{DS}(V_{TG})}, \tag{3}$$

where $V_{DS} = 0.1$ V. In order to determine the R_{PAR}, the "channel resistance" method is used,[22,23] which allows for the evaluation of both R_{PAR} as well as the effective channel length (L_{EFF}) from a series of transfer characteristic measurements at low-V_{DS} on devices with different mask (design) channel lengths (L_{MASK}). R_{PAR} is the resistance of the source and drain metal contacts including any other parasitic resistances at the source and drain ends. L_{EFF} can be different from L_{MASK}, depending on the accuracy of the fabrication process in areas such as the etching of the etch-stopper or source and drain metal contacts. In this method, it is assumed that the overall device resistance (R_{TOT}) is given by the sum of the effective channel resistance, R_{CH}*L_{EFF}, and R_{PAR}. R_{CH} is supposed to be gate modulated, while R_{PAR} and L_{EFF} are assumed to be independent from the gate bias, and the overall resistance is given by

$$\begin{aligned} R_{TOT}(V_{TG}) &= R_{CH}(V_{TG}) \times L_{EFF} + R_{PAR} \\ &= R_{CH}(V_{TG}) \times L_{MASK} + R_{EXT}(V_{TG}), \end{aligned} \tag{4}$$

having defined

$$R_{EXT}(V_{GS}) = R_{PAR} - R_{CH}(V_{GS}) \times \Delta L, \tag{5}$$

with the effective channel length reduction $\Delta L = L_{MASK} - L_{EFF}$. For a given V_{TG}, using the linear least-squares method, it is possible to determine $R_{CH}(V_{TG})$ and $R_{EXT}(V_{GS})$ by fitting R_{TOT} against L_{MASK}, as given in Eq. (4). The gradient and R_{TOT}-intercept give the R_{CH} and R_{EXT}, respectively, at each V_{GS}. The R_{PAR} and ΔL are determined from the intercept and gradient of the linear least-squares fitting of R_{EXT} against R_{CH}.

Given that the top-gate only controls 10% of the channel; the R_{CH} is dominated by the resistance of the offset regions. As depicted in Fig. 6, negative V_{TG} results in the increase of the R_{CH} as it depletes the offset regions of carriers—pushing their Fermi level deeper into the gap. In contrast, positive V_{TG} decreases the R_{CH} as it shifts the Fermi level of the offset regions towards E_C by supplying them with electrons—a process we are going to refer to as "pseudo-doping." This pseudo-doping effect results in the dramatic increase in μ_{FE} when constant positive V_{BG} is applied because μ_{FE} is inversely proportional to R_{CH} (Fig. 6(b)). Using the resistance data in Fig. 6, the positions of the Fermi level (E_C-E_F) were derived from conductivity, σ,

$$\sigma = \sigma_0 \times \exp\left[\frac{-(E_C - E_F)}{k_B T}\right], \tag{6}$$

where k_B and T are, respectively, the Boltzmann constant and the temperature in Kelvin The conductivity prefactor, σ_0, is obtained by assuming the value of E_C-E_F to be 0.15 eV at $V_{BG} = 0$ V; as determined by the combined analysis of current-voltage and capacitance-voltage characteristics from our previous works.[24–26] The values of E_C-E_F at V_{BG} of 15 and −1.5 V were calculated to be 0.05 and 0.35 eV,

respectively. These values confirm that the larger gate (bottom gate), effectively controls the position of the Fermi level.

This dual gate TFT may present a unique advantage in n-type pseudo-CMOS circuits. Dual gate TFTs have been used in the past in inverter circuits, where they act as depletion load TFTs.[13–21] We propose the use of this device, instead of the conventional dual gate TFT, as the load of TFT of a ratioed inverter as shown in Fig. 7. Fig. 7(a) shows the equivalent circuit schematic of a conventional depletion load inverter, where the length of the top gate is equal to that of the bottom gate and a constant top gate bias is applied to shift the V_{TH} negatively, while the bottom gate is connected to the output.[21] Fig. 7(b) shows the proposed inverter, where the length of the top gate is smaller than that of the bottom gate (e.g., 2 μm) and a constant bottom gate bias is applied to shift the V_{TH} negatively, while the top gate is connected to the output. Simulated results for these two schematics are presented in Figs. 8(a)–8(d), respectively, for conventional depletion load invertor and proposed depletion load invertor. For the simulations, a SMART SPICE simulator was used. It is evident that the proposed depletion load inverter has better inverting characteristics compared to the conventional depletion load inverter. For input $V_{DD} = 20$ V, the gain of the proposed inverter is ~97 V/V, while that of the conventional inverter is only ~26 V/V. Such a significant improvement is consistent with the high mobility exhibited by the proposed dual gate TFT.

In conclusion, we have shown that the mobility of a-IGZO TFTs can be significantly increased by a pseudo-doping effect that is induced by a secondary gate. The secondary gate controls the Fermi-level by either acting as an electron supplier (when a positive gate bias is applied to it) or depleting the semiconductor of electrons. In this proposed dual gate TFT, it is required that the primary is made as short as possible, such that partial gate modulation is achieved. When the secondary gate acts as an electron supplier (pseudo-doping), the field-effect mobility of the TFT will dramatically improve, owing to the large supply of electrons in the un-modulated regions (offsets). The use of this dual gate TFT as a depletion load TFT of an invertor significantly improves the gain—presenting a unique advantage in n-type pseudo-CMOS circuits.

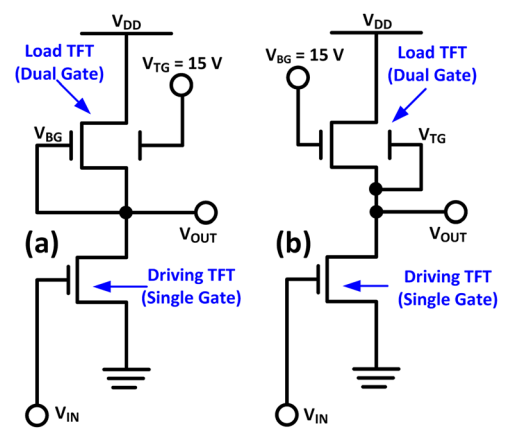

FIG. 7. Equivalent circuit schematic of ratioed inverters with depletion load dual gate TFTs and single gate driving TFTs: (a) Conventional depletion load TFT, where the length of the top gate is equal to that of the bottom gate and a constant top gate bias is applied to shift the V_{TH} negatively, while the bottom gate is connected to the output. (b) Proposed depletion load TFT, where the length of the top gate is smaller than that of the bottom gate (e.g., 2 μm) and a constant bottom gate bias is applied to shift the V_{TH} negatively, while the top gate is connected to the output.

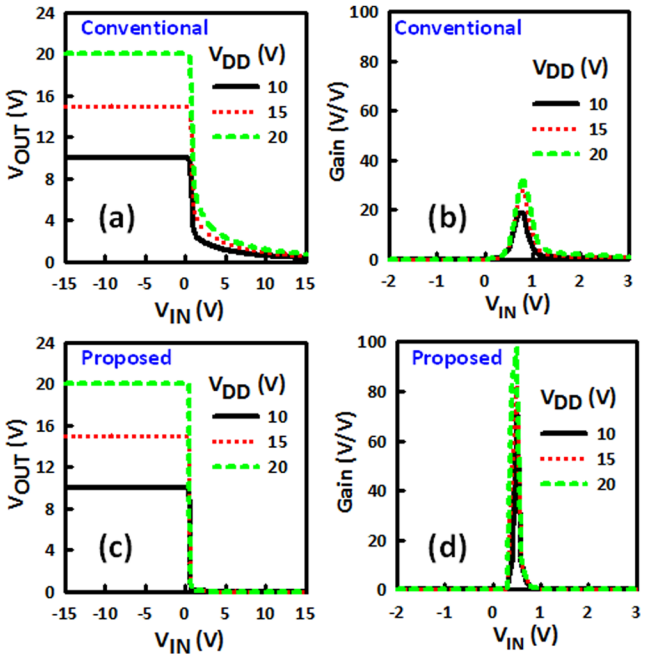

FIG. 8. Simulated voltage transfer curves (VTCs) of the inverters and corresponding plots of the gain when the length of top gate L_{TG} is (a and b) 26 μm (equivalent circuit in Fig. 7(a)) and (c and d) 2 μm (equivalent circuit in Fig. 7(b)). $L_{BG} = 20$ μm and the W/L ratio of the load TFT is equal to 20 μm/20 μm and that of the driving TFT is equal to 200 μm/20 μm. Simulations were performed by a SMART SPICE simulator.

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[1]T. Kamiya, K. Nomura, and H. Hosono, Sci. Technol. Adv. Mater. **11**, 044305 (2010).
[2]T. Kamiya, K. Nomura, and H. Hosono, J. Disp. Technol. **5**, 468 (2009).
[3]J. S. Park, W.-J. Maeng, H.-S. Kim, and J.-S. Park, Thin Solid Films **520**, 1679 (2012).
[4]K. Nomura, T. Kamiya, and H. Hosono, J. Soc. Inf. Disp. **18**, 789 (2010).
[5]K. H. Ji, J.-I. Kim, H. Y. Jung, S. Y. Park, R. Choi, U. K. Kim, C. S. Hwang, D. Lee, H. Hwang, and J. K. Jeong, Appl. Phys. Lett. **98**, 103509 (2011).
[6]K. Ide, Y. Kikuchi, K. Nomura, M. Kimura, T. Kamiya, and H. Hosono, Appl. Phys. Lett. **99**, 093507 (2011).
[7]P.-T. Liu, Y.-T. Chou, L.-F. Teng, F.-H. Li, C.-S. Fuh, and H.-P. D. Shieh, IEEE Electron Device Lett. **32**, 1397 (2011).
[8]K. H. Ji, J.-I. Kim, Y.-G. Mo, J. H. Jeong, S. Yang, C.-S. Hwang, S.-H. K. Park, M.-K. Ryu, S.-Y. Lee, and J. K. Jeong, IEEE Electron Device Lett. **31**, 1404 (2010).
[9]K. Nomura, T. Kamiya, and H. Hosono, Appl. Phys. Lett. **99**, 53505 (2011).
[10]S. Lany and A. Zunger, Phys. Rev. B **72**, 035215 (2005).
[11]A. Janotti and C. G. Van de Walle, Rep. Prog. Phys. **72**, 126501 (2009).
[12]S. J. Clark, J. Robertson, S. Lany, and A. Zunger, Phys. Rev. B **81**, 115311 (2010).
[13]J. M. Lee, I. T. Cho, J. H. Lee, and H. I. Kwon, Jpn. J. Appl. Phys. **48**, 100202 (2009).
[14]C. A. Lee, S. H. Jin, K. D. Jung, J. D. Lee, and B.-G. Park, Solid-State Electron. **50**, 1216 (2006).

[15]C. Baek and S.-M. Seo, Appl. Phys. Lett. **94**, 153305 (2009).
[16]H. Lim, H. Yin, J.-S. Park, I. Song, C. Kim, J. Park, S. Kim, S.-W. Kim, C. B. Lee, Y. C. Kim, Y. S. Park, and D. Kang, Appl. Phys. Lett. **93**, 063505 (2008).
[17]K. Takechi, M. Nakata, K. Azuma, H. Yamaguchi, and S. Kaneko, IEEE Trans. Electron Devices **56**, 2027 (2009).
[18]H.-W. Zan, W.-T. Chen, C.-C. Yeh, H.-W. Hsueh, C.-C. Tsai, and H.-F. Meng, Appl. Phys. Lett. **98**, 153506 (2011).
[19]J.-M. Lee, I.-T. Cho, J.-H. Lee, and H.-I. Kwon, Appl. Phys. Lett. **93**, 093504 (2008).
[20]H.-W. Zan, C.-C. Yeh, H.-F. Meng, C.-C. Tsai, and L.-H. Chen, Adv. Mater. **24**, 3509 (2012).
[21]M. J. Seok, M. H. Choi, M. Mativenga, D. Geng, D. Y. Kim and J. Jang, IEEE Electron Device Lett. **32**, 1089 (2011).
[22]P. Bhattacharya, M. Bari, and K. Rao, Jpn. J. Appl. Phys., Part 1 **32**, 3409 (1993).
[23]A. Valletta, M. Rapisarda, L. Mariucci, A. Pecora, G. Fortunato, C. Caligiore, E. Fontana, F. Tramontana, and S. Leonardi, Thin Solid Films **517**, 6353 (2009).
[24]P. Migliorato, M. Seok, and J. Jang, Appl. Phys. Lett. **100**, 073506 (2012).
[25]P. Migliorato, M. D. H. Chowdhury, J. G. Um, M. Seok, and J. Jang, Appl. Phys. Lett. **101**, 123502 (2012).
[26]J. G. Um, M. Mativenga, P. Migliorato, and J. Jang, Appl. Phys. Lett. **101**, 113504 (2012).