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Electro-optically switched compact coupled photonic crystal waveguide directional coupler

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In this paper, we present a compact photonic crystal directional coupler in a silicon on insulator platform electro-optically switched at 150 kHz with a switching time of 620 ns under a low voltage operation of 2.9 V. The switch design utilizes a coupled photonic crystal structure designed to operate in the slow light regime. Switching is attained by modulating the coupling coefficient of the coupled photonic crystal waveguide system by using a p-i-n diode to modulate the carrier concentration with a density of $\sim 10^4$ A/cm^2 across the plane of the photonic crystal. © *2010 American Institute of Physics*. [doi:10.1063/1.3330927]

In recent years, interest within silicon photonic switches in a silicon on insulator (SOI) platform has grown. Devices currently in literature rely on high-Q cavities or long interaction lengths to electrically modulate or selectively route optical signals on SOI. The high-Q cavity devices supply optical modulation with small device footprints but suffer from reduced bandwidth and switching speeds.[1] Devices exploiting long interaction lengths offer high bandwidth while requiring large areas on chip and increased power requirements.[2] However, to achieve higher density integrated chips, a compact slow light photonic crystal with a device footprint below 70 μm^2 is needed.[3] In this paper, we present a potential design toward such goal. Our planar photonic crystal directional coupler, built in a 260 nm SOI platform is designed to have a bandwidth of ~2.5 nm and a compact interaction length of 9.7 μm.[4] Our device uses two coupled line defect photonic crystal waveguides with overlapping modes, one even and one odd, allowing the power within one waveguide to be coupled into the neighboring waveguide. The interaction length required to transfer the power from one waveguide to the next often needs to occur over distances greater than 100 μm in conventional coupled photonic crystal waveguides (CPhCWG).[2] By engineering the dispersion properties of the even mode to be flat, seen in Fig. 1, the group velocity of the electromagnetic traveling mode is slowed relative to the group velocity in an equivalent line defect waveguide in a photonic crystal with uniform hole diameters. As a result of entering the slow light regime of the photonic crystal, the light observes more of the material as it propagates through the structure, allowing the coupler length to be less than 10 μm with an effective interaction length being much longer. While this is advantageous for compact device design it places a great burden and challenge on the fabrication of such devices, as in this case any minor fabrication tolerances and defects are highly magnified and will in turn highly hinder the operation of the entire device. This slow propagation of light also allows for subtle changes to the material's index of refraction while largely affecting the dispersion properties of the photonic crystal.

The CPhCWG directional coupler, shown in Fig. 1, is composed of two line defect waveguides separated by three rows of air holes in a hexagonal lattice arrangement with a hole radius and lattice constant ratio of $r/a \sim 0.3$, respectively. Additionally, the diameters of three rows of air holes are dilated by 90 nm to flatten the even mode and maximize the slow light effect. The structure interaction length is 9.7 μm, intrinsically coupling the 1556 nm wavelength to

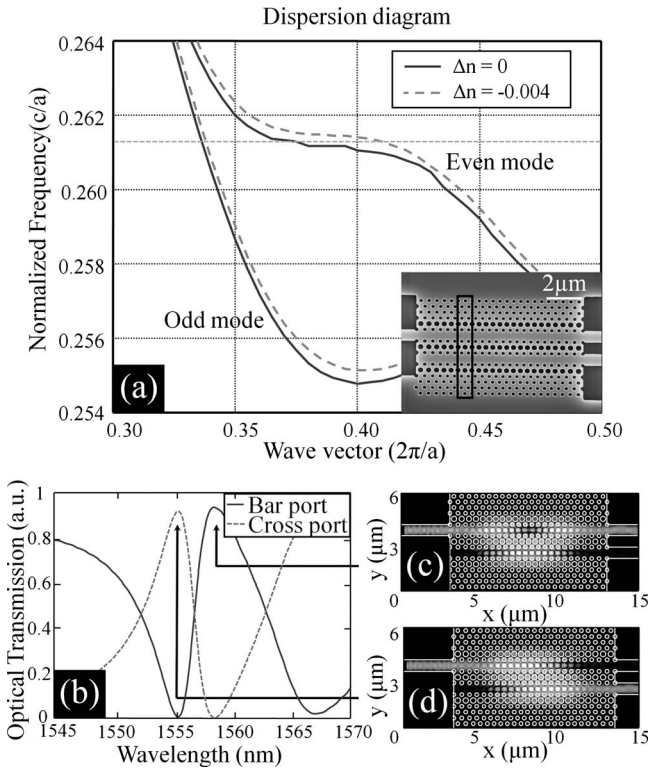

FIG. 1. PWM and FDTD simulated characteristics for the CPhCWG. (a) Dispersion diagram for even and odd modes with a shift in the refraction index of $\Delta n = -0.004$. A shift in the refraction index yields a large change in the even mode wave vector at the normalized frequency of ~0.261. Inset shows SEM image of photonic waveguide with PWM computation region boxed. (b) Optical transmission between bar and cross ports of photonic device in the "OFF" state. [(c) and (d)] FDTD simulation snapshots of optical power being transmitted through bar and cross ports, respectively.

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the neighboring cross port with a bandwidth of ~2.5 nm. To actively switch the device, it is found in FDTD simulations that a change in the index of refraction of $\Delta n = -0.004$ is sufficient to shift the spectra by ~3 nm to switch select wavelengths between bar and cross ports. This change in the index can be facilitated by the thermo-optic effect, by optical free carrier generation, or electrical free carrier injection. Although all the methods are capable of producing the appropriate shift in the index of silicon, thermo optic switches have shown to have slow switching speeds, above 1 μs,[5] and out of plane optical pumping, although fast, is difficult to integrate on chip with complementary metal oxide semiconductor (CMOS) fabrication processes.[6] Fortunately, by fabricating a p-i-n diode laterally across the photonic crystal, free carriers are readily able to be injected into the PhC on the time scale of <1 ns (Ref. 7) and still maintain a feasible integration to CMOS fabrication. Under forward bias, a p-i-n diode can inject free carriers into the intrinsic region of the CPhCWG, inducing a change in the real part of the refractive index and the absorption coefficient of the silicon at a wavelength of 1550 nm dictated, respectively, by

$$\Delta n = -8.8 \times 10^{-22} \Delta N_e - 8.5 \times 10^{-18} (\Delta N_h)^{0.8},$$

$$\Delta \alpha = 8.5 \times 10^{-18} \Delta N_e + 6.0 \times 10^{-18} \Delta N_h, \quad (1)$$

where ΔN_e and ΔN_h are the perturbations of electron and hole carrier concentrations in cm^{-3}.[8,9] To achieve the $\Delta n = -0.004$ index change necessary to switch our device, we need a free carrier injection of $\sim 10^{18}$ cm^{-3}. Inherently, the density of free carriers injected under forward bias also contributes to an optical absorption of ~14 cm^{-1}.

The photonic crystal directional coupler is patterned using e-beam lithography and etched into a 260 nm thick silicon device layer via reactive ion etching. The device geometry was realized through exposure dose scaling and pattern size biasing to obtain hole diameters with 2 nm tolerances. The photonic crystal is driven using a p-i-n diode built into the 260 nm SOI platform, positioned to span the width of the PhC, injecting carriers transversely across the direction of light propagation [Fig. 2]. The p-i-n diode is fabricated using UV lithography and thermal diffusion to realize n-type and p-type regions of an impurity concentration $\sim 10^{18}$ cm^{-3}.[10] The diode was designed to have a 5 μm intrinsic region to accommodate the width of the PhC, assuring the optical mode is isolated from free carriers in the intrinsic silicon while the device is in the "OFF" state. This isolation allows for the largest change of free carrier concentration between device states, and reduction in free carrier optical absorption around high impurity concentrations, explained in by the optical absorption coefficient (α) in Eq. (1). For electrical probing, ohmic contact pads are made using ~10 nm titanium adhesion layer followed by ~150 nm of gold.

The device is experimentally characterized by launching a tunable laser into the input silicon rib waveguide via a single mode polarization maintaining lensed fiber rotated to launch a transverse electric field into the plane of the photonic crystal. The rib waveguide width is then tapered down coupling the laser into the line defect waveguide of the CPhCWG, where the p-i-n diode modulates the silicon refractive index of the photonic crystal causing the CPhCWG to switch the launched laser light between the bar and cross port. The port outputs are coupled to silicon rib waveguides and collected by a multimode lensed fiber attached to a high-speed photodetector. The CPhCWG was passively characterized using an Agilent tunable laser to measure the throughput spectrum of the bar and cross port while the device is in the "OFF" state, shown in Fig. 3. The transmission of both ports are low beyond the wavelength 1565 nm due to the optical signal unable to efficiently couple into the CPhCWG.

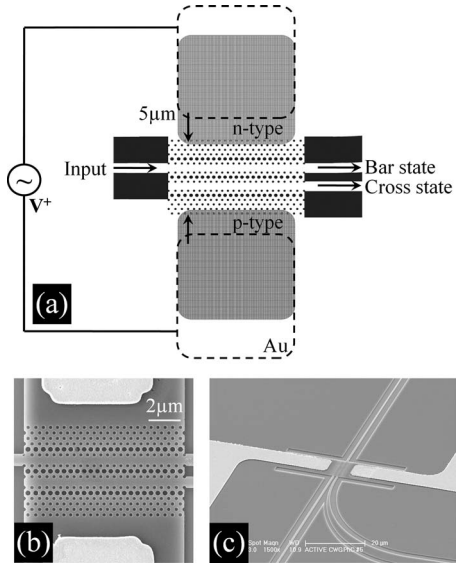

FIG. 2. (a) CPhCWG device design schematic with p-i-n diode. (b) SEM image of CPhCWG fabricated with p-i-n diode spanning vertically across image. (c) SEM image of silicon waveguides coupling in and out of CPhCWG on SOI platform with gold contacts entering from left and right of image.

The device was actively characterized by launching the wavelength the CPhCWG coupled to the cross port, (e.g., 1555.5 nm) shown in Fig. 3, into the device while monitoring the optical power coupled to the bar port. The p-i-n diode was then electrically driven with a high speed function generator, and tuned to inject the necessary level of free carriers across the photonic crystal to blueshift the spectrum and couple the light to the bar port. The switching speed of the device was tested by electrically modulating the p-i-n diode at 150 kHz with a generated square wave. The square wave applied a pulsed forward bias with a duty cycle of 50%. The applied voltage was tuned to switch the device to the "ON" state with a forward bias of +2.9 V, resulting in switching the optical signal from the cross port to bar port with an extinction ratio of −14.8 dB. The p-i-n diode was switched

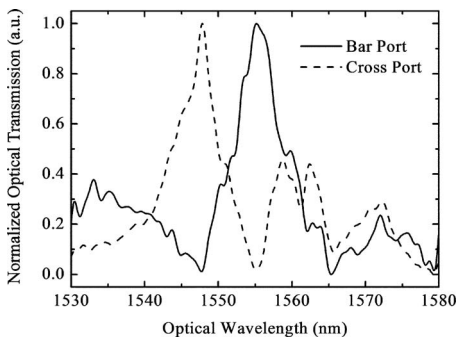

FIG. 3. Experimental measured spectrum of bar and cross ports while CPhCWG is in the "OFF" state.

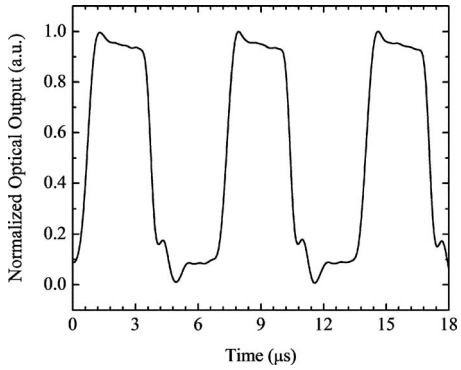

FIG. 4. Modulated optical signal of bar port, with an electrical driving frequency of 150 kHz switching between V_{on}=+2.9 V and V_{off}=0.0 V. The smaller oscillations seen after the transition of device states is an artifact of the current preamplifier used in the optical detection setup.

to the "OFF" state by removing the bias and allowing the free carriers to recombine in the intrinsic region. It was seen that the optical signal was modulated between the two ports at a frequency of 150 kHz, shown in Fig. 4, with a 10% to 90% rise time of 620 ns and a fall time of 500 ns. The state of the device under forward bias is seen directly as the increased optical signal of the bar port. The aforementioned rise and fall times show an operational switching speed of ~900 kHz. A reverse bias of −1.0 V was tested to aid in sweeping free carriers from the intrinsic region in the transition of device state "ON" to "OFF," however it did not show a noticeable contribution to the fall time of the modulated signal.

This rise time is presently limited by the existing preamplifier in the optical detection setup. The thermal effects due to carrier injection of $\sim 10^4$ A/cm^2 are believed to have too slow of a response to effect the switching speeds seen with the frequencies used.[5] A noticeable thermal contribution to the photonic crystal switching was seen at frequencies around and below ~50 kHz. Beyond improvements of the detection setup, the switching speed can be improved by reducing the width of the intrinsic region, thereby allowing for a shorter fill time of free carriers in the intrinsic region. The disadvantage is that the optical mode will reside partially in the adjacent highly doped regions, resulting in higher optical absorption.

In summation, the CPhCWG directional coupler using slow light enhancement was demonstrated with a device length under 10 μm. The CPhCWG was electrically switched via free carrier injection supplied by a p-i-n diode integrated into a SOI platform at voltages below 3 V. We demonstrated device switching at frequencies of 150 kHz with a switching time of 620 ns, capable of an operational switching speed of ~900 kHz, being limited by the present measurement system. Improvements to the testing equipment are currently being made to accurately measure the device response at higher switching frequencies.

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