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Control over the interface properties of carbon nanotube-based optoelectronic memory devices

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Optoelectronic nonvolatile memory elements based on polymer-coated carbon nanotube devices can serve as building blocks in programmable circuits. Although essential for improving the circuit performances, the details of the charge trapping mechanism in these mixed organic/inorganic optoelectronic devices are not fully elucidated. The detailed mechanism was investigated by intercalating layers of a hydrophobic organic dielectric (parylene) at different interfaces in the device structure. A thin parylene layer separating the SiO_2/nanotube interface from the photosensitive polymer coating is presented as an optimized solution in terms of charging, stability, and robustness.
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As a one-dimensional material, carbon nanotubes (CNTs) are extremely sensitive to their electrostatic environment. In a field effect transistor configuration (CNTFET),[1,2] CNT were used to probe trapped charges located in the vicinity of the FET channel, in particular in the gate dielectric. Their sensitivity reaches single charge detection[3–5] and their properties are suited to study non-volatile memory elements (NVMEs).[6,7] By combining CNTFETs with a photosensitive coating, one can develop an interesting class of optoelectronic NVMEs called optically gated carbon nanotube field effect transistors (OG-CNTFETs).[8,9] The operating mode of OG-CNTFETs relies on an optically driven charging step (write) associated with the electrical control of the density of stored charges (reset). The association of these two types of commands, one global (optical) and one local (electrical), together with the possibility to program continuously the channel resistivity within a large range has opened new opportunities in device circuitry.[10–13] In particular, we recently showed that OG-CNTFETs can be used to implement artificial synapses in neural-network type of circuits[12] and used this strategy to build a demonstrator of circuit able to learn its function in a post fabrication step.[13] Despite progresses in the collective use of OG-CNTFETs, the mechanism of the charge storage/release is not yet entirely clarified.[14,15] Indeed, the non-volatile memory effect is accompanied by an additional volatile contribution, which origin was not fully explained. Its effect being detrimental for circuit performances, new experiments are required to first understand and then solve this issue.

Recent work on CNTFETs and graphene FETs on SiO_2 shed new light on the ubiquitous role of oxygen and adsorbed water on their sensitivity to air exposure.[16,17] The use of comparative experiments on hydrophilic SiO_2 and hydrophobic parylene surfaces deposited on doped silicon substrates proves extremely useful in identifying the relevant contributions coming from the environment.[17–19] Following this methodology, we explored in this Letter the use of parylene layers intercalated at different places in the layered structure of OG-CNTFETs. This approach revealed key elements responsible for the charging/discharging mechanisms in OG-CNTFETs. This understanding led to the optimization of the operating modes of the NVMEs by using an air blocking layer in the stack.

A standard OG-CNTFET consists of a CNTFET entirely covered by a thin film (~5-10 nm) of a photosensitive polymer (typically *poly(3-octylthiophene)* (P3OT)) (Fig. 1(a)). The channel can be either an individual CNT[9,15] or a network of CNTs.[11,14] In this study, we used networks, but the conclusions hold for both cases and do not depend on the network density, which only impacts the current levels. The general operation principle is as follows: a 100 ms illumination pulse at $\lambda = 457$ nm ($h\nu = 2.7$ eV, corresponding to a strong absorption band of the polymer) photo-generates excitons inside the polymer layer (E_g (P3OT) ~ 2.4 eV). At positive gate bias ($V_{GS} > 0$), a fraction of the excitons dissociates. The photo-generated holes are depleted from the device through the drain electrode while the electrons accumulate toward the P3OT-SiO_2 interface and get trapped.[14,15] The trapped electrons apply a static negative potential to the CNTFET channel that freezes the device in its on-state. When the light is turned-off, part of the on-state conductivity (Fig. 1(a)) remains stable (non-volatile part) while another part decays at a time scale of a few seconds (volatile part). The trapped electrons can be released by simply applying negative gate bias pulses. The density of trapped charges can be adjusted in order to stabilize a large range of programmable memory states,[11] which is the key characteristic used to build circuits with function learning capabilities.[12,13] In a study comparing different gate dielectrics, the non-volatile part of the memory effect was ascribed to the direct trapping of electrons in the SiO_2 layer.[14] The origin of the volatile part remained however unclear although it imposed important limitations to the performances of OG-CNTFETs-based programmable circuits, i.e., a delay after the illumination was needed in order to stabilize the device.

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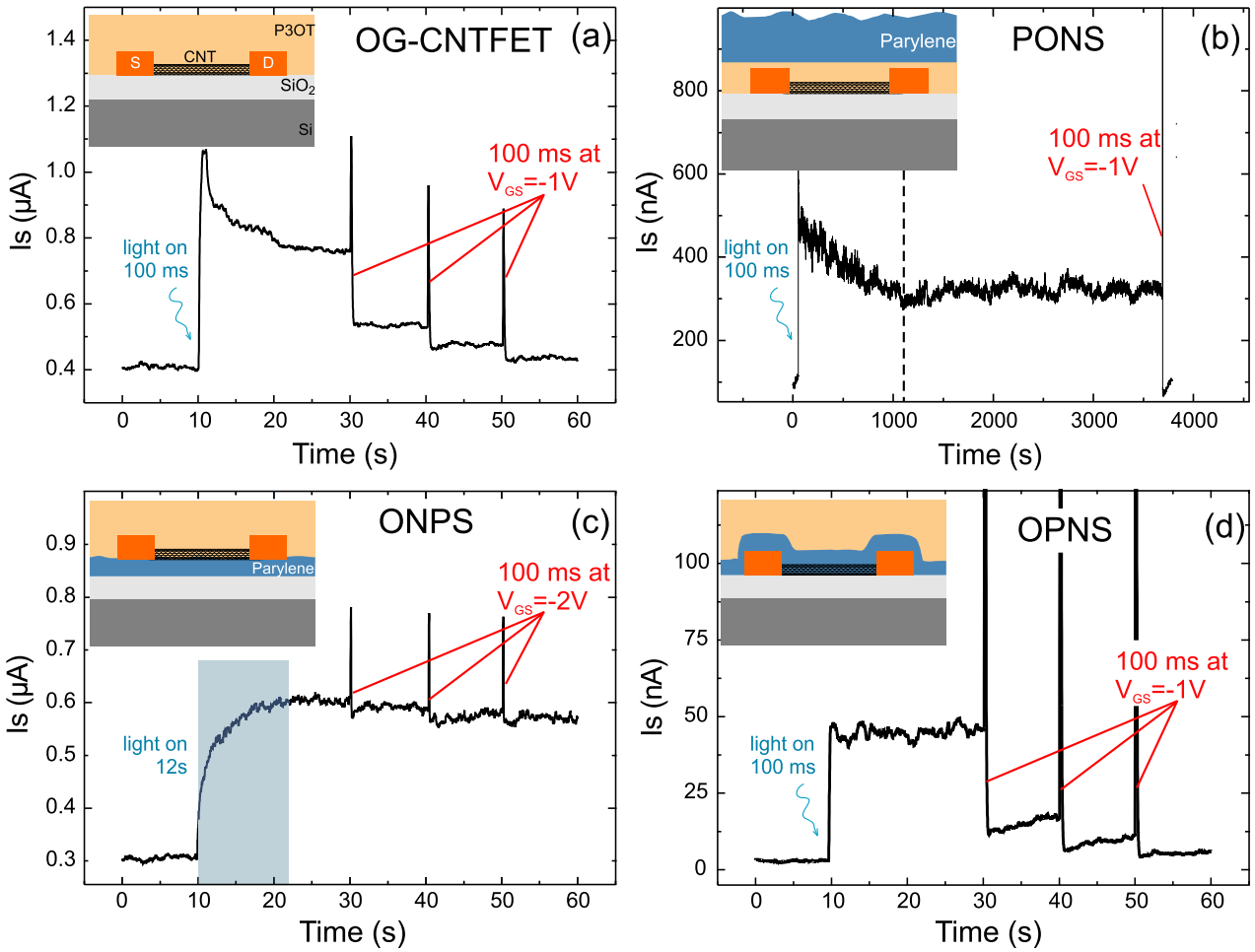

FIG. 1. Memory operation of (a) an OG-CNTFET, (b) an OG-CNTFET capped with a 170 nm thick parylene layer (called PONS), (c) an OG-CNTFET where a 10 nm thin parylene layer is intercalated between SiO_2 and the nanotubes (called ONPS), and (d) an OG-CNTFET where a 7 nm-thin parylene layer is deposited between the nanotubes and the P3OT (called OPNS). In all cases, the SiO_2 thickness is 10 nm below the device and 150 nm below the macroscopic contact pads. The channel of the transistors is composed of a random network of SWNTs, the density of which sets the current levels. Measurements are performed in the dark. Light is only applied during 100 ms in (a), (b), and (d) and during 12 s (blue shaded area) in (c).

A first hint about the origin of the volatile part of the light-induced response comes from the time scale of the current trace, which points toward an electrochemical charge transfer process involving the oxygen-water redox couple, as proposed in CNT- and graphene-FETs on SiO_2.[16,17] To investigate the possible role of such species from air on the stability of the memory effect, we first performed experiments with OG-CNTFETs encapsulated below a 170 nm-thick layer of parylene. This layer is known to form an excellent physical barrier against moisture and oxygen. The *parylene/organic/nanotubes/SiO*$_2$ (PONS) devices have the same general operation trends (Fig. 1(b)) as that of the reference device (Fig. 1(a)), except that the relaxation time of the volatile part has increased by a factor 50 (from ~20 s to ~1000 s). We ascribe this difference to the partial removal of water (and O_2) molecules from the SiO_2 surface of the PONS devices through the permeable P3OT layer,[20] which readily occurs in the vacuum chamber used for the deposition of the parylene film. Once deposited, the parylene film efficiently seals the structure and allows the device to operate in air.

To further clarify the role of the different interfaces, we studied devices in which a 10 nm thick parylene layer was intercalated, as shown in Fig. 1(c), between the SiO_2 layer and the nanotubes. We call this geometry ONPS for *organic/nanotubes/parylene/SiO*$_2$. In such configuration, applying the usual illumination conditions (100 ms light pulse) was not enough to fully turn-on the devices. We thus applied light for 12 s, as shown in Fig. 1(c). If the charge trapping mechanism of interest was related to trap states located in the P3OT layer, the performance should be independent of the dielectric type and both the conventional structure (Fig. 1(a)) and the ONPS one (Fig. 1(c)) would yield the same results. The very low charging efficiency of the ONPS structure thus confirms the central role of the nanotube/SiO_2 interface. At this point, two physical reasons could explain the slower charging rate of the ONPS devise: (i) a lower density of traps in the parylene layer compared to SiO_2[21,22] or (ii) a slow charging of SiO_2 traps through the parylene layer. Indeed, a similarly slow charging effect on the parylene dielectric was reported for organic FETs under electrical stress,[23] and electron leaks across the layer is favoured by the large electric field at the CNT's apex[24] and by the roughness of the parylene layer.

Beside the charging time, another striking difference between the ONPS structure and conventional OG-CNTFETs concerns the absence of the slow current decay in the ONPS case at the light turn-off state. The absence of a

volatile part of the memory effect allows us to exclude the possibility that mobile charges or electron-hole recombination in the P3OT layer are responsible for the current decay observed in the absence of parylene (such effects would also be observed in the ONPS case). This strengthens the point mentioned above that trap states in the P3OT layer only play a minor role, if any.

A third important difference between Figs. 1(a) and 1(c) concerns the significantly reduced efficiency of the gate bias pulses to reset the ONPS device conductivity, even though the −2 V gate bias used corresponds to the same electric field strength as in conventional OG-CNTFETs (by considering the addition of a 10 nm layer of parylene in the gate stack). Actually, the optically programmed state of the ONPS structure is almost irreversible: applying $V_{GS} = -6$ V for 2 h is necessary to recover the initial state. One could hypothesize that the charges responsible for the memory effect in the ONPS case are trapped in the parylene layer itself. This would imply that the associated traps have activation energy higher than the one of SiO_2 traps, which is very unlikely. In addition, stable trapping would occur in the PONS structure as well, which is obviously not the case in Fig. 1(b) since a gate bias pulse of −1 V is enough to reset the device conductivity. Conversely, this behaviour is better explained by electrons trapped in the SiO_2, with parylene acting as a barrier inhibiting electrons to flow back toward the channel at the reset step.

Overall, the role of the parylene layer in the ONPS case is twofold: it reduces the water (and thus the O_2) concentration at the SiO_2 surface, which suppresses the volatile part of the memory effect, and it limits the vertical flow of electrons to and from the SiO_2 trap states during both the light-induced charging and the electrical discharging phases.

In order to better discretise the charge transfer effects occurring between the P3OT layer, the CNTs, and SiO_2, a fourth device geometry was studied. Before the deposition of the P3OT layer, a 7 nm parylene layer was intercalated on top of the CNTs to form the *organic/parylene/nanotubes/SiO_2* structure (OPNS) shown in Fig. 1(d). In this OPNS configuration, as for the conventional OG-CNTFETs and the PONS structure, a 100 ms illumination pulse was enough to turn-on the device. Therefore, the charging time is similar for all device structures having CNTs in direct contact with SiO_2.

In this OPNS geometry, no volatile part is observed at light turn-off, which is similar to the ONPS case. In both Figs. 1(c) and 1(d), the structure corresponds to the configurations in which the parylene covers the SiO_2 surface, and no SiO_2/P3OT interfaces are present. The ONPS and OPNS structures behave however very differently upon application of gate bias pulses. While the discharging operation is almost impossible in the ONPS case, its efficiency in the OPNS case is similar to the one of the reference structure and of the PONS structure, i.e., in the three configurations where the CNTs directly lie on the SiO_2 layer.

The insertion of the parylene layer between the P3OT and the SiO_2 (OPNS and ONPS devices) efficiently prevents the slow decay of the photo-induced current (volatile part of the memory), which represents a clear benefit in performance as it suppresses the need for a stabilization delay after the light-induced charging step.

From the above comparison of the four device structures, a mechanism consistent with all the observed behaviours can be sketched. The volatile part of the memory effect can readily be ascribed to an electrochemical charge-transfer (ECT) process between adsorbates on the SiO_2 layer and the CNTs/P3OT. Based on recent work on the air sensitivity of CNTFETs on SiO_2,[16,17] the known H_2O/O_2 redox couple are likely involved as acceptor states. The key element is the water layer adsorbed at the surface of SiO_2, which is hydrophilic under atmospheric conditions. Not considered in previous studies of OG-CNTFETs, this water layer can dissolve oxygen according to Henry's law to form the O_2/H_2O solution in the vicinity of the CNTs. This sets the conditions for the redox reaction: $O_2 + 4H^+ + 4e^- \leftrightarrow 2H_2O$. A convenient way to determine the kinetics of such a charge transfer is through the Marcus-Gerischer (MG) theory.[25] Within this model, the redox potential provides the average energy levels at equilibrium of all the individual redox species. As depicted in Fig. 2, the energy levels of the reduced species can be seen as donor states and the energy levels of the oxidized species as acceptor states. These energy levels in a liquid electrolyte are fluctuating due to the polarisation of the solvent, resulting in an energy distribution and renormalization. Therefore, the

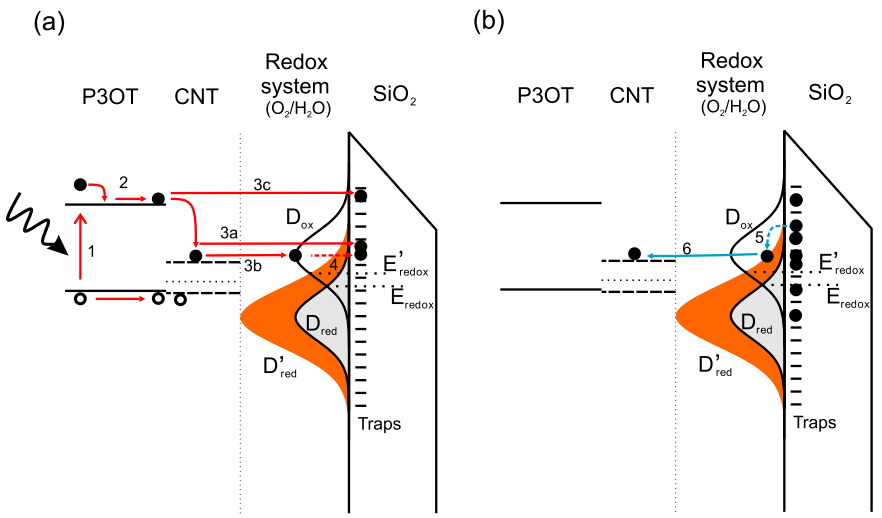

FIG. 2. Schematic energy band diagrams (at $V_{GS} > 0$) of the P3OT/CNT/SiO_2 interface in the presence of a water adlayer in conventional OG-CNTFETs (without parylene): (a) during illumination and (b) at light turn-off. The O_2/H_2O redox system is responsible for the volatile part of the memory effect.

solution within this model and by analogy to semiconductors can be rationalized, with some restrictions, as bands of occupied and unoccupied states.[25] In Fig. 2, the bands and the density of states of the redox couple were drawn separately for the sake of clarity, but they may be overlapping in the device configuration.

We first discuss the trapping/de-trapping operation in a conventional OG-CNTFET using Fig. 2(a). The CNT network and the P3OT are considered as semiconductors. During illumination at $\lambda = 457$ nm (2.7 eV), the photo-generated electrons are pumped to higher P3OT energy states (1) due to the ~0.3 eV excess photon energy relative to the P3OT band-gap. Part of the produced excitons dissociate at the P3OT/CNT interface (2). At the applied bias ($V_{GS} > 0$ and $V_{DS} < 0$), holes are depleted from the p-type channel of the FET toward the drain electrode. Part of the excess electrons in the CNT channel are directly transferred to SiO_2 traps, attracted by the favourable electric field imposed by the gate bias (3 a). A second part of these electrons are transferred to the acceptor states of the redox system (3 b), thus increasing the density of donor states $D_{red} \rightarrow D'_{red}$ and shifting up the chemical potential of the solution ($E_{redox} \rightarrow E'_{redox}$). Once filled the acceptor states can be further stabilised at the SiO_2 surface (4). Some of the excitons may also directly dissociate at the P3OT/SiO_2 interface (3 c). After switching the light OFF, in the absence of photogenerated electrons, the solution returns towards equilibrium ($E'_{redox} \rightarrow E_{redox}$), the reverse reaction occurs (reduction) and the electron transfer back towards the CNT network (5,6), leading to the volatile part of the memory, while trapped electrons in the SiO_2 remain stored (non-volatile memory effect). At the reset step, the negative electric field provided by the gate bias efficiently de-traps the stored electrons from the SiO_2.

Within our model, when the device is capped with a parylene layer as in the PONS structure (Fig. 1(b)), owing to the reduced intake of water and oxygen at the CNT/SiO_2 interface, the DOS of the redox system (D_{ox} and D_{red}) are lowered, which strongly limits the charge transfer. This picture is consistent with the much slower current decay. In the case of the OPNS geometry, photo-generated electrons are transferred during illumination from the P3OT to the carbon nanotubes and then trapped in the SiO_2 layer. The hydrophobic parylene covers the SiO_2 and, as a result, water is kept away from the interface preventing the electrochemical charge transfer. This situation provides stable operation and optimum performances. In the absence of water, no charge relaxation in the dark is observed because of the absence of a decay channel for the electrons to transfer back into the nanotubes. The CNTs being in the vicinity of the SiO_2 traps, the reset operation is very efficient and similar to the one of a classical OG-CNTFET. The OPNS geometry thus represents the most appropriate configuration for the targeted use in programmable circuits.

Carbon nanotube optoelectronic memories are currently studied in our group as artificial synapses in adaptive circuits. Such circuit is trained at performing a selected function in analogy with the learning process in neuronal systems.[12,13] The sequence to reach a given function is composed of (i) the illumination time, (ii) the stabilization delay needed to reach the initial stable state (corresponding to all OG-CNTFETs set in their most conductive state), and (iii) the learning time. The response of the circuit to changing inputs is compared to the excepted value for each input combination, and the state of each device is updated until the function output converges toward the correct response. With classical OG-CNTFETs, the main contribution to the total duration of a learning cycle (time to change the function of the circuit) corresponds to the stabilization delay. By introducing the OPNS geometry in such circuit, a stable state is obtained as soon as the illumination is stopped. The time to reconfigure the function of the circuit is, therefore, drastically reduced.

Once programmed, a given state of conductivity must remain stable. Fig. 3(a) shows the response of the programmed ON-state after illumination with the absence of any sign of decay (for 700 s in the example of Fig. 3(a)). In contrast, a slight increase of the current is observed, which is due to the electrical stress at positive gate bias ($V_{GS} = 5$ V). This increase, which is not related to the optical gating mechanism, exists also in CNTFETs but would be absent for "normally OFF" devices (FETs in their off-state at $V_{GS} = 0$) because the optical "write" operation would then be performed at $V_{GS} = 0$. Note that concerning stability, we also tested the impact of temperature on the OG-CNTFET

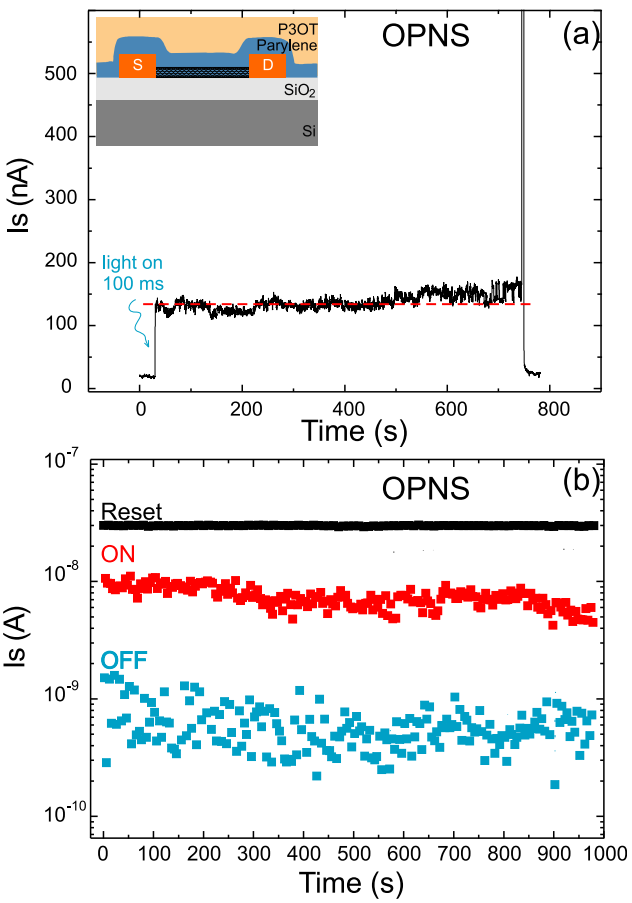

FIG. 3. (a) Stability of the programmed ON-state for an OPNS and (b) successive cycles composed of the following steps: optical write/read of the programmed "ON state" in the dark/electrical reset/read of the "OFF state." Both the "OFF" and "ON" states are measured in the dark before and after illumination respectively. "Reset" corresponds to the current during the negative gate bias pulse used to bring the device back to its initial high-resistance state.

operation and observed no degradation of the stability at 50°C. At 85°C, the retention and reset mechanisms were little impacted but the optical charging time was significantly increased and current instabilities were observed. Without additional investigation of thermal effects, operation at temperature above 50°C should be avoided.

For the proposed use in reconfigurable circuits, the memory devices must also support multiple write/read/erase/read cycles (Fig. 3(b)). We thus verified the robustness of the OPNS geometry by performing >100 cycles. The ON/OFF ratio remains roughly constant while the ON and OFF states show some variability. In the example of Fig. 3(b), the ON/OFF ratio is limited, due to the presence of metallic CNTs in the CNT network, an issue that would be absent for single-tube devices[9] or for CNT networks pattern in stripes[11] or prepared from sorted CNTs. For the type of circuits we studied, the variability of the programmed states is however not an issue. Indeed, in a learning process, the conductivity is adjusted for each device in small steps from its initial value to the value required for the targeted function. Controlling the precise value of the initial conductivity is useless in such approach. The extreme tolerance of circuits with learning capabilities to device variability is one of the main reasons why they are currently considered.

In conclusion, we showed that an electrochemical charge transfer process, most likely related to the presence of H_2O/O_2 species at the SiO_2 surface, is at the origin of the partial volatility of OG-CNTFET memory devices. By using parylene layers intercalated at different positions in the material stack composing OG-CNTFETs, we were able to sketch the charge transfer mechanisms leading to the operation of these memory devices. Based on this understanding, we proposed an optimized configuration in which a thin hydrophobic organic layer separates the CNTs on SiO_2 from the light absorbing material. This configuration barely affects the charging time and does not impact the programming efficiency while totally suppressing the need for a stabilization delay at light turn-off. This new design thus represents the best trade-off for the use of OG-CNTFETs in reconfigurable circuits.

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