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Negative Capacitance in Organic/Ferroelectric Capacitor to Implement Steep Switching MOS Devices

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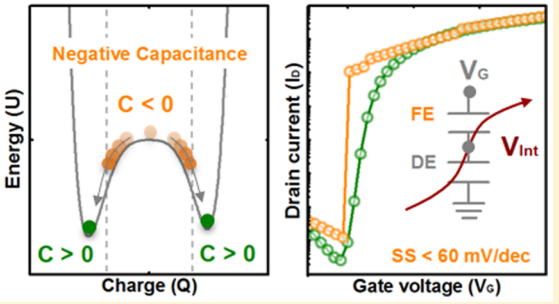
Supporting Information

ABSTRACT: Because of the "Boltzmann tyranny" (i.e., the nonscalability of thermal voltage), a certain minimum gate voltage in metal−oxide−semiconductor (MOS) devices is required for a 10-fold increase in drain-to-source current. The subthreshold slope (SS) in MOS devices is, at best, 60 mV/decade at 300 K. Negative capacitance in organic/ferroelectric materials is proposed in order to address this physical limitation in MOS technology. Here, we experimentally demonstrate the steep switching behavior of a MOS device—that is, SS ∼ 18 mV/decade (much less than 60 mV/decade) at 300 K—by taking advantage of negative capacitance in a MOS gate stack. This negative capacitance, originating from the dynamics of the stored energy in a phase transition of a ferroelectric material, can achieve the step-up conversion of internal voltage (i.e., internal voltage amplification in a MOS device). With the aid of a series-connected negative capacitor as an assistive device, the surface potential in the MOS device becomes higher than the applied gate voltage, so that a SS of 18 mV/decade at 300 K is reliably observed.



KEYWORDS: *negative capacitance, steep switching, metal−oxide−semiconductor field-effect transistor (MOSFET), ferroelectrics*

Over the past few decades, complementary metal−oxide−semiconductor (CMOS) technology has been successfully scaled down every two years. Particularly for sub-100 nm CMOS technology nodes, unprecedented technological innovations have enabled the timely development of CMOS technology; for example, stress engineering for 90 nm technology, the high-κ/metal-gate (HK/MG) technique for 45 nm technology, and advanced device structures such as the fin-shaped field-effect transistor (FinFET) for 22 nm technology. However, the power consumption of integrated circuits has significantly increased because of the limited scaling of power supply voltage (V_{DD}), or in technical terms, because of the nonscalability of thermal voltage (K_BT/q) (in accordance with the Boltzmann factor), which dictates that a certain minimum gate voltage is required for a 10-fold increase in drain-to-source current (i.e., the subthreshold slope (SS) is, at best, 60 mV/decade at 300 K). To address this physical limitation in CMOS technology, novel devices that employ turn-on mechanisms not governed by thermionic emission processes—such as Tunnel FETs (TFETs),[1] Feedback FETs (FBFETs),[2] nanoelectromechanical FETs (NEMFETs),[3] and negative capacitance FETs (NCFETs)[4,5] using ferroelectric materials[6−18]—have been developed. Among these, the NCFET is a promising CMOS-compatible candidate because (i) only a slight modification in the gate stack to include a ferroelectric material is required and (ii) previous developments such as stress engineering, the HK/MG technique, and the FinFET device structure can be employed. In this study, an organic/ferroelectric capacitor is first fabricated in order to experimentally realize the negative capacitance. It is then connected to a 1 μm MOS device. Afterward, the impact of negative capacitance on the "organic/ferroelectric capacitor plus MOS device" is investigated by analyzing the internal voltage vs gate voltage (V_{Int} vs V_G) and internal voltage gain vs gate voltage (V_{Int}/V_G vs V_G) plots. Sub-60-mV/decade SS is observed in the drain current vs gate voltage (I_D vs V_G) plot.

Experimental Results and Discussion. The switching speed of a MOS transistor can be represented by subthreshold slope, which is the inverse slope of the gate voltage vs drain current curve on a logarithmic scale when the applied gate voltage is in the subthreshold voltage region. The SS is mathematically expressed as eq 1, where V_G is gate voltage, I_D is drain current, φ_S is surface potential, K_B is the Boltzmann constant, T is temperature, and q is the electron unit charge

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$$SS = \frac{\partial V_G}{\partial \varphi_S}\frac{\partial \varphi_S}{\partial(\log_{10} I_D)} = \frac{\partial V_G}{\partial \varphi_S}\frac{K_B T}{q}\ln 10 \quad (1)$$

In eq 1, the second term—that is, $(K_B T/q)\ln 10$—is a constant value of 60 mV/decade at 300 K. Therefore, we focus on the first term, that is, the sensitivity of the applied gate voltage to the surface potential, which is referred to as the m-factor. The surface potential of conventional MOS devices is less than or approximately equal to the applied gate voltage, that is, $\varphi_s = V_G - \Delta V$. Because of the voltage drop ($\Delta V > 0$) in the dielectric insulation material (such as SiO_2 or HfO_2) of a MOS gate stack, the m-factor cannot be less than 1 ($m > 1$). This is valid for state-of-the-art MOS devices such as FinFETs and fully depleted silicon-on-insulator (FD-SOI) MOSFETs because the operation of these advanced devices is governed by thermionic emission processes. However, by enabling the positive feedback of voltages in a MOS gate stack, as suggested in previous research,[4] gate insulation layers consisting of ferroelectric materials such as $BaTiO_3$,[6] $Pb(Zr_{0.3}Ti_{0.8})O_3$,[7,8] and $P(VDF_{0.75}-TrFE_{0.25})$[9,10] (see Figure 1a) can lead to $\Delta V < 0$

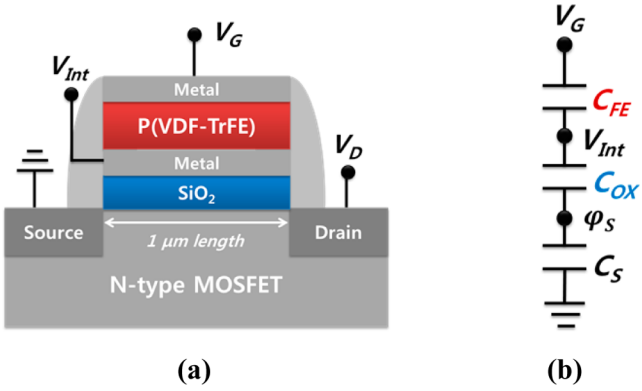

Figure 1. (a) Diagram showing the MOS capacitor connected in series with the ferroelectric capacitor and (b) a simple capacitor voltage divider. Note that the channel length and width of the n-type MOSFET are 1 and 10 μm, respectively.

(i.e., internal voltage amplification). Therefore, the surface potential can be higher than the applied gate voltage (i.e., $m < 1$), resulting in the negative capacitance effect of the ferroelectric insulator in a MOS device.

The relationship between capacitance and free energy is expressed in eq 2, where C_{FE} is capacitance of the ferroelectric capacitor, U_{FE} is free energy of the ferroelectric capacitor, and Q is charge. The energy characteristic of a ferroelectric capacitor, depicted in Figure 2, is calculated from $U_{FE} = \alpha P^2 + \beta P^4 + \gamma P^6 + E_{ext}P$, where P is the ferroelectric polarization of the ferroelectric capacitor, E_{ext} is the externally applied electric field, $\alpha = \alpha_0(T - T_c)$, T_c is the Curie temperature, $\alpha_0 = 1.75 \times 10^7$ Jm/C^{2}K, $\beta = -0.375 \times 10^{12}$ Jm^5/C^4, and $\gamma = 0.316 \times 10^{14}$ Jm^9/C^6 for $P(VDF_{0.75}-TrFE_{0.25})$.[11]

$$C_{FE} = \left[\frac{d^2 U_{FE}}{dQ^2}\right]^{-1} \quad (2)$$

Here, it should be noted that "negative capacitance" is used to refer to "negative differential capacitance" because of a small-signal concept of the capacitance and the relationship between C_{FE} and U_{FE} in eq 2. Previous studies[4,8] have discussed the fact that the negative capacitance exists not in a static state but in a

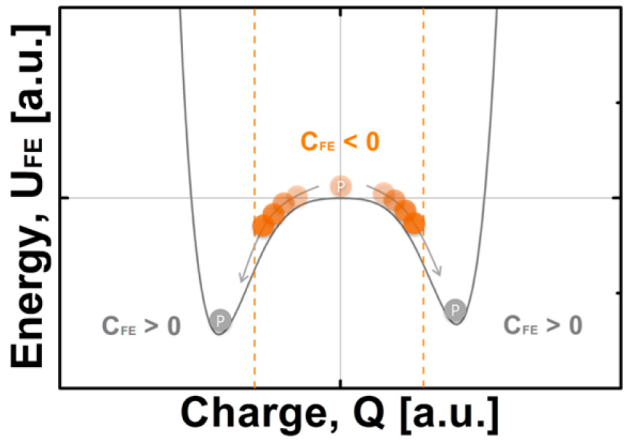

Figure 2. Free energy landscape (energy vs charge) of a ferroelectric capacitor in equilibrium.

dynamic state. More specifically, while switching from one stable polarization to the other, a ferroelectric material reveals its negative capacitance. Thus, direct measurement of the negative capacitance in a single ferroelectric capacitor is very difficult because of the instability of the negative capacitance. However, if a series dielectric capacitor (e.g., a gate oxide capacitor in a MOS gate stack) is connected in series with the ferroelectric capacitor, this instability can be removed.[4,8] This type of configuration enables the ferroelectric capacitor to act as a voltage transformer that amplifies the input voltage (e.g., the gate voltage of a MOS device).

In order to observe the negative capacitance effect in a MOS device, a ferroelectric capacitor was fabricated. An 80 nm thick titanium nitride (TiN) metal layer was deposited on a bulk silicon substrate via DC magnetron sputtering. This metal layer is necessary to achieve full functionality of the ferroelectric capacitor, for two reasons: (i) it ensures that the ferroelectric capacitor is compatible with the TiN gate material used in modern HK/MG MOS technology and (ii) it blocks the leakage current path between the ferroelectric material and the silicon substrate—a ferroelectric material loses its functionality in the presence of leakage currents. A solvent of methyl ethyl ketone (MEK) was used to prepare a 1 wt % solution of $P(VDF_{0.75}-TrFE_{0.25})$ ferroelectric material. The solution was heated on a hot plate (at ~60 °C) for more than 1 h and then spin coated on top of the TiN layer at 1500 rpm for 30 s to create a ferroelectric insulation layer of ~19 nm in the ferroelectric capacitor (see Figure S1 in Supporting Information). The specimen was then annealed on a hot plate at ~140 °C for 1 h. Thereafter, a 42 nm thick gold top electrode was deposited via thermal evaporation. To confirm the impact of the negative capacitance of the fabricated ferroelectric capacitor on the SS of the MOS transistor, the ferroelectric capacitor was connected in series with a 1 μm MOSFET (see Figure S4 in Supporting Information). A semiconductor characterization system (Keithley 4200-SCS) was used for all measurements.

In order to experimentally verify the voltage amplification produced by the negative capacitance in the MOS gate stack, the V_{Int} vs V_G curve of the MOS gate stack including both the ferroelectric insulator and the dielectric insulator was plotted. Figure 3a shows internal voltage vs gate voltage for various drain voltages in an n-type MOS (NMOS) transistor. It is noteworthy that the voltage amplification in the organic/ferroelectric capacitor can be achieved only when the

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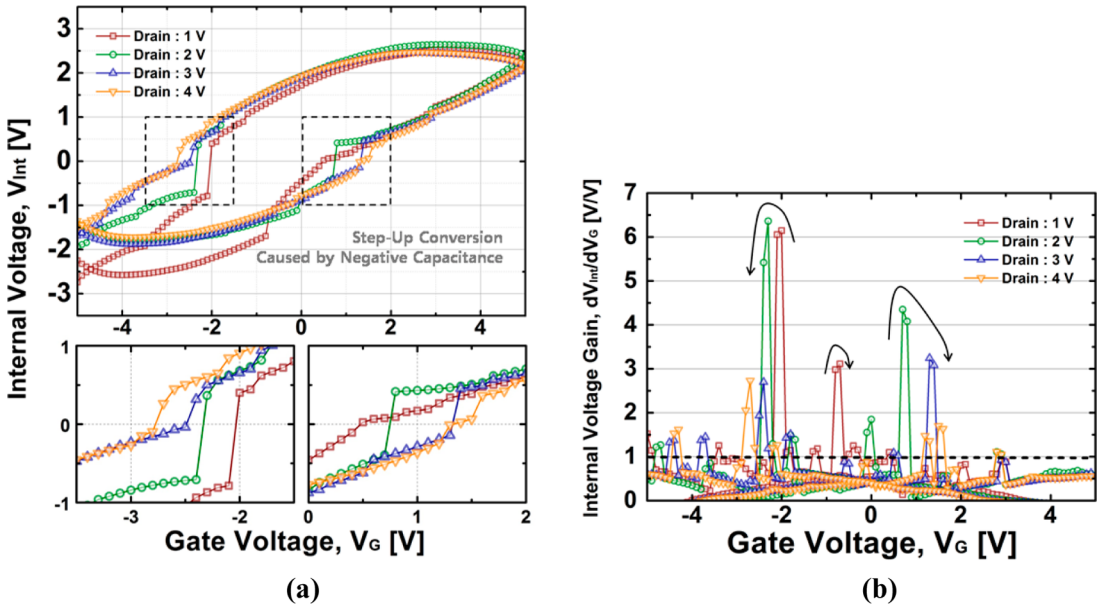

Figure 3. (a) Internal voltage vs gate voltage and (b) internal voltage gain vs gate voltage curves for different drain voltages [i.e., 1 V (red), 2 V (green), 3 V (blue), and 4 V (yellow)] in an NMOS transistor. The step-up conversion of the internal voltage is accomplished through the negative capacitance effect of the organic/ferroelectric capacitor (see the regions enclosed in dashed-line boxes in Figure 3a), and as a result the internal voltage gain increases to 6.4 V/V in the NMOS transistor.

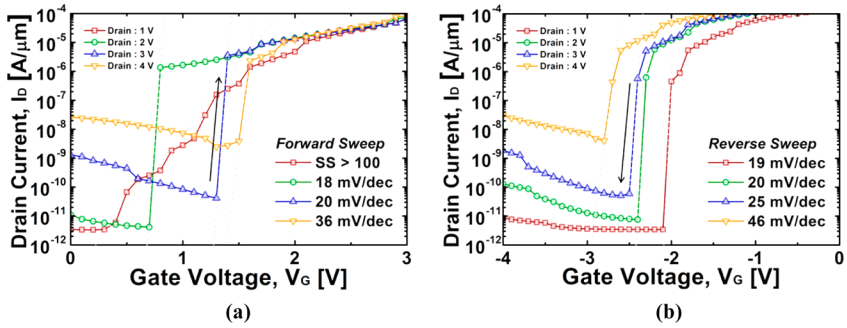

Figure 4. Measured I_D as a function of V_G with (a) forward and (b) reverse gate voltage sweep for different drain voltages [1 V (red), 2 V (green), 3 V (blue), and 4 V (yellow)] with the organic/ferroelectric capacitor connected in series with the NMOS transistor. The steep switching behavior (SS < 60 mV/decade at 300 K) due to the negative capacitance effect is explicitly demonstrated (see the complete hysteresis loop in Figure S6 of Supporting Information). The region in which the steep switching behavior is observed corresponds to the region of the step-up conversion of the internal voltage. Note that the SS of the NMOS transistor without the organic/ferroelectric capacitor is 92 mV/decade (see Figure S3 in Supporting Information).

$P(VDF_{0.75}-TrFE_{0.25})$ molecular chain is rotated 180° (i.e., phase transition of the ferroelectric material), but the voltage amplification in inorganic/ferroelectric materials such as $BaTiO_3$ and $Pb(Zr_{0.3}Ti_{0.8})O_3$[12] can be accomplished through ionic displacement. In order to completely change the phase of the organic/ferroelectric material, the applied gate voltage should be higher than the coercive voltages[8] (i.e., −1 V and +2.3 V) of the organic/ferroelectric capacitor (see Figure S2 in Supporting Information). The gate voltage of the NMOS transistor was varied from −5.0 V to +5.0 V and back to −5.0 V. As shown in Figure 3a (particularly in the dashed-lined boxes), a step-up conversion of the internal voltage (i.e., voltage amplification) is explicitly observed as a result of the phase transition of $P(VDF_{0.75}-TrFE_{0.25})$. In order to quantitatively determine how much voltage amplification is achieved, V_{Int}/V_G vs V_G curves of the NMOS transistor were plotted (see Figure 3b). Step-up conversion of the internal voltage is accomplished through the negative capacitance effect of the organic/ferroelectric capacitor, and as a result the value of the internal voltage gain dramatically increases to 6.4 V/V in the NMOS transistor. This increase in the internal voltage allows the surface potential to be higher than the gate voltage, but only when the voltage drop in the dielectric insulation layer of the MOS gate stack (i.e., ΔV between V_{Int} and φ_s) is smaller than the difference between V_G and V_{Int}. If this is the case, $dV_G/d\varphi_s$ in eq 1 can be less than 1, resulting in sub-60-mV/decade SS at 300 K. In order to experimentally observe the steep switching behavior of the transistor, the input transfer characteristics (I_D vs V_G) were measured (see Figure 4).

To experimentally observe the steep switching behavior of the MOS device, the following two conditions must be satisfied: (i) the surface potential corresponding to a certain gate voltage must be amplified (i.e., m-factor <1) as a result of the phase transition of the ferroelectric material; (ii) the gate voltage mentioned in (i) must be in the switching region of the MOS device. As shown in Figure 4 (i.e., drain current vs gate voltage curves for the n-type MOS device with the ferroelectric capacitor), the steep switching explicitly occurs because the two

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conditions are satisfied in the NMOS transistor at 300 K. The SS decreased to 18 (19) mV/decade for the NMOS device under forward (reverse) sweeping of the gate voltage. However, the steep switching is not observed (forward sweeping) when the drain voltage is 1 V because the condition (ii) is not satisfied (see Figure 3a). In other words, the fundamental reason is originated from the "capacitance matching" issue between the negative capacitance and the drain-voltage-dependent MOS capacitance.[14,19]

Though steep switching behavior is achieved in the MOS transistor, there is unwanted hysteresis caused by the remnant polarization of the organic/ferroelectric capacitor (see Figure S6 in Supporting Information). Moreover, drain voltage also contributes to the hysteresis to some degree because of the electrostatic coupling between the channel and drain region in the MOS device.[19] Although a theoretical solution for these issues has been proposed in previous papers,[4,8,13−15] this solution is not adequately supported by experimental investigations. In order to take full advantage of the negative capacitance effect in MOS technology, these issues must be thoroughly investigated in the future.

In summary, the SS of MOS devices can be significantly improved by simply connecting an organic/ferroelectric capacitor in series with the MOS transistor. With the aid of a series-connected negative capacitor (i.e., with the internal voltage amplification produced by the negative capacitance component of the organic/ferroelectric capacitor), the surface potential in the MOS device increases beyond the applied gate voltage. Therefore, including an organic/ferroelectric insulation layer in a MOS gate stack is a promising technique for continuously scaling down the current HK/MG MOS technology. In other words, the "HK/ferroelectric-material/MG" gate stack could become a solution to implementing steep switching devices for ultralow-power applications. Furthermore, if the organic/ferroelectric capacitor as an assistive device is placed in the back end of line (BEOL) for the purpose of improving the performance of the front end of line (FEOL) MOS device, we can continue to employ advanced device structures such as FinFETs and FD-SOI MOSFETs at sub-14-nm MOS technology nodes without the need for another new transistor structure, such as the gate-all-around transistor.

Conclusion. Because of the increasing demand for ultralow-power MOS device technology, the negative capacitance FET has recently gained prominence because of its compatibility with current MOS technology as well as its steep switching characteristics. In this study, the effects of negative capacitance on MOS devices were experimentally demonstrated and investigated. An organic/ferroelectric capacitor was fabricated using P($VDF_{0.75}$−$TrFE_{0.25}$) material and connected in series with the gate electrode of a MOS device in order to observe the negative capacitance characteristics of the MOS device. The V_{Int} vs V_G curve showed that step-up conversion of the internal voltage occurred because of the phase transition of the organic/ferroelectric capacitor (i.e., the negative capacitance), and the V_{Int}/V_G vs V_G curve showed that the surface potential in the MOS gate stack was amplified (i.e., m-factor < 1). Furthermore, steep switching behavior in the I_D vs V_G curve (i.e., SS < 60 mV/decade at 300 K) was clearly and reliably observed. The SS of the "organic/ferroelectric capacitor plus NMOS device" was dramatically improved—to 18 mV/decade at 300 K—compared with the NMOS device alone.

■ ASSOCIATED CONTENT

Supporting Information

Detailed description of the fabrication steps for the ferroelectric/organic capacitor, the cross-sectional TEM image of the capacitor, and additional measurement data. The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acs.nanolett.5b01130.

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Author Contributions

J.J. and C.S. conceived and designed all the experiments. J.J. performed all the measurements. W.Y.C. prepared MOS devices used in this work. J.J., W.Y.C., J.-D.P., J.W.S., H.-Y.Y., and C.S. discussed the results and commented on the manuscript.

Notes

The authors declare no competing financial interest.

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