Interface states in GaAs/Al x Ga1−x As heterostructures grown by organometallic vapor phase epitaxy

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Our results show that, similar to oxidation, Al deposition on $Hg_{1-x}Cd_xTe$ results in a local Hg depletion. This conclusion, however, cannot be generalized to all other interface formation processes involving $Hg_{1-x}Cd_xTe$. Preliminary results on Ge deposition show indeed no evidence for Hg depletion and a local chemical composition close to that of the cleaved substrate. The experimental conditions were similar those of the Al overlayer experiments. Therefore, the preliminary results on Ge overlayers also rule out spurious causes for the Hg depletion during Al deposition, e.g., radiant thermal annealing of the substrate.

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[7]C. J. Powell, R. J. Steiner, P. B. Needham, and T. J. Briscoll, Phys. Rev. B **16**, 1370 (1977). The escape depth should actually be larger in our case since the photoelectron kinetic energy is smaller. This gives even stronger evidence that the decrease in the Hg/Cd intensity ratio cannot be due to Cd atoms diffusing towards the surface.
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Interface states in GaAs/$Al_xGa_{1-x}As$ heterostructures grown by organometallic vapor phase epitaxy

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The GaAs/$Al_xGa_{1-x}As$ interface grown by organometallic vapor phase epitaxy has been studied by transient capacitance techniques. No electron emissions have been observed from deep states at or near the interface of a GaAs/$Al_{0.2}Ga_{0.8}As$ junction. Highly nonexponential transients were recorded for emissions near the interface, which arise from states with an apparent activation energy of 0.15 eV. Dominant deep traps were detected in the GaAs and $Al_{0.2}Ga_{0.8}As$ in regions away from the interface. The implications of the results have been discussed.

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Organometallic vapor phase epitaxy (OMVPE) is being widely used for the controlled growth of GaAs-$Al_xGa_{1-x}As$ heterostructures in optoelectronic devices.[1-3] Properties of the GaAs/$Al_xGa_{1-x}As$ interface are intimately related to device performance. A careful study of traps or other spatially localized states near the OMVPE GaAs/$Al_xGa_{1-x}As$ interface, arising from lattice mismatch or grown-in defects, has not been made. Such studies have only been made for similar heterostructures grown by liquid phase epitaxy (LPE) (Ref. 4) and more recently by molecular beam epitaxy (MBE) (Ref. 5). In this letter we report the observation of interface states near the n-GaAs/n-$Al_xGa_{1-x}As$ junction grown by OMVPE using transient capacitance techniques.

The structure used is depicted in Fig. 1 and was grown on Sn-doped GaAs substrates at 750 °C. The purest available sources of trimethylgallium, trimethylaluminum, arsine, and diethylzinc were used. The V/III ratio for the different layers varied but was ~ 10. The thicknesses of the different layers in the heterostructures are as follows: 2.5-μm undoped n-$Al_{0.2}Ga_{0.8}As$, 0.9-μm undoped n-GaAs, 1.5-μm p-$Al_{0.2}Ga_{0.8}As$, and ~ 1-μm p-GaAs. The hole concentration in the last two layers is $\geqslant 1.0\times 10^{17}$ cm^{-3}. It was important to ensure that the undoped n-GaAs layer had the right doping and thickness, so that the edge of the depletion region could be swept through the GaAs/$Al_{0.2}Ga_{0.8}As$ interface. The composition of the ternary layer was purposely chosen similar to those more commonly used in practical devices. Alloyed Ag-Sn and Au-Zn ohmic contacts were formed on

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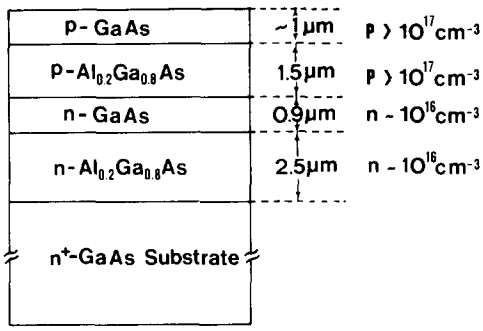

FIG. 1. Schematic diagram of GaAs/$Al_xGa_{1-x}As$ heterostructures used in this study.

the n and p sides of the wafers, respectively. Diodes of area 0.5–1.0 mm^2 were formed by cleaving.

The net electron concentration profile in regions of the n-GaAs and n-$Al_{0.2}Ga_{0.8}As$ layers near the heterointerface is shown in the upper part of Fig. 2. The profile was obtained by capacitance-voltage measurements with a 1-MHz bridge. It may be noticed that the expected accumulation layer on the GaAs side of the interface[6] is almost absent. The interface is found to be located at about 0.9 μm from the p-$Al_{0.2}Ga_{0.8}As$-n-GaAs junction. Transient capacitance measurements with varying quiescent reverse bias applied to the diode were performed to detect trapping states in regions near the interface. This method was used, in preference to deep level transient spectroscopy (DLTS), to allow the careful recording and analysis of nonlinearities in the transient signal due to large trap densities or high-field effects.

In regions far from the interface emissions from the well known 0.82-eV dominant electron trap were observed in GaAs and from the 0.82- and 0.65-eV electron traps in $Al_{0.2}Ga_{0.8}As$.[7]

The trap concentration profile $N_T(d)$ was calculated

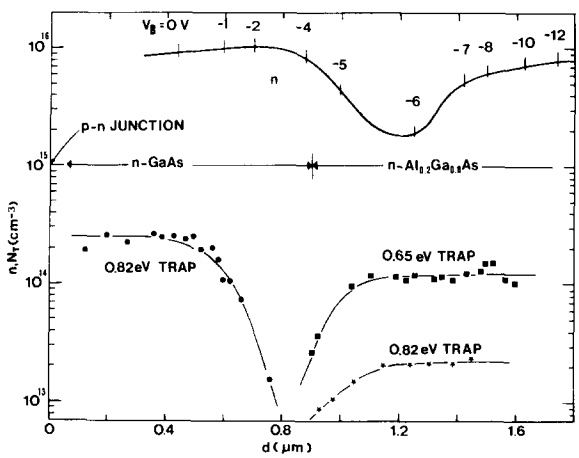

FIG. 2. Spatial electron concentration and electron trap concentration profiles in the n-type layers of a p^+-$Al_{0.2}Ga_{0.8}As$/n-GaAs/n-$Al_{0.2}Ga_{0.8}As$ heterojunction. The profiles of electron concentration and the concentrations of the 0.82-eV trap in GaAs and 0.65-eV trap in $Al_{0.2}Ga_{0.8}As$ were measured at 20 °C. The concentration profile of the 0.82-eV trap in $Al_{0.2}Ga_{0.8}As$ was measured at 89 °C. The vertical markings on the carrier concentration profile represent the depletion layer edge at the bias values indicated.

from

$$N_T(d) = -N_D(W)\frac{W^2}{d\,\Delta d}\frac{\Delta C}{C}, \tag{1}$$

where W is the depletion layer width at the quiescent reverse bias, $N_D(W)$ is the net donor density at the edge of the depletion layer, ΔC is the capacitance change at the instant $t = 0^+$ after the application of the majority-carrier pulse, C is the device capacitance for the quiescent reverse bias, and Δd is the change in the depletion layer width with the application of the majority-carrier pulse. The value of Δd, which in our experiments was typically $\sim 0.05\,\mu$m, determines the spatial resolution of the distribution of traps. The depth d is given by

$$d = W - \lambda$$
$$= W - \sqrt{2\epsilon\epsilon_0(E_T - E_F)/e^2N_D}, \tag{2}$$

where λ is the distance between the edge of the depletion layer and the point where the Fermi level crosses the trap level, E_F is the Fermi Energy, and E_T is the trap activation energy. The majority-carrier pulse height and the value of reverse bias were so chosen that $\Delta d \ll d$. An important experimental consideration should be mentioned. The free-carrier concentration at the leading edge of the depletion region is low compared to that in the bulk.[8] Consequently the capture rate given by $c = \sigma_n v_{\rm th} n$, where σ_n is the thermal electron capture cross section and $v_{\rm th} = (3\ {\rm kT}/m_n^*)^{1/2}$ is the electron thermal velocity, is also small. Thus, the filling times have to be sufficiently large to fill the entire trap population. This was ascertained by ensuring saturation of ΔC due to trap filling.

The concentration profiles of the bulk traps in GaAs and $Al_{0.2}Ga_{0.8}As$ were obtained by using Eqs. (1) and (2) and are shown in the lower part of Fig. 2. The nearly uniform values of the bulk electron concentration, away from the heterointerface depletion region, were used to calculate the trap concentration profiles across the interface. It may be noted that the trap concentrations decrease drastically near the interface. The 0.82-eV electron traps in both GaAs and $Al_{0.3}Ga_{0.7}As$ are the same center. but are observed at different temperatures.[7] A similar trend was observed for hole traps near LPE-grown GaAs/$Al_xGa_{1-x}As$ interfaces, and was interpreted as being due to the Debye length limitation of the spatial resolution.[4] In our case, the change in the profile appears to be much more diffused.

A new electron emission was observed near the interface around room temperature. Careful measurements of the capacitance transients related to this emission revealed the following features: the temperature dependence of the emission time constant was very weak, and the transients were highly nonexponential. Both these features are depicted in Fig. 3. The inset shows the recorded transient at two temperatures. The Arrhenius plots were obtained from time constants τ_s and τ_l extrapolated from the fast and slow portions, respectively, of each capacitance transient. It is noteworthy that both time constants yield an apparently identical activation energy of 0.15 eV from detailed balance considerations. The concentration profile of the trap in the n-GaAs and n-$Al_{0.2}Ga_{0.8}As$ layers near the heterojunction is shown in Fig. 4. The peak value of the trap concentration,

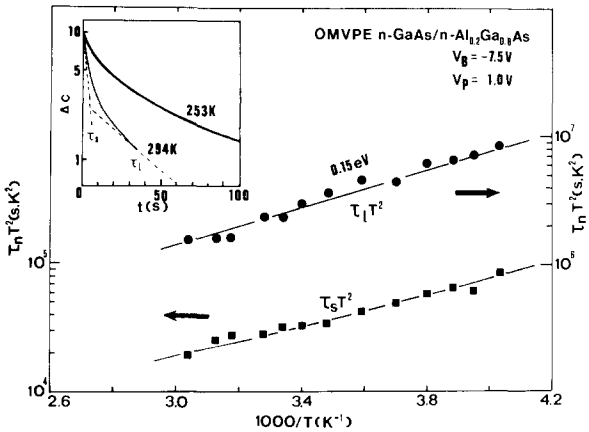

FIG. 3. Temperature dependence of electron emission time constants near the n-GaAs/n-$Al_{0.2}Ga_{0.8}As$ interface. The capacitance transients are highly nonexponential as shown in the inset. τ_s and τ_l are the time constants corresponding to the fast and slow portions of the transients. V_B is the quiescent reverse bias and V_p is the magnitude of the majority-carrier pulse applied to the diode.

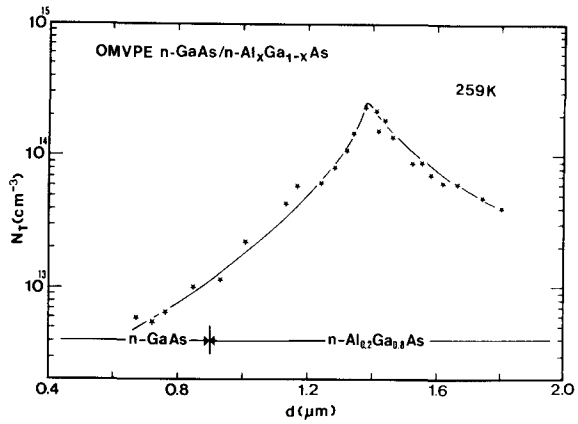

FIG. 4. Concentration profile of the electron trap detected near the n-GaAs/n-$Al_{0.2}Ga_{0.8}As$ interface.

which is measured in the ternary layer, is 2.3×10^{14} cm^{-3} and has a full width at half-maximum of 0.14 μm. It is apparent that the trap is fairly localized near the interface and hence can be associated with it.

The highly nonexponential emission capacitance transients and the apparently low activation energy of the interface states near room temperature are indicative of a band of overlapping states rather than a discrete level. Surface states on GaAs also show similar emissions, the time constants of which are almost independent of temperature. A continuum of states can also explain the large shift in the peak position of the interface state concentration from the interface, as seen in Fig. 4. It must be remembered that the distance d in the abscissa of Fig. 4 is given by $d = W - \lambda$, where λ is dependent on the trap depth. The profile in Fig. 4 was derived with $E_T = 0.15$ eV. For example, a value of $E_T = 0.64$ eV will shift the peak position of the interface trap density to the interface. It is therefore most likely that the observed emissions arise from a broadband of interface states with their density profile exhibiting a broad peak at an energy depth which might be larger than 0.15 eV.

The difference in time constant at room temperature for the electron emission from the 0.82-eV traps in GaAs and $Al_{0.2}Ga_{1-x}As$ at room temperature is about two orders of magnitude.[7] The difference in time constants corresponding to the fast and slow portions of the emission transient from the trap near the interface is also two orders of magnitude. One might, therefore, be tempted to conclude that the observed nonexponential transient in the interface region results from simultaneous emission from the 0.82-eV traps in the two sides. This explanation can, however, be ruled out, since in that case, at least one of the time constants should have given a thermal activation energy of 0.82, or a value close to it, instead of the measured 0.15 eV.

Our data are insufficient to predict the origin of the interface states or even the exact location of the traps which give rise to the observed emission. Recent work by us[9] has shown that a two-dimensional electron gas (2DEG) (Ref. 10) is formed at the OMVPE $Al_xGa_{1-x}As$-substrate GaAs:Cr interface. A similar 2DEG may be present at the grown junction under study. The measured activation energy could then be very indirectly related to the effective barrier height resulting from the conduction-band discontinuity. Excess carriers are possibly trapped during the injection pulse and are emitted over the barrier ($\sim$0.4 eV) when the diode is switched back to a quiescent reverse bias. Experiments are in progress to study these aspects in more detail. The conclusive evidence of this study is that there are probably no deep traps at the GaAs/$Al_xGa_{1-x}As$ interface grown by OMVPE. The high quality of interfaces grown by OMVPE has also been indirectly demonstrated by the performance of laser structures.[11]

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