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Life-Cycle Energy Demand and Global Warming Potential of Computational Logic

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Computational logic, in the form of semiconductor chips of the complementary metal oxide semiconductor (CMOS) transistor structure, is used in personal computers, wireless devices, IT network infrastructure, and nearly all modern electronics. This study provides a life-cycle energy analysis for CMOS chips over 7 technology generations with the purpose of comparing energy demand and global warming potential (GWP) impacts of the life-cycle stages, examining trends in these impacts over time and evaluating their sensitivity to data uncertainty and changes in production metrics such as yield. A hybrid life-cycle assessment (LCA) model is used. While life-cycle energy and GWP of emissions have increased on the basis of a wafer or die, these impacts have been reducing per unit of computational power. Sensitivity analysis of the model shows that impacts have the highest relative sensitivity to wafer yield, line yield, and die size and largest absolute sensitivity to the use-phase power demand of the chip.

Introduction

Whether broader adoption of information technology results in increased impact on the environment is an important question posed in policy and business. The questions of whether reading news on a hand-held device or purchasing books online reduces environmental impact are two examples from the recent literature (*1*, *2*). Among the numerous components of the IT infrastructure, semiconductor chips are among the most resource-intensive to produce as well as the most difficult to characterize for the purposes of life-cycle assessment (LCA). While it may be possible to estimate the environmental impacts of a cable or plastic computer housing knowing only their masses and material types, the impacts associated with a semiconductor chip are not represented well by the substance of the device itself. While a logic chip weighs only a few grams, the chemicals and water required to produce it weigh many kilograms. In many LCA studies of electronics, the lack of LCA data for computer chips has been acknowledged as an important topic for future work and the need for a more detailed and transparent life-cycle inventory for semiconductor products has been noted previously (*3*–*7*).

Complementary metal oxide semiconductor (CMOS) is the dominant device structure for digital logic. The central processing unit (CPU) in desktops, laptops, hand-held devices, and servers, as well as nearly all embedded logic (the chips in appliances and toys) is CMOS-based. Every one to three years, a new generation or technology node of CMOS is introduced, based on design laws which have been established through industrial collaboration. Due to the cooperation necessary to plan and achieve the goals for each generation there is considerable homogeneity among the devices, making it possible to represent CMOS logic using a generic form at each technology node. This paper presents an energy LCA for chips of generic CMOS logic over a 15 year period, from the 350 nm node (ca. 1995) to the 45 nm node (ca. 2010). This study is composed of production LCA data, based on emissions measurements, process formulas, and equipment electrical tests, combined with previously published LCA data for chemicals, electricity, and water, as well as publicly available use-phase data for computer chips.

Methodology

This life-cycle inventory (LCI) includes materials production, wafer processing, die packaging, transportation, and use of the logic chip. (For an overview of semiconductor manufacturing processes, please refer to a related paper in this journal (*8*).) The LCA model is hybrid, using a combination of process-based LCA and economic input−output (EIO) LCA data (Table 1) (*9*). The functional unit is one chip, but to allow further analysis and investigate trends, results are also presented per wafer and per million instructions per second (MIPS).

Because there is almost no recoverable value in a discarded IC, it is assumed that the IC is disposed of in a landfill at end-of-life (EOL). EOL energy and global warming potential (GWP) are therefore considered to be zero.

Inventory Model Structure. The contributors to the life-cycle energy requirements (e_{total}) and GWP of life-cycle emissions (g_{total}) are illustrated in eqs 1 and 2.

$$e_{total} = e_{up} + e_{inf} + e_{prod} + e_{trans} + e_{use} \quad (1)$$

$$g_{total} = g_{up} + g_{inf} + g_{prod} + g_{trans} + g_{use} \quad (2)$$

e_{up}: energy for upstream materials
g_{up}: GWP of emissions due to upstream materials
e_{inf}: energy for infrastructure
g_{inf}: GWP of emissions due to infrastructure
e_{prod}: energy for production
g_{prod}: GWP of emissions due to production
e_{trans}: energy for transportation
g_{trans}: GWP of emissions due to transportation
e_{use}: use-phase energy
g_{use}: GWP of emissions due to use-phase energy

Energy and global warming potentials for chemical production, i.e., upstream activity, are given by e_{up} in eq 3 and g_{up} in eq 4. Process chemicals are split into two sets, the

TABLE 1. Summary of Data Sources

silicon	process LCA
chemicals	process and EIO−LCA
infrastructure and equipment	EIO−LCA
fabrication	process LCA
electricity	process LCA
water	process LCA
transportation	process LCA
use	process LCA

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first set of m chemicals for which EIO−LCA data are used (*9*), and a second set of q chemicals for which process LCA data are used. $e_j^{\$}$ is the energy consumption per dollar value of chemical j, c_j is the cost per unit mass of j, and m_{ij} is the mass of j consumed in process step i. The wafer yield (Y_{wafer}) is the percentage of good die per wafer, the line yield (Y_{line}) is the percentage of finished wafers of those started, and gross yield (n_{die}) is the number of dies per wafer.

$$e_{up} = \frac{1}{Y_{wafer}Y_{line}n_{die}}\left[\sum_{j=1}^{m} e_j^{\$}c_j\sum_{i=1}^{n} m_{ij} + \sum_{k=1}^{q} e_k^m\sum_{i=1}^{n} m_{ik}\right] \quad (3)$$

$e_j^{\$}$ is the energy consumption per dollar value of chemical j

c_j: cost per unit mass of j

m_{ij}: mass of j consumed in process step i

e_k^m: energy consumption per unit mass of chemical k

m_{ik}: mass of k consumed in process step i

$g_j^{\$}$: GWP of emissions per dollar value of chemical j

$$g_{up} = \frac{1}{Y_{wafer}Y_{line}n_{die}}\left[\sum_{j=1}^{m} g_j^{\$}c_j\sum_{i=1}^{n} m_{ij} + \sum_{k=1}^{q} g_k^m\sum_{i=1}^{n} m_{ij}\right] \quad (4)$$

c_j: cost per unit mass of j

m_{ij}: mass of j consumed in process step i

g_k^m: GWP of emissions per unit mass of chemical k

m_{ik}: mass of k consumed in process step i

The energy and greenhouse gas (GHG) emissions due to facility infrastructure and capital equipment are found using the EIO−LCA method. The EIO−LCA model is described completely in the literature (*10, 11*).

The total energy used in production (e_{prod}) consists of all electricity and natural gas used by production tools and the facility infrastructure, as given in eq 5. Equation 6 describes the GWP of production which includes both energy-related emissions and direct GHG releases.

$$e_{prod} = \frac{1}{Y_{wafer}Y_{line}n_{die}}\left[\sum_{i=1}^{n}\left(\frac{t_i p_i + e_{CH_4}t_i m_{i,CH_4} + \hat{e}_w^v\hat{u}_i t_i}{\varepsilon_i u}\right) + \frac{p_{hvac} + p_{lt} + p_{tri} + p_{cda} + p_{exh}}{c}\right] \quad (5)$$

t_i: duration of process i

p_i: process tool and POU abatement power consumption for process i, per chamber

e_{CH_4}: energy per unit mass methane

m_{i,CH_4}: mass flow of methane for pocess i

$\hat{e}_w$: vector of volumetric energy requirements for ultrapure, process cooling, and city water flow, per chamber

$\hat{u}_i$: vector of ultrapure, process cooling, and city water flows for process i, per chamber

ε_i: process utilization for process step i

u: tool utilization

p_{hvac}: facility HVAC power consumption

p_{lt}: facility lighting power consumption

p_{tri}: facility treatment system power consumption

p_{cda}: facility CDA power consumption

p_{exh}: facility exhaust system power consumption

c: facility production capacity

t_i: duration of process i

$$g_{prod} = \frac{1}{Y_{wafer}Y_{line}n_{die}}\left(\sum_{i=1}^{n} t_i\hat{m}_i\hat{g} + l + e_{prod}g_e^{prod}\right) \quad (6)$$

$\hat{m}_i$: vector of mass flows of all process chemicals for process i

$\hat{g}$: vector of GWP per unit mass of all process chemicals

l: CO_2 emissions per wafer due to facility methane use

g_e^{prod}: GWP of electricity used in production

Energy and emissions due to transportation are given in eqs 7 and 8 by e_{trans} and g_{trans}, where the two legs of transportation refer to transport from the water fabrication facility (fab) to assembly plant, and from assembly site to use. e_{trans} and g_{trans} are derived from transport distances d for each leg i, where t denotes truck; $r$denotes rail; b denotes boat, and a denotes air freight, and the product and packaging mass for leg i is m_i.

$$e_{trans} = \frac{1}{Y_{wafer}Y_{line}n_{die}}\left[\sum_{i=1}^{2}(d_{i,t}e_t^d m_i + d_{i,r}e_r^d m_l + d_{i,b}e_b^d m_l + d_{i,air}e_{air}^d m_l)\right] \quad (7)$$

$$g_{trans} = \frac{1}{Y_{wafer}Y_{line}n_{die}}\left[\sum_{i=1}^{2}(d_{i,t}g_t^d m_i + d_{i,r}g_r^d m_l + d_{i,b}g_b^d m_l + d_{i,air}g_{air}^d m_l)\right] \quad (8)$$

e_t^d: energy use per mass transported a unit distance

g_t^d: GWP per mass transported a unit distance

m_i: product and packaging mass over leg i

$d_{i,x}$: distance over leg i transported by mode x

In eq 9, the use-phase energy consumption is found as the product of device power (p_{use}), power supply efficiency (ε_{supp}) and lifespan (t_{life}). The equation for use-phase GWP emissions applies the GWP intensity of use-phase electricity (g_e^{use}) to use-phase energy consumption (eq 10).

$$e_{use} = p_{use}\varepsilon_{supp}t_{life} \quad (9)$$

$$g_{use} = g_e^{use}e_{use} \quad (10)$$

"Upstream" Materials. *Silicon.* There are several processing steps that raw silica undergoes to become a pure silicon wafer, the substrate of semiconductor devices. The high embedded energy of the final product (2000 kWh/kg) is due not only to the energy intensity of these processes, but also a cumulative low yield caused by the losses at each step (*5*). Further description of the energy requirements and environmental emissions of high-purity silicon production are available from previous work (*5, 12*).

Water. The environmental impacts of the Santa Clara water supply are modeled using information from the Santa Clara Valley Water District and a previous LCA of California water supplies by Stokes and Horvath (*13*). The resulting GWP emission factor per liter of Santa Clara water is 0.6 g CO_2eq.

Chemicals. Among the life-cycle impacts of semiconductor products, the importance of energy-related emissions from the production of high purity chemicals has been noted previously (*5, 7, 14, 15*). The limited LCA data available for exotic and high-purity semiconductor process chemicals remains a challenge in quantifying these impacts. While LCA data are available for some basic chemicals used in wafer manufacturing, such as elemental gases and common acids, it is usually representative of the industrial grade, with a purity of 99% or lower, rather than ultrahigh-purity or semiconductor grade (99.9997% to 99.9999999% pure). The detailed method of LCA data collection as well as impact factors and data sources are provided in the Supporting Information.

Infrastructure and Equipment. GWP emissions and energy consumption for fab construction and equipment for both the California and China scenarios are represented by U.S.

averages, which are determined by each industry sector's impacts per dollar in EIO−LCA (*9*).

GWP and Primary Energy Demand of Electricity. In the fabrication stage, electricity emissions factors are specific to California and China. In the use stage, the location is assumed to be California, and the California electricity emissions factor is used. The environmental impacts associated with electricity supplied to the California plant are evaluated using two previous LCAs of electricity generation, data from the EPA and information from Santa Clara's electric utility, Pacific Gas and Electric. The life-cycle GHG emission factors (g CO_2eq/kWh) for natural gas, coal, large scale hydroelectric, and solar photovoltaic power are taken from Pacca and Horvath (*16*), while that for nuclear electricity is taken from Fthenakis (*17*). Direct GHG emissions for geothermal and biomass combustion are taken from the EPA (*18*). Small hydro is considered to have the same impacts as large hydro. A national average for the Chinese grid of 877 g CO_2eq/kWh, based on a previous LCA (*19*), is used for the production scenario in China.

To facilitate comparison with preceding studies, the convention of 10.7 MJ of primary energy per kWh electricity is used. This represents a worldwide average value for fuel consumption in electricity production (*5*). The primary energy intensity of electricity supplied in Santa Clara is not documented, and thus is taken as the worldwide average. The fuel intensity of electricity in China is higher, with an average value of 12.6 MJ per kWh of electricity, due to an average lower conversion efficiency of power plants as well as higher transmission and distribution losses (*19*).

Semiconductor Manufacturing. In this analysis the primary model for wafer manufacturing is located in Santa Clara, California. A separate scenario for production in China is developed to demonstrate the environmental effects of using China's electricity supply and neglecting perfluorinated compound (PFC) abatement. Although PFC emissions may be abated in some fabs in China, the general trend is that there are no controls on PFC emissions at Chinese production sites. The abatement of some PFC emissions has been regulated by the Kyoto Protocol (in Annex I and II nations) and, in 1999, the World Semiconductor Council (WSC), which includes the semiconductor industry associations of Japan, Europe, Korea, Taiwan, and the United States, committed to PFC emissions reductions of 10% from 1995 or 1999 baseline levels by the end of 2010. However, more than half of semiconductor production occurs outside of Kyoto Protocol Annex I and II nations, and, in 2008, about 20% of semiconductor production capacity was held by China, Singapore, and Malaysia where the semiconductor industry consortia have not joined the WSC. Assuming the realization of China's current development plan with no PFC abatement, by the year 2020 GWP of semiconductor PFC emissions in China will surpass that of all semiconductor production in the rest of the world combined (*20*).

Facility and Process Equipment Energy Demand. Rising energy costs as well as pressure to achieve GHG emission goals have driven fabs to reduce their total energy consumption. U.S. Census data from 1995 to 2005 show that the total electricity consumed by the U.S. semiconductor industry, when normalized per area of silicon it has consumed, has not increased significantly from 1995 to 2005 (*21, 22*). (Normalizing per unit of silicon area rather than by economic value allows energy consumption to be analyzed without the confounding effects of the increasing economic value of products and the off-shoring and outsourcing of fabrication.) This has largely been achieved through energy efficiency improvements to nearly all of the major fab systems: water cooling, exhaust, water flow, clean room airflow, clean dry air (CDA) and facility nitrogen delivery systems, and chamber vacuum pumps. Power requirements for facility systems are determined using facility energy consumption models, which are developed based on data from industry and technical reports (*23, 24*) and accounts for the energy efficiency improvements in industry.

Power and facilities requirements for process tools are from previously published process equipment measurements (*8*) and abatement equipment requirements are based on manufacturers' specifications. The mass flows of GHG emissions are taken from previously published process-specific data (*8*).

Transportation. Chips are typically cut and packaged at a facility separate from the wafer fabrication site, often in a different country or on a separate continent (*25*). Semiconductor products therefore travel twice within the production phase: wafers are transported from the fab to an assembly plant, where they are cut into die, packaged, and tested. Finished chips are then transported to the place of eventual use. Wafers travel 3000 miles by air and 50 miles by truck from front- to back-end manufacturing stages, and the same distance plus another 150 miles by truck to the point of use. Energy consumption and GWP of emissions for truck and air freight from Facanha and Horvath (*26, 27*) are used.

Use Phase. The use phase represents the power consumption of the chip assuming an average power supply efficiency of 70% and a product lifetime of 6000 h (3 years, 8 h per day, 5 days per week, 50 weeks per year) in a 70% active state, consistent with the literature (*28, 29*). The average chip power demand has risen from 14 to about 140 W over the past 15 years. The steady increase in power requirements for logic chips is the main cause of rising energy-related life-cycle impacts, as will be shown in the Results section.

Results

As technology has progressed, life-cycle energy use and GHG emissions for logic have been increasing per wafer and per die but decreasing when normalized by computational power. The increases in per-wafer and per-die life-cycle impacts have one dominant cause: the escalation of use-phase chip power. The growth in per-wafer impacts, however, is also due to the lengthening of the manufacturing process flow and concomitant expansion in manufacturing infrastructure and equipment, as shown in Figure 1. At each technology node, the complexity of device design has increased, and the number of process steps required to produce a finished wafer has risen. In this model, for example, production of a finished wafer of 350 nm logic entails 147 process steps while the process flow for a 45 nm device consists of 251. This lengthening of the process flow follows from increasingly detailed construction necessary to scale down the device's transistors as well as additional interconnect layers to wire them together.

Growth in manufacturing and materials-related impacts over time has been counteracted by shrinking die sizes, which allow more die to fit on each wafer (Figure 2). For all technology generations, the use phase represents the largest proportion of energy-related impacts per die among the life-cycle phases. The dominance of the use phase has also increased over time, with use contributing about 57% of life-cycle GWP per die at the 350 nm node, and 97% at the 45 nm node. Despite the long shipping distances, GWP of transportation is almost insignificant due to the small mass of the product.

GWP of production emissions in China is much higher than that in California due to differences in electricity supply and the lack of PFC abatement in the Chinese fab (Figure 2). At the 45 nm node, GWP of unabated PFC emissions is about equal to the GWP of all fabrication electricity in the California scenario. Unabated PFCs emissions have a GWP 12 times higher than when abated, resulting in the additional emission of almost a quarter million metric tons of CO_2eq annually.

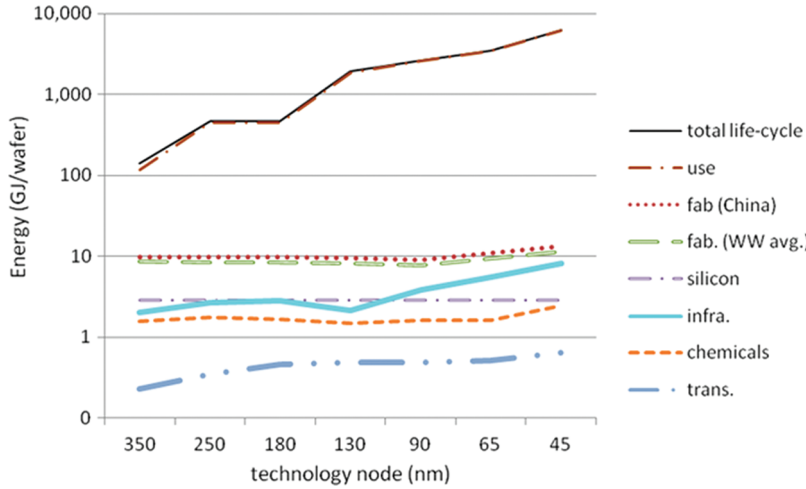

FIGURE 1. Energy use per 300 mm wafer equivalent, by life-cycle stage, over seven technology nodes.

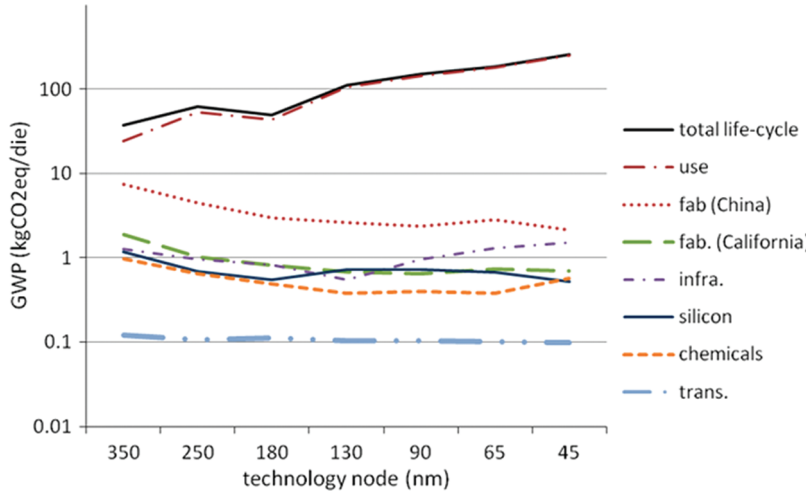

FIGURE 2. GWP per die, by life-cycle stage, over seven technology nodes.

NF_3 is not regulated by the Kyoto Protocol but is among the PFCs used in highest volume in the semiconductor industry (*30, 31*). Although NF_3 is largely broken down into F_2 during processing, a small amount (about 1%) leaves the chamber unreacted. In this model, at the latest technology generation, a fab with a capacity of 10,000 wafer-starts per week and no PFC abatement emits almost 17,000 t of CO_2 equivalent per year of NF_3.

The improvement of several production performance metrics has allowed reductions in the manufacturing energy and GWP per chip. Line yield reflects wasted processing used for process monitoring and wafer loss in the form of damage or breakage. Although wafer damage has remained the same over the years, at about 2%, the number of test or monitor wafers per finished wafer has been reduced over the past decade, resulting in higher average line yields (*32*−*35*), which in this model rise from 63% to 88% over the 15 year period. Although reduced feature sizes have made maintaining wafer yield (the number of good die per wafer) difficult, wafer yields for full scale production have not fallen with decreasing device dimensions. Mature wafer yield is assumed to be 75% for all technology nodes, based on ITRS reports (*36*).

Over the period observed in this study, the computational power of an average CPU grows roughly exponentially, which results in a significant reduction in GWP per computational unit of chip (Figure 3). The question as to whether the appropriate functional unit is a single chip or 1000 MIPS worth of chip is not clear-cut because as the computational capacity per area of finished wafer has increased, the computational demands of computing have also increased.

As web-based applications and thin clients such as cell phones are used more frequently, computational load shifts to data centers on the Internet and away from desktops and laptops. In this arrangement, data center servers can allocate memory and operational demands to reduce the number of active devices such that the functional unit may more appropriately be a metric of computing power than a physical device. However, the additional demands of communication over a network add to the total energy consumption of Internet-based applications. Evaluation of the benefit of network-based, thin-client computing over local desktop computing requires consideration of additional factors concerning the applications and network. These types of questions represent a productive area for further analysis.

Uncertainty Assessment. Best case, worst case, and expected values of results are calculated from lower bound, upper bound, and nominal model parameters. The uncertainty range and data source for each parameter as well as the upper and lower bounds for energy use and GWP of emissions at the 45 nm node are presented in the Supporting Information.

The life-cycle stage with the greatest data uncertainty is chemical production. Of the chemicals included in the model, 30 are represented by process data from textbooks and manuals, 27 are accounted for by using EIO−LCA, and the remaining 53 are assigned a common value based on a

previous study of chemical life-cycle inventory modeling (*37*). (The energy values, uncertainty, and data sources for each chemical are presented in Tables 1−3 in the Supporting Information.) The data for the latter group have an uncertainty range of 75% below and 25% above the nominal value (*37*), which constitutes the largest contribution to uncertainty in the model's chemicals data. The chemicals with the greatest contribution to uncertainty differ for each technology generation, but the top contributors for all nodes include ammonia, CMP slurries and agents, phosphine (PH_3), carbon tetrafluoride (CF_4), hydrogen, and silane (SiH_4). Life-cycle data for ultrahigh-purity forms of these chemicals would have the greatest benefit to uncertainty reduction in future LCA of semiconductors.

Sensitivity Analysis. Given that the parameter values are limited within a finite range, and because the output of the model is monotonic over these values, the sensitivity of the model is evaluated using local methods via differential analysis (*38*). The simple derivative is used to determine the absolute and relative sensitivities of energy consumption and global warming potential to each model parameter (eqs 11 and 12). Energy and GWP impacts have the highest relative sensitivity to wafer yield, line yield, and net die per wafer, followed by tool and facility utilization factors. Although the relative sensitivity of impacts to use-phase power is lower than to other parameters, processor power demand is the variable with the most absolute influence over life-cycle energy in all technology generations. The energy and GWP intensity of chemicals production, which have the largest uncertainty of all model variables, are among the parameters to which impacts results are the least sensitive.

$$S_x^E = \left.\frac{\delta E}{\delta x}\right|_o \tag{11}$$

$$\bar{S}_x^E = \left.\frac{\delta E}{\delta x}\right|_o \frac{E(x_o)}{x_o} \tag{12}$$

Of all production-related parameters, the life-cycle energy per die is most sensitive to the line yield, wafer yield, and gross die per wafer, as shown in eqs 13, 14, and 15. These relations reveal that the lower the original yield, the greater the influence a percentage change in yield improvement has on energy consumption. At the 350 nm node, for example, the line yield is 58% and the wafer yield is 75%, so improvement in line yield would have a greater effect than wafer yield.

$$\frac{\delta(e_{total})}{\delta Y_{line}} = -(Y_{line})^{-2} e_{subtot} \tag{13}$$

$$\frac{\delta(e_{total})}{\delta Y_{wafer}} = -(Y_{wafer})^{-2} e_{subtot} \tag{14}$$

$$\frac{\delta(e_{total})}{\delta n_{die}} = -(n_{die})^{-2} e_{subtot} \tag{15}$$

where

$$e_{subtot} = \left[\sum_{j=1}^{m} e_j^{\$} c_j \sum_{i=1}^{n} m_{ij} + \sum_{k=1}^{q} e_k^m \sum_{i=1}^{n} m_{ij}\right] + \left[\sum_{i=1}^{n} \frac{t_i p_i + \hat{e}_w^v \hat{w}_i t_i}{\varepsilon_i u} + \left(\frac{p_{hvac} + p_{lt} + p_{trt} + p_{cda} + p_{exh}}{c}\right)\right] + \left[\sum_{l=1}^{2} (d_t e_t^d m_l + d_r e_r^d m_l + d_b e_b^d m_l + d_{air} e_{air}^d m_l)\right]$$

The energy used in production alone is also equally sensitive to both the tool utilization (u, the percentage time that the tool is on) and process utilization (ε, the percentage time that the tool is active while on) as to yield (eqs 16 and 17). Although the idle power is lower than active power, any time spent idling results in wasted power. Equivalently, any decrease in tool utilization results in wasted power at the facility level because fans, pumps, and facility systems continue to operate during tool downtime. Because utilization factors affect only the production stage, their influence on life-cycle impacts is weaker than that of the yield parameters.

$$\frac{\delta(e_{total})}{\delta u} = u^{-2}\left(\frac{1}{\varepsilon_i Y_{wafer} Y_{line} n_{die}}\right)\left[\sum_{i=1}^{n} t_i p_i + \hat{e}_w^v \hat{w}_i t_i\right] \tag{16}$$

$$\frac{\delta(e_{total})}{\delta \varepsilon_i} = \varepsilon_i^{-2}\left(\frac{1}{u Y_{wafer} Y_{line} n_{die}}\right)\left[\sum_{i=1}^{n} t_i p_i + \hat{e}_w^v \hat{w}_i t_i\right] \tag{17}$$

The capacity of the facility, i.e., the number of wafers produced per day or week, can also raise or lower the energy consumption (eq 18), but is limited by a number of factors. Production volume is governed by throughput, the number of manufacturing tools in the fab and the design of the production flow, and the quantity of tools can be increased only up to a point before facility systems must be resized,

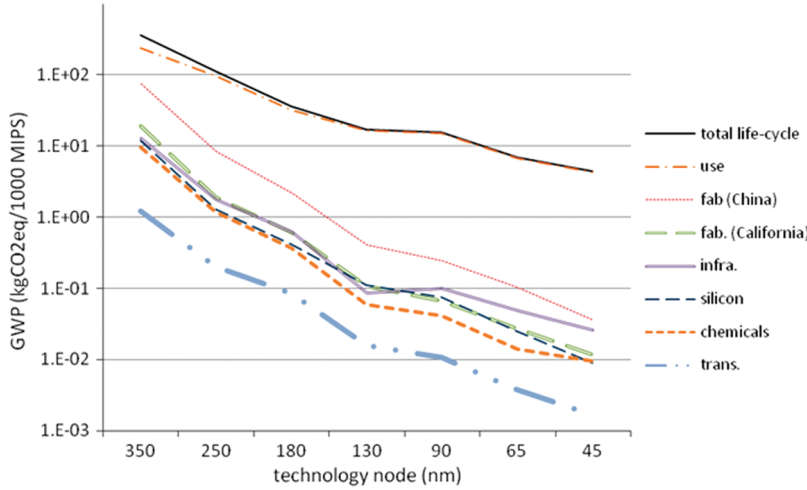

FIGURE 3. GWP per 1000 MIPS of computational power.

or their efficacy suffers. In other words, capacity (c) is limited by the facility power consumption parameters p_{hvac}, p_{lt}, p_{trt}, p_{cda}, and p_{exh} in a relationship that is described outside of this model.

$$\frac{\delta(e_{total})}{\delta c} = \frac{1}{c^2}\frac{1}{Y_{wafer}Y_{line}n_{die}}(p_{hvac} + p_{lt} + p_{trt} + p_{cda} + p_{exh}) \quad (18)$$

Changes in yield, utilization, and capacity have a nonlinear effect on life-cycle energy and global warming emissions, and thus have high relative sensitivity values, while the use-phase power, the global warming intensity of electricity (at the locations of production and use), and the power consumption of facility systems and individual tools all have a direct relationship with varying degrees of influence. The rank of these variables according to their influence over life-cycle energy and GWP emissions differs for each technology node. However, impacts have the highest absolute sensitivity to use-phase power consumption at all technology nodes. (The fraction of life-cycle energy consumption taken by the use phase changes over the generations but remains high, as illustrated in the Results section.) At the 45 nm node, life-cycle energy has the next highest absolute sensitivities to the primary energy intensity of use-phase electricity and the power consumption of wafer fabrication equipment and facility operations.

Life-cycle GWP, like energy, has the highest relative sensitivity to line and wafer yields, and net die per wafer. At the 45 nm node, GWP has the highest absolute sensitivity to the power consumption of the chip in the use phase, followed by the GWP intensity of use-phase electricity, the status of PFC abatement, the GWP of electricity used in wafer manufacturing, and the energy consumption of wafer fabrication (eqs 19−21).

$$\frac{\delta(g_{total})}{\delta g_e^{use}} = e_{use} \quad (19)$$

$$\frac{\delta(g_{total})}{\delta g_x^{d}} = \frac{1}{Y_{wafer}Y_{line}n_{die}}\sum_{i=1}^{2}(d_{i,x}m_i) \quad (20)$$

$$\frac{\delta(g_{total})}{\delta g_e^{prod}} = e_{prod} \quad (21)$$

Discussion

The results of this life-cycle energy analysis enable LCA practitioners to answer important questions concerning the energy-related environmental impacts of computing with greater certainty than ever before. The energy and GWP life-cycle impacts of semiconductor chips presented in this analysis are more complete, accurate, and transparent than those of any previous study, and data are presented for chips spanning many generations, from 1995 to 2010. The quality of data is high: all of the LCA data, with the exception of chemicals and infrastructure data, are specific to the processes, geographical location, and time period of the study (as shown in the Supporting Information). Though life-cycle energy and emissions data for high-purity chemicals would be useful for future semiconductor LCA, the uncertainty in chemicals data is mitigated by the comparatively small contribution of upstream activity to total life-cycle energy and GWP.

The constant increase in logic device power demand over the past 15 years is in part due to unavoidable dynamics which arise from transistor scaling, but while there are technical limitations on the design decisions that determine a chip's power demand, more effort should be made to limit the energy consumption of logic ICs, particularly CPUs for nonmobile computers. The reduction in per-MIPS impacts is an encouraging finding, but if the computational power of the average computer is increasing at roughly the same rate as transistor density, this result is just a red herring.

The importance of more comprehensive policy for semiconductor PFC emissions or the participation by China, Singapore, and Malaysia in the WSC agreement is demonstrated by the GWP impacts of the fab lacking PFC abatement. Although semiconductor NF_3 emissions represent a very small fraction of global GHG emissions, its regulation in future global warming policy should also be considered.

The results of this study highlight the most important practices actors at each life-cycle stage should employ to reduce the energy consumption and GWP of semiconductor logic. Individual or institutional computer users can adjust power settings and employ energy-saving practices such as shutting down computers at night. Computer manufacturers should address use-phase GWP impacts by building products with low power chips, more efficient power supplies, and power-saving modes. IC producers, in turn, should design more energy efficient logic chips, particularly for nonmobile applications which are currently not optimized for energy use. In the production stage, the most critical steps that IC manufacturers can take are (in order of importance): implement PFC abatement, supply the fab with clean power, continue to increase both line and wafer yields, size and operate their facility systems efficiently, and purchase energy-efficient processing equipment. At every technology node evaluated in this study, however, the use stage consumes the most energy and is the largest contributor to life-cycle GWP, and this share has been growing over time. Thus, with regard to energy-related impacts in the life-cycle of semiconductor logic, operational and technological practices which reduce use-phase energy consumption should be the highest priority at this time.

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Note Added after ASAP Publication

Errors in Table 1 and eq 5 were discovered in the version posted ASAP on September 3, 2009. The corrected version was posted on September 29, 2009.

Supporting Information Available

Section A: Methodological Details, Data Sources and Parameter Uncertainty; Section B: Supplemental Results; Section C: Data Quality. This information is available free of charge via the Internet at http://pubs.acs.org.

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