High-Performance CdSe:In Nanowire Field-Effect Transistors Based on Top-Gate Configuration with High-κ Non-Oxide Dielectrics

ARTICLE *in* THE JOURNAL OF PHYSICAL CHEMISTRY C · FEBRUARY 2010

Impact Factor: 4.77 · DOI: 10.1021/jp1007895

High-Performance CdSe:In Nanowire Field-Effect Transistors Based on Top-Gate Configuration with High-κ Non-Oxide Dielectrics

Zhubing He,[†] Wenjun Zhang,*[,†] Wenfeng Zhang,[†] Jiansheng Jie,[†,‡] Linbao Luo,[†] Guodong Yuan,[†] Jianxiong Wang,[†] C. M. L. Wu,[†] Igor Bello,[†] Chun-Sing Lee,[†] and Shuit-Tong Lee*[,†]

Center Of Super-Diamond and Advanced Films (COSDAF), Department of Physics and Materials Science, City University of Hong Kong, Hong Kong SAR, China, and School of Science, Hefei University of Technology, Hefei 230009, Anhui, China

Received: January 27, 2010

A dual-gate field-effect transistor (FET) based on the same single indium-doped CdSe nanowire using Si_3N_4 and SiO_2 as top- and back-gate dielectrics, respectively, was fabricated. This dual-gate FET enabled direct comparison of the device performance of FETs in both top- and back-gate configurations. Remarkably, the field-effect mobility, peak transconductance, and I_{on}/I_{off} ratio of the Si_3N_4 top-gate FET were 52, 142, and 2.81×10^5 times larger than the respective values of the SiO_2 back-gate FET. Meanwhile, the threshold voltage and the subthreshold swing of the top-gate FET decreased to -1.7 V and 508 mV/decade, respectively, which are better than the best values ever obtained in FETs based on II−VI semiconductor nanomaterials including CdSe nanowires. The roles of device configurations and gate materials in the FET characteristics and the evaluation of electronic and transport properties of nanostructures based on that were discussed. Two kinds of basic logic circuits, "AND" and "OR", were constructed with the top-gate transistors, which could also utilize light-input to realize a phototransistor action to take advantage of its photoresponse properties.

Introduction

As a basic functional component in integrated circuits, displays, and memory devices, field-effect transistors (FETs) play a core role in current electronic industry. In parallel with the large progress in nanomaterials research, much attention has recently focused on the realization of nano-FETs based on one-dimensional (1D) nanostructures, such as carbon nanotubes (CNTs),[1–3] semiconductor nanowires (NWs) and nanoribbons (NRs),[4–10] and organic NWs.[11] They are regarded as a promising candidate for scaling down CMOS devices.[12] NWs with high crystallinity, smooth surfaces, and controlled diameters can now be prepared in high-yield,[13] allowing continual improvement of the integrity of nanowire-based electronics, which may relieve the technological and physical limitation for conventional silicon electronics.[14] Indeed, nano-FETs based on silicon NWs (SiNWs) and CNTs have demonstrated distinctive performances over state-of-the-art silicon MOSFETs.[15,16] Moreover, it has now become a common and standard practice to characterize the electronic and transport properties of nanowires based on the characteristics of the FET fabricated from a single nanowire.

In contrast to the exciting progress in CNT- and SiNW-based FETs, those based on II−VI semiconductor nanostructures typically show poor device characteristics, such as small field-effect mobility, low on-current, and large threshold voltage, relative to their film counterparts. Two factors are considered responsible for the poor performance of II−VI nanostructure FETs: (i) undoped II−VI materials such as CdSe, CdS, and ZnS are highly insulating and have difficulty forming ohmic contacts, leading to FETs with small on-current and low field-effect mobility. (ii) Most nano-FETs are constructed in a simple back-gate configuration with SiO_2 as the dielectric layer, which is usually inefficient in controlling the conduction channel by gate voltage, thus yielding nonoptimal device performance. Herein, to elucidate the effects of the above two factors, we select indium-doped cadmium selenide (CdSe:In) NWs as a paradigm to fabricate n-channel II−VI NW FETs. To minimize material fluctuation, FETs in both top-gate and back-gate configurations were respectively constructed from the same single NW, and characterized, so that the effects of device design on device properties can be delineated immune from materials dependence.

CdSe is an important II−VI direct band gap (1.74 eV) semiconductor with attractive electronic,[17–20] spintronics,[21] and optoelectronic properties.[22,23] It has promising application potentials for biosensing/bioimaging,[24,25] light-emitting diode,[26] and photodetector.[27,28] Nanodevices based on CdSe nanostructures have attracted much interest;[29,30] however, lack of control in electrical properties has hindered their practical applications. Recently, we have achieved controlled n-type conduction in CdSe NWs via in situ or postgrowth doping and obtained reliable ohmic contacts between the doped NWs and indium electrodes.[31] In this work, we report that, by using high-k Si_3N_4 gate dielectric and top-gate device geometry, the performance of CdSe:In NW-based FETs can be drastically improved. Taking advantage of the excellent and stable performance of top-gate transistors, we successfully realized two kinds of basic logic circuits, "AND" and "OR", and further combined them with the inherent photoresponse properties of CdSe:In NWs. We expect a similar method can be applicable to other II−VI nanostructures, which may find applications in new-generation nanoelectronics and nano-optoelectronics.

* To whom correspondence should be addressed. E-mail: apwjzh@cityu.edu.hk (W.Z.); apannale@cityu.edu.hk (S.-T.L.).
[†] City University of Hong Kong.
[‡] Hefei University of Technology.

10.1021/jp1007895
Published on Web 02/22/2010

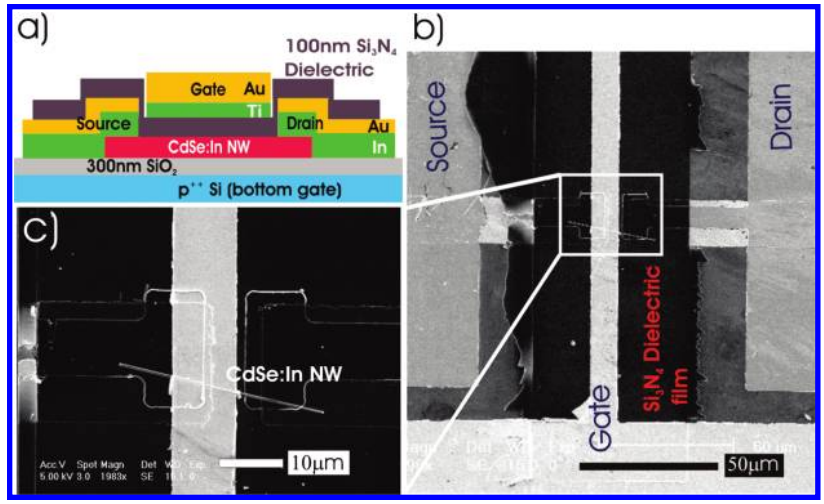

Figure 1. (a) Configuration of a single CdSe:In NW-based top-gate MOSFET with Si_3N_4 as gate dielectric film. (b,c) Low- and high-magnification SEM images of the typical top-gate FET with Si_3N_4 as gate dielectric film.

Experimental Methods

Synthesis. Single-crystal CdSe:In NWs with a carrier concentration up to 10^{19} cm^{-3} were synthesized by evaporating indium doping source at 700 °C in a chemical vapor deposition process. The experimental details have been described previously.[31]

Device Construction and Measurements. Briefly, to fabricate nano-FETs from single CdSe:In NWs, the as-synthesized NWs were first dispersed in ethanol, and then spread on a SiO_2 (300 nm)/p^+-Si substrate at a desired density. The source and drain electrodes (In 180 nm/Au 20 nm) were patterned on NWs by a photolithography process. A Si_3N_4 film (100 nm), which served as the gate dielectric, was grown by RF sputtering at room temperature on the NW and source/drain electrodes. Finally, the top-gate electrode (Ti 20 nm/Au 60 nm) was deposited on the Si_3N_4 layer via photolithography. Electrical measurements were accomplished by using a Keithley 4200 semiconductor characteristics measurement system at room temperature.

Results and Discussion

Figure 1 shows the schematic cross-section structure of the CdSe:In NW FET (Figure 1a) and the SEM images for a typical device fabricated from a single NW (Figure 1b and c). The diameter of the NW is about 100 nm. Figure 1a shows that two nano-FETs in either top-gate or back-gate configurations are fabricated from the same NW. In the conventional back-gate configuration, the degenerately doped-Si substrate serves as the back-gate, and the 300 nm thick SiO_2 layer acts as the gate dielectric. In the top-gate configuration, the 100 nm thick Si_3N_4 layer is the gate insulator, and the NW channel is modulated by the localized Ti/Au gate electrode. This unique device structure enables us to study the effects of device configuration on device performance, thus avoiding the inevitable fluctuation of the electrical properties from NW to NW.

Figure 2 depicts the electrical characteristics of the NW FET in the back-gate configuration. From the $I_{ds}-V_{ds}$ curves taken for different V_{gs} ranging from −50 to 40 V (Figure 2a), we find that V_{gs} shows poor control of I_{ds}, although the linear curves reveal ohmic contact between the electrodes and the NW. The n-type conductivity of the CdSe:In NW can be confirmed from the transport characteristics of the FET in Figure 2b, in which I_{ds} monotonously increases with increasing V_{gs}. A small I_{on}/I_{off} ratio of ∼1.02 and transconductance (g_m) of ∼5 nS at $V_{ds} = 1$ V are deduced from Figure 2b. We noted that the device could not be depleted even at a large negative V_{gs} of −50 V. Field-effect electron mobility (μ_{eff}) is estimated according to the equation: $\mu_{eff} = g_m L^2/CV_{ds}$, where L is the channel length and C is the channel capacitance. Assuming a cylinder on an infinite plate model of the NW FET, the channel capacitance is then given by $C = 2\pi\varepsilon_0\varepsilon_r L/\ln(4h/d)$, where ε_0 is the dielectric constant of vacuum, ε_r is the relative dielectric constant of gate insulator material, h is the gate insulator film thickness, and d is the NW diameter. On the basis of the above equations, C and μ_{eff} are estimated to be 0.57 fF and 3.18 $cm^2/(V\cdot s)$, respectively. The μ_{eff} value is far smaller than the mobility reported for single-crystal CdSe (∼800 $cm^2/(V\cdot s)$).[32] Moreover, the electron

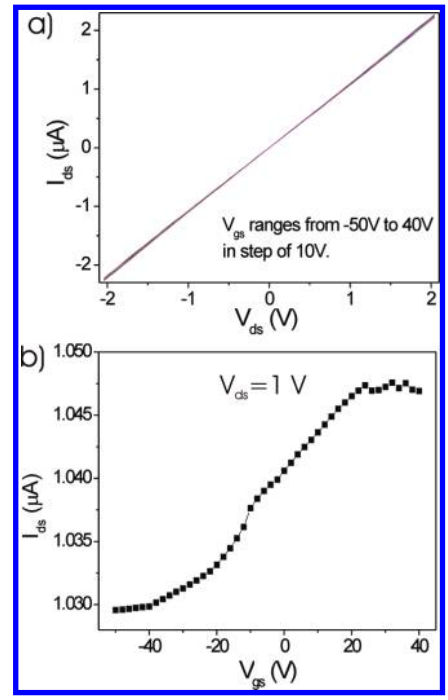

Figure 2. (a) $I_{ds}-V_{ds}$ curve of a single CdSe:In NW back-gate MOSFET (shown in Figure 1) using 300 nm thermally oxidized SiO_2 film as gate dielectric, with gate voltages ranging from −50 to 40 V in steps of 10 V. (b) $I_{ds}-V_{gs}$ curve characteristics of the back-gate FET at $V_{ds} = 1$ V.

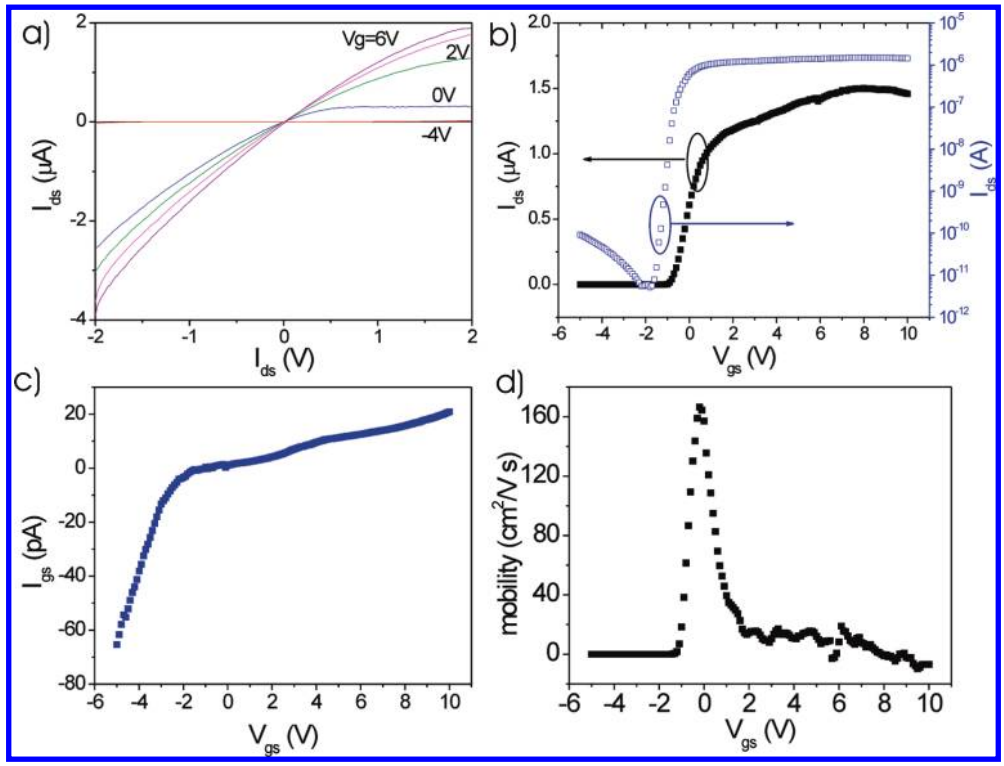

Figure 3. (a) $I_{ds}-V_{ds}$ curve of the same single CdSe:In NW-based top-gate FET (shown in Figure 1) using sputtered 100 nm Si_3N_4 film as gate dielectric, with gate voltage ranging from −4 to 6 V in steps of 2 V. (b) $I_{ds}-V_{gs}$ curve characteristics of the top-gate FET at $V_{ds} = 1$ V. The "■" and blue "□" correspond to linear scale and log scale $I_{ds}-V_{ds}$ curves, respectively. (c,d) The leakage current between gate electrode and NW channel, and the characteristic of $\mu_{eff}-V_{gs}$ of the top-gate FET, respectively.

concentration n can be deduced to be 5.0×10^{18} cm^{-3} by using $n = \sigma/e\mu_{eff}$, where σ is the conductivity of the NW measured at $V_{gs} = 0$ V.

As compared to the back-gate NW FET, the top-gate FET exhibits much better performance, as shown in Figure 3. For the latter FET, $I_{ds}-V_{ds}$ curves strongly depend on the V_{gs} applied on the top-gate, and the device can be modulated from depletion to accumulation states by a much smaller V_{gs} ranging from −4 to 6 V. Significantly, a large I_{on}/I_{off} ratio of 2.87×10^5 can be deduced from the $\lg(I_{ds})-V_g$ curve in Figure 3b. The transconductance g_m has a peak value of 0.71 μS at $V_{ds} = 1$ V, and a small threshold voltage (V_{th}) of only −1.7 V is required to fully deplete the device according to the logarithmic curve. It is noticed that the Si_3N_4 gate dielectric shows good insulating characteristic; the leakage current (I_{gs}) is lower than 70 pA in the V_{gs} range from −5 to 10 V (Figure 3c). The leakage current has little influence on the on-current (I_{on}), but dominates the off-current (I_{off}) when $V_{gs} < -2$ V, which induces an obvious increase of I_{ds} in the negative V_{gs} direction from −2 to −5 V (logarithmic curve in Figure 3b). It is expected that the leakage current can be further reduced by optimizing the deposition of Si_3N_4 dielectric film during the sputtering process.

It has been shown that the couple of gate with the NW is profoundly affected by the gate oxide and device geometry.[33] For the top-gate NWFET, the aforementioned formula for channel capacitance should be corrected to $C = 2\pi\varepsilon_0\varepsilon_r L/\ln(1 + 2h/d)$, and C is 1.87 fF for the device with a 100 nm thick Si_3N_4 gate dielectric. Accordingly, μ_{eff} is estimated and the μ_{eff} versus V_g curve is plotted in Figure 3d. It is noted that the $\mu_{eff}-V_{gs}$ dependence follows the same trend as that observed in conventional MOSFET.[34−37] μ_{eff} has a peak value near zero gate voltage and decreases at both positive and negative gate voltage directions. According to previous analysis,[34] μ_{eff} starts to increase only as V_{gs} approaches the flat band voltage (V_{fb}), which is typically less than 0 V due to the presence of positively charged donor-type surface states. The enhanced surface roughness scattering at higher V_{gs} regime leads to a decrease of μ_{eff}, while Coulomb scattering due to fixed interface state charges and ionized impurity charges is responsible for the reduction of μ_{eff} at negative V_{gs}.[35,36] In addition, the $\mu_{eff}-V_g$ dependence is asymmetric with a fast roll-off at voltage close to the threshold voltage. This feature is also in accordance with the observations in GaAs thin film MOSFET,[37] indicating the good subthreshold characteristics of the top-gate CdSe:In NWFET. From Figure 3d, the peak mobility reaches 166 $cm^2/(V\cdot s)$ at $V_{ds} = 1$ V and $V_{gs} = -0.1$ V, which is the highest value reported thus far for CdSe nanomaterials[27,28] and films,[38,39] although it is still smaller than that reported for single-crystal CdSe[32] and Si NWFET devices (350 $cm^2/(V\cdot s)$).[40] Accordingly, the electron concentration deduced from the top-gate structure is 9.5×10^{16} cm^{-3}, which is 2 orders of magnitude lower than that calculated from the SiO_2 back -gate structure. As compared to the planar SiO_2 back-gate FET fabricated from the same NW, the critical device parameters including the field-effect mobility, peak transconductance, and I_{on}/I_{off} ratio of the top-gate NWFET are remarkably enhanced by 52, 142, and 2.81×10^5 times, respectively.

Because of the limitation of the nanostructure dimensions, the electronic and transport properties of nanostructures are usually studied by characterizing single-object FETs. Most nano-FETs are constructed in a simple back-gate configuration with SiO_2 as the dielectric layer. However, as we demonstrated in this work, the gate voltage is less efficient in manipulating the source−drain current in such a configuration. As a result, the "real" overall electronic and transport properties of the nanostructures studied cannot be revealed exactly and may lead to incorrect evaluation of nanomaterials properties. For example, the electron mobility of the same NW deduced from the FET in top-gate configuration (1.66×10^2 $cm^2/(V\cdot s)$) is 2 orders of

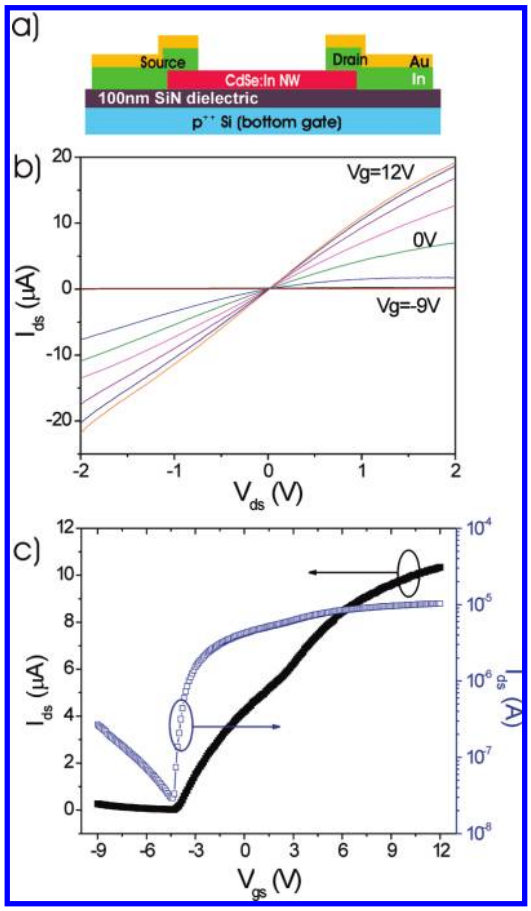

Figure 4. (a) Configuration of a single CdSe:In NW-based back-gate FET using 100 nm sputtered Si_3N_4 film as gate dielectric. (b) $I_{ds}-V_{ds}$ curve of the FET with gate voltages ranging from −9 to 12 V in steps of 3 V. (b) The $I_{ds}-V_{gs}$ curve characteristics of the FET at $V_{ds} = 1$ V. The "■" and blue "□" correspond to linear scale and log scale $I_{ds}-V_{ds}$ curves, respectively.

magnitude larger than that from SiO_2 back-gate configuration (3.18 $cm^2/(V\cdot s)$). Correspondingly, the electron concentration calculated from the two device configurations based on the same single NW also differs by 2 orders of magnitude. The electron mobility obtained from top-gate configuration is closer to that reported for CdSe single crystals, and thus is believed to be more reliable, reflecting the high-quality single-crystal nature of the CdSe:In NWs.[31] This work demonstrates that a proper protocol of single-wire FETs is needed for accurate evaluation of the intrinsic characteristics of the nanowires. Moreover, FETs in a single-nanowire top-gate configuration are technically easier to construct than that in a back-gate configuration as building blocks for integration into large-scale computing circuits.

It is known that both the gate dielectric materials and the device geometry may contribute to FET performance enhancement. To differentiate between the two contributions, planar back-gate FETs based on single CdSe:In NWs were also fabricated using 100 nm thick Si_3N_4 film as the gate insulator. The Si_3N_4 layer was deposited on a p^{++} silicon wafer (0.05−0.1 Ω cm) under the same conditions for making the top-gate FET. The detailed device structure is illustrated in Figure 4a. Notably, in contrast to the SiO_2 back-gate NWFET, the gate voltage in Si_3N_4 back-gate NWFET has a distinct effect on the source−drain current in the voltage range from −9 to 12 V, as revealed by the V_g-dependent $I_{ds}-V_{ds}$ curves in Figure 4b. From the transport characteristics in Figure 4c, the peak transconductance, I_{on}/I_{off} ratio, and threshold voltage are deduced to be about 1.1 μS, 3.15 × 10^3, and −4.4 V, respectively, at $V_{ds} = 1$ V. The transconductance value is higher than that in the top-gate FET, which mainly arises from the shorter channel length in the back-gate FET (2 μm vs 6 μm). The channel capacitance and field-effect mobility were calculated to be 0.49 fF and 90.5 $cm^2/(V\cdot s)$, respectively. Although the mobility is much higher than that obtained from the SiO_2 back-gate FET, it is only about one-half of that for the top-gate NWFET. Moreover, the current leakage increased by nearly 3 orders of magnitude as compared to the top-gate NWFET, and led to a snub-nosed tail of the $\lg(I_{ds})-V_{gs}$ curve in the region from −9 to −4 V in Figure 4c. In the top-gate FET, the localized gate electrode mainly overlaps with the NW channel. Therefore, the leakage current is reduced due to the small diameter of NWs. In contrast, the gate overlaps with NW channel and the large source and drain electrode pads in the back-gate FET; consequently, the defects in the sputtered Si_3N_4 film, such as pinholes and voids, provide many more possibilities for current penetration through the dielectric film under the gate, leading to a larger leakage current. On the other hand, based on the electrostatic potential simulation,[21] the electrostatic potential distribution around the NW channel in the top-gate geometry is more uniform than that in the planar back-gate geometry, which also contributes to improvement in device performance. Our results demonstrate that both the high-k dielectric material and the proper device architecture are essential in realizing high-performance NWFETs.

TABLE 1: Device Characteristics of CdSe:In FETs in Different Configurations

	SiO_2 back-gate	Si_3N_4 back-gate	Si_3N_4 top-gate
I_{on}/I_{off} ratio	1.02	3.15 × 10^3	2.87 × 10^5
transconductance, g_m /μS	5 × 10^{-3}	1.1	0.71
threshold voltage, V_T/V	−40	−4.4	−1.7
capacitance, C/fF	5.66	4.86	18.7
mobility, $\mu_{eff}/(cm^2/V\cdot s)$	3.18	90.5	1.66 × 10^2
subthres. swing, S/(mV/decade)	1.77 × 10^6	1.13 × 10^3	5.08 × 10^2

Besides the parameters illustrated above, another important parameter evaluating the performance of MOSFET is the subthreshold swing (S), which is crucial to transistor miniaturization. A small S is desired for low threshold voltage and low power operation of FETs scaled down to small sizes.[41] For MOSFET,[42] S is determined by $S = \ln(10)[dV_{gs}/d(\ln I_{ds})]$. Accordingly, the subthreshold swing values of SiO_2 back-gate, Si_3N_4 back-gate, and Si_3N_4 top-gate FETs are 1.77 × 10^6, 1.13 × 10^3, and 5.08 × 10^2 mV/dec, respectively. The reduction of S is very significant via varying gate geometry and materials. The S value (508 mV/dec) of Si_3N_4 top-gate FET is only 1 order of magnitude higher than the theoretical limit of $S = (k_BT/e)\ln(10) \approx$ ~60 mV/dec at room temperature, where T is temperature, k_B is Boltzmann's constant, and e is the elementary charge. For comparison, the key performance parameters for the CdSe:In NW based FETs with different gate geometry and gate materials are summarized in Table 1.

We have also studied device performances under white light illumination. Because of the high sensitivity of CdSe to visible light, illumination using an incandescent light source increased the threshold voltage of a top-gate transistor from −1.8 to −3.7 V, as shown in Figure 5a. Under illumination, more excitons are generated, and therefore the carriers in the channel are depleted at a higher negative gate voltage. The $I_{ds}-V_{gs}$ curves measured in dark revealed slight hysteresis at a sweeping rate of 6 V/s, which, however, became negligible under illumination. Figure 5b shows the $V_{out}-V_{in}$ (V_g) dependencies for two different top-gate FETs connected in the circuit as depicted in the inset

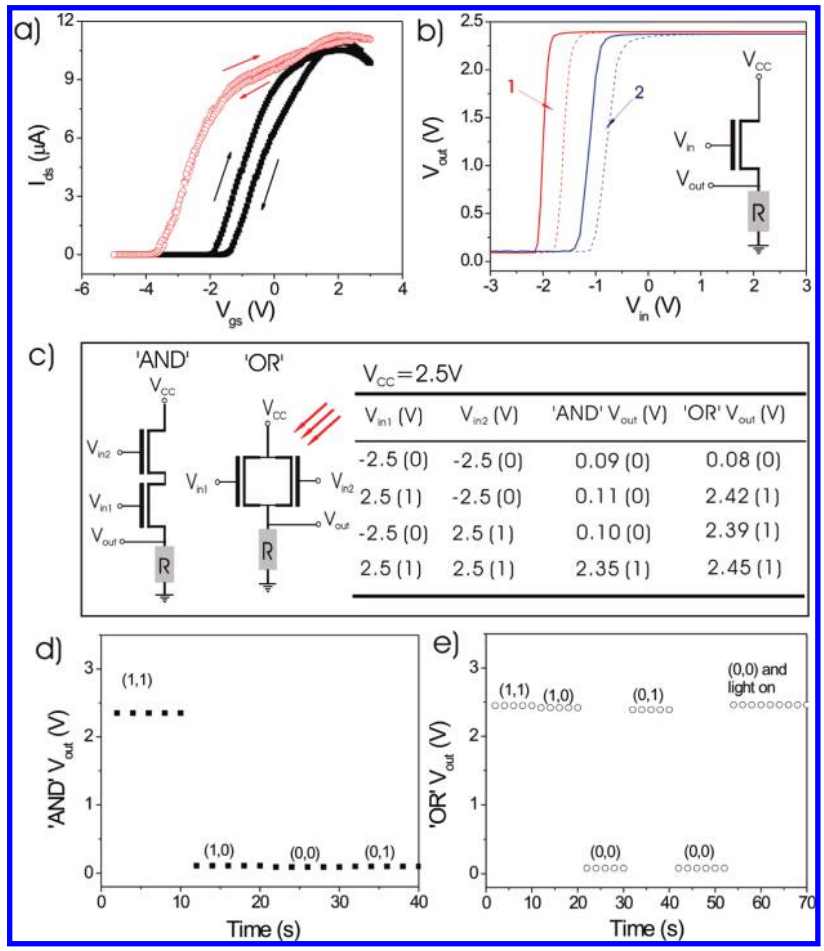

Figure 5. (a) Hysteresis loops of $I_{ds}-V_{gs}$ curves of a top-gate transistor, measured in dark (■) and under illumination (red ○), respectively. V_{gs} sweeps from −5 to 3 V and back to −5 V at a sweep rate of 6 V/s. (b) $V_{out}-V_{in}$ dependencies for two different top-gate FETs connected in the circuit as depicted in the inset. R is a constant resistor of 100 MΩ. The measurements were conducted at a constant V_{cc} = 2.5 V. V_{in} sweeps from −3 to 3 V and back to −3 V at sweeping rates of 6 and −6 V/s, respectively. The solid line is forward and the dashed line is backward for each transistor. (c) The schematic configuration of the typical "AND" and "OR" circuits design based on two transistors. The inset table summarizes the experimental results for the two logic gates. (d) A typical switch response from the "AND" circuit. (e) A typical switch response from the "OR" circuit, where the final change shows the light-induced switch on when the two inputs are set as logic 0.

in Figure 5b. The two FETs are denoted as transistors 1 and 2, respectively. R is a constant resistor of 100 MΩ. The measurements were conducted at a constant V_{cc} = 2.5 V, and the sweeping rate of V_{in} was 6 V/s. For both transistors, V_{out} showed sharp responses to V_{in}, and the performance gain (defined as dV_{out}/dV_{in} in the inflection regions of the $V_{out}-V_{in}$ curves) is nearly six at a sweeping rate of 6 V/s, which is similar to that reported for NOR gates based on p-Si NWs.[43] Although the turn-on voltages for the transistors are different, both transistors can be considered in "ON" states (logic 1) at V_{in} = 2.5, and in the "OFF" state (logic 0) at V_{in} = −2.5 V, where $V_{out} > 2$ V is defined as "ON" and $V_{out} < 0.5$ V as "OFF" state, respectively. Note that the hysteresis broadening does not affect the switching performance. Two top-gate transistors were connected in series and in parallel to construct two basic logic circuits, "AND" and "OR", respectively, as shown in Figure 5c. As summarized in the table in Figure 5c, logic "AND" and "OR" circuits with great performance gain and stability were successfully realized. Figure 5d and e reveals the reasonable operation speeds and high reproducibility of both "AND" and "OR" circuits in the time scale. In addition, by combining the photoelctronic response characteristics of CdSe NW transistors (Figure 5a), comprehensive photosensitive switches were demonstrated. When light turns on as denoted by the three red arrows (Figure 5c), the state of the "OR" logic gate switches to the "ON" state with a V_{out} value of 2.46 V, when the two input signals are both set as logic 0. It functionalizes as common logic gates, taking advantage of the photoconductivity of CdSe NWs.

Conclusions

In summary, device configuration and gate dielectric materials have been shown to have dominant influences on the performance of FETs based on single indium-doped CdSe NWs. Top- and back-gate FETs were constructed from the same CdSe:In NW so as to eliminate material-dependent fluctuation of electrical properties of NWs. Remarkably, the field-effect mobility, peak transconductance, and I_{on}/I_{off} ratio of the top-gate FETs using Si_3N_4 as gate material are 52, 142, and 2.81 × 10^5 times larger than the respective values of the back-gate FETs using SiO_2 as gate material. Because of the limitation of the nanostructure dimensions, the electronic and transport properties of nanostructures were usually studied by characterizing single-object FETs. This work demonstrates that a proper protocol of FETs is needed for more accurate evaluation of the intrinsic characteristics of nanomaterials. Meanwhile, the threshold voltage decreased from −40 to −1.7 V, and the subthreshold swing dropped sharply from 1.77 × 10^6 to 5.08 × 10^2 mV/decade, indicating great improvement in reduction of power consumption via device miniaturization. Moreover, the top-gate

transistors showed only slight hysteresis. On the basis of the excellent and stable performance of top-gate transistors, two kinds of basic logic circuits, "AND" and "OR", were successfully realized, which are capable of incorporating the inherent photoresponse properties of CdSe NWs. Device configuration and choice of gate dielectric materials are shown to be crucial in dictating nanoelectronic and nano-optoelectronic device performance.

Acknowledgment. This work was supported by the Strategic Research Grant of the City University of Hong Kong (Project No. 7002290) and Research Grants Council of Hong Kong SAR (No. CityU5/CRF/08). The Program for New Century Excellent Talents in University of the Chinese Ministry of Education (NCET-08-0764) and National High Technology R&D Program of China (863 Program) (No. 2007AA03Z301) are also acknowledged.

References and Notes

(1) Javey, A.; Kim, H.; Brink, M.; Wang, Q.; Ural, A.; Guo, J.; McIntyre, P.; McEuen, P.; Lundstrom, M.; Dai, H. *Nat. Mater.* **2002**, *1*, 241.

(2) Wind, S. J.; Appenzeller, J.; Martel, R.; Derycke, V.; Avouris, P. *Appl. Phys. Lett.* **2002**, *80*, 3817.

(3) Yang, M. H.; Teo, K. B. K.; Gangloff, L.; Milne, W. I.; Hasko, D. G.; Robert, Y.; Legagneux, P. *Appl. Phys. Lett.* **2006**, *88*, 113507.

(4) Nguyen, P.; Ng, H. T.; Yamada, T.; Smith, M. K.; Li, J.; Han, J.; Meyyappan, M. *Nano Lett.* **2004**, *4*, 651.

(5) Kim, B.-K.; Kim, J.-J.; Lee, J.-O.; Kong, K.-j.; Seo, H. J.; Lee, C. J. *Phys. Rev. B* **2005**, *71*, 153313.

(6) Koo, S.-M.; Li, Q.; Edelstein, M. D.; Richter, C. A.; Vogel, E. M. *Nano Lett.* **2005**, *5*, 2519.

(7) Keem, K.; Jeong, D.-Y.; Kim, S.; Lee, M.-S.; Yeo, I.-S.; Chung, U. I.; Moon, J.-T. *Nano Lett.* **2006**, *6*, 1454.

(8) Tu, R.; Zhang, L.; Nishi, Y.; Dai, H. *Nano Lett.* **2007**, *7*, 1561.

(9) Dayeh, S. A.; Susac, D.; Kavanagh, K. L.; Yu, E. T.; Wang, D. *Nano Lett.* **2008**, *8*, 3114.

(10) Horng-Chih, L.; Hsing-Hui, H.; Chun-Jung, S.; Tiao-Yuan, H. *IEEE Electron Device Lett.* **2008**, *29*, 718.

(11) Briseno, A. L.; Mannsfeld, S. C. B.; Jenekhe, S. A.; Bao, Z.; Xia, Y. *Mater. Today* **2008**, *11*, 38.

(12) Organization, I. , 2007.

(13) Wu, Y.; Cui, Y.; Huynh, L.; Barrelet, C. J.; Bell, D. C.; Lieber, C. M. *Nano Lett.* **2004**, *4*, 433.

(14) Wei, L.; Ping, X.; Lieber, C. M. *IEEE Trans. Electron Devices* **2008**, *55*, 2859.

(15) Cui, Y.; Zhong, Z.; Wang, D.; Wang, W. U.; Lieber, C. M. *Nano Lett.* **2003**, *3*, 149.

(16) Xiang, J.; Lu, W.; Hu, Y.; Wu, Y.; Yan, H.; Lieber, C. M. *Nature* **2006**, *441*, 489.

(17) Klein, D. L.; Roth, R.; Lim, A. K. L.; Alivisatos, A. P.; McEuen, P. L. *Nature* **1997**, *389*, 699.

(18) Tans, S. J.; Devoret, M. H.; Dai, H. J.; Thess, A.; Smalley, R. E.; Geerligs, L. J.; Dekker, C. *Nature* **1997**, *386*, 474.

(19) Wang, C. J.; Shim, M.; Guyot-Sionnest, P. *Science* **2001**, *291*, 2390.

(20) Woo, W. K.; Shimizu, K. T.; Jarosz, M. V.; Neuhauser, R. G.; Leatherdale, C. A.; Rubner, M. A.; Bawendi, M. G. *Adv. Mater.* **2002**, *14*, 1068.

(21) Ouyang, M.; Awschalom, D. D. *Science* **2003**, *301*, 1074.

(22) Hodes, G.; Albu-Yaron, A.; Decker, F.; Motisuke, P. *Phys. Rev. B* **1987**, *36*, 4215.

(23) Ichimura, M.; Sato, N.; Nakamura, A.; Takeuchi, K.; Arai, E. *Phys. Status Solidi A* **2002**, *193*, 132.

(24) Alivisatos, P. *Nat. Biotechnol.* **2004**, *22*, 47.

(25) Michalet, X.; Pinaud, F. F.; Bentolila, L. A.; Tsay, J. M.; Doose, S.; Li, J. J.; Sundaresan, G.; Wu, A. M.; Gambhir, S. S.; Weiss, S. *Science* **2005**, *307*, 538.

(26) Colvin, V. L.; Schlamp, M. C.; Alivisatos, A. P. *Nature* **1994**, *370*, 354.

(27) Jie, J. S.; Zhang, W. J.; Jiang, Y.; Lee, S. T. *Appl. Phys. Lett.* **2006**, *89*, 133118.

(28) Jiang, Y.; Zhang, W. J.; Jie, J. S.; Meng, X. M.; Fan, X.; Lee, S. T. *Adv. Funct. Mater.* **2007**, *17*, 1795.

(29) Robel, I.; Bunker, B. A.; Kamat, P. V.; Kuno, M. *Nano Lett.* **2006**, *6*, 1344.

(30) Zhang, Y.; Tang, Y.; Lee, K.; Ouyang, M. *Nano Lett.* **2008**, *9*, 437.

(31) He, Z. B.; Jie, J. S.; Zhang, W. J.; Zhang, W. F.; Luo, L. B.; Fan, X.; Yuan, G. D.; Bello, I.; Lee, S. T. *Small* **2009**, *5*, 345.

(32) Rode, D. L. *Phys. Rev. B* **1970**, *2*, 4036.

(33) Khanal, D. R.; Wu, J. *Nano Lett.* **2007**, *7*, 2778.

(34) Wieder, H. H. *Appl. Phys. Lett.* **1974**, *25*, 206.

(35) Brews, J. R. *J. Appl. Phys.* **1975**, *46*, 2193.

(36) Sun, S. C.; Plummer, J. D. *IEEE Trans. Electron Devices* **1980**, *27*, 1497.

(37) Moon, B.; Lee, S.; Shur, M.; Morkoc, H.; Gopinath, A. *IEEE Trans. Electron Devices* **1993**, *40*, 1711.

(38) Lee, M. J.; Judge, C. P.; Wright, S. W. *Solid-State Electron.* **2000**, *44*, 1431.

(39) Gan, F. Y.; Shih, I. *IEEE Trans. Electron Devices* **2002**, *49*, 15.

(40) Gunawan, O.; Sekaric, L.; Majumdar, A.; Rooks, M.; Appenzeller, J.; Sleight, J. W.; Guha, S.; Haensch, W. *Nano Lett.* **2008**, *8*, 1566.

(41) Muller, R. S.; Kamins, T. I. *Device Electronics for Integrated Circuits*; Wiley: New York, 1986.

(42) Sze, S. M. *Physics of Semiconductor Devices*; Wiley: New York, 1981.

(43) Huang, Y.; Duan, X. F.; Cui, Y.; Lauhon, L. J.; Kim, K. H.; Lieber, C. M. *Science* **2001**, *294*, 1313.

JP1007895