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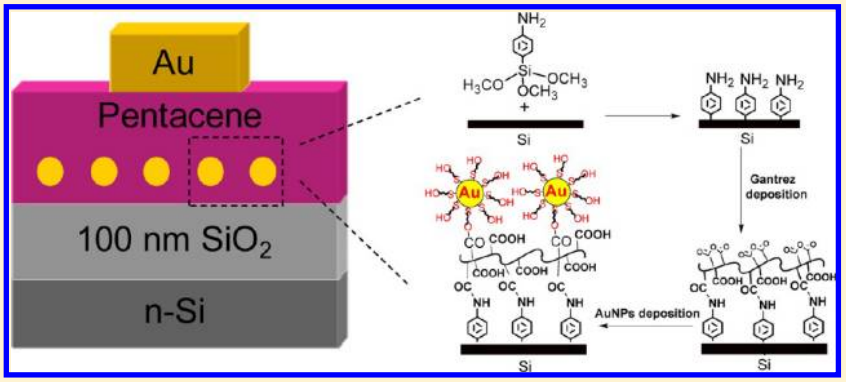
Covalent Assembly of Gold Nanoparticles: An Application toward Transistor Memory

Raju Kumar Gupta,[†] Gao Ying,[‡] M. P. Srinivasan,[§] and Pooi See Lee*[,†]

[†]School of Materials Science and Engineering, Nanyang Technological University, 50 Nanyang Avenue, Singapore 639798

[‡]Energy Research Institute @ NTU (ERI@N), Nanyang Technological University, Singapore 637553

[§]Department of Chemical and Biomolecular Engineering, National University of Singapore, 4 Engineering Drive 4, Singapore 117576



ABSTRACT: This work reports a versatile approach utilizing covalent assembly of functionalized gold nanoparticles for organic field-effect transistor (OFET) based memory devices. 11-Mercapto-1-undecanol functionalized gold nanoparticles (AuNPs) having size of 5 ± 0.5 nm were synthesized and immobilized onto SiO_2 substrate through covalent binding using a functionalized polymer as a surface modifier. The pentacene OFET-based memory devices utilizing such covalently bound gold nanoparticles with nanoparticle density of 5×10^{11} cm^{-2} exhibited a large memory window (7.7 V), high on/off ratio between memory states (10^5), and long retention time (>10 000 s). The present synthetic route for memory devices incorporating covalently immobilized gold nanoparticles has several advantages such as solution processable, enhanced device stability, low-cost, and low-temperature process and will be a step toward realization for low-cost, lightweight, flexible, logic display driver, and flash memory applications.

INTRODUCTION

Metal nanoparticle films have been the subject of much research in the field of materials science, primarily due to the interest in their optical and electronic properties.[1] Gold nanoparticles are most frequently used due to their chemical stability, size-related electronic, magnetic, and optical properties, and their applications in catalysis and biology.[2] Two-dimensional assemblies of monodisperse nanoparticles with controlled size in the nanometer range have potential applications in solid-state electronic devices. The use of organic materials provides a simplified manufacturing process yielding low-cost, flexible, and lightweight devices.[3,4] With the development of organic electronics, there has been much focus on organic transistors,[5,6] organic light-emitting diodes,[7,8] and organic photovoltaic cells[9,10] and thus necessitates the development of organic memories which are solution-processable and easily integratable with the transistors. Memory devices have applications for flexible display drive logic, high-end computing and smart cards.[11] OFET-based memory is considered a promising candidate for realization of organic memory because of its nondestructive read-out, complementary integrated circuit architectural compatibility, and single-transistor realization.[12,13]

Organic memory devices have been demonstrated via an organic/metal nanoclusters/organic structure where metal nanoparticles were incorporated into a semiconducting organic layer.[14] Trapping of charges at the nanoparticles has been proposed as one possible mechanism.[15] Nanoparticle-based memories are attractive in this respect due to reduced leakage from defects in the underlying dielectric, multibit storage capability, and promise of miniaturization.[16−18] Thermal evaporation has been utilized to create metallic nanoparticles for transistor memory.[19−21] Although evaporated nanoparticle memories have shown good performance, however, metallic contamination in the gate oxide layer and/or diffusion of metallic components to the interface of the memory devices can occur during synthesis of metallic nanoparticles.[22] Other limitations include the use of vacuum techniques as well as the challenges of independently controlling the diameter, spacing, and number of nanoparticles.[23]

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For the realization of metal nanoparticles based memory devices, formation of high-density and uniformly distributed nanoparticles is the key requirement.[17,24] Shortcomings in the nanoparticle-based memory devices such as metallic contamination, formation of metal compounds, and nonuniformity in size and shape of metallic nanoparticles can be overcome by including presynthesized nanoparticles in the devices.[25,26] In the case of presynthesized nanoparticles used in spin-coating-based memory devices, spun-cast polymer nanoparticle blends result in uncontrolled nature of particle size distribution due to random distribution of nanotraps throughout the host matrix. Randomly distributed nanoparticles will result in different numbers of nanoparticles within each unit device and, thus, may show nonuniform device performance. Assembly of as-synthesized nanoparticles for nonvolatile memory applications may lead a solution to above-mentioned problems.

Furthermore, the stability of nanostructures containing organic thin films has emerged as one of the critical issues in organic electronic devices since degradation of organic devices occurs largely due to changes in morphology, loss of interfacial adhesion, and interdiffusion of components.[27] For example, drop-cast films of capped nanoparticles have been investigated for electron transfer[28] and as chemical sensors.[29,30] However, drop-cast films lose adhesion to the substrate when exposed to the solvent media. Recently, the Langmuir−Blodgett deposition of organically passivated AuNPs has been reported for flash memory application,[31] ester-modified Pd nanoparticles have been immobilized on the substrate through hydrogen bonding,[32] and citrate-capped AuNPs have been electrostatically assembled on to carbon surfaces.[33] But these nanoparticle films are not mechanically robust due to weak interlayer bonding. A key factor in addressing this issue will be assembling the nanoparticles covalently onto a desired surface in order to provide the required stability.

The usage of polymeric surfaces in assembling nanoparticles is of particular interest since polymeric surfaces provide more binding sites as compared to monomers for nanoparticle assembly. Some of the attachment methods used for assembling nanoparticles at polymer surfaces are hydrogen bonding,[34,35] gold−thiol bonding,[36] and electrostatic interactions.[37−39] However, these methods do not produce a strong linkage between the particles and the substrates, which in turn limits their applicability. Films with covalent interlayer bonding are more advantageous to withstand elevated temperature, polar solvent attack, mechanical wear, and abrasion due to their robustness.[40,41] Lately, covalently assembled nanostructures have been shown to have better performance in terms of mechanical stability or strength.[42−44] Also, covalently bound nanoparticles have previously shown applications for photovoltaics[27] and antibacterial property.[45]

In this work, we report a versatile approach to enhance the stability of OFET-based memory devices through covalent assembly of functionalized gold nanoparticles. Characterization techniques such as transmission electron microscopy (TEM), field emission scanning electron microscopy (FESEM), and atomic force microscopy (AFM) were employed to investigate particle morphology and their immobilization on the surface. In addition, the electrical characterization of covalently bound AuNPs as a charge-trapping layer in OFET-based memory applications was also investigated. Hysteresis in source/drain current as a function of applied gate voltage was observed due to the charge-trapping in AuNPs. The pentacene OFET-based memory devices having such covalently bound gold nanoparticles exhibited memory window of 7.7 V, on/off ratio of 10^5, and retention time of more than 10 000 s. To the best of our knowledge, this work represents the first attempt to fabricate a OFET-based memory device utilizing covalently immobilized gold nanoparticles.

EXPERIMENTAL SECTION

Materials. Hydrogen tetrachloroaurate(III) trihydrate ($HAuCl_4 \cdot 3H_2O$) (≥99.9%, Aldrich), *p*-aminophenyltrimethoxysilane (APhS) (90%, Gelest), 11-mercapto-1-undecanol (MUD) (≥97%, Fluka), tetraoctylammonium bromide (TOAB) (98%, Aldrich), sodium borohydride ($NaBH_4$) (98%, Lancaster), poly(methyl vinyl ether-*alt*-maleic anhydride) (Gantrez) ($M_n \sim 311\,000$, $M_w \sim 1\,080\,000$) (Aldrich), *i*-propyl alcohol (≥99%, Merck), tetrahydrofuran (THF) (≥99%, Merck), and *N*, *N*′-dimethylformamide (DMF) (≥99%, Fisher Scientific) were all used as received. Pentacene (sublimed) was purchased from Sigma-Aldrich.

Synthesis of Thiol-Stabilized Gold Nanoparticles. Synthesis of gold nanoparticles was carried out as mentioned earlier.[46] Briefly, into a stirred solution of TOAB (0.6 g) in 40 mL of toluene, a solution of $HAuCl_4$ (0.2 g) in 20 mL of deionized (DI) water was added. After 5 min, the biphasic solution was separated and the organic phase was placed in a 125 mL conical flask and stirred vigorously at 250 rpm. A solution of $NaBH_4$ (0.2 g) in 15 mL of DI water was added dropwise over a period of 10 min, resulting in red-colored solution. After the solution was stirred for 1.5 h, the two phases were separated and the organic phase was vigorously washed with 0.1 M HCl, 0.1 M NaOH, DI water, and saturated brine. Later, exchange of the TOAB capping layer with MUD was performed. To a stirred solution of MUD (0.15 g) in 17 mL of DMF, a solution of TOAB-capped AuNPs in toluene (34 mL) was added dropwise under N_2 atmosphere. The stirring was continued for 2 h, after which the solvents were concentrated to 0.5 mL in a rotary evaporator, and *i*-propyl alcohol was added and evaporated to near dryness. The nanoparticles were flocculated through addition of *i*-propyl alcohol (0.5 mL) followed by acetone (30 mL). Excess MUD and TOAB were removed by centrifugation of the suspension and removal of the solvent, followed by addition of *i*-propyl alcohol (0.5 mL) and acetone (30 mL). This process was repeated four times to ensure complete removal of excess MUD and TOAB. Finally, the nanoparticle precipitate was then dried under nitrogen environment overnight at room temperature.

Immobilization on Silicon Surface. Silicon substrates were cleaned by successive sonication in methanol and acetone for 30 min each, and later treated with "piranha solution" (7/3 (v/v) mixture of concentrated sulfuric acid and 30% hydrogen peroxide) at 75 °C for 45 min. They were then copiously rinsed with deionized water and blow dried with nitrogen. Assembly of aminosilane was performed as described elsewhere,[47] wherein the hydroxyl-covered substrates were rinsed with toluene and then immersed in a 3 mM APhS solution in toluene for 2 h. The above amine-terminated substrates were immersed in a 0.5% (w/v) THF solution of Gantrez for 1 h under nitrogen environment. The substrates were removed from the solution, rinsed rigorously, and sonicated for 5 min with THF, rinsed again with THF, and finally blow dried with nitrogen. The thus-obtained anhydride-terminated substrates were immersed in a 100 μg/mL solution of MUD-capped gold nanoparticles in DMF in a three-necked flask under nitrogen environment. The contents of the flask were held at 90 °C for 1 h with stirring.

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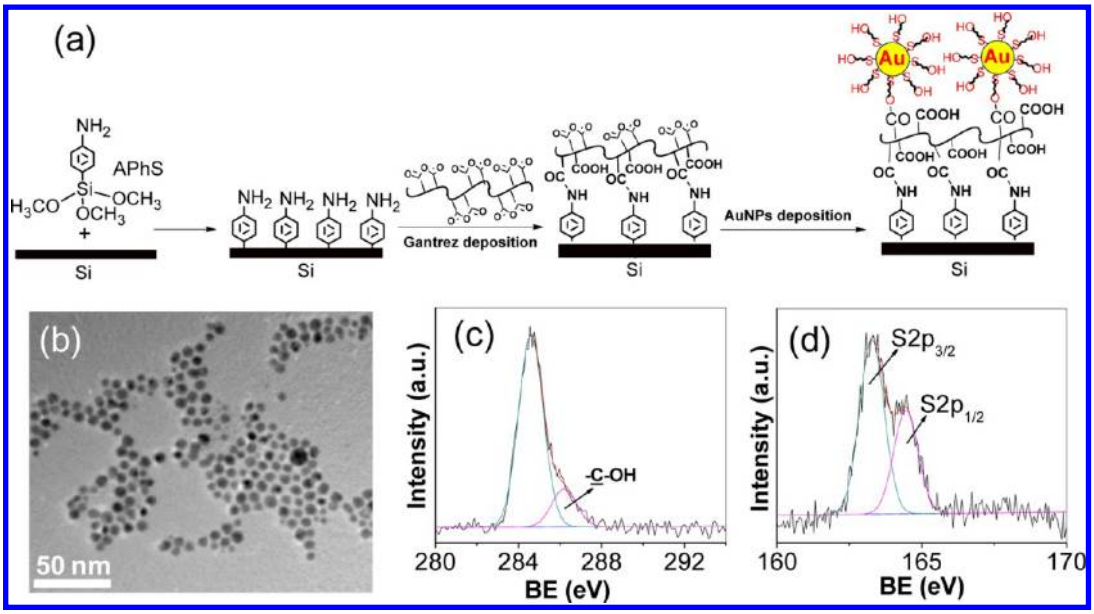

Figure 1. (a) Schematics for the immobilization of MUD-capped gold nanoparticles on to a hydroxyl-terminated silicon surface. (b) TEM image of MUD-capped gold nanoparticles, and X-ray photoelectron spectra of MUD-capped gold nanoparticles showing the (c) C 1s region and (d) S 2p region.

Subsequently, the substrates were rinsed with DMF followed by sonication for 5 min in DMF to remove any physically bound nanoparticles and rinsed again with DMF as well as acetone, and were finally blow dried with nitrogen. Details of various deposition steps are shown in Figure 1a.

Device Fabrication. A heavily n-doped silicon wafer ⟨100⟩ with a 100 nm surface layer of silicon dioxide (SiO_2) was used as the substrate/gate electrode, with the top SiO_2 layer serving as the gate dielectric. AuNPs were immobilized on to SiO_2 substrate through covalent binding using Gantrez polymer as surface modifier. The pentacene OFET memory devices were fabricated on AuNPs immobilized Si substrate. The pentacene (sublimed grade) was thermally evaporated, at a deposition rate of 0.1 nm s^{-1} and a pressure of 10^{-7} Torr, to form a 50 nm thick film. Subsequently, a series of gold source/drain contacts (thickness of 50 nm) were deposited by vacuum thermal evaporation through a shadow mask to create a series of transistors with various channel length (L) and width (W) dimensions. Schematics of an organic field-effect transistor memory device having gold nanoparticles as floating gate memory elements is shown in Figure 2. Patterned transistors with channel length of 90 μm and channel width of 4000 μm were used for $I-V$ measurements. Silicon oxide at the backside of the silicon wafer of the transistor device was removed with sandpaper to provide a conductive gate contact. Reference devices have only Gantrez deposition on SiO_2 substrate. The output and transfer characteristics of the memory transistors were measured under vacuum (1×10^{-4} Torr) in the dark at room temperature using a Keithley 4200 semiconductor characterization system and a cryogenic probe station (TTP6, Lakeshore). The FET mobility was extracted using the following equation in the saturation regime from the gate sweep

$$I_D = \mu Ci(V_G - V_T)^2(W/2L)$$

where I_D is the drain current, μ is the field-effect mobility, Ci is the capacitance per unit area of the gate dielectric layer (SiO_2, 100 nm, Ci = 27 nF cm^{-2}), and V_G and V_T are gate voltage and threshold voltage, respectively.

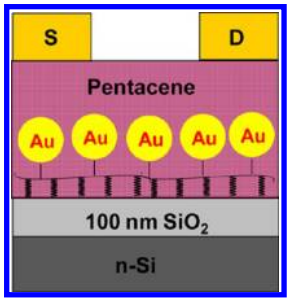

Figure 2. Schematics of an organic field-effect transistor (OFET) memory device having immobilized MUD-capped gold nanoparticles as floating gate memory elements.

Characterization. Samples for transmission electron microscopy (TEM) (JEM-2010, JEOL, Tokyo, Japan) were prepared by placing a few drops of the nanoparticle-containing solution on 3 mm Formvar/carbon-coated copper grids (Electron Microscopy Sciences, Philadelphia, PA). Excess solution was removed by an absorbent paper and the sample was dried overnight in air before scanning. The size distribution of particles was determined from histograms obtained using TEM images. The surface morphology of the films was examined by AFM (atomic force microscopy; NanoScope IIIa, Digital Instruments). All images were collected in air using the tapping mode and a monolithic silicon tip. The drive frequency was 330 ± 50 kHz, and the voltage was between 3.0 and 4.0 V. The drive amplitude was about 300 mV and the scan rate was 1.0−1.5 Hz. XPS measurements were made on a Kratos Analytical AXIS HSi spectrometer with a monochromatized Al Kα X-ray source (1486.6 eV photons) at a constant dwell time of 100 ms and a pass energy of 40 eV. The X-ray source was run at a reduced power of 150 W. The pressure in the analysis chamber was maintained at 7.5×10^{-9} Torr or lower during each measurement. All binding energies (BEs) were referenced to the C 1s hydrocarbon peak at 284.6 eV. The nanoparticle assemblies were examined for their density, distribution, and

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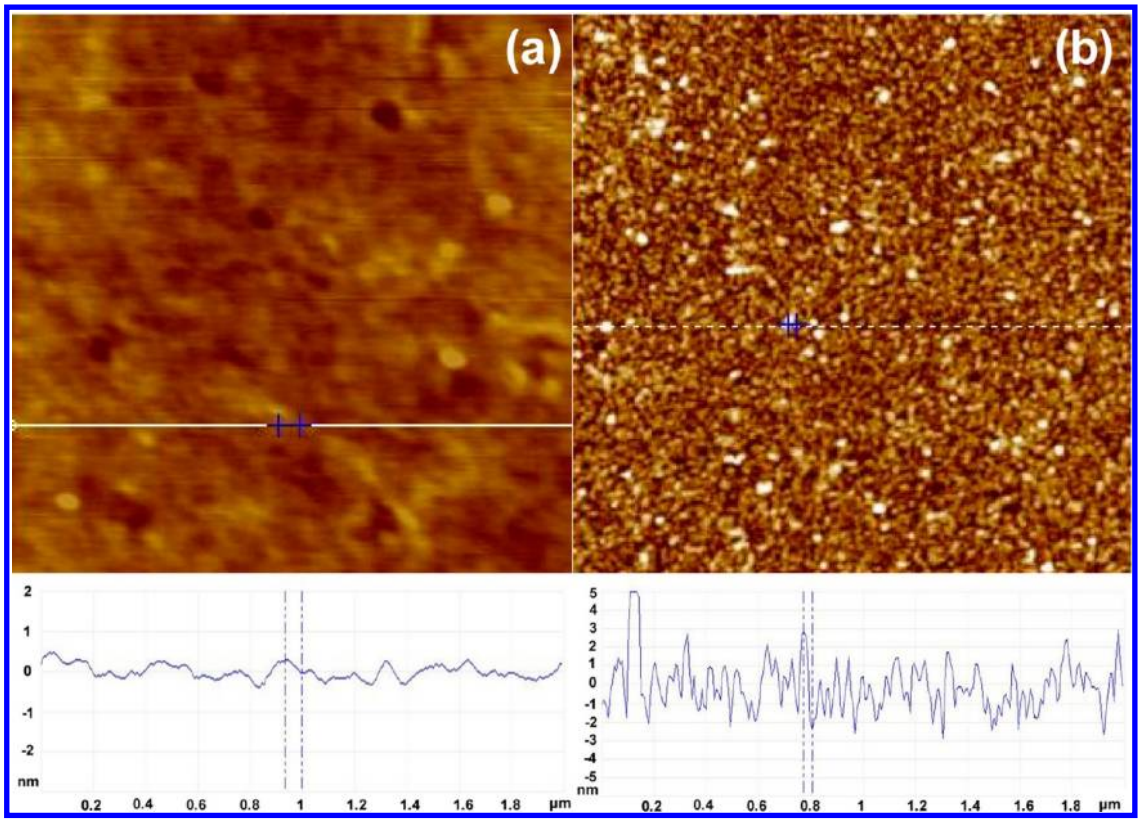

Figure 3. Tapping mode AFM images ($2 \times 2\ \mu m^2$) and z profiles for (a) a Gantrez-deposited Si surface, and (b) similar surface after immobilization of MUD-capped gold nanoparticles.

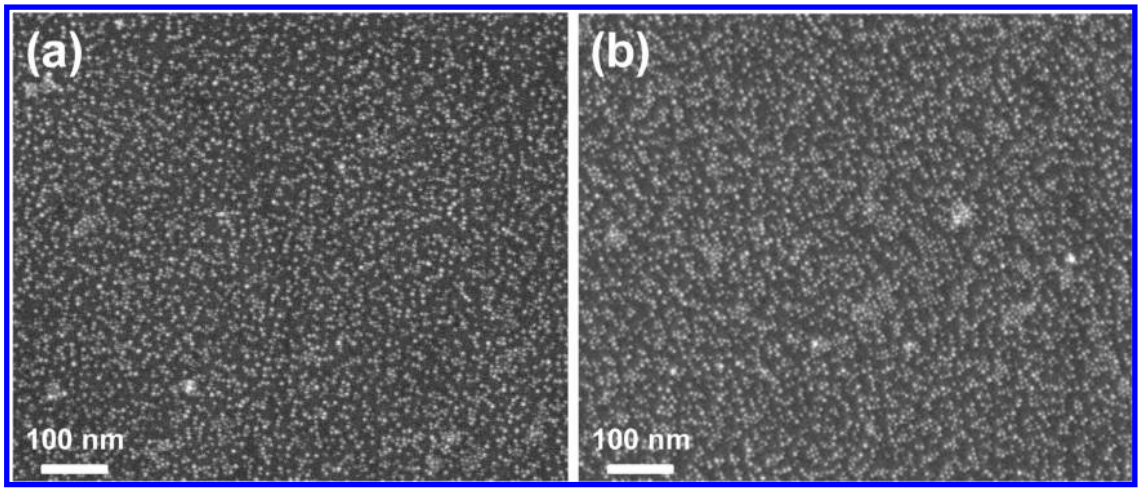

Figure 4. FESEM images for MUD-capped AuNPs immobilized on Si surface: (a) after rinsing, and (b) after 5 min sonication.

homogeneity using field emission scanning electron microscopy (FESEM) (JSM-7600F, JEOL, Japan).

RESULTS AND DISCUSSION

TEM micrograph of the synthesized MUD-capped AuNPs is shown in Figure 1b. The nanoparticles are approximately spherical, with an average Au core diameter of 5 ± 0.5 nm. The presence of alcohol functionality in the synthesized MUD-capped AuNPs is confirmed by the XPS spectra of C 1s region having the C−O component at 286.2 eV as shown in Figure 1c. Figure 1d represents the S 2p region, with peaks observed at 163.3 and 164.4 eV corresponding to the thiolates, confirming the absence of unreacted or oxidized thiol species.[48] Successful covalent immobilization of Gantrez and MUD-capped AuNPs has been demonstrated using XPS.[49] AFM images for Gantrez-deposited Si substrate and AuNPs immobilized on Si substrate are shown in Figure 3. The root-mean-square roughness for the Gantrez-deposited image is 0.3 nm, confirming the smooth surface after deposition of Gantrez film, whereas that in the immobilized nanoparticle image is 1.4 nm. Figure 3b shows a single layer of nanoparticles for AuNPs immobilized on Si substrate. The nanoparticle layer average height, measured at voids, is 4.6−5.4 nm, in agreement with the nanoparticle size (Figure 1b), indicating single layer of MUD-capped AuNPs. Highly dispersed and well-separated AuNPs are observed after the immobilization process, showing no evidence of aggrega-

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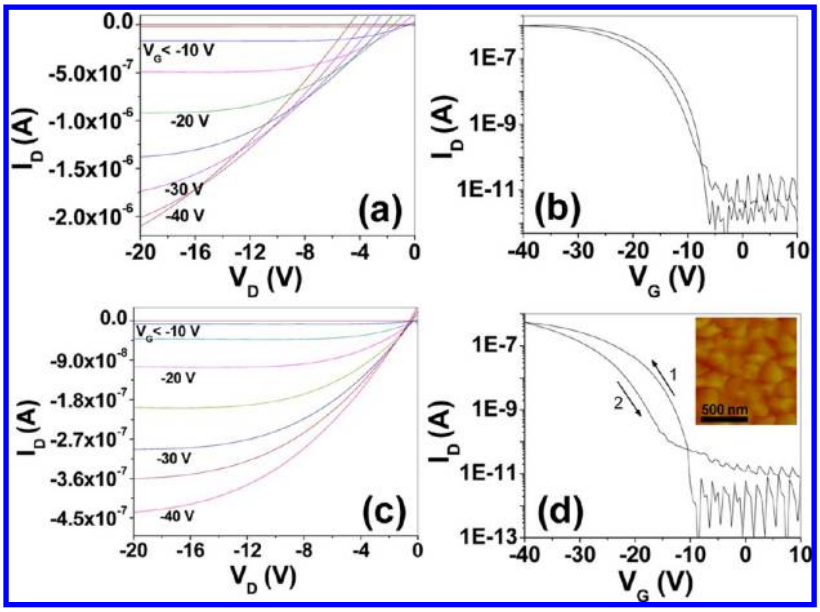

Figure 5. Output characteristic curves (I_D vs V_D) (left column) and transfer curves (I_D vs V_G) (right column) for a pentacene OFET having Gantrez-deposited Si substrate (panels a and b) and a pentacene OFET memory having immobilized MUD-capped gold nanoparticles (panels c and d). Output characteristics were measured at different gate biases (from 0 to −40 V with a step of 5 V) for devices with a channel length of 90 μm and a width of 4000 μm; transfer characteristics of the same pentacene devices were measured at the drain voltage (V_D) of −20 V. The inset shows the pentacene morphology on the gold nanoparticles immobilized Si substrate.

tion during the immobilization step (Figure 4a). Stability of such covalently anchored nanoparticles was checked by sonicating the substrate-bound nanoparticle systems in DMF for 5 min. There is no loss of nanoparticles observed after the sonication step, thereby ensuring the firm attachment of the particles to the substrates (Figure 4b). The nanoparticle density after the sonication step is calculated to be 5×10^{11} cm^{-2}. However, loss of the nanoparticle density was observed after the sonication processing when nanoparticles were bound to the substrate through hydrogen or electrostatic binding.[49]

Figure 5 presents the typical output and transfer characteristics of the floating gate pentacene-based OFET memory device (channel length of 90 μm and width of 4000 μm). The observed transistor characteristics show reproducible and stable device performance; the additional floating gate layer does not distort the standard OFET performance. The measured values of the typical hole mobility (μ_{hole}) and on/off ratio ($I_{on/off}$) were 0.003 cm^2 V^{-1} s^{-1} and 10^5, respectively, for all the devices. The deposited polycrystalline pentacene thin film on the floating gate layer consists of grain sizes of approximately 0.2 μm (inset of Figure 5d). The control transistors utilizing Gantrez-deposited Si substrate (without AuNPs) yielded comparable device performance with on/off ratio of 10^5-10^6. An informative measure of the memory effect is the hysteresis window of the transfer curve upon double sweeping. The anticlockwise I_D-V_G hysteresis loop further indicates that there is a net hole trapping effect. A memory window of 7.7 V was observed for pentacene OFET-based memory device having covalently bound MUD-capped AuNPs (Figure 5d), when the gate bias was swept between +40 and −40 V. However, there was negligible trapping effect (<1 V) for control pentacene transistor (without AuNPs) as shown in Figure 5b. The extent of the observed memory window is similar to the previously reported gold nanoparticles obtained from electron-beam evaporation or electrostatic binding.[50,51] Thus, memory devices fabricated from solution processable covalently assembled nanoparticles will be an alternative to expensive electron-beam evaporation technique due to their low-cost and ease of fabrication. Operating voltages for the OFET memory devices can be further tailored by using thinner dielectrics or high dielectric constant materials.[52] The hysteresis window (ΔV_{th}) was used to determine the number of the stored charge density per unit area (Δn) according to the equation: $\Delta n = \Delta V_{th}$Ci/e, where e is the elementary charge and Ci is the capacitance of the gate dielectric per unit area. The charge carrier density can be calculated as 1.4×10^{12} cm^{-2}. Assuming that charge is uniformly stored in the floating gate of OFET, it can be inferred that on average about 3 holes are stored per Au nanoparticle as observed earlier.[53]

A mechanism for the charge trapping is further suggested as follows. The highest occupied molecular orbital (HOMO) level of pentacene (at ∼5.0 eV) is close to the work function of MUD-capped AuNPs (4.5 eV).[54,55] When a negative gate voltage is applied, the hole carriers induced in pentacene molecules at the interface can transfer into the AuNPs and be trapped there. The trapped hole charges in the AuNPs form an internal electric field which partially offsets the external applied electric field. This results in the low-conductivity state of the channel; this is called the programming process. On the other hand, with a positive bias applied, the hole charges can be detrapped from the AuNPs to the surrounding pentacene. This results in the high-conductivity state of the channel; this is called the erasing process.

One of the important parameters of any storage device is its memory retention time, which is defined as the time for which the memory can be read out clearly to be in the on or in the off state. The data retention properties were measured as a function of the retention time using the memory devices in the programmed/erased states. Figure 6 shows the current measured at 0 V gate voltage at a constant source-drain bias of −20 V, after the device was "turned on" at a pulse of 40 V for 30 s or "turned off" at a pulse of −40 V for 30 s. The on-current

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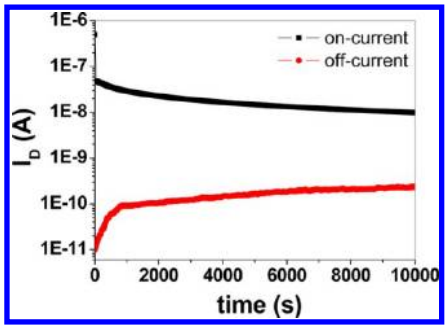

Figure 6. Retention characteristics of the devices having immobilized MUD-capped gold nanoparticles that were measured at V_D = −20 V and V_G = 0 V after programming and erasing by applying a gate bias of −40 and 40 V for 30 s at V_D = 0 V.

(I_{on}) and off-current (I_{off}) were well separated with respect to the elapsed time. Notably, both the programmed and erased states degraded with time, but overall, the stored data was well maintained, and moreover distinguishable on/off ratio was obtained even after 10 000 s reading. The good retention performance of the OFET devices is result of the MUD (long alkyl chain) capping around AuNPs which allows slow trapping and detrapping of the charge carriers in gold nanoparticles.[56]

CONCLUSIONS

In conclusion, we have demonstrated the possibility of realizing integrated ultra-high-density OFET memory devices having covalently bound gold nanoparticles. Detailed structural characterizations have been performed for covalently immobilized gold nanoparticles on silicon surface. FESEM and AFM images show the surface morphology of the well-separated immobilized nanoparticles. The OFET devices having such covalently bound gold nanoparticles showed large on/off current ratio at about 10^5 and good data retention of more than 10 000 s. The OFET memory device presented herein may be applied to a variety of potential applications, including novel nonvolatile organic memory, which would be useful for low-cost, lightweight, flexible, logic display driver and flash memory.

AUTHOR INFORMATION

Corresponding Author

*E-mail: pslee@ntu.edu.sg.

Notes

The authors declare no competing financial interest.

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