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Enhanced Performance and Fermi-Level Estimation of Coronene-Derived Graphene Transistors on Self-Assembled Monolayer Modified Substrates in Large Areas

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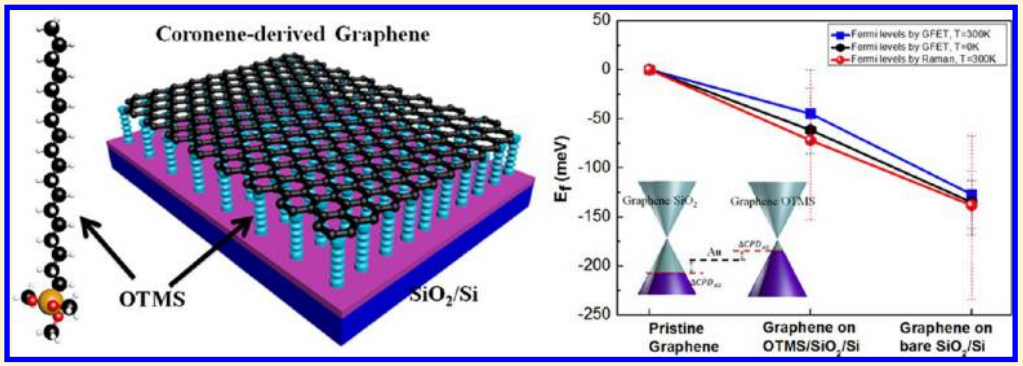
Supporting Information



ABSTRACT: The performance of graphene field effect transistors (GFETs) strongly depends on the interface between graphene sheets and the underlying substrates. In this work, we report that an octadecyltrimethoxysilane (OTMS) SAM modified conventional SiO_2/Si substrate can consistently enhance the performance of coronene-derived large-area graphene FETs. The improved transport properties in terms of boosted carrier mobility (up to 10 700 ± 300 $cm^2 V^{-1} s^{-1}$), long mean free path, nearly vanished hysteretic behavior, and remarkably low intrinsic doping level are mainly attributed to the strong suppression of interfacial charge impurity scattering and remote interfacial phonon (RIP) scattering, less adsorption of dipolar adsorbates, and the attenuated charger transfer at the interface of graphene and dielectric. The intrinsic doping levels (the Fermi energy) of graphene on OTMS-modified and bare SiO_2 have been quantitatively estimated and confirmed by the Dirac points of GFETs, the Raman mapping of *G*-peak positions, and the surface potential maps by KPFM. The facile fabrication of a graphene device over a large area provides an unprecedented combination of high performance and low cost for the future application of all carbon-based nanoelectronics.

1. INTRODUCTION

Graphene, a one-atom-thick sp^2-bonded carbon sheet, has attracted intense attention as a promising material for high-speed field-effect transistors (FETs).[1−5] The performance of graphene FETs strongly depends on the interface between graphene sheets and the underlying substrates.[3] It is well-known that the electrical transport properties of graphene on a standard SiO_2/Si substrate are deleteriously affected not only by intrinsic scattering sources, such as longitudinal acoustic phonon,[3] lattice defects, and grain boundaries formed during the growth process,[6] but also by various extrinsic scattering mechanisms, i.e., charged impurities, interfacial roughness, remote interfacial phonon (RIP),[3,7,8] and residual species during the etching and transfer processes.[6,9] For mechanically exfoliated graphene, extraordinary carrier mobilities have been observed on different substrates, e.g., 15 000 $cm^2 V^{-1} s^{-1}$ on bare SiO_2 substrates,[2] 60 000 $cm^2 V^{-1} s^{-1}$ on high-quality hexagonal boron nitride (h-BN),[10] and 200 000 $cm^2 V^{-1} s^{-1}$ for suspended graphene.[4] Nevertheless, fabrication of atomically flat h-BN and suspended graphene is highly challenging in practical device applications.[10,11] Recently, Wang's group[11] and Xu's group[12] have reported that the carrier mobility of mechanically exfoliated graphene on a modified SiO_2/Si substrate by organic self-assembled monolayers (SAMs) can exceed 45 000 $cm^2 V^{-1} s^{-1}$. This is mainly due to the effective suppression of charged-impurity and remote interfacial phonon (RIP) scatterings.[7,8,11,12] However, all of the fabricated devices were limited by the small sizes of graphene sheets, which are unsuitable for graphene-based integrated circuits in the future.

In this work, we report that the performance of coronene-derived large-area graphene field effect transistors (GFETs) can

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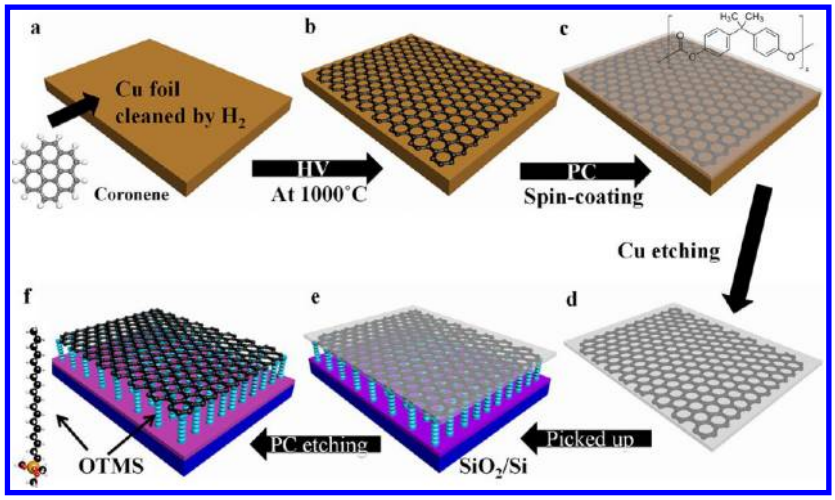

Figure 1. Process flow of graphene growth and transfer procedure. (a) Coronene molecules introduced to precleaned copper surface. (b) Graphene formed on Cu foil at 1000 °C in high vacuum. (c) Spin poly(bisphenol A carbonate) onto graphene. Top inset, repeating chemical structure unit of PC. (d) Etch copper in 0.1 M ammonium persulphate ($(NH_4)_2S_2O_8$) solution. (e) Transfer PC-supported graphene sheets to target substrate. (f) Remove PC, leaving graphene on OTMS/SiO_2/Si substrate. Inset, structure of octadecyltrimethoxysilane (OTMS), $C_{21}H_{46}O_3Si$, C-atom (black), H-atom (white), O-atom (red), and Si-atom (brown).

be consistently enhanced by applying octadecyltrimethoxysilane (OTMS, $C_{21}H_{46}O_3Si$) SAMs[13,14] onto a bare SiO_2/Si substrate. As one kind of coplanar polycyclic aromatic hydrocarbon (PAH) with 6-fold rotational symmetry, coronene has been demonstrated to be a superior solid carbon source for high-quality and large-area graphene synthesis.[15] Furthermore, instead of poly(methyl methacrylate) (PMMA), poly(bisphenol A carbonate)[16,17] has been adopted in our transfer process to obtain a clean graphene surface. For the graphene transferred onto OTMS modified substrates, the carrier mobility can be increased up to 10 700 ± 300 $cm^2 V^{-1} s^{-1}$ at room temperature, which is 2−4 times larger than that of conventional GFETs on a bare SiO_2/Si substrate. The transfer hysteresis is suppressed even under ambient conditions by preventing the adsorption of dipolar species by graphene.[7] The Dirac point is markedly shifted back, indicting a low intrinsic doping level.[7,11,12,18,19] However, in the previous literature,[7,11,12,19] experimental assessment of the doping effect associated with substrates was only by the transfer curves of GFETs (i.e., the shift of the charge neutrality points). Alternative means to probe the doping effect due to the substrates can be beneficial for exploring the electrical properties of graphene. What's more, the precise shifts of Fermi levels of graphene on SAM modified substrates have not been quantitatively addressed as compared to that on bare SiO_2/Si substrates. Here, we demonstrate the combined use of GFET measurements, micro Raman mapping, and Kelvin probe force microscopy (KPFM) to comprehensively investigate the intrinsic Fermi levels of graphene on the OTMS-modified SiO_2/Si substrate as well as on the bare SiO_2/Si substrate. By numerical evaluation of Fermi−Dirac integrals, the accurate relationships between the Fermi-level and the carrier density of graphene at different temperatures (0 to ∼400 K) have been obtained, and thus the exact intrinsic Fermi levels of graphene on OTMS and bare SiO_2 can be quantitatively estimated from the curve intersections. The excellent transport properties of graphene on the OTMS-modified SiO_2/Si substrate show that SAM modified SiO_2/Si substrates are very promising for large-area and low-cost carbon-based integrated electronics.

2. EXPERIMENTAL SECTION

2.1. Synthesis and Transfer of Coronene-Derived Graphene. Figure 1 shows a schematic diagram of graphene growth and the transfer process. The underlying growth mechanism has been systematically discussed in the previous work.[15] In a typical growth process, the commercially available Cu foil (99.8%) was annealed by forming gas (20% H_2 + 80% Ar) for 30 min to reduce native CuO and to increase the size of copper grain. Afterward coronene molecules were evaporated onto copper surface (1000 °C) to form graphene sheet without exposure to H_2 under high vacuum conditions as shown in Figure 1, panels a and b. The sample was then cooled down to room temperature in high vacuum. At present, poly(methyl methacrylate) (PMMA) is commonly used for graphene transfer in the literature.[20,21] However, its residue on the graphene surface is hardly to be completely removed and to attain the clean graphene surface in large area.[22] Therefore, we chose poly(bisphenol A carbonate) (abbreviated as PC, ∼1.5 wt % in chloroform)[16,17] as the supporting layer since it can be easily removed by organic solvents. The PC/chloroform solution was spin-coated on the top of the graphene sheets formed on the copper surface (see Figure 1c), and then the sample was baked at 150 °C for 180 s to remove the solvent. Subsequently, the Cu foil was cut into two pieces, both of which were etched with 0.1 M ammonium persulphate ($(NH_4)_2S_2O_8$) solution through the following electrochemical reaction:[23]

$$Cu + S_2O_8^{2-} \rightarrow Cu^{2+} + 2SO_4^{2-}$$

Following that the floating PC/graphene layers were thoroughly cleaned by DI water and transferred to 300-nm SiO_2/Si substrates with and without ultrasmooth OTMS-SAM modification, respectively (see Figures 1d−f and S1). To remove the PC layer and avoid graphene damage, the two samples were put into acetone−buffered chloroform solvent (1:1 in volume) for 1 h and after that in pure chloroform for another 1 h. Finally, the two substrates with graphene were rinsed in IPA and dried by nitrogen.

2.2. Characterization of Coronene-Derived Graphene. Raman spectroscope (514 nm Renishaw in Via) was used to characterize the quality, thickness, and doping levels of

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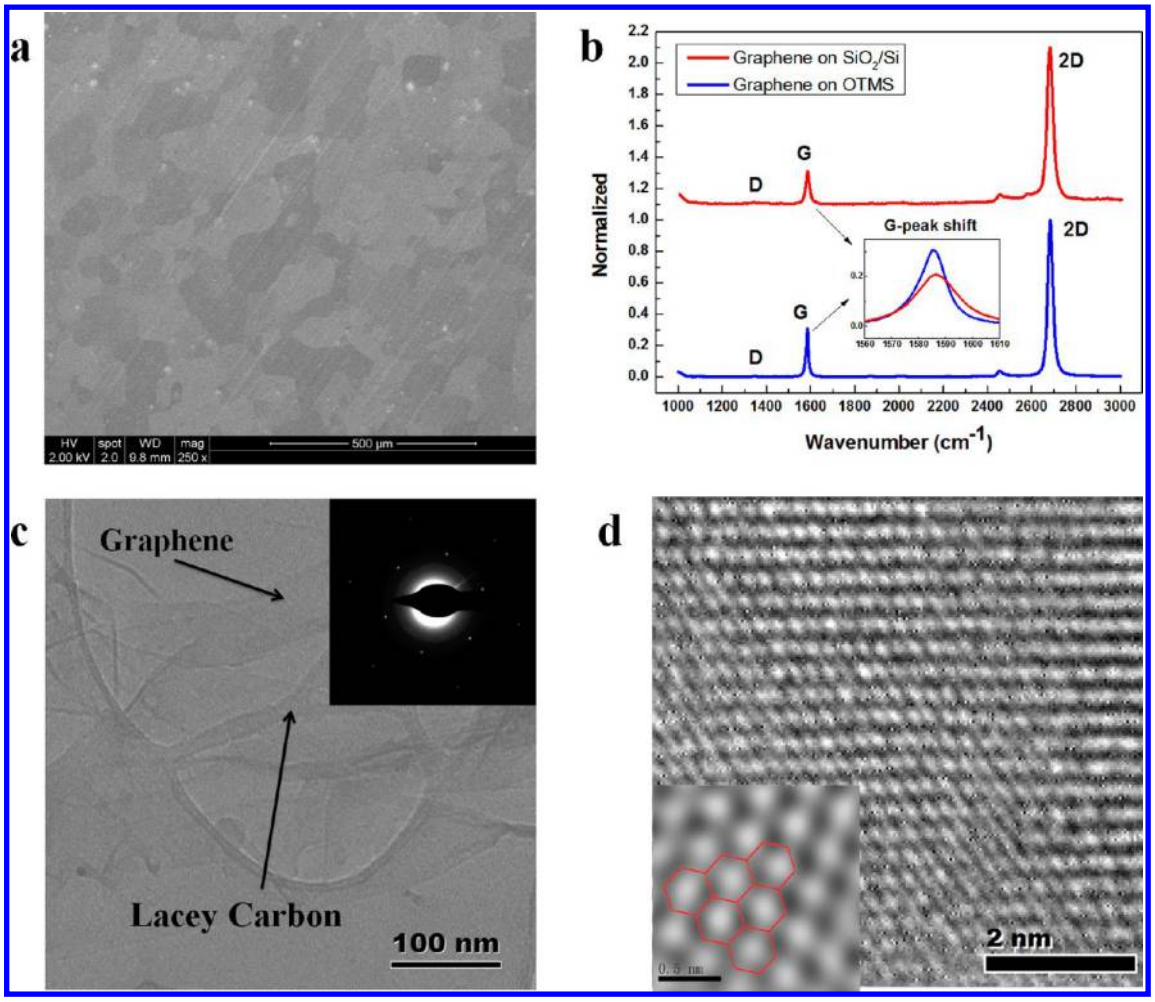

Figure 2. (a) SEM image of as grown graphene sheets on a copper surface; the different brightnesses of copper grains is due to the electron channeling effect. (b) Raman spectra of transferred graphene sheets on bare SiO_2/Si (red) and OTMS SiO_2/Si (blue) substrates. Inset, G-peak downshift of graphene on OTMS/SiO2/Si. (c) TEM image of freely suspended graphene film on lacey carbon TEM grid. Inset, SAED pattern of coronene-drived graphene. (d) High-resolution bright field TEM image of monolayer graphene. Inset, the perfect hexagon lattice of graphene.

transferred graphene in ambient conditions at room temperature. The current−voltage (I−V) characteristics of the GFETs were measured with a Keithley 4200 semiconductor characterization system in vacuum at room temperature. SEM and TEM images were obtained by LEO 1450VP (operated at 2 kV) and FEI TecnaiF20 (operated at 200 kV), respectively. KPFM measurements were performed by a Dimension 3100 atomic force microscope (Veeco) in air.

3. RESULTS AND DISCUSSION

Figure 2a is a scanning electron microscopy (SEM) image of the as-grown graphene sheets on copper surface. The underlying copper grains show different brightness due to the electron channeling effect.[21,24] Raman spectroscopy (with 514 nm laser excitation) was used to evaluate the quality, the layer number and doping level of graphene[25−27] on SiO_2 (red line in Figure 2b) and OTMS (blue line in Figure 2b), respectively. The defect-related D-peak (~1350 cm^{-1}) was negligible for both samples, indicating the high quality of the coronene-derived graphene sheets. The G^* band (~2450 cm^{-1}) is due to an intervalley double resonance (DR) Raman process involving one iTO phonon and one LA phonon.[28] Monolayer graphene can be identified according to the intensity ratios of G-peak (~1580 cm^{-1})/$2D$-peak (~2680 cm^{-1}), which here were less than 0.3[26] and the height of the graphene sheets by AFM[23] (see Figure S1d). Since the G-peak varied with doping level,[25,27] a remarkable Raman red shift (inset in Figure 2b) was observed for the graphene sheet on OTMS modified SiO_2/Si in comparison with the sheet on bare SiO_2/Si, suggesting a doping level reduction after OTMS modification. The coronene-derived graphene was further characterized by transmission electron microscope (TEM). Figure 2c displays the graphene sheets suspended on a lacey carbon TEM grid. The selected area electron diffraction (SAED) pattern (inset in Figure 2c) shows the characteristic hexagonal crystalline structure of graphene. Figure 2d presents a high-resolution bright field TEM image obtained from a single-layer area, in which hexagons in the single-layer graphene can be clearly observed (left inset).

Electrical transport measurements were carried out on GFETs fabricated with graphene sheets transferred onto both 300-nm SiO_2/Si and OTMS/300-nm SiO_2/Si substrates. To prevent further contamination induced during the lithography process, spun gold (diameter: 25 μm) was used as an additional electrode mask for the fabrication of back-gated graphene FET as shown Figure 3a. Electrodes (50 nm-thick Au films) were prepared by thermal evaporation on the graphene sheets. The ratio of the channel length (L) over channel width (W) on the graphene sheet was typically 1/6, with $L \approx 30$ μm (inset in Figure 3b). The drain voltage (V_{ds}) was 20 mV, and all electrical measurements

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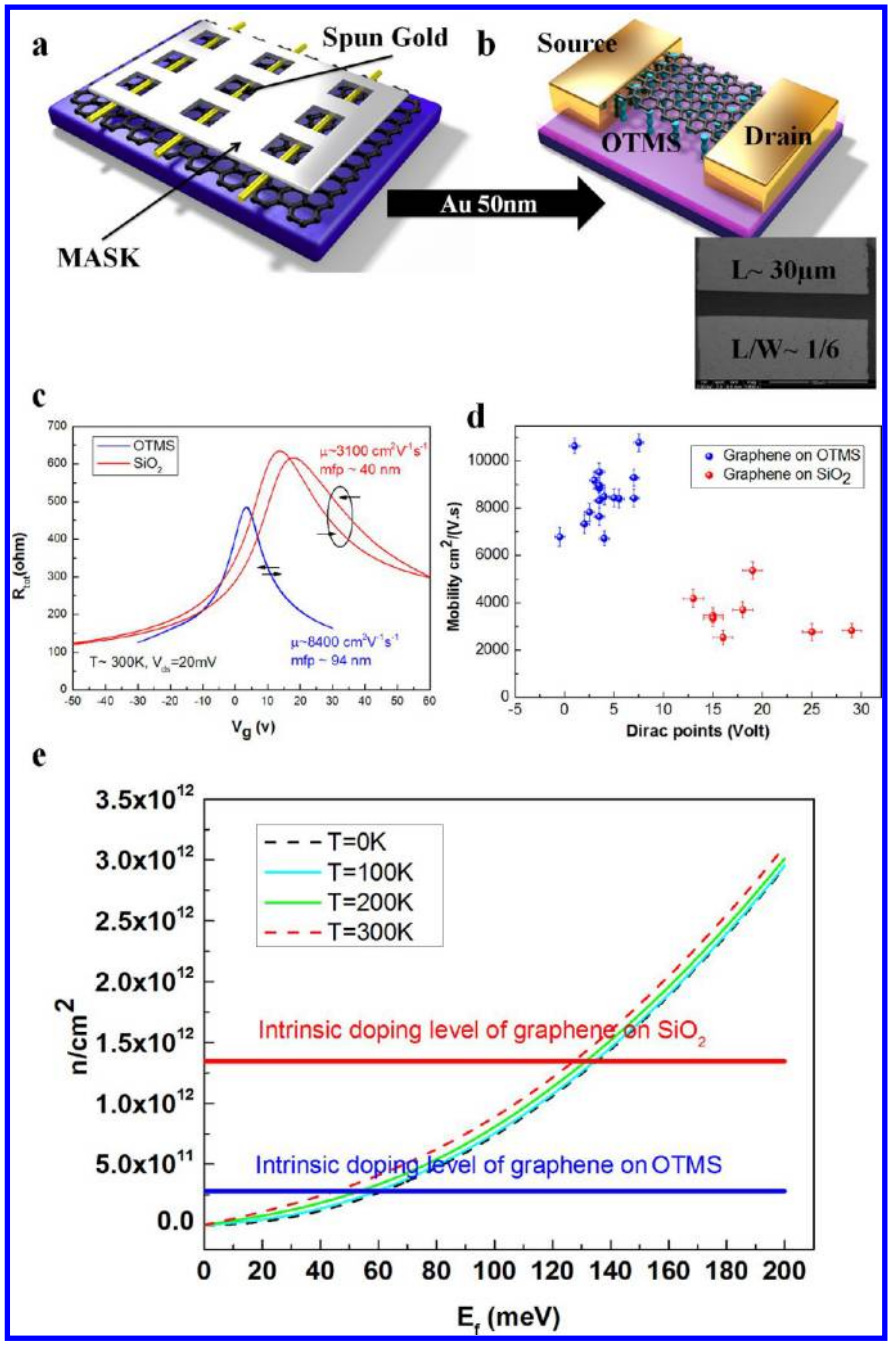

Figure 3. (a and b) Schematics of the fabrication of lithography-free graphene FETs by using spun gold (OD: 25 μm) as channel mask. Inset in panel b, a typical SEM image of GFET. (c) Typical field effect measurements (total device resistance versus sweep bottom-gate voltage) for graphene on OTMS (blue curve) and graphene on bare SiO_2/Si (red cure). (d) Carrier mobility versus neutrality point for 17 GFETs on OTMS (blue circles) and 8 GFETs on SiO_2/Si (red circles). (e) Numerical calculation results of graphene carrier density versus the Fermi level at different temperatures. The horizontal red and blue lines are corresponding to the average intrinsic doping levels (obtained from GFETs) for graphene on SiO_2 and OTMS, respectively. The exact intrinsic Fermi levels of graphene on OTMS and bare SiO_2/Si can then be estimated from the intersections.

were performed in vacuum at room temperature. The typical transfer curves (the device resistance versus ramped back-gate voltage V_g) of both the GFET on OTMS modified SiO_2/Si and the GFET on SiO_2/Si were depicted in Figure 3c, from which the carrier mobility could be obtained by fitting the following equations (see Supporting Information SI-1 for the reason why we employ this model).[29,30]

$$R_{tot} = R_{contact} + \frac{L/W}{e\mu\sqrt{{n_0}^2 + n^2}} \quad (1)$$

$$n = \frac{C_{ox}(V_g - V_{Dirac})}{e} \quad (2)$$

where $R_{tot} = V_{ds}/I_{ds}$ is the total resistance of the device including the contact resistance $R_{contact}$ and the channel resistance, e is the elementary charge, n_0 represents the residual carrier density due to charge impurities,[31] and n is the carrier concentration induced by back-gate bias. The areal capacitance of 300-nm SiO_2 gate dielectric C_{ox} is ~11.5 nF/cm^2. The estimated carrier mobility for graphene on bare SiO_2 is in the range of 2000−5000 cm^2 V^{-1} s^{-1}

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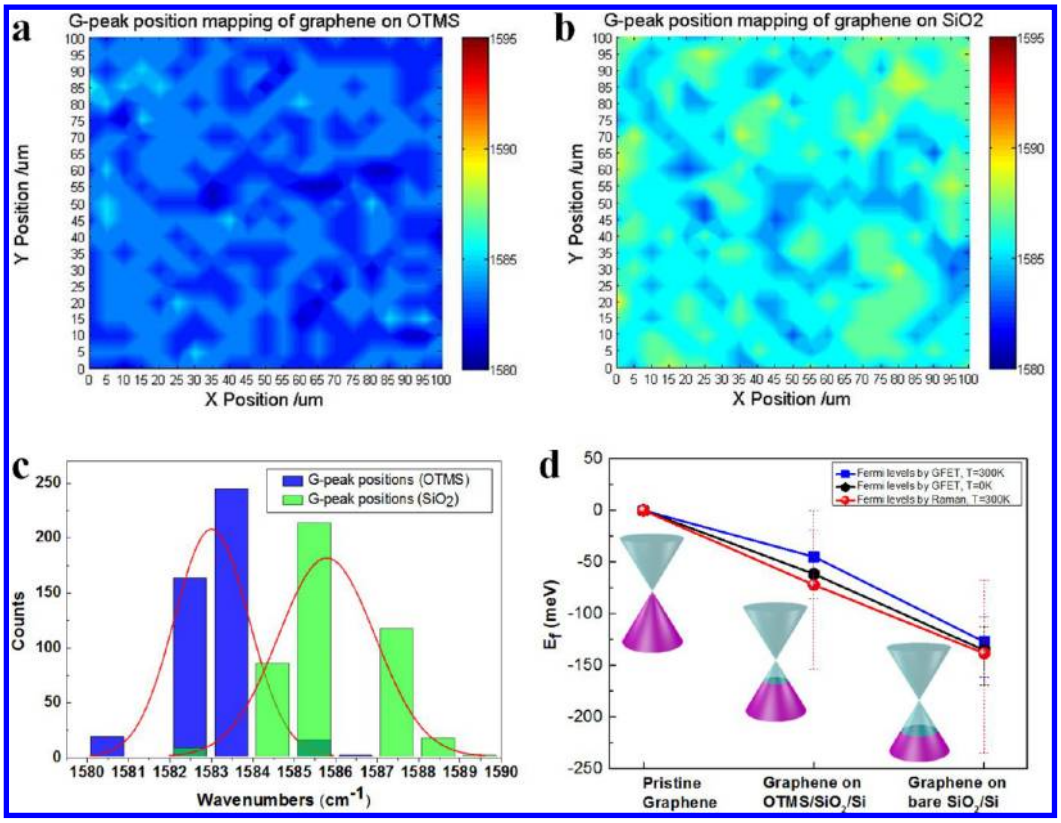

Figure 4. Spatial Raman mapping of the *G*-peak positions for graphene on (a) OTMS and on (b) bare SiO_2/Si. (c) Histograms of the *G*-peak positions for graphene on OTMS (blue) and on bare SiO_2/Si (green). (d) Estimated intrinsic Fermi levels for graphene on OTMS and on bare SiO_2/Si from *G*-peak Raman mapping (red line) and from Dirac points of GFETs with zero temperature approximation (black line) and at room temperature (blue line). The error bars indicate the full range of experimental data.

(3500 ± 320 cm^2 V^{-1} s^{-1} on average). A much higher mobility up to $10\,700 \pm 300$ cm^2 V^{-1} s^{-1} (8600 ± 400 cm^2 V^{-1} s^{-1} on average) is achieved for graphene on OTMS modified SiO_2, as shown in Figure 3d. This value is comparable with the mobility of single-crystalline CVD graphene on hexagonal boron nitride (h-BN) by using the same fitting model.[30] In addition to the field-effect mobility, the scattering time (τ) and the mean free path (mfp) are also major concerns for graphene devices and can be estimated by[32]

$$\tau = \frac{\hbar\sigma}{e^2 v_F}\sqrt{\frac{\pi}{|n|}} \tag{3}$$

$$\text{mfp} = v_F\tau \tag{4}$$

where $v_F = 1 \times 10^6$ m/s is the Fermi velocity[1] and σ is the sheet conductivity which can be extracted by $\sigma = (L/W)/(V_{ds}/I_{ds} - R_{contact})$. The resultant intrinsic mean free path (at $V_g = 0$) for graphene on OTMS/SiO_2 (blue curve in Figure 3c) is ~94 nm, and for graphene on bare SiO_2, it is only ~40 nm (red curve in Figure 3c), indicting a considerable reduction of charged impurity scattering for GFETs on OTMS modified SiO_2/Si.[8] Moreover, due to less adsorption of dipolar adsorbates as well as the strong suppression of charge transfer between graphene and dielectric interface,[7,8] hysteresis in the transfer characteristics nearly vanishes for the GFETs on OTMS/SiO_2. The charge neutrality points (V_{Dirac}) of GFETs on OTMS/SiO_2 are considerably back-shifted (from 18.75 ± 1 V to 3.852 ± 0.5 V on average), as compared to those of GFETs on bare SiO_2 due to the low intrinsic doping levels.[8,11,12,18] The corresponding intrinsic doping levels for graphene on OTMS/SiO_2 ($(2.77 \pm 0.36) \times 10^{11}$ cm^{-2}) and bare SiO_2 ($(1.35 \pm 0.072) \times 10^{12}$ cm^{-2}) are obtained by setting $V_g = 0$ in eq 2. Most of the GFETs on OTMS/SiO_2 are still unintentionally and lightly p-type doped. This is probably owing to the organic residues during the transfer process.[6] At $T = 0$ K, the shift of Fermi energy induced by doping effect from the Dirac point is a simple expression

$$E_F = \text{sgn}(n)\hbar v_F\sqrt{\pi|n|} \tag{5}$$

where sgn(n) is the sign function of n.[1,25,33] By utilizing this zero temperature approximation, the calculated average values of the Fermi levels (at $V_g = 0$) for graphene on OTMS modified SiO_2 and bare SiO_2 are -61.5 ± 4.1 and -135 ± 3.7 meV, respectively (black line in Figure 4d). However, because all of the GFETs were measured at room temperature ($T \approx 300$ K) and the Fermi–Dirac distribution is highly dependent on temperature, the effect of temperature should be taken into account. Generally, the carrier density of graphene at nonzero temperature T is given by[34]

$$n = \frac{2(k_B T)^2}{\pi(\hbar v_F)^2}\Gamma(2)\left(F_1\left(\frac{E_F}{k_B T}\right) - F_1\left(-\frac{E_F}{k_B T}\right)\right) \tag{6}$$

where k_B is the Boltzmann constant, $\Gamma(s)$ is the Gamma function of order s and $F_s(E_F/k_BT)$ is the s order Fermi-Dirac integrals. Figure 3e displays the relationship between the Fermi energy E_F and the carrier concentration n at different temperatures through numerical methods.[35,36] At room temperature ($T \approx 300$ K, the red dashed line in Figure 3e), due to the broadening of the Fermi-Dirac distribution, the obtained Fermi levels for graphene on OTMS/SiO_2 (blue solid line in Figure 3e) and bare SiO_2 (red

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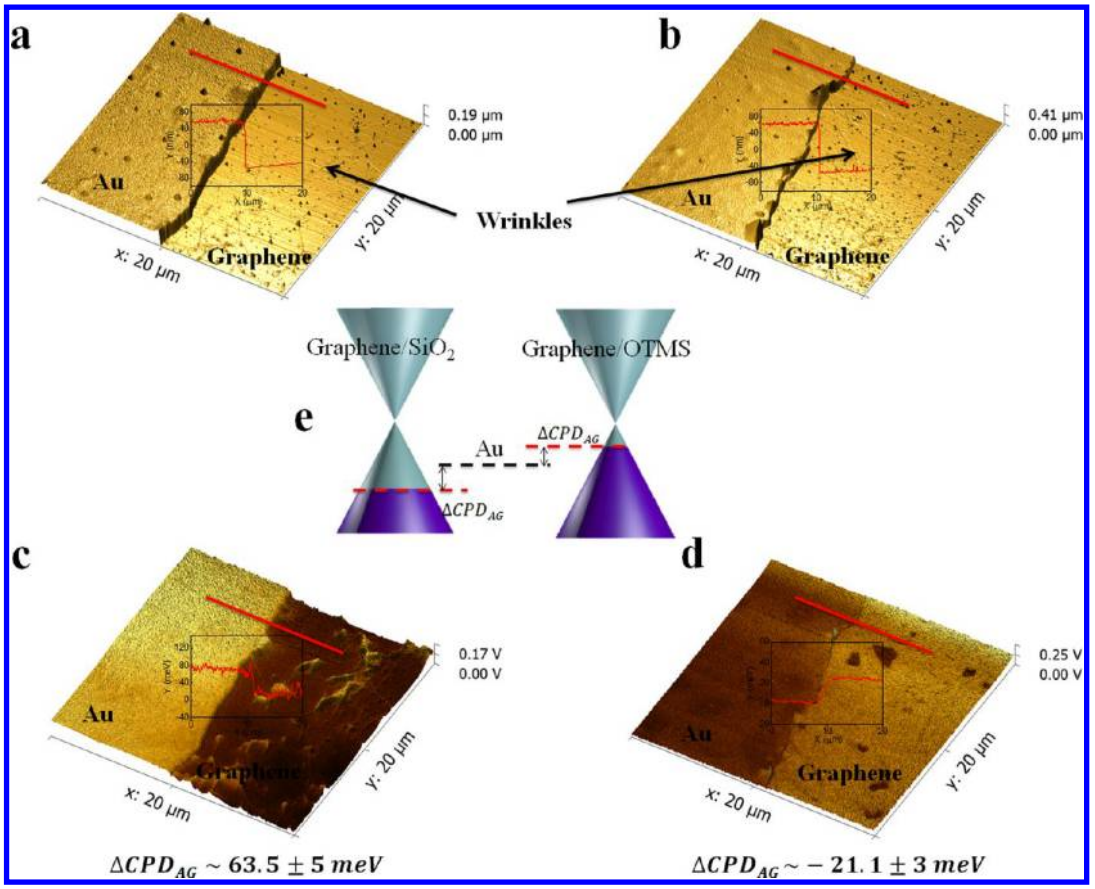

Figure 5. 3D AFM topographic images of graphene sheets on bare SiO_2 (a) and OTMS substrates (b) with Au reference electrodes. Insets in panels a and b: the height profiles of AFM topographic images along the red line. The 3D surface potential maps of Au reference electrodes and graphene sheets on bare SiO_2 (c) and OTMS substrates (d), showing opposite color contrasts. The fluctuation of graphene surface potential may be attributed to wrinkles and cracks that formed during the graphene growth and transfer process. (See more details in Figure S2 and original 2D AFM and KPFM images in Figure S4.) Insets in panels c and d: the profiles of the KPFM images along the red lines. (e) Schematic diagram for the energy level alignment of Au and graphene on SiO_2 and OTMS substrates, respectively.

solid line in Figure 3e) are reduced to -44.9 ± 4.8 and -127.6 ± 3.7 meV on average, respectively (blue line in Figure 4d).

To further quantitatively determine the intrinsic Fermi levels of graphene (at $V_g = 0$) on OTMS/SiO_2 and SiO_2, unpolarized Raman mapping was performed on both graphene/OTMS/SiO_2 and graphene/SiO_2 samples in ambient conditions at room temperature. Since the doping-induced change in Raman spectra is much larger for the *G*-peak (originated from E_{2g} phonon) than for the 2*D*-peak,[25,27] therefore the shift of *G*-peak can be used to estimate the Fermi levels for graphene sheets on different substrates.[27,37,38] The explicit Raman shift of *G*-peak can be described by[27]

$$\frac{1}{\lambda_G} - \frac{1}{\lambda_{G0}} = \frac{A_{uc}D^2}{4\pi^2 c\hbar^2 \omega_G M v_F^2} \left\{ |E_F| + \frac{\hbar\omega_G}{4} \ln\left| \frac{2|E_F| - \hbar\omega_G}{2|E_F| + \hbar\omega_G} \right| \right\} \quad (7)$$

where λ_G and λ_{G0} are the *G* band wavelengths for doped and pristine graphene, respectively, A_{uc} is the area of graphene unit cell, *D* is the electron−phonon coupling strength, *M* is the mass of carbon atom, ω_G is the *G*-mode angular frequency, and *c* is the speed of light. For the right side of eq 7, the second logarithm term is negligible as compared with the first linear term in the high density limit.[27] Recently a simplified linear relationship between the Fermi energy and the shift of *G*-peak has been proposed based on experimental results[37,38]

$$\frac{1}{\lambda_G} - 1580\ \text{cm}^{-1} = 42\ \text{eV}^{-1}\,\text{cm}^{-1} \times |E_F| \quad (8)$$

Therefore, the *G*-peak positions of graphene on both OTMS/SiO_2 and SiO_2 substrates were mapped, and their corresponding spectral distributions are plotted in Figure 4, panels a and b, respectively. The mapping area was 100 μm × 100 μm, which was close to the dimensions of graphene FET. By comparing the colors of Figure 4, panels a and b, the *G*-peak positions of graphene on bare SiO_2/Si are entirely upshifted due to its relatively high doping level. The histograms of *G*-peak positions are plotted in Figure 4c, and the mean values are 1583.02 ± 0.35 and 1585.81 ± 0.35 cm^{-1} for graphene on OTMS/SiO_2 and SiO_2, respectively. The corresponding averaged Fermi levels are -71.9 ± 8.3 and -138 ± 8.3 meV, respectively, which are slightly larger than those obtained by GFEFs (-44.9 ± 4.8 meV with OTMS and -127.6 ± 3.7 meV without OTMS). By considering the fact that all Raman spectra were taken under ambient conditions and, when exposed to atmosphere, graphene samples were likely to be p-type doped by physisorbed O_2 and moisture,[39,40] we conclude that the values obtained through Raman mapping (red line in Figure 4d) are in good agreement with the Fermi levels estimated from the Dirac points of graphene FETs (blue line in Figure 4d).

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As one powerful spatially resolved microscope that can provide insight into the local electrical properties of graphene,[41,42] the KPFM (Kelvin probe force microscope) measurements were performed to further quantitatively estimate the shift of intrinsic Fermi levels of graphene on OTMS/SiO_2 with respect to that on bare SiO_2. Since the accurate work function of the AFM tip may change from sample to sample,[42] Au reference electrodes[43] were fabricated on both graphene/SiO_2 and graphene/OTMS/SiO_2 samples through a fully dried photolithography-free process,[44] as shown Figure 5, panels a and b. The Au layer (~110 nm in thickness) was thick enough to screen the electrical influence of the underlying graphene.[41] The contact potential diffenence (CPD) between the AFM tip and the local surface of Au or graphene can be written as[45]

$$\mathrm{CPD_A} = \phi_{\mathrm{tip}} - \phi_{\mathrm{Au}} \tag{9}$$

$$\mathrm{CPD_G} = \phi_{\mathrm{tip}} - \phi_{\mathrm{graphene}} \tag{10}$$

where ϕ_{tip}, ϕ_{Au}, and ϕ_{graphene} are the work functions of the tip, Au reference electrode, and graphene, respectively. Figure 5, panels c and d show the surface potential images of graphene/SiO_2 and graphene/OTMS/SiO_2, respectively. The CPD maps reveal opposite color contrasts between the Au and the graphene regions, indicating that $\mathrm{CPD_A} > \mathrm{CPD_G}$ for the graphene/SiO_2 sample, whereas $\mathrm{CPD_A} < \mathrm{CPD_G}$ for the graphene/OTMS/SiO_2 sample. By considering that the workfunctions of exposed graphene and gold are in the range of 4.7−5.1[41,46,47] and 4.8 − 4.9 eV,[41,47] respectively, the measured data are in good agreement with the previously reported values. The difference between the intrinsic Fermi levels of graphene sheets on OTMS/SiO_2 and on bare SiO_2 can thus be obtained by determining the $\Delta\mathrm{CPD_{AG}}$ (see Figure 5e), which here is defined as

$$\Delta\mathrm{CPD_{AG}} \equiv \mathrm{CPD_A} - \mathrm{CPD_G} = \phi_{\mathrm{graphene}} - \phi_{\mathrm{Au}} \tag{11}$$

and the resultant mean value is 84.6 ± 8 meV, which is close to those obtained by GFEFs (82.7 ± 8.5 meV) and by Raman mapping (66 ± 16.6 meV).

4. CONCLUSIONS

In summary, we have demonstrated the markedly enhanced performance of coronene-derived large-area graphene transistors by placing octadecyltrimethoxysilane (OTMS) SAMs at the conventional interface of graphene/gate dielectric in GFETs. The improved transport properties in terms of increased carrier mobility (up to 10 700 ± 300 $\mathrm{cm^2\ V^{-1}\ s^{-1}}$), long mean free path, nearly vanished hysteretic behavior, and considerably low intrinsic doping level are mainly attributed to the effective suppression of interfacial charge impurity scattering and remote interfacial phonon (RIP) scattering, less adsorption of dipolar adsorbates, and reduced charge transfer at the interface of graphene and dielectric. The intrinsic Fermi levels of graphene on both OTMS/SiO_2/Si and bare SiO_2/Si substrates have been estimated from the Dirac points of GFETs, which are further confirmed by G-peak Raman mapping and by KPFM. The facile fabrication of graphene devices over a large area provides a unique combination of high performance and low cost for all carbon-based nanoelectronics in future.

■ ASSOCIATED CONTENT

Supporting Information

AFM and KPFM images of transferred graphene on SiO_2/Si substrate, and the discussion of different methods reported in the literature for extracting graphene mobility. This material is available free of charge via the Internet at http://pubs.acs.org.

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Notes

The authors declare no competing financial interest.

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