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Fabrication of Ion-Implanted Si Nanowire p-FETs

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We have successfully demonstrated p-type silicon nanowire field-effect transistors (Si NW p-FETs) prepared using B-ion implantation with a dose of 1×10^{13} ions/cm^2 and an energy of 10 keV. The experimental I_D-V_{DS} characteristics for B-implanted Si NW FETs revealed a clear p-channel FET behavior with a hole mobility of ~6.9 cm^2/(V•s), a hole concentration of $\sim 1.1 \times 10^{19}$ cm^{-3}, and a transconductance of ~29 nS/μm at a V_{DS} of 0.1V. The B-implanted Si NWs were annealed at a temperature of 950 °C for 30 and 60 s. The 2D-ATHENA and ATLAS software were used to accurately simulate the device fabrication process and the electrical performance, respectively.

1. Introduction

At present, nanowire-based electronic devices are fabricated by using semiconductor nanowires (NWs) assembled onto contact platforms for field-effect transistors (FETs).[1–3] Previous studies demonstrated that p−n junction diodes were formed by the assembly of crossed nanowires with n- and p-type NWs even though these devices had a large leakage problem due to inefficient junction contacts between two assembled NWs.[4–7] This problem can be potentially solved by the fabrication of in situ doped superlattice structures and sequentially doped linear p−n junction NWs.[8,9] Gudiksen et al. demonstrated the superlattice structure of GaAs/GaP and in situ doped p−n junction structures (n-Si/p-Si and n-InP/p-InP) designed to minimize the interface junction problem.[8] Furthermore, the performance of the nanowire-based devices is limited by the lack of doping control of semiconductor NWs since the doping is the key process for controlling the conductivity and mobility of Si and other semiconductor crystals. In addition, the doped nanowires with a certain doping concentration (e.g. $>10^{15}$ cm^{-3}) are also required for the nanoscale sensor applications with two-terminal contacts as well as the nanowire-based devices such as Schottky diode, p−n junction diode, bipolar junction transistors (BJT), etc. Previous studies have shown that the doping of the nanoscale Si NWs and other semiconductor NWs was only achieved by in situ doping during nanowire growth.[1,4,5,7–9] However, it was difficult to provide the dopants into the selective area in semiconductor nanowires from the in situ chemical doping. Ion implantation of the selective areas in semiconductor nanowires represents an interesting approach to address the above problems. Recently, Hayden et al. studied ion implantation to fabricate the source and drain in Si NW FETs.[10] A lateral n-channel metal-oxide field-effect transistor (MOSFET) with normally off enhanced mode device performance was successfully fabricated. Similarly, Cohen et al. also fabricated a Si NW FET with epitaxial doped source and drain contacts using selective area ion implantation.[11] Nevertheless, most previous works on ion implantation of the semiconductor NWs have not produced enough information such as the effects on activation annealing and the dopant controllability for channel-doping purpose. In addition, to date there has been no systematic study on electrical characteristics of implanted Si NW FETs.

This paper reports on the fabrication and electrical characteristics of p-type Si NW FET prepared by using boron (B) ion implantation. The ion implantation was performed on randomly dispersed intrinsic Si NWs with a dose of 1×10^{13} ions/cm^2 and an energy of 10 keV. The influence of activation annealing on the electric characteristics of B-implanted Si NW FETs is also discussed. To support the electrical characterization and the effects on activation annealing of B-implanted Si NW FETs, a numerical simulation study was carried out. The 2D-ATHENA and ATLAS software were used to accurately simulate the device fabrication process and the electrical performance, respectively.[12] The aim was to build up a Si NW p-FET with an optimized ion implantation process for doping the channel and not only the source and drain contacts compared to previous studies.[1,4,5,7–11] Fabricating Si NW FETs by using ion implantation is very attractive due to the high doping-value controllability and selective area doping and it can prove the advantages of the method not only for NW FETs but also for NW-based p−n junctions, bipolar junction transistors (BJTs), and generally bipolar devices.

2. Experimental Details

The Si NWs used in these studies were synthesized by a vapor−liquid−solid method in a chemical vapor deposition (CVD) quartz-tube furnace (2 in.) with $SiCl_4$ as a silicon precursor and gold as the catalyst.[13,14] The Si NWs were not intentionally doped. The NWs had diameters in the range of 70−150 nm and lengths of 3−10 μm. The p-FETs with Si NWs were fabricated by using B-implanted Si NWs and conventional e-beam lithography (EBL). Parts a−e of Figure 1 show schematic diagrams of the fabrication processes (Steps a−e) for the B-implanted Si NW FETs. As shown in Figure 1a, a

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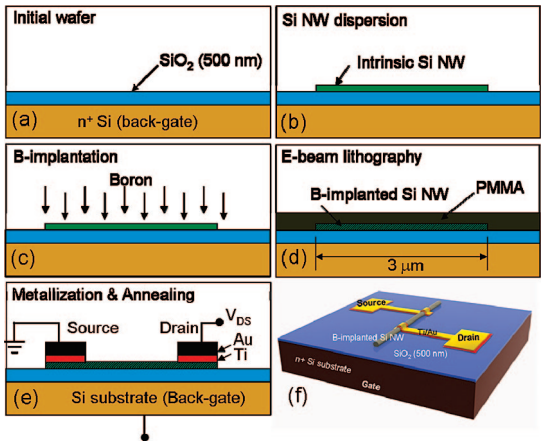

Figure 1. Schematic diagrams showing the cross-sectional view of the fabrication processes (Steps a−e) for the B-implanted Si nanowire (NW) field-effect transistor (FET) with three-probe scheme. (a) Thermal oxidation of the initial Si wafer. (b) Si nanowire dispersion on a Si wafer. (c) Ion-implantation with B-ions and activation annealing at 950 °C for 30−60 s. (d) Conventional e-beam lithography. (e) Source and drain metallization and lift-off. (f) A schematic of the B-implanted Si NW FET.

500 nm thick Si oxide layer was used as an insulating gate oxide layer on heavily doped n-type Si substrates, normally used as a back-gate in three-probe FET structures. Then, the Si NW suspension (Figure 1b) was dispersed on the patterned SiO_2/Si substrates (0.5 × 0.5 cm^2). Boron ion implantation (dose of 1 × 10^{13} ions/cm^2 and energy of 10 keV) was performed on the Si NWs, which were positioned on the Si substrates (Figure 1c). Postimplantation annealing was performed at a temperature of 950 °C for 30 and 60 s by rapid thermal annealing (RTA). Source and drain contacts (Ti/Au = 50/150 nm) were defined by conventional electron-beam lithography (EBL) and a lift-off process (Figure 1d−e) after etching the native oxide by dipping in diluted hydrofluoric (BHF) acid. To get low resistivity ohmic contacts to the Si NWs, the B-implanted Si NW FETs were annealed again at a temperature of 400 °C in a N_2 environment prior to the electric transport measurement. Figure 1f shows a schematic of B-implanted Si NW FET. Figure 2a shows the simulated B-dopant depth profile, which is generated by a SRIM simulation, for implanted B in Si NWs with a dose of 1 × 10^{13} ions/cm^2 and an energy of 10 keV.[15]We prepared two sets of samples called A (A1, A2, A3, A4) and B (B1, B2, B3) series. All samples (A and B series) were performed by ion implantation with a dose of 1 × 10^{13} ions/cm^2 and energy of 10 keV at room temperature. To illustrate the distribution and to study the effect on activation annealing, a repeatability test on FET device performance was undertaken. The first set (4 samples) and the second set (3 samples) were annealed at a temperature of 950 °C for 30 and 60 s, respectively, using rapid thermal annealing (RTA). The p-FETs performed current−voltage measurements at room temperature with use of a HP 4156C semiconductor parameter analyzer in the range of 20 fA−100 mA on a cascade probe station.

3. Results and Discussion

As shown in Figure 2a, the SRIM simulation suggested that the implantation corresponded to a depth of ∼100 nm, which was the same as the size of the Si NW that was utilized for the ion implantation, and a hole carrier concentration of >2 × 10^{18} cm^{-3} near the surface of Si NW. Figure 2b shows the field-emission scanning electron microscope (FE-SEM) image of the

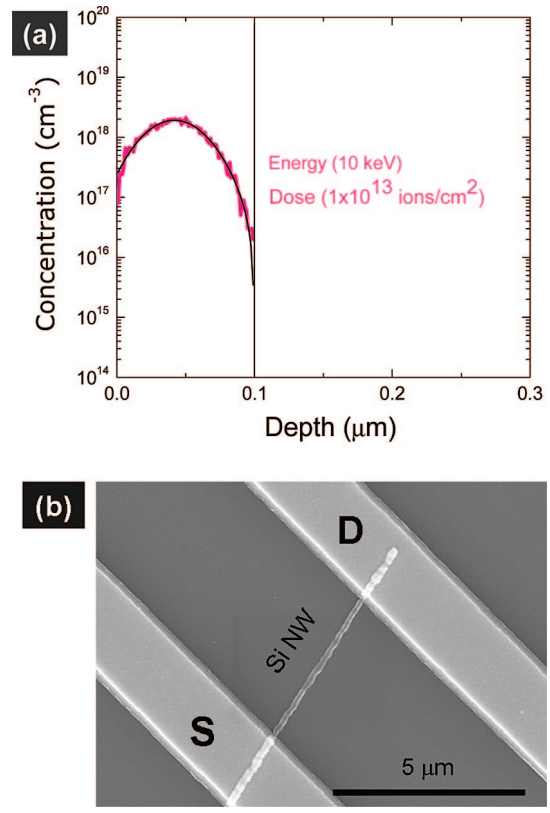

Figure 2. (a) Simulated depth profile of B ions in the Si nanowire. The dose and energy for ion implantation were 1 × 10^{13} ions/cm^2 and 10 keV, respectively. The simulation was performed by a SRIM simulator.[13] (b) A field-emission scanning electron microscope (FE-SEM) image of B-implanted Si NW FET. The activation annealing was performed at a temperature of 950 °C for 60 s in an N_2 environment.

B-implanted Si NW p-FET. The intrinsic Si NW FETs were also fabricated without an implantation step allowing for a comparison of the device characteristics with those of the B-implanted Si NW FETs. Unfortunately, no FET characteristics were obtained, indicating that the intrinsic NW itself had an extremely high resistance (>1 TΩ), as well as a high contact resistance between the metal contacts (source or drain electrode) and intrinsic Si NW. On the other hand, the total resistance of the B-implanted Si NWs was achieved at 200−700 kΩ with lengths of 2−10 μm. First of all, we present the electrical characteristics of B-implanted Si NW FETs after activation annealing at 950 °C for 30 s compared with the results of Si NW FETs annealed for 60 s at the same temperature. Panels a and b of Figure 3 show the drain current versus the source-drain voltage (I_D−V_{DS}) curves of Si NW p-FET annealed at a temperature of 950 °C for 30 and 60 s at different V_G, respectively. The insets of panels a and b of Figure 3 show the drain current versus the gate voltage (I_D−V_G) characteristics of Si NW p-FET annealing at a temperature of 950 °C for 30 and 60 s at different V_{DS}, respectively. A FET channel modulation was achieved by applying a bias to the Si substrate that was used as a large-area gate in the FET structure as shown in Figure 1e. Moreover, the fabricated Si NW FETs show clear p-type semiconductor behavior from the gate transport characteristics in all cases. As shown in Figure 3a,b, the I−V characteristics also suggested that the Si NW FETs annealed for 30 s show peak transconductance (g_m) of 3.5 ± 1.2 nS at a V_{DS} of 0.1−0.2 V and in the range of V_G = −40 to +40 V while Si NW FET annealed for 60 s has a relatively weak gate effect with a g_m of 2.9 ± 0.7 nS (V_{DS} = 1 V and V_G = −40 to 40 V). Assuming

the channel width equals the diameter of the nanowire (~100 nm), the normalized transconductance for the Si NW FETs annealed for 30 and 60 s was estimated to be ~35 and ~29 nS/μm, respectively. These values are significantly lower than those of the state-of-the-art MOSFET devices (~0.6 mS/μm). It can be understandable in FET devices with relatively high hole concentration in the channel. Moreover, the Si NW p-FETs annealed for 30−60 s have an extremely low I_{on}/I_{off} ratio of ~1.2−2.5 owing to the high hole concentration as expected by the SRIM simulation. The detailed information from the electrical measurements of B-implanted Si NW p-FETs is summarized in Table 1. Furthermore, the hole mobility (μ) can be estimated by using[2,3]

$$\frac{dI_D}{dV_G} = \frac{\mu C}{L^2} \quad (1)$$

Here L is the length of the active nanowire channel and C is the capacitance of the Si NW. The capacitance is given by

$$C = \frac{2\pi\epsilon_0\epsilon L}{\ln\left(\frac{2h}{r}\right)} \quad (2)$$

Here, h is the dielectric thickness of SiO_2 (500 nm) and r (~50 nm) is the radius of the Si NW with a quasi-ircular cross-section approximation. The hole carrier concentration was estimated with the relationship $I = pq\mu EA$, where p is the hole carrier concentration, E is the electric field, μ is the hole mobility (which were obtained by eqs 1 and 2), and A is the area of the Si NW. The estimated hole carrier density and the field-effect carrier mobility of B-implanted Si NW FETs annealed for 30 s with a dose of 1×10^{13} ions/cm^2 were determined to be ~$6.3 \times 10^{17} \pm 3.4 \times 10^{17}$ cm^{-3} and ~ 11.8 ± 10.3 cm^2/(V·s), respectively (see Table 1). The estimated hole concentration for Si NW FET (annealed 30 s) is lower than the values expected by the SRIM simulation as shown in Figure 2a. We could expect that the duration of activation annealing is not enough to completely activate the implanted B-ions in Si NWs. Thus, it is important to explore the effects of the activation annealing. To this end, we have carried out the activation annealing studies on Si NW p-FETs performance with different annealing time from 30 to 60 s. To illustrate the distribution and repeatability on FET device performance, we fabricated two sets of samples (7 samples in total; see Table 1 and the Experimental Section). Panels a and b if Figure 4 show the distribution of the hole mobility and hole carrier concentration of the B-implanted Si NWs FETs annealed for 30 and 60 s. The p and μ changed to ~$1.1 \times 10^{19} \pm 1.0 \times 10^{18}$ cm^{-3} and ~6.9 ± 2.7 cm^2/(V·s), respectively, after increasing the annealing time from 30 to 60 s (see table 1 for more detailed information of the calculation). The SRIM simulation suggested that the hole carrier concentration (p) of the Si NWs with a dose of 1×10^{13} ions/cm^2 corresponded to ~2×10^{18} cm^{-3} at the Si NW surface. It is worth noting that our experimental results on the hole concentration were slightly higher than the values expected by the SRIM simulation. Additional studies are required to further understand this phenomenon.

To further support the previous conclusion on the activation of the hole carriers in the Si NWs, a 2D numerical simulation was carried out by using the commercial ATHENA simulator (SILVACO Inc.).[12] Panels a and b of Figure 5 show the simulated hole concentration profile (ca. >2×10^{18} cm^{-3}) of the hole carriers along the nanowire for various annealing times (30 and 60 s). The figure shows that the sample annealed at a temperature of 950 °C for 30 s has a small peak of concentration at the middle of the nanowire. After 30 s more annealing, the profile is more uniform along the nanowire. These results confirm our experimental results, indicating 60 s RTA are enough for the dopants activation in Si NWs. Apart from the exploration of the carrier concentration dependence on annealing time, we proceed to the device electrical behavior simulation using a ATLAS simulator.[12] Recently, Hang et al. showed that ATLAS simulator is able to produce a rough estimation of the nanowire/interface quality (estimation of fixed charge density (Q_f) and interface trap density (Q_{it}) values) and carriers a mobility value by correctly fitting the experimental with simulated $I-V$ curves.[16] Figure 5c shows the simulated I_D-V_{DS} and I_D-V_G characteristics of the B-implanted Si NW FETs with a dose of 1×10^{13} ions/cm^2. In the simulation, a diameter of 100 nm and a channel length of 2 μm were used for the calculations. An excellent agreement between experiment and simulation is obtained for (a) maximum body hole mobility and surface mobility equal to ~400 and ~22 cm^2/(V·s), respectively, (b) density of fixed charge $Q_f \sim 3 \times 10^{10}$ cm^{-2}, and (c) density of interface trap $Q_{it} \approx 3 \times 10^{11}$ eV^{-1} cm^{-2}. According to the above mobility parameters, ATLAS calculates a total mobility value equal to ~60 cm^2/(V·s). The parameters maximum body hole mobility and surface mobility are specific to the model of mobility in MOSFETs used by SILVACO.[12] In our case, these

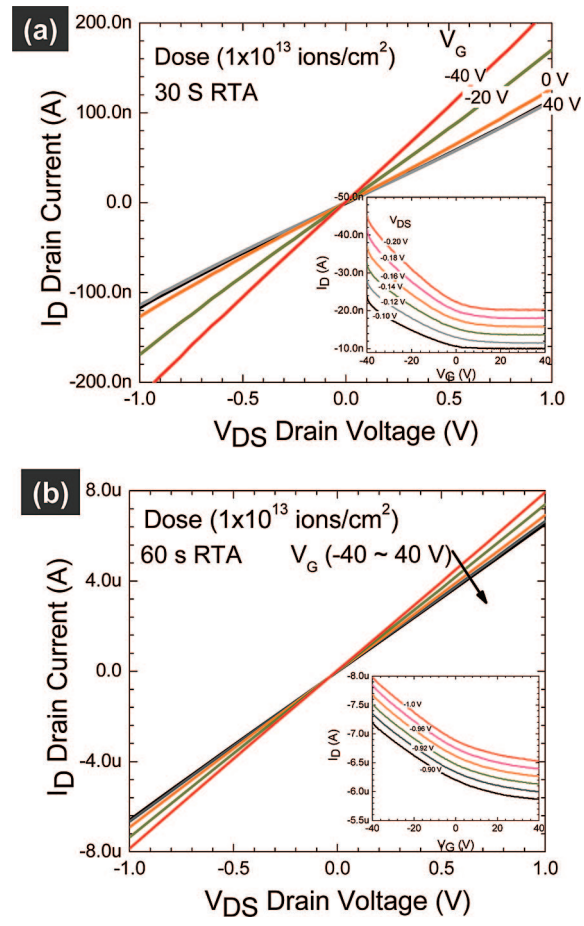

Figure 3. (a) I_D-V_{DS} characteristic curves as a function of V_G (−40, −20, 0, 20, and 40 V) for B-implanted Si NW FET annealed at 950 °C for 30 s. The inset of part a shows the I_D-V_G curves as a function of V_{DS} (−0.10, −0.12, −0.14, −0.16, −0.18, and −0.20 V) for B-implanted Si NW FETs annealed for 30 s (sample A2). (b) I_D-V_{DS} curves at different V_G (−40, −20, 0, 20, and 40 V) for B-implanted Si NW FET annealed at 950 °C for 60 s. The inset of part b shows the I_D-V_G curves as a function of V_{DS} (−0.90, −0.92, −0.94, −0.96, −0.98, and −1.0 V) for sample B2. All samples were prepared by ion implantation with a dose of 1×10^{13} ions/cm^2 and 10 keV.

TABLE 1: Detailed Electrical Information from the Calculations for B-Implanted Si Nanowire (NW) Field-Effect Transistors (FETs)

				transconductance			
dose (ions/cm^2)	samples[a]	channel length (μm)	capacitance C(F)	g_m (nS)	V_{DS} (V)	hole mobility μ (cm^2/(V•s))	hole concn p (cm^{-3})
1×10^{13}	A1	5.3	3.8×10^{-16}	4.8	0.2	18	1.2×10^{18}
	A2	6.3	4.6×10^{-16}	2.6	0.1	23	5.2×10^{17}
	A3	7.0	5.1×10^{-16}	4.9	3	1.6	2.9×10^{17}
	A4	2.2	1.6×10^{-16}	3.1	0.2	4.6	4.9×10^{17}
	B1	1.1	8.0×10^{-17}	3.2	1	4.9	1.1×10^{19}
	B2	2.2	1.6×10^{-16}	3.3	1	10	1.2×10^{19}
	B3	2.0	1.5×10^{-16}	2.1	1	5.7	1.0×10^{19}

[a] Samples A1, A2, A3, and A4 were annealed at 950 °C for 30 s. Samples B1, B2, and B3 were annealed at 950 °C for 60 s.

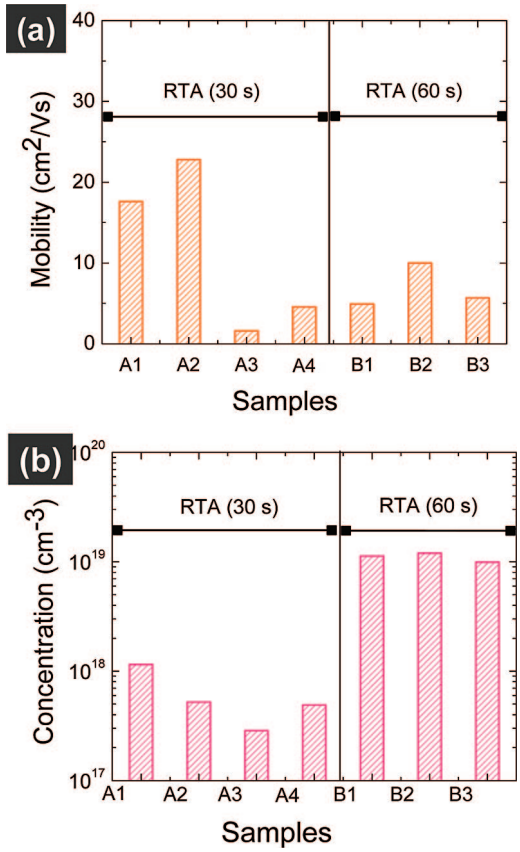

Figure 4. The distribution of the estimated hole mobility (a) and hole carrier concentration (b) of B-implanted Si NW FETs annealed at 950 °C for 30 and 60 s (samples A and B series).

values are lower than the corresponding ones used for fitting bulk silicon MOSFETs. The lack of bibliography data for the mobility value in Si based NW FETs does not allow us, for the time being, to attribute this reduction to a physical effect like increased surface to volume ratio, increased surface roughness, high interface traps, etc.

4. Conclusion

In summary, we have successfully fabricated p-type silicon nanowire field-effect transistors (Si NW FETs) prepared using B-ion implantation with a dose of 1×10^{13} ions/cm^2 and energy of 10 keV. The experimental I_D-V_{DS} characteristics for B-implanted Si NW FETs with a dose of 1×10^{13} ions/cm^2 after 950 °C annealing for 60 s exhibited clear p-channel FET behavior with a hole mobility of ~6.9 cm^2/(V•s), a hole concentration of ~1.1×10^{19} cm^{-3}, and a transconductance of ~29 nS/μm at a V_{DS} of 0.1V. The experimental current−voltage

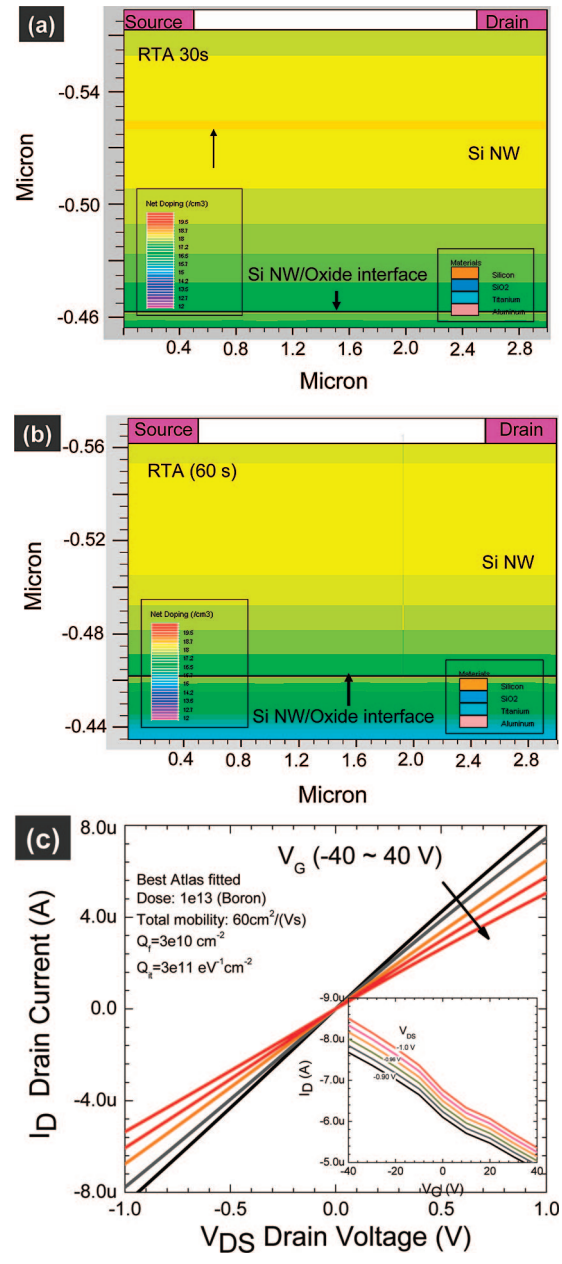

Figure 5. The simulated hole concentration profile along nanowires for B-implanted Si NWs annealed at a temperature of 950 °C for (a) 30 and (b) 60 s. The simulation was performed by a 2D Athena simulator. (c) The simulated I_D-V_{DS} characteristic curve as a function of V_G of −40, −20, −10, 0, 20, 10 and 40 V for B-implanted Si NW p-FET using 2D Athena and Atlas simulators. The inset of part c shows the simulated I_D-V_G curves of B-implanted Si NW FETs at the different V_{DS} (−0.9 to −1.0 V).

characteristics of B-implanted Si nanowire FET corresponded well with the numerical simulation results (2D ATHENA and ATLAS simulation) and a rough estimation of NW/oxide interface quality was presented. A study on the optimized implantation process in Si NW FETs is being initiated for fully depleted and high I_{on}/I_{off} ratio FETs for the high-performance bipolar device applications. The results reported here should have significant implication in fabricating and designing highly efficient future nanoscale devices such as Junction FET (JFET), BJT, and p−n junction diodes.

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