Synthesis of High Quality n-type CdSe Nanobelts and Their Applications in Nanodevices

ARTICLE *in* THE JOURNAL OF PHYSICAL CHEMISTRY C · AUGUST 2009

Impact Factor: 4.77 · DOI: 10.1021/jp9031139

7 AUTHORS, INCLUDING:

Tuo Sun
Peking University
5 PUBLICATIONS **122** CITATIONS
SEE PROFILE

Yu Ye
University of California, Berkeley
41 PUBLICATIONS **862** CITATIONS
SEE PROFILE

Synthesis of High Quality *n*-type CdSe Nanobelts and Their Applications in Nanodevices

Cui Liu, Peicai Wu, Tuo Sun, Lun Dai,* Yu Ye, Renmin Ma, and Guogang Qin*

State Key Laboratory for Mesoscopic Physics and Department of Physics, Peking University, Beijing 100871, People's Republic of China

Received: April 2, 2009; Revised Manuscript Received: May 24, 2009

Cd-enriched ambient, high quality *n*-type CdSe nanobelts (NBs) with various electron concentrations (from $\sim 10^{16}$ to 10^{18} cm^{-3}), which can meet different device requirements, were synthesized via the chemical vapor deposition (CVD) method. The electron mobilities are much higher than those reported previously for CdSe one-dimensional (1D) nanostructures. High performance single CdSe NB field effect transistors (NB-FETs) and CdSe NB/p^+-Si heterojunction light emitting diodes (HLEDs) are fabricated and studied. The NB-FETs have the best performance among the reported CdSe 1D nano-FETs with an on−off ratio of $\sim 3 \times 10^8$, a threshold voltage of ~ -4.1 V, and a maximum transconductance of ~ 1.49 μS. The room temperature electroluminescence spectra of the HLEDs consist of only an intense CdSe band-edge emission peak (~708 nm) with a full width at half-maximum of about 29 nm.

Introduction

Semiconductor one-dimensional (1D) nanostructures are good candidates for the building blocks of functional nanodevices such as waveguides,[1−3] photoconductive switches,[4] sensors,[5] acoustic resonators,[6] field effect transistors (FETs),[7,8] and light-emitting diodes (LEDs).[9−11] CdSe, as an important II−VI semiconductor material, has unique physical properties such as the direct band gap of 1.74 eV and the electron mobility of 450−900 $cm^2/V \cdot s$.[12−18] However, the unintentionally doped CdSe nanostructures usually have high resistivity, which limits their performance both in electronic and optoelectronic devices.[12] Therefore, finding effective ways to control doping in CdSe nanostructures is very urgent in exploring their application in nanodevices. So far, the reported *n*-type CdSe 1D nanostructures were usually synthesized with indium (In) as the dopant.[12,13] However, we find that the qualities of the In doped *n*-CdSe nanostructures are not so good, e.g., the morphology, electrical, and optical properties of the CdSe nanostructures will be deteriorated by introducing the In atoms, and hence, the performances of the devices are limited. In this paper, we report the synthesis of high quality *n*-type CdSe nanobelts (NBs) via a Cd-enriched chemical vapor deposition (CVD) growth process. Single CdSe NB-FETs and CdSe NB/p^+-Si heterojunction LEDs (HLEDs) have been fabricated and studied. As far as we know, among the CdSe nano-FETs reported so far, the as-fabricated FETs have several best parameters. It is worth noting that the unintentionally doped CdSe NBs are of high resistivity, neither clear field effects nor electroluminescence (EL) can be obtained from them.

Experimental Section

The *n*-type CdSe NBs were synthesized via the CVD method in a tube furnace. CdSe (99.99%) powders and a Cd (99.99%) particle were used as the source, and pieces of Si wafer covered with 10 nm-thick thermally evaporated Au catalysts were used as the substrates. A quartz boat loaded with CdSe, Cd, and Si substrates in sequence was inserted into a quartz tube placed in the tube furnace, with CdSe at the upstream side of the Ar gas flow. The distance between CdSe and Cd was about 2−10 cm, and those between CdSe and Si substrates were 10−15 cm. Before heating, the quartz tube was pumped by a rotation pump for 20 min to remove the O_2 inside. After that, the furnace was rapidly heated to 700 °C. During the growth process, high-purity Ar flow-rate kept at a constant of 100 sccm with the quartz tube being kept pumped. The local temperatures for CdSe, Cd, and Si substrates were about 700, 600−700, and 500−600 °C, respectively. The synthesis duration was about 0.5 h. After the synthesis process, the products on the substrates were characterized by a field emission scanning electron microscope (FESEM; Amray 1910 FE) and a high-resolution transmission electron microscope (HRTEM; Tecnai F30) equipped with an energy-dispersive X-ray (EDX) spectroscope. The single CdSe NB-FETs were fabricated as follows: First, the CdSe NB suspension was dropped on oxidized p^+-Si substrates (the SiO_2 layer was about 400 nm). Then, UV lithography, thermal evaporation, and lift-off processes were used to fabricate the source and drain In/Au (10/100 nm) ohmic contact electrodes on a single CdSe NB. p^+-Si substrates were used as the back gate. The single *n*-CdSe NB/p^+-Si HLEDs were fabricated as follows: First, p^+-Si pads (200 μm long, 50 μm wide) were patterned by UV lithography followed by inductively coupled plasma etching on silicon-on-insulator (SOI) substrates with 100 nm thick p^+-Si and a 380 nm thick box. Then, the natural oxide layer on the p^+-Si surface was etched by dilute HF solution. Finally, CdSe NBs were assembled across the edges of the Si pads to form nanoheterojunctions. In/Au ohmic contact electrodes to CdSe NBs were defined the same way as that mentioned in the NB-FET fabrication. The electrical transport measurements on the CdSe NB-FETs and the HLEDs were conducted with a semiconductor characterization system (Keithley 4200). The photoluminescence (PL) and electroluminescence (EL) spectra of single CdSe NBs and HLEDs were measured with a micro-zone confocal Raman spectroscope (HORIBA Jobin Yvon, LabRam HR 800) equipped with a color charge-coupled device (CCD). For PL measurements, the 325 nm line of a He−Cd laser (Kimmon IK3301R-G) was used as the excitation source.

* Corresponding authors. E-mail: qingg@pku.edu.cn (G.Q.); lundai@pku.edu.cn (L.D.).

10.1021/jp9031139 CCC: $40.75
Published on Web 07/01/2009

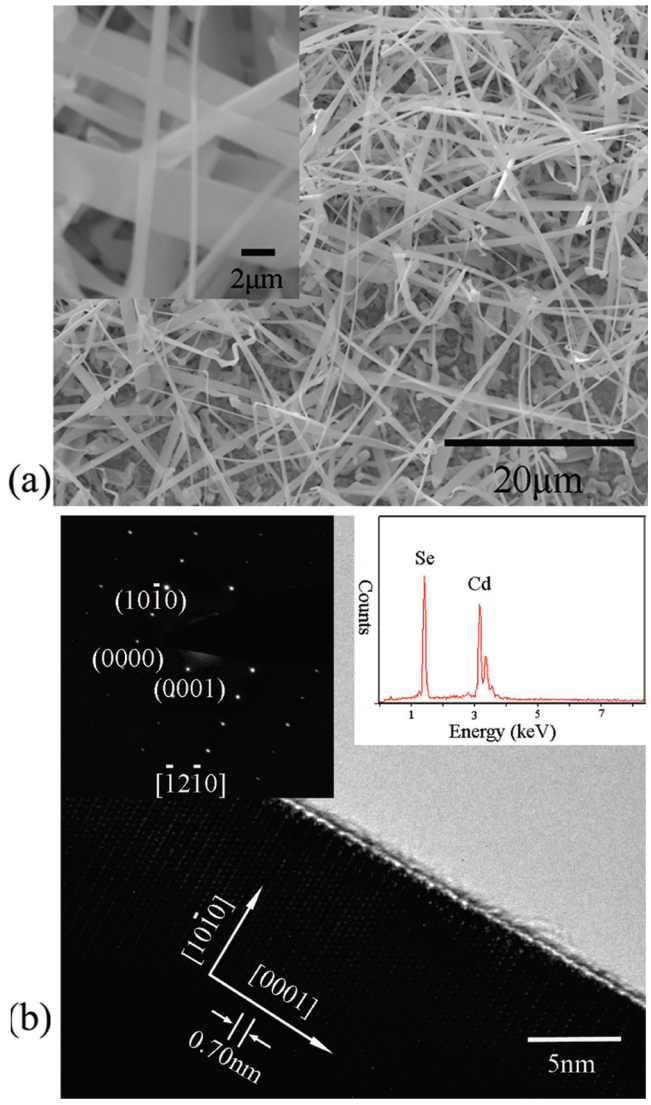

Figure 1. Typical morphology of the as-synthesized *n*-CdSe NBs. (a) A FESEM image of CdSe NBs. The inset is a magnified FESEM image. (b) HRTEM image of a CdSe NB. The inset at the upper-left corner is the corresponding SAED pattern. The inset at the upper-right corner is the EDX data of the CdSe NB.

Results and Discussion

Figure 1a shows a typical FESEM image of the CdSe NBs. The inset is a magnified FESEM image. Each CdSe NB has smooth surface and uniform width along the growth direction. The NBs are usually several hundred micrometers in length, submicrometer to several micrometers in width, and 50−200 nm in thickness.

Figure 1b shows an HRTEM image of a CdSe NB. The crystal planes with the spacing distances of about 0.70 and 0.38 nm can be seen along and perpendicular to the growth direction, respectively. According to JCPDS card No. 02-0330, these planes can be indexed as the hexagonal CdSe (0001) and (10$\bar{1}$0) planes. The inset at the upper-left corner of Figure 1b is the corresponding selected area electron diffraction (SAED) pattern recorded along the [1$\bar{2}$10] zone axis. The HRTEM image together with the SAED pattern reveals that the CdSe NB is a single crystal with the hexagonal structure, and its growth direction is [0001]. The inset at the upper-right corner of Figure 1b is the EDX spectrum taken from the CdSe NB. It consists of only Cd and Se signals with an atomic ratio ∼51:49.

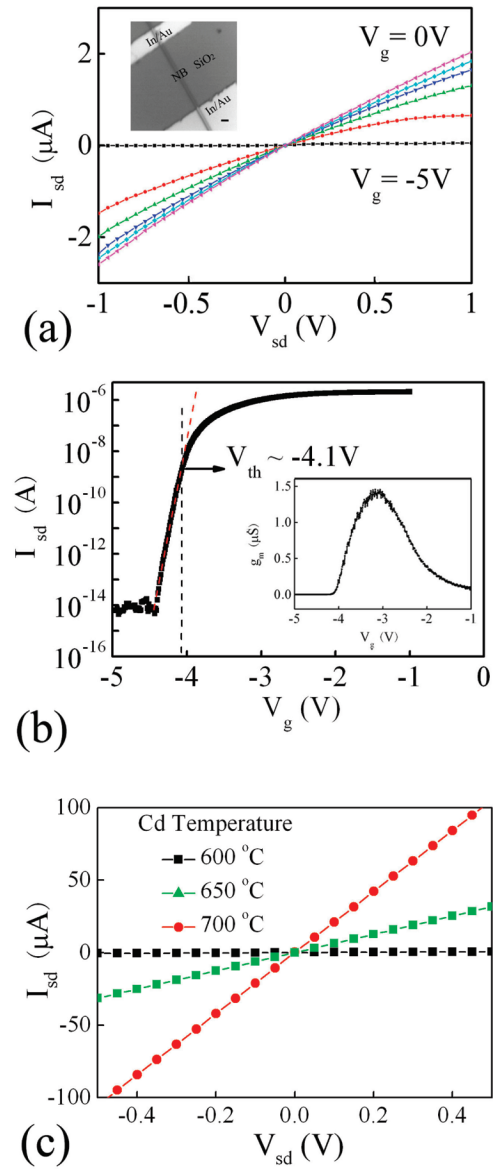

Figure 2. Performance of single *n*-CdSe NB-FETs. (a) Room temperature $I_{sd}-V_{sd}$ curves of a typical single *n*-CdSe NB-FET based on the CdSe NB synthesized under a Cd temperature of ∼600 °C with gate voltages changing from −5 to 0 V incremented by 1 V. The inset is an FESEM image of the device. The scale bar is 2 μm. (b) Log $I_{sd}-V_g$ curve of the NB-FET shown in part a at V_{sd} = 1 V. The inset is a g_m-V_g curve of the FET at V_{sd} = 1 V. (c) $I_{sd}-V_{sd}$ (with V_g suspended) of three FETs made on CdSe NBs synthesized under Cd temperatures of ∼600 (black), 650 (green), and 700 (red) °C, respectively.

So far, the only effective way to evaluate the doping level in nanowires or nanobelts is fabricating and measuring the nano-FETs based on them. Figure 2a shows the source-drain current (I_{sd}) versus source-drain voltage (V_{sd}) curves at various gate biases (V_g) for a typical single CdSe NB-FET. The CdSe NBs were synthesized under a Cd temperature of ∼600 °C. For a given V_{sd}, I_{sd} increases when V_g changes from −5 to 0 V. This indicates that the CdSe NB is of *n*-type. The inset is an FESEM image of the single CdSe NB-FET. The width *w* and thickness *T* of the CdSe NB are about 1 μm and 200 nm, respectively. The channel length *L* of the NB-FET is about 20 μm. From the $I_{sd}-V_{sd}$ curve measured at V_g = 0 and the dimension of the NB, we can obtain the resistivity (ρ) of the NB to be about 0.5 Ω·cm.

Figure 2b shows the $I_{sd}-V_g$ curve on an exponential scale measured at $V_{sd} = 1$ V. An on−off ratio of $\sim 3 \times 10^8$ is obtained when V_g changes from −2 V (on-state) to −5 V (off-state). As far as we know, this value is much higher than those reported previously for CdSe nano-FETs. The threshold voltage (V_{th}) obtained at the point deviated from the linear region of the curve is ∼−4.1 V. The inset shows the transconductance ($g_m = dI_{sd}/dV_g$) versus V_g curve. The maximum transconductance obtained is ∼1.49 μS. The subthreshold swing is obtained to be about 65 mV/dec from the linear region of the $I_{sd}-V_g$ curve shown in Figure 2b, which is determined by the equation $S = \ln 10[dV_g/d(\ln I_{sd})]$.[9] This value is close to the theoretical limit $S = (K_BT/q)\ln(10) \equiv 60$ mV/dec.[9,19] S is a key parameter for transistors, and transistors with smaller S values tend to be switched on−off with faster speed. The electron concentration (n) is estimated to be about 1.2×10^{16} cm^{-3} from the equation $n = CV_{th}/(ewTL)$,[19,20] where C is the gate capacitance. C is given by $C = \varepsilon\varepsilon_0 Lw/h$,[19,20] where ε (∼3.9) is the relative dielectric constant of SiO_2, h (∼400 nm) is the thickness of the silicon oxide layer. The mobility (μ_e) of the NB can be estimated to be about 800 cm^2/V·s with the equation $\mu_e = g_m(L^2/CV_{sd})$.[19,20] The electron concentration can also be obtained from the equation $n = 1/(\rho e \mu_e)$ to be about 1.5×10^{16} cm^{-3}, which is close to the value of 1.2×10^{16} cm^{-3} obtained above. It is worth noting that the unintentionally doped CdSe NBs are of high resistivity, no clear field effect can be observed from the FETs made on them. From the above EDX data, we could infer qualitatively that in our case the atomic ratio of Cd and Se is bigger than 1. There are several reports previously in the literature that Se vacancies serve as shallow donors in CdSe.[12,13] We think the Se vacancies (created by the Cd-enriched ambient during the synthesis process) may also act as the shallow donors in our case.

Furthermore, we can control the electron concentrations in CdSe NBs in a range of $10^{16}-10^{18}$ cm^{-3} by controlling the local temperatures of Cd particles in a range of 600−700 °C. Figure 2c shows the $I_{sd}-V_{sd}$ curves (with V_g suspended) of three FETs made on CdSe NBs synthesized under Cd temperatures of ∼600, 650, and 700 °C, respectively. The dimensions of the NBs are similar. We can see that the channel conductance increases with Cd temperature rising. The result shows that the electron concentrations inside the CdSe NB increase when the Cd vapor pressure increases.

In order to obtain EL at lower forward biases, we chose the CdSe NBs with higher electron concentrations (∼10^{18} cm^{-3}) in fabricating single n-CdSe NB/p^+-Si HLEDs. The $I-V$ curve of an HLED is shown in Figure 3a. We can see a good rectification characteristic. The turn-on voltage is around 1.5 V. The FESEM image of the HLED is shown in the inset. Figure 3b shows the room temperature EL spectra at various forward biases. The room temperature PL spectrum of the single CdSe NB is shown in the inset for comparison. The detected EL spectra have peaks around 708 nm with a full width at half-maximum (fwhm) of about 29 nm and are free from deep-level defect emissions, coinciding with the PL spectrum of the CdSe NB. Therefore, we think the 708 nm peak results from the band-edge emission from CdSe NB. It is worth noting that in our case the native oxide layer (SiO_{2-x}) on the Si surface had been etched by dilute HF solution before fabricating the HLEDs, which will greatly reduce the Si/CdSe interface emission around 700 nm.[21,22]

Conclusion

In conclusion, high quality n-type CdSe NBs with various electron concentrations (∼$10^{16}-10^{18}$ cm^{-3}) were synthesized via a CVD method in a Cd-enriched atmosphere. Introducing Cd instead of In during the growth helps to improve the morphology and electronic and optoelectronic qualities of CdSe NBs. High performance single n-CdSe NB-FETs and n-CdSe NB/p^+-Si HLEDs are fabricated. The NB-FETs have the best performance among the reported CdSe 1D nano-FETs with an on−off ratio of $\sim 3 \times 10^8$, a threshold voltage of ∼−4.1 V, and a maximum transconductance of ∼1.49 μS. The room temperature EL spectra of the HLED consist of only an intense band-edge emission peak (∼708 nm) of CdSe with the a fwhm of about 29 nm. Our results predict a bright prospect for the CdSe NBs in the nanodevice applications.

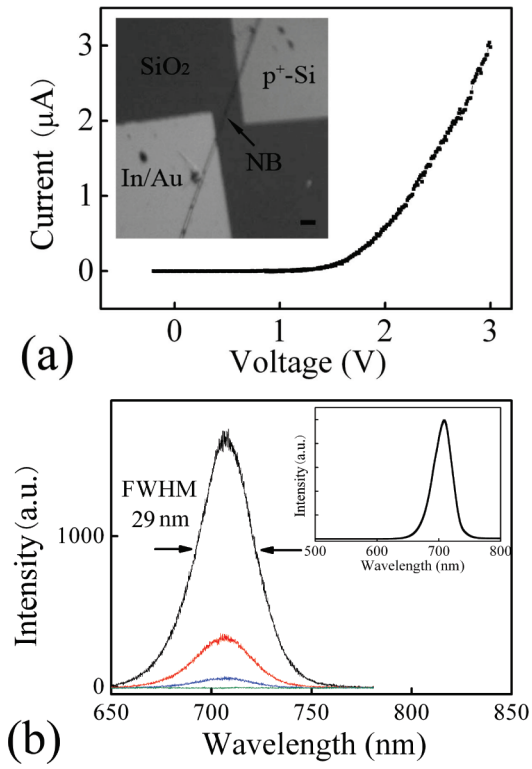

Figure 3. Characteristics of a single n-CdSe NB/p^+-Si HLED. (a) $I-V$ characteristic. The inset is an FESEM image. The scale bar is 5 μm. (b) Room temperature EL spectra of the HLED under forward biases from 2 to 5 V incremented by 1 V. The inset is the room temperature PL spectrum of the single CdSe NB.

Acknowledgment. This work was supported by the National Natural Science Foundation of China under grant nos. 60576037, 10774007, 10574008, and 50732001 and by the National Basic Research Program of China (Nos. 2006CB921607, 2007CB613402).

References and Notes

(1) Pan, Z. W.; Dai, Z. R.; Wang, Z. L. *Science* **2001**, *291*, 1947.
(2) Law, M.; Sirbuly, D. J.; Johnson, J. C.; Goldberger, J.; Saykally, R. J.; Yang, P. *Science* **2004**, *305*, 1269.
(3) Pan, A.; Liu, D.; Liu, R.; Wang, F.; Zhu, X.; Zou, B. *Small* **2005**, *1*, 980.
(4) Gao, T.; Li, Q. H.; Wang, T. H. *Appl. Phys. Lett.* **2005**, *86*, 173105.
(5) Ying, P.; Ni, Z.; Xiu, W.; Jia, L.; Luo, Y. *Chin. Phys. Lett.* **2006**, *23*, 1026.
(6) Buchine, B. A.; Hughes, W. L.; Degertekin, F. L.; Wang, Z. L. *Nano Lett.* **2006**, *6*, 1155.
(7) Duan, X.; Niu, C.; Sahi, V.; Chen, J.; Parce, J. W.; Empedocles, S.; Goldman, J. L. *Nature London* **2003**, *425*, 274.
(8) Liu, C.; Dai, L.; You, L. P.; Xu, W. J.; Ma, R. M.; Yang, W. Q.; Zhang, Y. F.; Qin, G. G. *J. Mater. Chem.* **2008**, *18*, 3912–3914.
(9) Ma, R. M.; Dai, L.; Huo, H. B.; Yang, W. Q.; Qin, G. G. *Appl. Phys. Lett.* **2006**, *89*, 203120.

(10) Liu, C.; Dai, L.; You, L. P.; Xu, W. J.; Qin, G. G. *Nanotechnology* **2008**, *19*, 465203.
(11) Huang, Y.; Duan, X.; Lieber, C. M. *Small* **2005**, *1*, 142.
(12) He, Z.; Jie, J.; Zhang, W.; Zhang, W.; Luo, L.; Fan, X.; Yuan, G.; Bello, I.; Lee, S. T. *Small* **2009**, *5*, 345–350.
(13) Jie, J. S.; Zhang, W. J.; Jiang, Y.; Lee, S. T. *Appl. Phys. Lett.* **2006**, *89*, 133118.
(14) Dai, G.; Zhang, Q.; Peng, Z.; Zhou, W.; Xia, M.; Wan, Q.; Pan, A.; Zou, B. *J. Phys. D: Appl. Phys.* **2008**, *41*, 135301.
(15) Doh, Y. J.; Maher, K. N.; Ouyang, L.; Yu, C. L.; Park, H.; Park, J. *Nano. Lett.* **2008**, *8*, 4552–4556.
(16) Shan, C. X.; Liu, Z.; Hark, S. K. *Nanotechnology* **2005**, *16*, 3133–3136.
(17) Jiang, Y.; Zhang, W. J.; Jie, J. S.; Meng, X. M.; Fan, X.; Lee, S. T. *Adv. Funct. Mater.* **2007**, *17*, 1795–1800.
(18) Pan, A.; Liu, R.; Zhang, Q.; Wan, Q.; He, P.; Zacharias, M.; Zou, B. *J. Phys. Chem. C.* **2007**, *111*, 14253–14256.
(19) Sze, S. M. *Physics of Semiconductor Devices*; Wilely: New York, 1981; pp 447 and 450.
(20) Huang, Y.; Duan, X.; Cui, Y.; Lieber, C. M. *Nano. Lett.* **2002**, *2*, 101.
(21) Yang, W. Q.; Huo, H. B.; Dai, L.; Ma, R. M.; Liu, S. F.; Ran, G. Z.; Shen, B.; Lin, C. L.; Qin, G. G. *Nanotechnology* **2006**, *17*, 4868–4872.
(22) Qin, G. G.; Huang, Y. M.; Lin, J.; Zhang, L. Z.; Zong, B. Q.; Zhang, B. R. *Solid State Commun.* **1995**, *94*, 607–612.

JP9031139