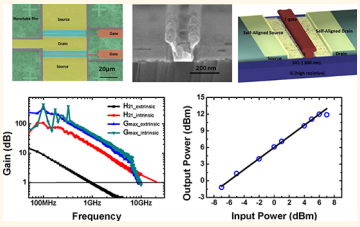
Self-Aligned T-Gate High-Purity Semiconducting Carbon Nanotube RF Transistors Operated in Quasi-Ballistic Transport and Quantum Capacitance Regime

Yuchi Che,[†] Alexander Badmaev,[†] Alborz Jooyaie,[‡] Tao Wu,[‡] Jialu Zhang,[†] Chuan Wang,[†] Kosmas Galatsis,[‡] Hani A. Enaya,[§] and Chongwu Zhou[†,*]

[†]Department of Electrical Engineering, University of Southern California, Los Angeles, California 90089, United States, [‡]Aneeve Nanotechnologies LLC, UCLA California Nanosystems Institute, Los Angeles, California 90095, United States, and [§]King Abdulaziz City for Science and Technology, Riyadh, Saudi Arabia

ABSTRACT Carbon nanotube RF transistors are predicted to offer good performance and high linearity when operated in the ballistic transport and quantum capacitance regime; however, realization of such transistors has been very challenging. In this paper, we introduce a self-aligned fabrication method for carbon nanotube RF transistors, which incorporate a T-shaped (mushroom-shaped) aluminum gate, with oxidized aluminum as the gate dielectric. In this way, the channel length can be scaled down to 140 nm, which enables quasi-ballistic transport, and the gate dielectric is reduced to 2—3 nm aluminum oxide, leading to quasi-quantum capacitance operation. A current-gain cutoff frequency (f_t) up to 23 GHz and a maximum oscillation frequency (f_{max}) of 10 GHz are demonstrated. Furthermore, the linearity properties of nanotube transistors are characterized by using the 1 dB compression point measurement with positive power gain for the first time, to our knowledge. Our work reveals the importance and potential of separated semiconducting nanotubes for various RF applications.



KEYWORDS: carbon nanotubes · semiconducting · quasi-ballistic · quantum capacitance · self-aligned fabrication · T-shaped gate · radio frequency transistor · linearity

Due to their unique properties including small size, high mobility, ballistic conductance, large current density, resistance against electromigration, and low capacitance,[1−3] single-walled carbon nanotubes are considered as promising candidates for next generation digital and analog electronics. It has been demonstrated that nanotubes can be used in integrated logic circuits such as inverters, ring oscillators, decoders, and thin-film macroscale electronics such as AMOLED displays.[4−13] On the other hand, carbon nanotubes have attracted significant research efforts as a material for future analog radio frequency (RF) electronics.[14−23] A combination of very high carrier mobility and current density with extremely small size and intrinsic capacitance makes nanotubes a highly promising material for ultrafast transistors. Most previous effort on CNT RF electronics focused on nanotubes prepared using chemical vapor deposition (CVD),[17] which involves high-temperature processing, usually provides around one-third metallic nanotubes and two-thirds semiconducting nanotubes, and is often limited to sample size. In contrast, separated carbon nanotubes can provide high-purity semiconducting nanotubes up to 95, 98, and 99% and can be dispersed at room temperature at wafer scale.[24,25] However, there has been rather limited study on RF electronics using separated carbon nanotubes, and two notable examples are RF transistors based on separated nanotubes using dielectrophoresis[16] and our own work using separated CNT networks with oxidized aluminum as the back gate.[20] We note that there has been no report of self-aligned RF transistors based on separated semiconducting nanotubes, even though self-aligned fabrication schemes have been recognized as an important way to scale down channel length and reduce parasitic capacitance for radio frequency transistors.[26−28] In addition, RF transistors with high linearity are highly desired to reduce signal distortion, and carbon nanotube RF transistors are predicted to offer good performance and high linearity when operated in the ballistic transport and

* Address correspondence to chongwuz@usc.edu.

Received for review May 4, 2012 and accepted July 6, 2012.

Published online 10.1021/nn301972j

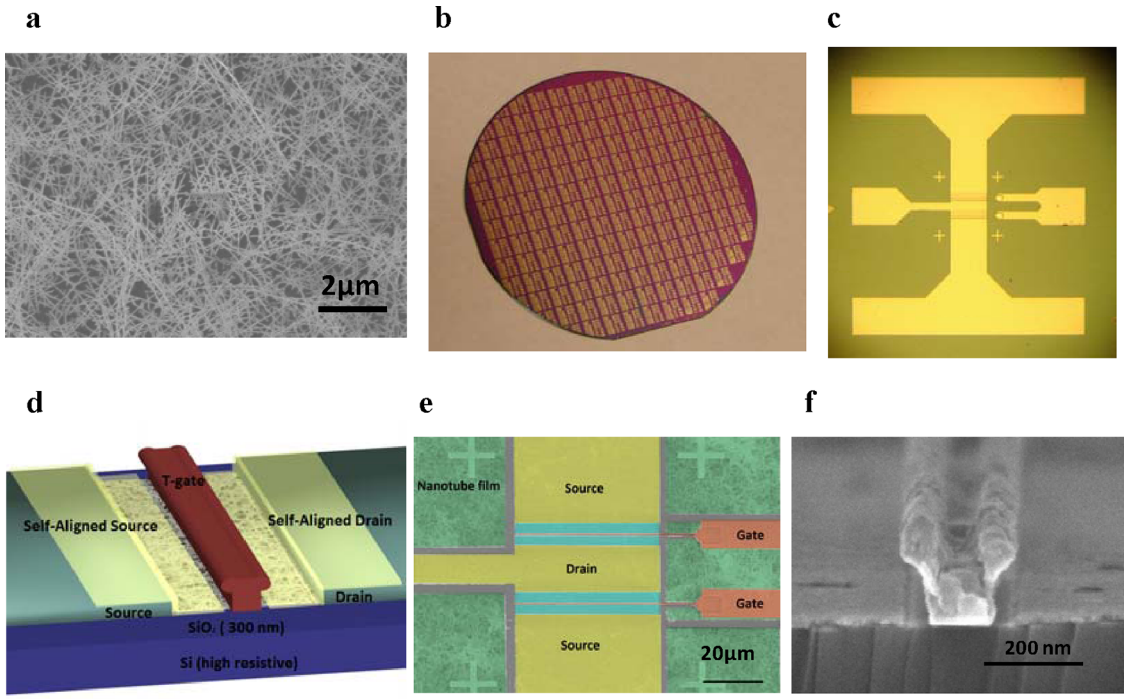


Figure 1. Fabrication of self-aligned T-gate transistors based on a uniform-separated nanotube thin film on Si/SiO_2 substrates. (a) SEM image of a separated nanotube film. (b) Photograph of a 4 in. Si/SiO_2 wafer with fabricated separated nanotube devices. (c) Zoomed-in optical image of an RF transistor with 50 μm channel width. (d) Schematic diagram of the self-aligned T-gate transistor with separated nanotubes as the channel. (e) SEM image of the channel region of a transistor. (f) Perspective-view SEM image of a T-shaped gate structure.

quantum capacitance regime; however, realization of such transistors has proven to be very challenging.

In this paper, we report self-aligned T-gate fabrication and linearity performance of radio frequency transistors based on high-purity 98% semiconducting carbon nanotubes. The channel length can be scaled down to 140 nm, which enables quasi-ballistic transport, and the gate dielectric is reduced to 2−3 nm aluminum oxide, leading to quasi-quantum capacitance operation. Measurements revealed highly linear $I-V_{GS}$ curves and g_m with very small variation for the transistors under active operation. We demonstrated that RF transistors consisted of separated semiconducting nanotube networks of current-gain cutoff frequency (f_t) up to 23 GHz and maximum oscillation frequency (f_{max}) of 10 GHz. Furthermore, we studied the device linearity for our self-aligned T-gate nanotube transistor as an important figure of merit. To the best of our knowledge, the 1 dB compression point measurement with positive power gain was performed for nanotube devices for the first time. Our results show that semiconducting nanotube transistors have great potential for high-frequency applications. The self-aligned T-gate fabrication has also been recently applied to graphene transistors by us.[29]

RESULTS AND DISCUSSION

Figure 1a shows a field emission scanned electron microscope (FESEM) image of a typical high-density and uniform-separated 98% semiconducting nanotube thin film (IsoNanotube-S from NanoIntegris, Inc.). Highly resistive silicon wafer (ρ > 5 kΩ·cm) with 300 nm SiO_2 was used as the substrate in order to reduce parasitic capacitance. We obtained a uniform thin film of separated nanotubes over a full wafer by using the solution-based deposition method with aminopropyltriethoxysilane (APTES) functionalization as reported in our previous work.[10,11] This highly scalable deposition method enables further wafer-scale fabrication of nanotube radio frequency transistors. Here, ground-signal-ground (GSG) coplanar waveguide structure was used to probe separated nanotube RF transistors, as shown in Figure 1b. The zoom-in optical microscope image of a separated nanotube RF transistor is presented in Figure 1c. Figure 1d exhibits the schematic image of separated nanotube transistors fabricated with T-shaped gate design. The carbon nanotube network shown in Figure 1d is based on the SEM image in Figure 1a. Details about the device fabrication process can be found in the Methods section. The SEM image of a representative separated nanotube RF transistor with 50 μm channel width is shown in Figure 1e. Figure 1f presents the perspective-view SEM image of a complete T-shaped structure. This self-aligned fabrication process provides a well-aligned separation with a small air gap between gate and source/drain electrodes, which significantly reduces parasitic fringe capacitance. The channel length of a nanotube transistor is then set by the foot of the T-gate structure. In this report, we obtained

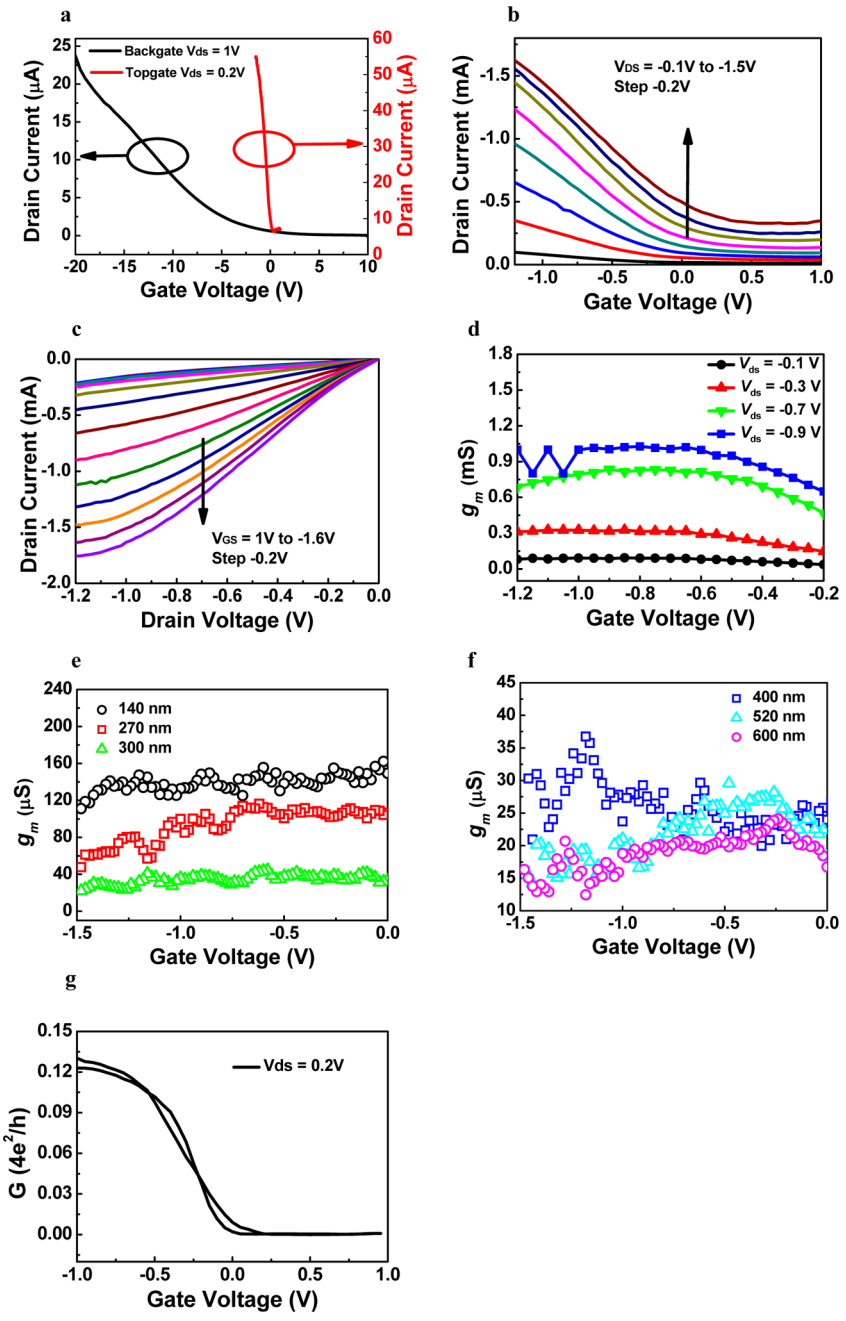


Figure 2. DC characteristics of self-aligned nanotube transistors. (a) Transfer characteristics ($I_{DS}-V_{GS}$) with a nanotube device of back-gate and top-gate control. (b) Transfer characteristics ($I_{DS}-V_{GS}$) of the nanotube transistor with various V_{DS}. (c) Output ($I_{DS}-V_{DS}$) characteristics of the nanotube transistor with various V_{GS}. (d) Characteristic g_m-V_{GS} measurement at various V_{DS}. (e) Characteristics of g_m-V_{GS} measured with devices of channel length ranging from 140 to 300 nm. (f) Characteristics of g_m-V_{GS} measured with devices of channel length ranging from 400 to 600 nm. (g) Conductance *versus* V_{GS} under V_{DS} = 0.2 V of single nanotube self-aligned T-gate device.

channel lengths from 600 down to 140 nm. The separation between source and drain electrodes is created by the T-gate cap, which can be controlled to be longer than the T-gate foot by 40 nm or so. The self-aligned source/drain deposition usually leads to a small ungated nanotube section ~10−20 nm for each side of source and drain. Combination of uniform high-density semiconducting nanotube films and T-gate self-aligned fabrication technique provides a platform for scalable and reliable fabrication of nanotube RF transistors, which pave the way for further study on the DC and RF performance of these devices.

First, we characterized the DC performance of self-aligned T-gate separated nanotube RF transistors. Figure 2a illustrates the transfer characteristics ($I_{DS}-V_{GS}$ curves) of back-gated modulation (black trace) and top-gated modulation (red trace) for a separated nanotube transistor with channel width W = 50 μm. The transistor had a channel length of 4 μm before the self-aligned source/drain deposition.

The black curve presents the back-gate dependence with V_{BG} swept from −20 to 20 V at a drain bias of 1 V. It exhibits a good on/off ratio over 10^3, which is decent for high-purity separated nanotube transistors.[10] After the self-aligned source/drain deposition, the effective channel length scaled down to 140 nm, and the top-gate transfer characteristics were measured with V_{TG} swept from −1.5 to 1 V at a drain bias of 0.2 V. As we discussed in our previous publication, self-oxidized aluminum oxide provides a high-quality dielectric without leakage current within the voltage we used. It is obvious that gate modulation of the nanotube transistor improved significantly after the self-aligned source/drain pattern. With the on-state current density of 1.1 μA/μm and the off-state current density of 0.14 μA/μm, the on/off ratio of the top-gate $I-V_G$ curve is around 7.9. The reduction in on/off ratio after self-aligned source and drain deposition is related to the channel length reduction from 4 μm to 140 nm, as metal tubes can bridge the source and drain directly when the channel length gets reduced. We note that this on/off of 7.9 was achieved for a channel of 140 nm by using 98% semiconducting nanotube solution, and it compares favorably with an on/off ratio of 4.7 we reported before for a channel of 500 nm using 95% semiconducting nanotube solution.[25] In addition, while semiconducting nanotubes contribute to transconductance for the nanotube transistor, metallic nanotubes do not contribute to transconductance and yet contribute to gate-channel capacitance. As a result, using semiconducting nanotubes of higher purity (such as 98% used here) should be beneficial for the transistor frequency performance.

More DC analysis of the self-aligned T-gate separated nanotube RF device is presented in Figure 2, including transfer characteristics ($I_{DS}-V_{GS}$ curves) at various drain bias (Figure 2b) and output characteristics ($I_{DS}-V_{DS}$ curves) with different gate bias (Figure 2c). One can note that the $I_{DS}-V_{GS}$ curves shown in Figure 2b are very linear for gate voltage between −0.5 and −1.2 V, corresponding to active transistor operation. The on-current of the nanotube transistor reaches 36 μA/μm at $V_{DS} = -1.5$ V. Saturation of drain current is observed under high bias (Figure 2c), which is crucial to obtain voltage gain. Besides, the g_m-V_{GS} curves derived from $I_{DS}-V_{GS}$ curves are plotted in Figure 2d. We note that the transconductance remains rather flat for V_{GS} between −0.5 and −1.2 V, indicating the potential for high linearity operation. By tuning the T-gate fabrication recipe, we scaled transistor channel length from 600 down to 140 nm. Figure 2e,f presents the g_m-V_{GS} curves of devices at $V_{DS} = 0.2$ V with channel length ranging from 140 to 300 nm and from 400 to 600 nm, respectively. It illustrates that transconductance increases with reduced channel lengths. As presented in Figure 2d,e, self-aligned T-gate separated nanotube transistors of 140 nm channel length show good linearity, supported by the flat gate dependence curves. As a good comparison, significant work in nanotube RF transistors has been achieved by Rogers's group,[17,30] while a carbon nanotube RF transistor made by Rogers's group has a channel of 700 nm and HfO_2 gate dielectric of 50 nm,[30] and the device showed variation of g_m from 2.5 mS at $V_{GS} = -0.8$ V to a peak value of 5 mS at $V_{GS} = -0.2$ V, and then a lower value of 3 mS at $V_{GS} = 0.2$ V.[30] In contrast, our transistors exhibited very uniform g_m and very high linearity, as shown in Figure 2b,d. We attribute the linearity of our devices to quasi-ballistic transport as a result of short channel length (140 nm in Figure 2b,d) and quasi-quantum capacitance operation due to the ultrathin gate dielectric (2−3 nm Al_2O_3) we used. It was predicted before that the nanotube transistor operated in the ballistic transport and quantum capacitance regime can offer high linearity.[31] Previously, extensive study was carried out by Dai *et al.* on nanotube ballistic transport, which revealed a mean free path of ~100 nm.[32] The self-aligned T-gate design eliminates misalignment and thus enabled us to fabricate nanotube transistors with channel length down to 140 nm, which is comparable to the mean free path and therefore results in quasi-ballistic transport.

As further evidence, we fabricated a self-aligned T-gate transistor with a single nanotube, and the conductance is measured to be 0.13 × ($4e^2/h$) at $V_{DS} = 0.2$ V and $V_{GS} = -1$ V, as shown in Figure 1g. Transmission coefficient of 0.13 is an underestimate of the real value as the transistor has metal−nanotube contact resistance and access resistance due to ungated nanotubes in series with the active channel resistance. We nevertheless note that the transmission coefficient of 0.13 is comparable to some of the devices reported.[32] Regarding quantum capacitance operation, we can calculate gate capacitance C_w of the carbon nanotube with the following equation:[33]

$$C_w = \frac{D}{C_Q{}^{-1} + C_g{}^{-1}} = \frac{D}{\left[C_Q{}^{-1} + \frac{1}{2\pi\varepsilon_0\varepsilon_s} \times \log\left[\frac{\sin h(2\pi tD)}{\pi RD}\right]\right]}$$

Here, C_Q is the quantum capacitance of nanotubes, D is the density of nanotube, ε_s is the dielectric constant, t is the thickness of the dielectric layer, and R is the radius of nanotube. With the device parameters, the electrostatic gate capacitance C_g for our T-gate nanotube transistor is ~3.5×10^{-10} F/m, which is close to the quantum capacitance value of 4×10^{-10} F/m (calculation details shown in Supporting Information). We stress that even better linearity can be achieved by further reduction of channel length to ensure complete ballistic transport and by possibly replacing ultrathin Al_2O_3 with other ultrathin high κ dielectric, such as HfO_2.

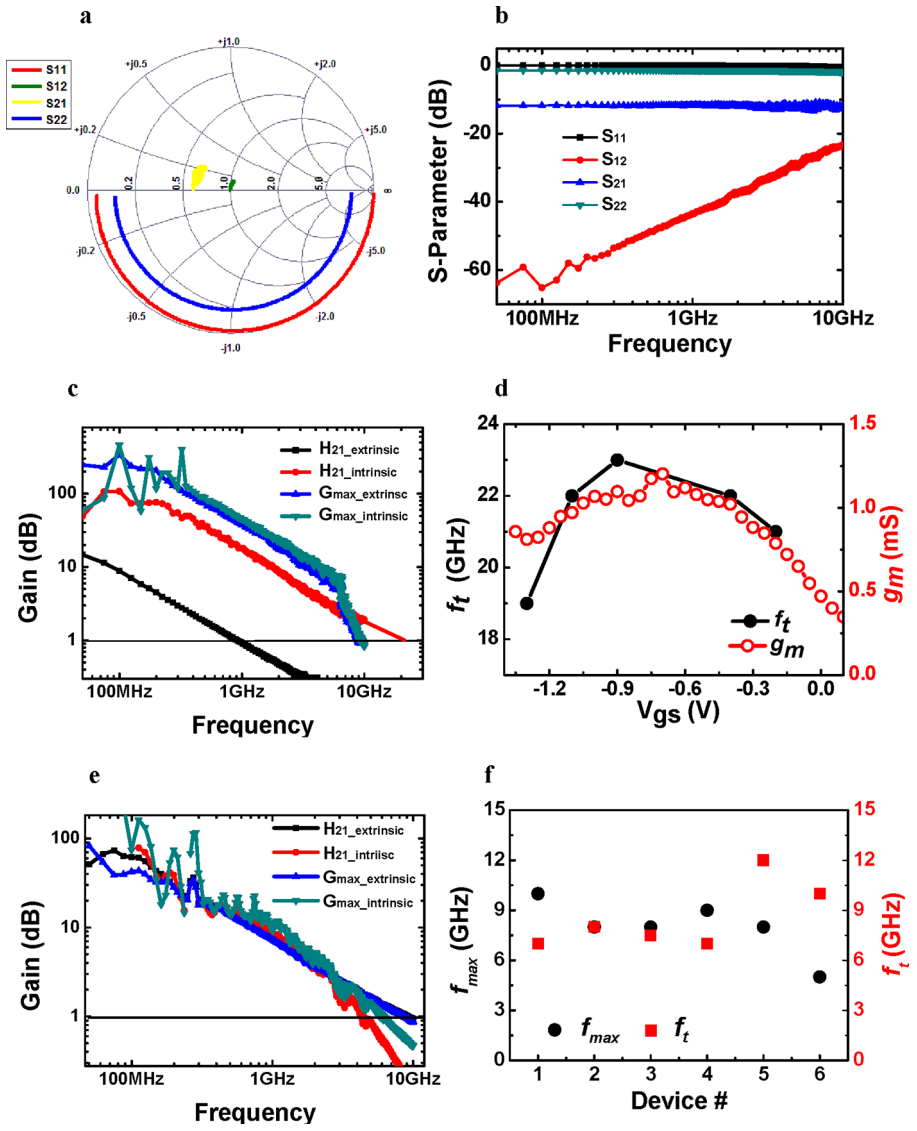


Figure 3. RF characteristics of a separated nanotube RF transistor on the Si/SiO_2 substrate (a−d) and a similar transistor on the quartz substrate (e,f). (a) Smith chart of as-measured S-parameters of the separated nanotube RF transistor on Si/SiO_2 (L = 140 nm, W = 50 μm). (b) As-measured S-parameters of the separated nanotube RF transistor. (c) Extrinsic and intrinsic current-gain H_{21} and maximum available gain G_{max} of the device on the Si/SiO_2 substrate derived from the measured S-parameters from 50 MHz to 10 GHz. (d) Transconductance and intrinsic cutoff frequency *versus* gate bias. (e) Extrinsic and intrinsic current-gain H_{21} and maximum available gain G_{max} of the device on the quartz substrate derived from the measured S-parameters from 50 MHz to 10 GHz. (f) Values f_{max} and f_t of different T-gate transistors on the quartz substrate.

The high-frequency behavior of the self-aligned T-gate separated nanotube RF transistors with 140 nm channel length was characterized by measuring S-parameters directly with a vector network analyzer (VNA) over the frequency range from 0.05 to 10 GHz. The calibration of the measurement to the probe tips was performed by using off-wafer short-open-load-through (SOLT) standard. Figure 3a,b illustrates the as-measured S-parameters for the device structure presented in Figure 1e. The gate electrode was biased at V_{GS} = −1.1 V, and the drain electrode was biased at V_{DS} = −1.5 V since this bias condition provides an optimal g_m, confirmed by DC measurement. Figure 3c presents both the extrinsic (before de-embedding) and intrinsic (after de-embedding) current-gain (H_{21}) and maximum available gain (MAG) frequency response of the nanotube RF transistor. To exclude the parasitic capacitance from the probing measurement, a de-embedding procedure was used to eliminate the effect of coplanar waveguide pads on the RF performance by measuring the on-chip "open" and "short" test structures. In this de-embedding method, the open structure only consists of coplanar waveguide pads outside the active area of nanotube transistor and the short structure has additional metal film shorting the gate−source and drain−source pads (Supporting Information S3). As a result, the intrinsic device performance after our de-embedding includes all of the important device features such as T-shaped gate and self-aligned source and drain electrode, which is

important and meaningful for circuit application. This kind of de-embedding procedure was applied to as-measured S-parameters to obtain the "device" performance. From Figure 3c, one can find the current-gain cutoff frequency (f_t) to be about 1 GHz before de-embedding and 22 GHz after de-embedding. The G_{max} curve indicates 10 GHz of unity power gain frequency f_{max} both before and after de-embedding. Figure 3d presents the gate bias dependence of the intrinsic cutoff frequency. The peak of cutoff frequency of 23 GHz occurs at the gate bias of −0.9 V. Since f_t is proportional to g_m, the variation of f_t follows the variation of g_m, while the small shift between g_m and f_t may come from the hysteresis of the nanotube transistor. The frequency response of this self-aligned T-gate separated nanotube transistor is significantly improved from our previous separated nanotube transistor of 5 GHz cutoff frequency,[25] and we attribute the improvement to the improved g_m and reduced parasitic capacitances with the self-aligned T-gate technology. In addition, the unity power gain frequency f_{max} of 10 GHz reported in this paper is one of the best performances for nanotube transistors reported to the date.

To confirm the intrinsic frequency performance of separated nanotube T-gate RF devices, we also performed the fabrication on the quartz substrate to exclude the effects of parasitic capacitances. The devices on the quartz substrate exhibit DC characteristics similar to that of devices on the silicon substrate. Both extrinsic and intrinsic frequency responses of a T-gate separated nanotube transistor with 30 μm channel width on the quartz substrate are illustrated in Figure 3e. It shows an extrinsic current-gain cutoff frequency of 12 GHz and power gain frequency of 8 GHz, which are comparable to the intrinsic performance of T-gate separated nanotube devices on silicon substrate discussed previously, proving the validity of our de-embedding method. Importantly, the extrinsic and intrinsic performances of T-gate devices on the quartz substrate are approximately the same because the insulating quartz substrate reduces the parasitic capacitance significantly. Figure 4f is a plot of f_t and f_{max} from different T-gate transistors with a channel length of ~140 nm on the quartz substrate, showing high yield and uniformity with cutoff frequency ranging from 4 to 12 GHz.

Linearity is a significant figure of merit for analog and RF/microwave circuit and system designs. Carbon nanotubes are anticipated to enable emerging designs and systems requiring highly linear transistors. Here, we also performed the linearity analysis for our self-aligned T-gate separated nanotube transistors. As is known, there are a few figures of merit capturing nonlinearity, and a 1 dB compression point and the intermodulation distortion are the most common ones. Between the two metrics, the 1 dB compression point is a device performance metric, whereas the intermodulation products are usually specified for circuits and devices as parts of a system. Furthermore, the intermodulation product metrics (third-order intercept point IIP3) points are usually higher than the 1 dB compression point by about 10 dB.

In order to characterize the nonlinearity metrics, the device under test should have either voltage gain or power gain. In previous publications, the linearity performance of the carbon-based transistors was estimated indirectly,[25,26] through use of either the transistor in a mixer or a resistively loaded transistor. In this work, we present the 1 dB compression point measurement of separated nanotube transistors with positive power gain, to our knowledge, for the first time. This is novel in the way of providing nonlinearity performance information about the device directly, which also has a positive power gain. Moreover, the device was characterized in a large signal domain, within the context it will be used to design the circuit with, which is another novel part of the characterization work.

The self-aligned T-gate separated nanotube transistors were used in constructing a class-A power amplifier, and to capture the impedance as well as nonlinearity information, their available power gain contours and impedance were characterized in a load/source pull system. The test setup is illustrated in Figure 4a. The load and source tuners synthesized a known/adjustable input and output impedance for the device under test (DUT). The reflected power and transmitted power were measured, corresponding to each input/output impedance, in order to characterize the available power gain corresponding to termination impedances seen by the DUT. The available power gain contours at 200 and 500 MHz were measured. The contours were significant in choosing the source impedance required in order to achieve the fixed available power gain, and the load impedance was conjugate matched on the output side. The available power gain contours at 200 and 500 MHz are shown in Figure 4b,c, respectively. As expected, as frequency was increased, the radii of the contours corresponding to a fixed available power gain decreased, reducing the flexibility in choosing the impedance. The 1 dB compression point was measured by fixing the source impedance, corresponding to a particular available power gain, and sweeping the power level from a low starting input power to higher values. Two 1 dB compression point plots, at 200 and 500 MHz input frequency, are illustrated in Figure 4d,e, respectively. The 200 MHz input frequency measurement is synthesized to achieve an available power gain of 8 dB and reveals a 1 dB output referred compression point of 11.6 dBm (Figure 4d). The 500 MHz input frequency measurement is synthesized to achieve an available power gain of 6 dB and reveals a 1 dB output referred compression point of 11.9 dBm (Figure 4e).

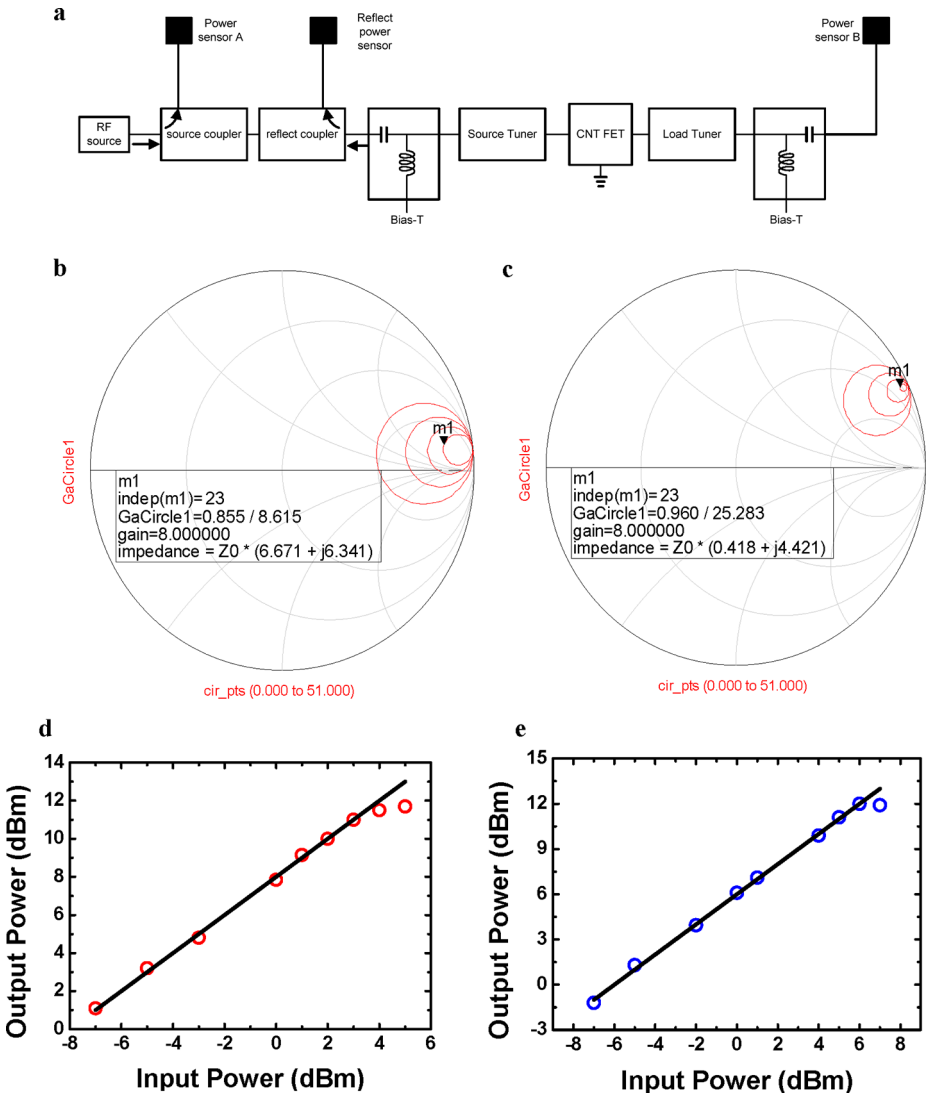


Figure 4. Linearity characteristics of T-gate self-aligned separated nanotube RF transistors. (a) Schematic of load and source pull setup system to capture the nonlinearity for the separated nanotube RF transistor. (b,c) Source impedance at the source tuner for 8 dB of power gain at 200 MHz (b) and 500 MHz (c); (d,e) 1 dB compression point plots at 200 MHz (d) and 500 MHz (e).

CONCLUSION

In conclusion, we applied the scalable self-aligned T-shaped gate design to semiconducting nanotube RF transistors. The nanotube transistors exhibit excellent on-chip device performance with channel length scaling down to 140 nm. With T-shaped gate structure, a cutoff frequency up to 23 GHz and power gain frequency of 10 GHz for separated nanotube transistors are achieved. The T-shaped gate design enables high-yield wafer-scale fabrication with controllable gate length scaling. Furthermore, we also characterized the linearity properties of nanotube transistors, with the 1 dB compression point measurement, in source/load pull setup, with positive power gain, to our knowledge, for the first time. Meanwhile, we are still working on the optimization of separated nanotube RF transistor fabrication, including using higher purity presepared semiconducting nanotube solution, improving the uniformity of nanotube film, further reducing device dimension, and decreasing parasitic effects such as access resistance from ungated section. Above all, our work reveals that the semiconducting nanotube RF transistor is an interesting and promising direction in high-frequency device and circuit exploration.

METHODS

Fabrication Steps of Self-Aligned T-Gate Separated Nanotube RF Transistors. Large-area uniform-separated 98% semiconducting nanotube thin film was deposited on a highly resistive silicon wafer ($\rho > 5$ k$\Omega \cdot$cm) and 300 nm SiO_2 was used for the solution-based deposition method with aminopropyltriethoxysilane (APTES) functionalization. Nanotube transistors with planar waveguide pads over a 4 in. wafer were first fabricated by

photolithography. The wafer was cut into small samples for gate patterning due to the limitation of e-beam lithography equipment. With bilayer electron beam resist of different sensitivity, a step-shaped side wall profile of the bilayer resist was achieved by exposing a high dose at the gate position center and a low dose at the adjacent area. After the deposition of aluminum film, a standard lift-off process produces the T-shaped gate (T-gate) stack. By heating the sample to 150 °C in air for about 1 h, the oxidation of the Al T-gate in air forms a thin dielectric layer at the interface between nanotubes and the gate electrode. Finally, palladium was deposited to create a self-aligned source and drain electrode with the T-shaped gate working as a shadow mask.

Conflict of Interest: The authors declare no competing financial interest.

Acknowledgment. We acknowledge financial support from Joint KACST/California Center of Excellence. We thank Professor Mark Hersam of Northwestern University, and Mr. Elliott Garlock and Dr. Nathan Yoder of Nanointegris for valuable discussions.

Supporting Information Available: Quasi-ballistic transport of T-gate transistor (S1); capacitance calculation (S2); de-embedding procedure (S3); hysteresis of the T-gate separated nanotube RF transistors (S4). This material is available free of charge *via* the Internet at http://pubs.acs.org.

REFERENCES AND NOTES

1. Durkop, T.; Getty, S. A.; Cobas, E.; Fuhrer, M. S. Extraordinary Mobility in Semiconducting Carbon Nanotubes. *Nano Lett.* **2004**, *4*, 35–39.
2. Zhou, X. J.; Park, J. Y.; Huang, S. M.; Liu, J.; McEuen, P. L. Band Structure, Phonon Scattering, and the Performance Limit of Single-Walled Carbon Nanotube Transistors. *Phys. Rev. Lett.* **2005**, *95*, 146805.
3. Javey, A.; Guo, J.; Farmer, D. B.; Wang, Q.; Yenilmez, E.; Gordon, R. G.; Lundstrom, M.; Dai, H. J. Self-Aligned Ballistic Molecular Transistors and Electrically Parallel Nanotube Arrays. *Nano Lett.* **2004**, *4*, 1319–1322.
4. Bachtold, A.; Hadley, P.; Nakanishi, T.; Dekker, C. Logic Circuits with Carbon Nanotube Transistors. *Science* **2001**, *294*, 1317–1320.
5. Derycke, V.; Martel, R.; Appenzeller, J.; Avouris, P. Carbon Nanotube Inter- and Intramolecular Logic Gates. *Nano Lett.* **2001**, *1*, 453–456.
6. Liu, X. L.; Lee, C.; Zhou, C. W.; Han, J. Carbon Nanotube Field-Effect Inverters. *Appl. Phys. Lett.* **2001**, *79*, 3329–3331.
7. Javey, A.; Wang, Q.; Ural, A.; Li, Y. M.; Dai, H. J. Carbon Nanotube Transistor Arrays for Multistage Complementary Logic and Ring Oscillators. *Nano Lett.* **2002**, *2*, 929–932.
8. Chen, Z. H.; Appenzeller, J.; Lin, Y. M.; Sippel-Oakley, J.; Rinzler, A. G.; Tang, J. Y.; Wind, S. J.; Solomon, P. M.; Avouris, P. An Integrated Logic Circuit Assembled on a Single Carbon Nanotube. *Science* **2006**, *311*, 1735–1735.
9. Ryu, K.; Badmaev, A.; Wang, C.; Lin, A.; Patil, N.; Gomez, L.; Kumar, A.; Mitra, S.; Wong, H. S. P.; Zhou, C. W. Cmos-Analogous Wafer-Scale Nanotube-on-Insulator Approach for Submicrometer Devices and Integrated Circuits Using Aligned Nanotubes. *Nano Lett.* **2009**, *9*, 189–197.
10. Wang, C.; Zhang, J. L.; Ryu, K. M.; Badmaev, A.; De Arco, L. G.; Zhou, C. W. Wafer-Scale Fabrication of Separated Carbon Nanotube Thin-Film Transistors for Display Applications. *Nano Lett.* **2009**, *9*, 4285–4291.
11. Wang, C. A.; Zhang, J. L.; Zhou, C. W. Macroelectronic Integrated Circuits Using High-Performance Separated Carbon Nanotube Thin-Film Transistors. *ACS Nano* **2010**, *4*, 7123–7132.
12. Zhang, J. L.; Wang, C.; Fu, Y.; Che, Y. C.; Zhou, C. W. Air-Stable Conversion of Separated Carbon Nanotube Thin-Film Transistors from p-Type to n-Type Using Atomic Layer Deposition of High-κ Oxide and Its Application in CMOS Logic Circuits. *ACS Nano* **2011**, *5*, 3284–3292.
13. Zhang, J. L.; Fu, Y.; Wang, C.; Chen, P. C.; Liu, Z. W.; Wei, W.; Wu, C.; Thompson, M. E.; Zhou, C. W. Separated Carbon Nanotube Macroelectronics for Active Matrix Organic Light-Emitting Diode Displays. *Nano Lett.* **2011**, *11*, 4852–4858.
14. Li, S. D.; Yu, Z.; Yen, S. F.; Tang, W. C.; Burke, P. J. Carbon Nanotube Transistor Operation at 2.6 GHz. *Nano Lett.* **2004**, *4*, 753–756.
15. Le Louarn, A.; Kapche, F.; Bethoux, J. M.; Happy, H.; Dambrine, G.; Derycke, V.; Chenevier, P.; Izard, N.; Goffman, M. F.; Bourgoin, J. P.; *et al.* Intrinsic Current Gain Cutoff Frequency of 30 GHz with Carbon Nanotube Transistors. *Appl. Phys. Lett.* **2007**, *90*, 233108.
16. Nougaret, L.; Happy, H.; Dambrine, G.; Derycke, V.; Bourgoin, J. P.; Green, A. A.; Hersam, M. C. 80 GHz Field-Effect Transistors Produced Using High Purity Semiconducting Single-Walled Carbon Nanotubes. *Appl. Phys. Lett.* **2009**, *94*, 243505.
17. Kocabas, C.; Kim, H. S.; Banks, T.; Rogers, J. A.; Pesetski, A. A.; Baumgardner, J. E.; Krishnaswamy, S. V.; Zhang, H. Radio Frequency Analog Electronics Based on Carbon Nanotube Transistors. *Proc. Natl. Acad. Sci. U.S.A.* **2008**, *105*, 1405–1409.
18. Rutherglen, C.; Jain, D.; Burke, P. Nanotube Electronics for Radiofrequency Applications. *Nat. Nanotechnol.* **2009**, *4*, 811–819.
19. Rouhi, N.; Jain, D.; Zand, K.; Burke, P. J. All-Semiconducting Nanotube Devices for RF and Microwave Applications. *2010 Proc. IEEE Microwave Symp.Dig.* **2010**.
20. Eron, M.; Lin, S.; Wang, D.; Schroter, M.; Kempf, P. L-Band Carbon Nanotube Transistor Amplifier. *Electron. Lett.* **2011**, *47*, 265.
21. Schroter, M., Kolev, P., Wang, D. Eron, M. A 4″ Wafer Photostepper-Based Carbon Nanotube Fet Technology for RF Applications. *2011 Proc. IEEE Microwave Symp. Dig.*, 2011.
22. Burke, P. J. AC Performance of Nanoelectronics: Towards a Ballistic Thz Nanotube Transistor. *Solid-State Electron.* **2004**, *48*, 1981–1986.
23. Alam, K.; Lake, R. Performance of 2 nm Gate Length Carbon Nanotube Field-Effect Transistors with Source/Drain Underlaps. *Appl. Phys. Lett.* **2005**, *87*, 073104.
24. Rouhi, N.; Jain, D.; Burke, P. J. High-Performance Semiconducting Nanotube Inks: Progress and Prospects. *ACS Nano* **2011**, *5*, 8471–8487.
25. Wang, C.; Badmaev, A.; Jooyaie, A.; Bao, M. Q.; Wang, K. L.; Galatsis, K.; Zhou, C. W. Radio Frequency and Linearity Performance of Transistors Using High-Purity Semiconducting Carbon Nanotubes. *ACS Nano* **2011**, *5*, 4169–4176.
26. Liao, L.; Bai, J. W.; Cheng, R.; Lin, Y. C.; Jiang, S.; Qu, Y. Q.; Huang, Y.; Duan, X. F. Sub-100 nm Channel Length Graphene Transistors. *Nano Lett.* **2010**, *10*, 3952–3956.
27. Ding, L.; Wang, Z. X.; Pei, T.; Zhang, Z. Y.; Wang, S.; Xu, H. L.; Peng, F.; Li, Y.; Peng, L. M. Self-Aligned U-Gate Carbon Nanotube Field-Effect Transistor with Extremely Small Parasitic Capacitance and Drain-Induced Barrier Lowering. *ACS Nano* **2011**, *5*, 2512–2519.
28. Farmer, D. B.; Lin, Y. M.; Avouris, P. Graphene Field-Effect Transistors with Self-Aligned Gates. *Appl. Phys. Lett.* **2010**, *97*, 013103.
29. Badmaev, A.; Che, Y. C.; Li, Z.; Wang, C.; Zhou, C. W. Self-Aligned Fabrication of Graphene RF Transistors with T-Shaped Gate. *ACS Nano* **2012**, *6*, 3371–3376.
30. Kocabas, C.; Dunham, S.; Cao, Q.; Cimino, K.; Ho, X. N.; Kim, H. S.; Dawson, D.; Payne, J.; Stuenkel, M.; Zhang, H.; *et al.* High-Frequency Performance of Submicrometer Transistors That Use Aligned Arrays of Single-Walled Carbon Nanotubes. *Nano Lett.* **2009**, *9*, 1937–1943.
31. Baumgardner, J. E.; Pesetski, A. A.; Murduck, J. M.; Przybysz, J. X.; Adam, J. D.; Zhang, H. Inherent Linearity in Carbon Nanotube Field-Effect Transistors. *Appl. Phys. Lett.* **2007**, *91*, 052108.
32. Javey, A.; Guo, J.; Wang, Q.; Lundstrom, M.; Dai, H. J. Ballistic Carbon Nanotube Field-Effect Transistors. *Nature* **2003**, *424*, 654–657.
33. Rosenblatt, S.; Yaish, Y.; Park, J.; Gore, J.; Sazonova, V.; McEuen, P. L. High Performance Electrolyte Gated Carbon Nanotube Transistors. *Nano Lett.* **2002**, *2*, 869–872.