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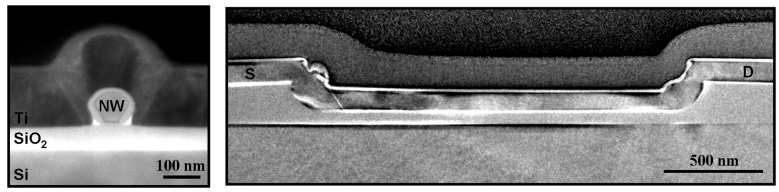

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Integratable Nanowire Transistors

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ABSTRACT

We report a structure to control nanowire location and growth direction and demonstrate top-gated, metal−oxide−semiconductor, field-effect transistors (MOSFETs) using this structure. The nanowires were engineered to grow against an oxide surface of a (001), silicon-on-insulator substrate, enabling straightforward fabrication of MOSFETs exhibiting an I_{on}/I_{off} ratio ∼104 and a subthreshold slope of ∼155 mV/decade. Though nanowires were engineered to grow in ⟨110⟩ directions, the nanowires still grew by the addition of {111} planes.

Metal-catalyzed, self-assembled, semiconducting nanowires have been proposed as the basis for fabricating nanometer-scale electronic, optical, and sensing devices without expensive, fine-scale lithography.[1,2] Despite their promising properties, difficulty controlling their location and integrating them prevents their widespread use. To date, most work has focused on growing the nanowires (NWs) on one substrate, removing them, then placing them on another substrate to connect them to electrodes, making integration difficult.[3−5] Alternatively, NWs can be grown in locations where devices can be fabricated. Nanowires can be grown vertically on (111) substrates[6,7] or horizontally above a surface to bridge between two electrodes;[8,9] however, processing the resulting nonplanar structures is difficult. Here we report a structure enabling control of nanowire location and growth direction, which we use to demonstrate top-gated, metal-oxide-semiconductor, field-effect transistors (MOSFETs) patterned using conventional planar technology. The nanowires were engineered to grow in crystallographic directions against the surface of the buried oxide (BOX) layer of a (100)-oriented, silicon-on-insulator (SOI) substrate. Trenches were cut into the top Si layer of the SOI substrate. Some of the buried oxide layer was etched isotropically, undercutting the top Si layer. Nanowires were selectively nucleated from this undercut region and grew against the oxide in a ⟨110⟩-type direction. These nanowires bridged between two Si regions subsequently used as the source and drain electrodes of the MOSFET, which exhibited an I_{on}/I_{off} ratio ∼104 and an inverse subthreshold slope of ∼155 mV/decade. Growing nanowires in contact with the surface in a predefined location makes the nanowires more robust to further processing and can enable the integration of multiple nanowire devices. This integration can help realize the full promise of semiconducting nanowires since practical applications of nanowire devices are likely to use a combination of top-down patterning with self-assembly to integrate nanowires with conventionally formed structures.

Si nanowires usually grow in ⟨111⟩-type directions.[10,11] Because of this favored growth direction, the nanowire orientation relative to the substrate surface can be partially controlled when the nanowires are grown epitaxially on substrates with different orientations. For example, on (111) substrates the nanowires grow primarily vertically; on (100) substrates they grow in the four equivalent ⟨111⟩-type directions about 35° from the surface plane; with (110) substrates the nanowires can be grown horizontally from vertical (111) planes exposed by anisotropic etching.[8,12] In this work we use an SOI wafer to connect two electrodes using nanowires grown between them; this structure compels the nanowires to grow in a ⟨110⟩-type direction. This growth direction control is achieved by etching a portion of the BOX layer to undercut the top Si layer and growing epitaxial nanowires from the exposed, undercut surface of the top Si layer. A nanowire starts growing downward in the ⟨111⟩ direction at an angle of ∼35° from the substrate surface plane; however, when it comes into contact with the oxide surface, its growth is forced into a ⟨110⟩-type direction parallel to and in contact with the horizontal oxide surface.

Fabrication of the first of two substrate structures that enabled this nanowire growth started with an SOI substrate consisting of a 100 nm thick, (100)-oriented, n^+-Si layer on a 200 nm BOX on a p^--Si handle wafer (see Supporting Information). A 70 nm Si_3N_4 layer was deposited on the n^+-Si, patterned, and used as a hard mask to etch the exposed Si with KOH (shown schematically in Figure 1a) to form electrically isolated electrodes. The BOX oxide was then etched with 10:1::NH_4F:HF (BOE) to undercut the top n^+-Si layer. Si nanowires were grown using the vapor−liquid−solid (VLS) mechanism[10] enabled by depositing preformed, 40 nm, colloidal Au nanoparticles only on exposed Si surfaces, as schematically pictured in Figure 1c and shown in Figure 2.

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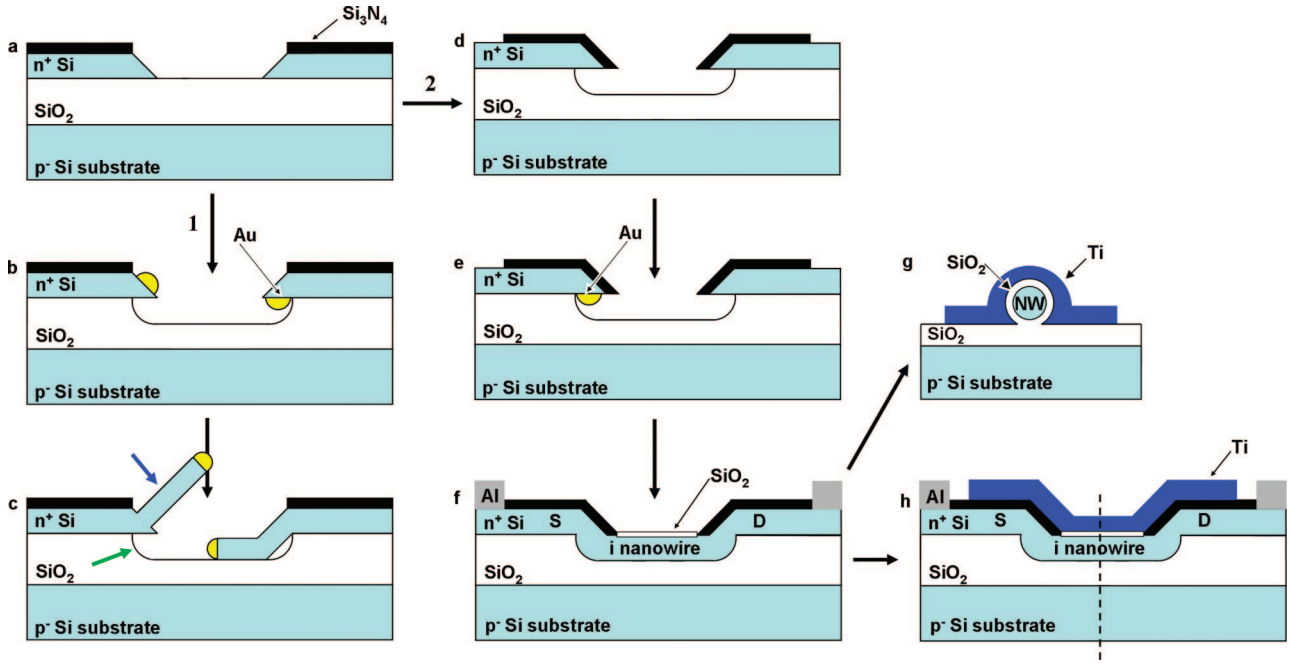

Figure 1. Process flow schematic: a, for both structures discussed; b and c, for growth test structure; d−h, for MOSFET; g, NW stands for nanowire.

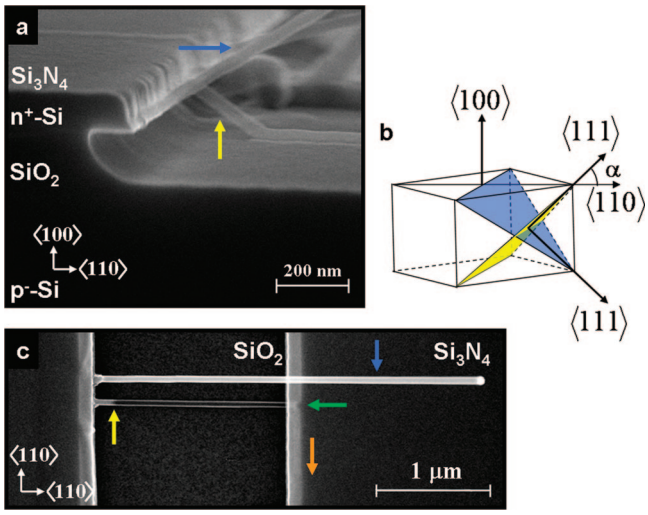

Figure 2. Scanning electron micrographs of the first structure and crystallographic orientation: a and c, cross-sectional and plan-view scanning electron micrographs of test structure without Si_3N_4 on the angled, KOH-etched sidewalls; b, crystallographic orientation corresponding to panel a. The angled Si sidewall is not protected in this structure.

This selective placement of Au was engineered by first exposing the entire structure to a mixture of 40 nm Au colloid and HF to deposit Au nanoparticles everywhere. The sample was then annealed at 400 °C in a H_2 ambient—above the Au/Si eutectic temperature—so that those Au nanoparticles in contact with Si alloyed with the Si. Au nanoparticles on the oxide and nitride surfaces did not alloy and were then removed by dipping the sample in BOE for 7 s and H_3PO_4 (at 155 °C) for 2.5 min to etch some of the oxide and nitride, respectively. This etching resulted in Au nanoparticles remaining only on exposed Si surfaces, namely, the KOH-etched surface and the undercut Si surface, as shown schematically on the left and right sides of Figure 1b, respectively. The nanowires were grown at 680 °C using SiH_4 and HCl in a H_2 ambient (see Supporting Information). With this structure NWs grew both upward and along the oxide surface as shown in Figures 1c and 2.

Panels a and c of Figure 2 are scanning electron micrographs of the sample just described in cross section and plan view, respectively. The sample depicted in Figure 2a was cleaved along a ⟨110⟩-type direction, with another ⟨110⟩-type direction almost perpendicular to the plane of the picture. In this figure, nanowires are seen to grow upward (blue arrow) from the unprotected, angled Si sidewall and downward (yellow arrow) from the exposed undercut region of the n^+ Si layer. The crystallographic orientation is illustrated, slightly skewed for perspective, in Figure 2b. From this schematic one can see that the ⟨111⟩-type directions (the nanowire growth directions) make an angle, α, of ~±35° with the substrate plane. This angle is observed between the upward- and downward-growing nanowires and the substrate plane in Figure 2a.

In Figures 2a, 2c, and 3 one can see that some nanowires nucleated at the bottom of the n^+-Si and grew epitaxially toward the BOX (yellow arrows in Figures 2a, 2c, and 3). These downward-growing nanowires are key to the device structure reported later. With further growth, the nanowire came into contact with the BOX and grew along the oxide surface in a ⟨110⟩-type direction. We believe that the mechanism of NW growth has not changed and that the NW is essentially still growing in a ⟨111⟩-type direction. The evidence for this is shown in Figure 3 where one can see that the interface between the NW and the Au catalyst is bounded by what appears to be a Si{111} plane. For typical unconstrained growth of a nanowire, the NW/catalyst interface is usually a {111} plane perpendicular to the growth

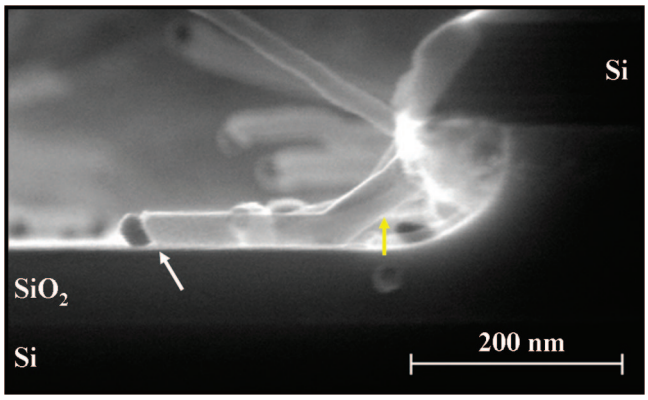

Figure 3. Scanning electron micrograph of NW cross section highlighting the interface between the Au catalyst and the NW. The interface between the Au catalyst and the Si NW appears to be bounded by a {111} Si plane suggesting that the NW is still growing incrementally in a ⟨111⟩-type direction; however, it is guided by the oxide surface to grow in a ⟨110⟩ direction.

direction. For the present case of growth guided by the oxide surface, the NW appears to incrementally grow in a ⟨111⟩ direction, i.e., adding {111} planes to elongate the NW, but macroscopically is forced to grow in a ⟨110⟩ direction—the projection of the ⟨111⟩ direction on the (100) plane—because it is guided by the oxide surface. In Figure 2c, the part of the nanowire that is in contact with the oxide surface has a darker contrast compared to the part not contacting the surface. This change in contrast is highlighted by the yellow arrow in Figure 2c and helps to differentiate nanowires growing against the surface from those growing in free space.

Growth along the oxide surface continues even when the nanowire reaches the undercut, curved oxide section (green arrow in Figure 1c). This curved oxide surface directs the nanowire growth upward toward the undercut Si surface on the opposite side from the nucleating end of the nanowire, enabling the connection between the two Si electrodes. The nanowire growing along the BOX in Figure 2c makes a mechanical and electrical connection to the undercut Si surface (green arrow in Figure 2c). The quality of this type of grown connection has been previously demonstrated using an analogous configuration with nanowire growth suspended above the surface.[9,13] Though difficult to see, after making this connection, this nanowire turns 90° and grows from this connection point underneath the undercut Si in the direction of the orange arrow and grows to about the end of the arrow. This type of growth under the undercut Si ledge is more obvious in Figure 4a (orange arrow).

To eliminate the spurious, upward-growing nanowires, the second structure in Figure 1 was fabricated. In this structure Si_3N_4 was deposited and anisotropically reactive ion etched (RIE) to cover the KOH etched angled Si sidewalls with Si_3N_4 before nanowire growth; thus, the only exposed Si surfaces were those exposed by the BOE on the underside of the top Si. With the deposition, anneal, and etch procedure described earlier, Si NWs nucleated from this exposed Si region. This time 100 nm Au colloid (see Supporting Information) was used as the catalyst for nanowire growth to ensure that the nanowires were always in contact with the oxide surface during growth, as shown schematically in Figure 1f. After the nanowires were grown across the gap between the source and drain (labeled "S" and "D," respectively, in Figure 1f), they were thermally oxidized to form a 13−21 nm oxide, 200 nm Al was deposited to make contacts to the source and drain, and 170 nm Ti was

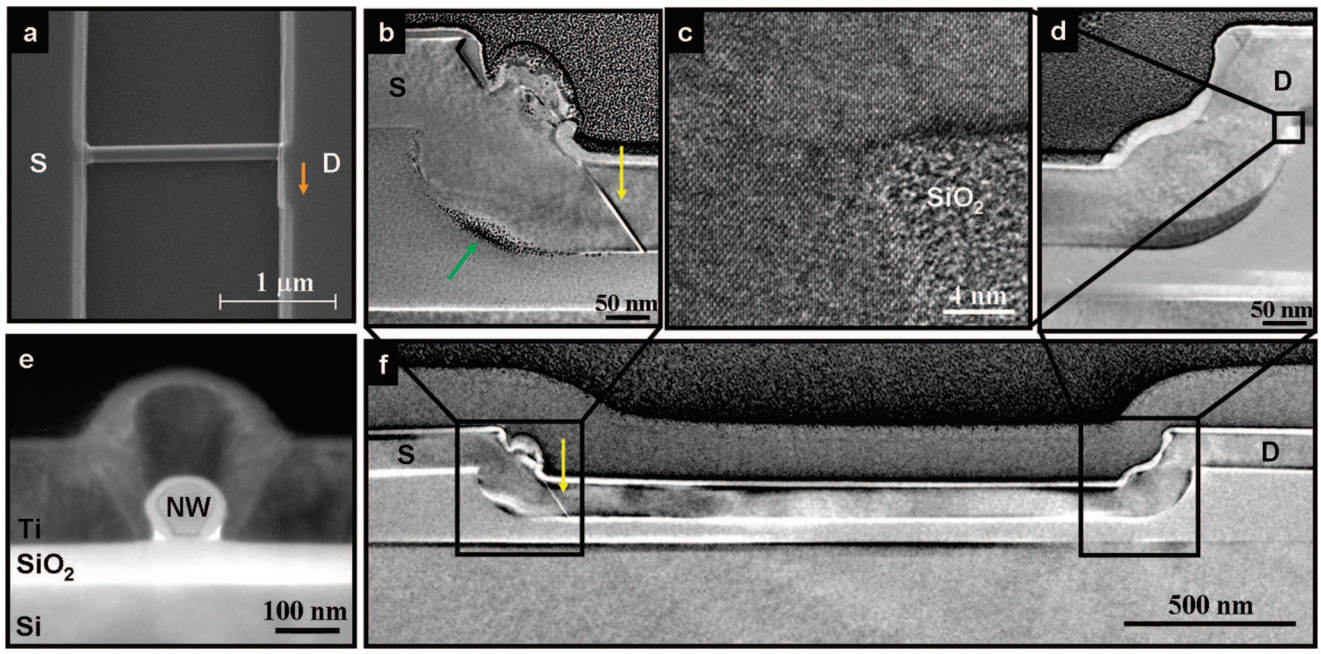

Figure 4. Electron micrographs of MOSFET fabricated from the second structure (with nitride covering the angled Si sidewall): a, plan-view scanning electron microscopy micrograph of 100 nm nanowire grown against the oxide surface between source, "S," and drain, "D"; e, perpendicular, cross-sectional transmission electron microscopy micrograph of an oxidized nanowire (NW) on BOX layer with gate oxide and a top Ti gate electrode; f, longitudinal, cross-sectional transmission electron micrograph of a nanowire connecting source and drain. Selected areas of interest are highlighted and magnified in panels b−d.

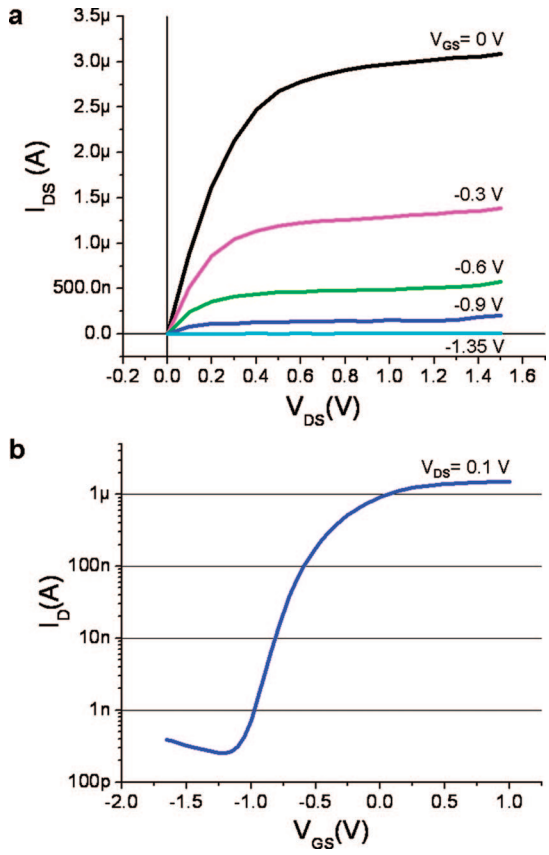

Figure 5. Transistor characteristics: a, drain characteristics for a two-nanowire device measured with gate voltages V_G from 0 to −1.35 V and the substrate at 0 V, showing good saturation; b, gate characteristics measured at drain voltage $V_D = 0.1$ V and the substrate at 0 V, showing I_{on}/I_{off} ratio of $\sim 10^4$ and inverse subthreshold slope of ∼155 mV/decade.

deposited as the top gate. This technique enabled building single and few bridging nanowire, top-gated, MOSFETs with the structure shown in Figure 1, panels g and h. Figure 1g illustrates the cross section of Figure 1h along the dashed line, showing the Ti gate and ∼13 nm thermal oxide around the nanowire.

Figure 4 shows scanning (Figure 4a) and transmission (Figure 4, panels b through f) electron micrographs (TEM), illustrating critical aspects of the growth and the device geometry. Figure 4a shows a plan-view image of a nanowire nucleated using 100 nm Au colloid and grown to connect two electrodes. With these larger diameter nanowires, the contrast change indicating a suspended nanowire section (yellow arrow in Figures 2c) was not seen (Figure 4, panels a and b). This suggests that all of the nanowire is in contact with the oxide, as confirmed by the cross sectional TEM along the length of the device shown in Figure 4f. In Figure 4, panels b, d, and f, one can see that the nanowire grew along the oxide surface connecting the source and drain. The nanowire growth started on the left side, and the nanowire grew to the right side. On the left, one can see a stacking fault (yellow arrow) in both panels b and f of Figure 4. Stacking faults are not deep-level recombination centers; instead, they act only as small potential barriers and therefore should not significantly affect device characteristics.[14,15] The fault may be caused by the nanowire growing into the flat oxide surface and being compelled to change growth direction. (In Figure 4b, the dotlike contrast highlighted by the green arrow is Pt and is an artifact of the focused-ion-beam TEM sample preparation.)

In Figure 4d one can see a hint of the interface where the nanowire made connection to the undercut Si. This interface was further examined in high-resolution TEM, shown in Figure 4c. From this image, one can see a largely epitaxial connection; most of the lattice planes are straight and no obvious dislocations are present. This image speaks to the high-quality, symmetric connection to the source and drain, which has been a problem with other nanowire devices.[16,17]

Figure 4e is a cross sectional TEM image of the nanowire device shown schematically in Figure 1g. From Figure 4e one can see the varying thickness of the thermal oxide and the faceted nature of the nanowire. The facets bounding the bottom half of the nanowire are roughly along {111}-type planes while the top of the nanowire remains curved. At this time it is not known if the nanowire grows in an asymmetric, faceted manner or if the oxidation process leads to the nanowire faceting. The oxide thickness varies from about 13 nm at the top to 21 nm at the center of a side facet.

The MOSFETs were electrically tested to study the on−off current ratio (I_{on}/I_{off}), the inverse subthreshold slope (S), the mobility, and the threshold voltage (V_T). Their characteristics are promising, especially for nonoptimized devices. Figure 5 shows the drain ($I_{DS} - V_{DS}$) characteristics for –1.35 V < V_G < 0 V and gate ($I_{DS} - V_{GS}$) characteristics at $V_{DS} = 0.1$ V for a two nanowire device. The drain characteristics show reasonable saturation (Figure 5a) and low contact resistance while the gate characteristics show an I_{on}/I_{off} ratio of ∼104. This high on−off current ratio ensures low energy consumption while in the off-state. S was about 155 mV/decade, on the low end of the range 120−609 mV/decade usually reported for similar devices.[16−20] The reasonable value of S indicates a low interface-state density, allowing good coupling between the gate and the channel, and is important for amplification and sensing applications and for charge storage. The threshold voltage extrapolated from the linear gate characteristics was approximately −0.6 V. Although the nanowire is nominally undoped, which should lead to a normally OFF MOSFET, surface states can induce mobile charge carriers even with no gate voltage applied, leading to a negative threshold voltage. In addition, possible autodoping from the heavily doped, n-type electrodes could also lead to a normally ON MOSFET. The effective mobility is calculated to be ∼510 cm^2/(V s), assuming the oxide thickness to be 13 nm and the effective width to be the nanowire diameter (100 nm). Alternatively, if the width is taken to be $\pi r = 157$ nm, the field-effect mobility is calculated to be 325 cm^2/(V s). These values again indicate the good coupling between the gate electrode and nanowire channel and a low interface-state density.

Before the gate electrode was added, transistor characteristics were measured using the SOI substrate as the gate electrode of the same device discussed above. The I_{ON}/I_{OFF} ratio was almost 10^5. The control of the nanowire conduc-

tance by the back gate shows the intimate physical and electrical contact between the nanowire and the oxide. It also suggests that a nanowire with no metal top-gate electrode can be used as a field-effect sensor with the sensor biased near the subthreshold regime, where the current is an exponential function of the charge near the exposed nanowire surface.

In summary, we have been able to engineer the nanowire growth direction so that the nanowire grows against a planar oxide surface in a ⟨110⟩-type direction. This nanowire growth geometry enables the use of conventional planar processing for device fabrication and integration. Using this structure, we demonstrated promising electrical results from prototype MOSFETs.

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Supporting Information Available: Description of the fabrication of the structures described in the paper. This material is available free of charge via the Internet at http://pubs.acs.org.

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