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Flexible Memristive Memory Array on Plastic Substrates

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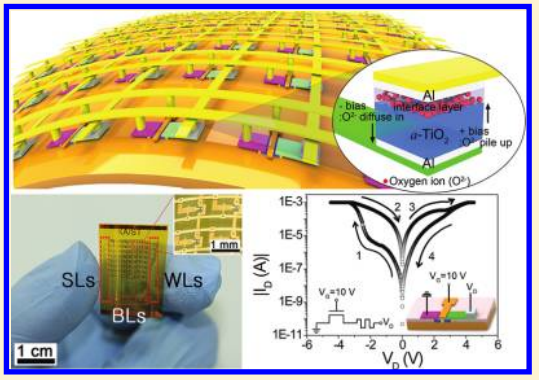
Supporting Information

ABSTRACT: The demand for flexible electronic systems such as wearable computers, E-paper, and flexible displays has recently increased due to their advantages over present rigid electronic systems. Flexible memory is an essential part of electronic systems for data processing, storage, and communication and thus a key element to realize such flexible electronic systems. Although several emerging memory technologies, including resistive switching memory, have been proposed, the cell-to-cell interference issue has to be overcome for flexible and high performance nonvolatile memory applications. This paper describes the development of NOR type flexible resistive random access memory (RRAM) with a one transistor−one memristor structure (1T-1M). By integration of a high-performance single crystal silicon transistor with a titanium oxide based memristor, random access to memory cells on flexible substrates was achieved without any electrical interference from adjacent cells. The work presented here can provide a new approach to high-performance nonvolatile memory for flexible electronic applications.



KEYWORDS: Memristor, flexible electronics, flexible nonvolatile memory, RRAM, 1T-1M

Flexible electronic systems have attracted great attention due to their advantages of excellent portability, conformal contact with curved surfaces, lightweight, and human friendly interfaces over conventional bulk silicon technology.[1−3] Many researchers have studied various flexible electronic devices such as integrated circuits (ICs),[4,5] organic light emitting diodes (OLEDs),[6] sensors,[7] and radio frequency identification (RFID) antennas.[8] Although these works have demonstrated the feasibility of flexible electronic devices, their applications have been restricted to one or just a few components of the electronics, and thus each electronic device must be integrated into a single device to perform its respective function within a flexible system. To realize such all-in-one flexible systems, the development of flexible memory is a key issue for data processing, information storage, and radio frequency (rf) communication.[9−11]

Nonvolatile resistive random access memory (RRAM) and the related memristor[12,13] (short for memory-resistor) have received attention as an alternative to charge-based memories such as dynamic random access memory (DRAM) and flash memory due to its simple structure, high switching speed, low power consumption, and high packaging density.[11,13−18] Several researchers including our group have reported flexible memristive memory with a simple cross-point-type array based on various oxide or organic materials such as GeO/HfON,[11] Al_2O_3,[15] ZnO,[16] TiO_2,[17,19] polyimide:6-phenyl-C61 butyric acid methyl ester (PI:PCBM),[20] and graphene oxide.[21]

Nonvolatile memory devices with a cross-point structure, however, suffer unavoidable cell-to-cell interference during memory access operation.[22−26] The cell-to-cell interference between neighboring memory cells occurs due to leakage current paths through adjacent low resistance state cells and induces not only unnecessary power consumption but also a misreading problem, a fatal obstacle in memory operation.[18,24−26] To fabricate a fully functional flexible memory and prevent these unwanted effects, each memory cell must be integrated with a switching component such as a transistor.[22−24] Unfortunately, most transistors built on plastic substrates (e.g., organic/oxide transistors) have insufficient effective mobility to drive conventional memory, compared to that of present silicon transistors.[27]

Herein, this paper describes a RRAM with a one transistor−one memristor (1T-1M) structure in a NOR type array on flexible substrates. High-performance flexible single crystal silicon transistors[28,29] were integrated with an amorphous titanium oxide (a-TiO_2) based memristor to control the logic state of memory. The 1T-1M RRAM unit cells were interconnected with each other through word, bit, and source lines in 8 × 8 NOR type array to control each memory unit cell independently. Finally, the first demonstration of random access memory operation of the RRAM on a flexible substrate was performed. The obtained results may open up new possibilities of realizing fully functional nonvolatile memory for high-performance flexible electronics.

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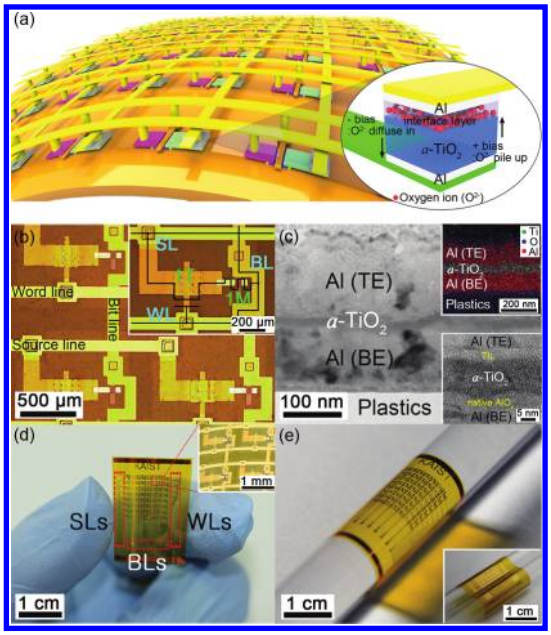

Figure 1. (a) A schematic of the device structure for an 8 × 8 matrix flexible RRAM on a plastic substrate. All memory cells are interconnected in a NOR type array for random access operation of the memory. The inset shows schematics of the model for resistive switching of the a-TiO_2 based memristor. The arrows in the inset depict the direction of the movement of oxygen ions. (b) A magnified optical image of the unit cells of RRAM array. The inset shows the structure of a memory unit cell of the 1T-1M RRAM and the corresponding circuit diagram. (c) A cross-sectional BFTEM image of an Al/a-TiO_2/Al structure on a plastic substrate. The upper inset shows the STEM energy dispersive spectroscopy (EDS) elemental mapping of Ti (green), O (blue), and Al (red). The lower inset shows the cross-sectional HRTEM image of the top interface layer (TIL) and bottom native AlO_x layer of Al/a-TiO_2/Al structure. (d) A photograph of the flexible RRAM device and a magnified view of unit cells. The metal (Au) pads are connected to WLs, BLs, and SLs for accessing each 1T-1M memory unit cell. The inset shows a magnified view of four memory unit cells and presents the mechanical stability in a bent state. (e) A photograph of the flexible RRAM device wrapped on a quartz rod. The inset shows that the flexible RRAM can provide conformal contact on curvilinear surfaces of two disposable pipets.

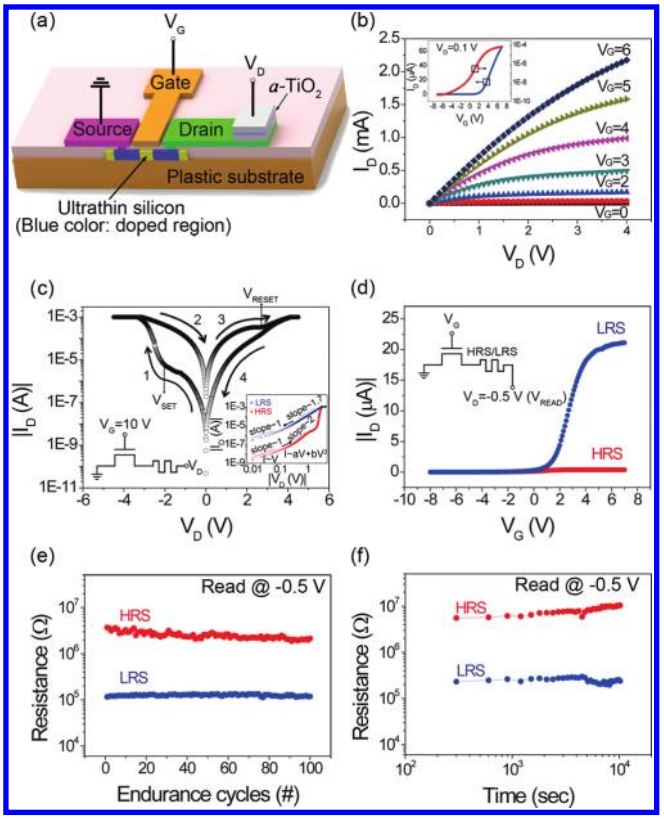

Figure 2. (a) Schematic structure of a 1T-1M RRAM unit cell consisting of two electronic parts: a NMOSFET and an a-TiO_2 based memristor. (b) Output performance of the NMOSFET (I_D−V_D curves) used as a switching transistor on a plastic substrate. The inset shows linear and log scale plots of transfer curves collected at V_D = 0.1 V. These I−V characteristics show that the performance of the flexible transistor can be used as a switching element of memory on a plastic substrate. (c) Typical drain current−voltage (I_D−V_D) characteristics of the RRAM device on a flexible substrate and circuit diagram (left inset). The arrows in the figure depict the direction of the voltage sweep. The right inset shows a double-logarithmic plot in the negative sweep region. (d) Drain current−gate voltage (I_D−V_G) curves of the 1T-1M RRAM device at a fixed reading voltage of −0.5 V with respect to the resistance state of memory and the related circuit diagram (inset). The drain currents show distinct differences depending on the state of memory, indicating that the logic state of the unit cell can be easily read at fixed reading voltage. (e) Endurance test of the RRAM measured during 100 sweep cycles. (f) Retention time of the RRAM read at −0.5 V.

Figure 1a shows a schematic of the device structure for an 8 × 8 flexible RRAM array on a plastic substrate. The n-channel metal−oxide−semiconductor field effect transistors (NMOSFET) have channel length of 10 μm, contact overlap of 20 μm, and channel width of 200 μm. Doped silicon nanomembranes (100 nm thickness) on a plastic substrate transferred from a silicon-on-insulator (SOI) wafer were used as an active layer of the transistor, as described in the author's previous papers.[28,29] For a resistance switching material, a-TiO_2 (14 nm thickness) was deposited between the Al top and bottom electrodes by plasma-enhanced atomic layer deposition (PEALD) at the drain region.[17] All memory cells was interconnected in a NOR type array through the word, bit, and source line for random access operation of the memory (see Supporting Information for details on the fabrication of a flexible RRAM on a plastic substrate, Figure S1). Resistance switching phenomenon of the a-TiO_2 based memristor is believed to be due to the drift of oxygen ions at the top interface layer as voltage-bias polarity, as depicted in the inset of Figure 1a. The top interface layer (Al−Ti−O phase) is formed during Al electrode deposition due to strong oxygen affinity of Al metal. When a sufficient negative bias is applied to the top electrode, the oxygen ions diffuse into the a-TiO_2 region, causing the device to switch to the on state.[30,31]

Figure 1b shows a magnified optical image of the unit cells of the 1T-1M RRAM array corresponding to the circuit diagram in the inset. The gate and source electrode are respectively connected to the word (WL) and source line (SL) in the row direction to control the transistor, and the Al top electrode is connected to the bit line (BL) for logic state change of a memory unit cell. The integrated transistors play a significant role of maintaining the logic state of memory cells when other cells are randomly accessed, which is the main advantage of this configuration over cross-point type circuitry where a switching element does not exist. Figure 1c shows a cross-sectional bright-field transmission electron microscopy (BFTEM) image of uniform metal−insulator−metal (MIM) layers (120 nm Al/14 nm

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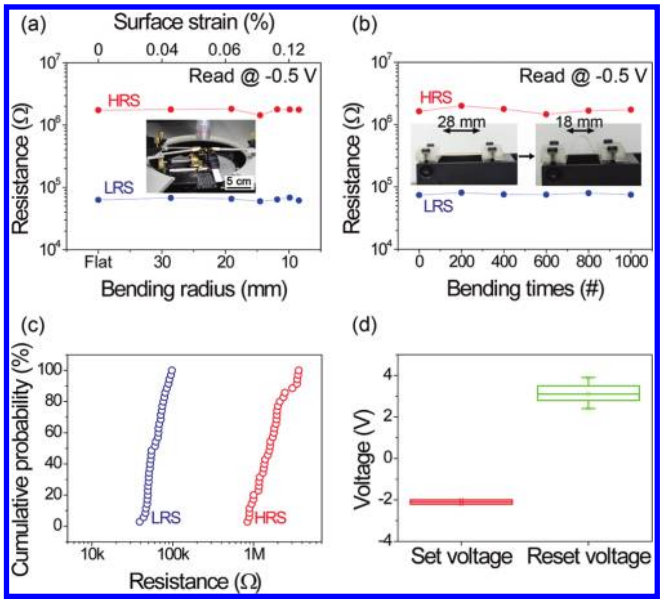

Figure 3. (a) The resistance ratio between the HRS and LRS as a function of the bending radius and surface strain. The inset is a photograph of an $I-V$ measurement being performed under a flexed condition. (b) Continuous bending fatigue test results up to 1000 iterations for the RRAM device. The insets show photographs of two repeated bending states. (c) Cumulative probability data of each the HRS and LRS obtained from $I-V$ curves of 35 unit cells. (d) SET and RESET voltage distributions of the RRAM depicted by a box-whisker plot obtained from $I-V$ curves of 35 unit cells.

a-TiO_2/120 nm Al) obtained from our memory cell fabricated on a plastic substrate. The elemental mapping of Ti (green), O (blue), and Al (red) by the scanning TEM method in the upper inset clearly indicates the existence of a middle titanium oxide layer between the two Al metal electrodes. The lower inset is a cross-sectional high-resolution TEM (HRTEM) image of stacked Al/a-TiO_2/Al layers on a plastic substrate, showing the distinct the top interface layer (TIL)[30−32] (see Supporting Information for TEM analyses of the top interface layer, Figures S2 and S3). Figure 1d presents a photograph of the flexible RRAM device and a magnified view on the plastic substrate. The flexible RRAM consists of an 8 × 8 memory cell matrix in a NOR type array with an active area of 1 × 1 cm^2 on a 25 μm thick polyimide film. The metal (Au) pads are connected to WLs, BLs, and SLs for accessing each 1T-1M memory unit cell. Figure 1e shows that this device has superb mechanical flexibility and does not fracture when rolled on a quartz rod of 10 mm diameter. Good ductility of the metal line and ultrathin inorganic materials can provide RRAM devices with good stability on flexible substrates.[17,29] The inset of Figure 1e illustrates that the flexible RRAM can provide conformal contact on a curvilinear surface. Such flexible capability will be valuable for implantable and flexible biomedical devices on wrinkled organs such as the brain and intestine.[33,34]

Figure 2a depicts the schematic structure of a 1T-1M RRAM unit cell consisting of two electronic parts: a NMOSFET and an a-TiO_2 based memristor. By applying voltage on the source/drain/gate electrodes, the logic state of the memory element can be controlled. Figure 2b shows the output performance of the NMOSFET (I_D-V_D curves) used as a switching transistor on a plastic substrate. The transistor had effective device mobility of 340 $cm^2/(V\cdot s)$ in the linear regime, obtained from the transfer curve in the inset of Figure 2b with an on/off ratio of 10^5. For resistance switching of the a-TiO_2 based memristor, current of at least roughly 300 μA is required to apply requisite voltage for switching between the top and bottom electrodes.[30] This NMOSFET device can easily fulfill this condition at low operating voltage ($I_D \sim 300$ μA at $V_D = 1$ V, $V_G = 3$ V). These results indicate that, in terms of its sufficient current level and on/off ratio, this flexible transistor using ultrathin single crystal silicon as an active layer can be used as a switching element of memory.

Figure 2c shows a typical drain current−voltage (I_D-V_D) curve of the 1T-1M RRAM device on a flexible substrate, with 10 V applied to the gate electrode in order to open the channel. The device is switched from the high-resistance state (HRS) to the low-resistance state (LRS) by sweeping the drain voltage from 0 V to a negative value over the SET voltage (V_{SET}). The LRS is retained during the voltage sweep back to a positive RESET voltage (V_{RESET}) and converts to the HRS at a higher voltage than V_{RESET}. This indicates that our RRAM device has asymmetric bipolar resistance switching (BRS) behavior with an on/off ratio of 50 at −0.5 V (reading voltage).

In order to investigate the current conduction mechanism in detail, double-logarithmic plots of the I_D-V_D curve for the negative voltage regions are illustrated in the right inset of Figure 2c. The log I_D-V_D plot of HRS shows Ohmic conduction behavior ($|I_D| \propto |V_D|$) in the low voltage region (<0.2 V) and gradually changed to a square dependence ($|I_D| \propto |V_D|^2$), as depicted in the inset of Figure 3c. This behavior is qualitatively interpreted to follow the shallow trap-associated space-charge-limited conduction (SCLC) theory, which is generally expressed by $I(V) = aV + bV^2$.[35,36] It is interesting that the slope of the log I−log V plot in the high-voltage region of the LRS is slightly lower than two (1.7). This BRS behavior of Al/a-TiO_2/Al memory devices can be explained by the change of trap distributions in the top interface layer (Al−Ti−O), which originates from the motion of oxygen ions due to external bias.[30,32] Figure 2d presents drain current−gate voltage (I_D-V_G) curves of the RRAM device at a fixed reading voltage of −0.5 V in the LRS and HRS. The drain currents show distinct differences depending on the state of memory, indicating that the logic state of the unit cell can be easily read at fixed reading voltage.[23]

Endurance and retention tests were conducted in order to investigate the reliability of the flexible RRAM. Figure 2e shows the endurance cycling test results at a reading voltage of −0.5 V obtained by repetitive on/off sweeping operation. During 100 endurance cycles, both the HRS and LRS retain their resistance values without significant change at the reading voltage, showing reproducible resistive switching. The retention property of RRAM was also characterized at room temperature to evaluate the data storage ability, and the results are shown in Figure 2f. The RRAM on the flexible substrate shows good retention characteristics up to 10^4 s without electrical degradation in both the LRS and HRS.

A mechanical bending test of the RRAM on a flexible substrate was performed in order to confirm the mechanical stability of the device for flexible memory applications, and the results are presented in panels a and b of Figure 3. Figure 3a shows the bending test results as a function of bending radii and surface strain. For the change of bending radius from 28.6 to 8.4 mm (corresponding to surface strain values ranging from 0.04 to 0.15%), the resistances ratio of the HRS and LRS does not appear to vary significantly. As shown in Figure 3b, the device also has

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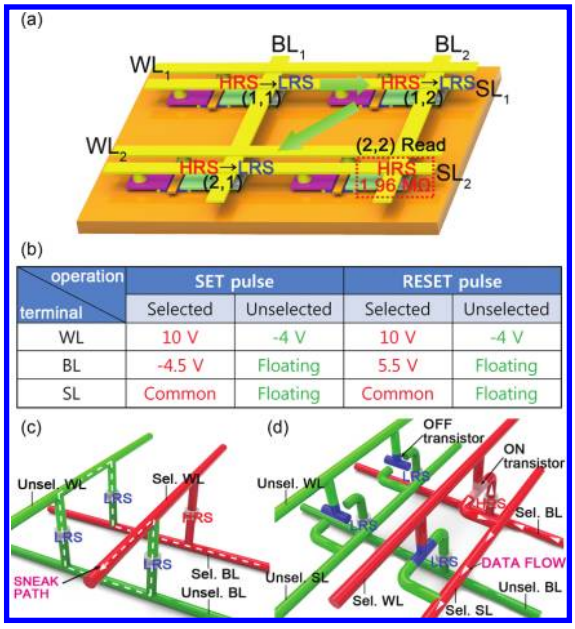

Figure 4. (a) Schematic illustration of the random access operation of 2 × 2 flexible RRAM cells. After the write process of (1, 1), (1, 2), and (2, 1) cells, the correct HRS signal (1.96 MΩ) of the selected (2, 2) cell can be read by applying the READ pulse on word and bit lines without any influence or interference from other memory cells. (b) Operation conditions for the memory cells arranged in a NOR type array. All pulse widths for SET/RESET/READ are fixed at 50 ms. (c) Illustration of a cross-point memory structure. The red and green lines indicate selected and unselected lines, respectively. The white dotted line denotes a possible misreading path (sneak path) through three neighboring low resistance cells. (d) An illustration of a 1T-1M RRAM structure. The red and green lines denote selected and unselected lines, respectively. The 1T-1M RRAM removes the electrical leakage path by turning off unaddressed memory cells and enables random access operation. The white arrows denote a correct data flow corresponding to the state of the (2, 2) cell.

good mechanical endurance during a bending fatigue test involving 1000 iterations of bending. A statistical analysis was conducted for the flexible RRAM to examine the uniformity of the device, and the results are given in panels c and d of Figure 3. The final yield of our integrated device that shows the stable 1T-1M working condition was about 60%. However, we believe that device yield would be improved if we adopt an automated fabrication process[37] or simple device structure such as one diode−one unipolar resistor (1D-1R) RRAM.[22] Figure 3c shows the cumulative probability data for each resistance state. Both the HRS and LRS exhibit a narrow distribution with good separation between the HRS and LRS. Figure 3d shows the SET and RESET voltage distributions obtained from $I-V$ curves. The distribution of the RESET voltage is slightly broader than that of the SET voltage. It seems that the contact resistance variation, caused by the nonuniform spin-on-doping (SOD) technique, more deeply influences output characteristics in positive voltage region.[38]

Figure 4a shows a schematic illustration of the random access operation for our 2 × 2 flexible RRAM cells in 8 × 8 memory arrays, and their operation conditions are summarized in Figure 4b. Fundamentally, the prevention of cell-to-cell interference during memory access operation can be confirmed by measuring 2 × 2 cells[22,24] and these results can be applied to the multi $n \times n$ memory cells operations.[22,24,25,39] The initial state of all memory cells was set to the HRS. By applying the SET pulse on the word and bit lines, (1, 1), (1, 2), and (2, 1) cells are sequentially converted from the HRS to the LRS (the writing process, see Figure S7i-iii in the Supporting Information). After the writing process of the above three cells is completed, the READ pulse (10 V to WL_2, −0.5 V to BL_2, and −4 V to WL_1) was applied to the (2, 2) cell in order to read the memory cell state. The correct HRS signal (1.96 MΩ) of the selected (2, 2) cell can be read without any influence or interference from other memory cells. However, for the case of a cross-point structure where the switching component does not exist, an independent read operation is not possible due to the electrical leakage path, called a sneak path, as illustrated in Figure 4c.[22−26] On the contrary, our 1T-1M RRAM removes the sneak path by turning off unaddressed memory cells and enables random access operation, as depicted in Figure 4d. Finally, after the (2, 2) cell was converted to the LRS by applying the SET pulse, all memory cells were returned back to the HRS in the order of (2, 2), (2, 1), (1, 2), (1, 1) by applying the RESET pulse to demonstrate the erasing process (see Figures S4−8, Supporting Information, for details of the writing/reading/erasing process).

In summary, we demonstrate a flexible 1T-1M RRAM array that is driven by high-performance flexible transistors and memristors. For fully functional and independent memory operations of write−read−erase, all memory cells were integrated with each other in a NOR type array. The developed device exhibited reliable and reproducible resistive switching, endurance, and retention properties. The flexible RRAM also had excellent mechanical stability upon harsh bending. The NOR type RRAM showed successful random access operation without any electrical interference. This flexible RRAM is expected to provide opportunities for neuromorphic devices[40] and other flexible memory structures such as 1D-1R memory[22] and three-dimensional (3D) stacking memory[41] for high device yield and packing density.

■ ASSOCIATED CONTENT

Supporting Information. The detailed fabrication procedures of flexible 1T-1M NOR type RRAM on a plastic substrate (Figure S1), ADF-STEM and BF-STEM images of Al/a-TiO_2/Al memristor (Figure S2), magnified ADF-STEM image and corresponding EDS line elemental profile taken from the top Al electrode to bottom (Figure S3), selection of the transistor turn-off voltage (Figure S4), resistance behavior in transistor OFF condition (Figure S5), and random access operation for 2 × 2 flexible RRAM cells (Figures S6−8). This material is available free of charge via the Internet at http://pubs.acs.org.

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■ REFERENCES

(1) Reuss, R. H.; Chalamala, B. R.; Moussessian, A.; Kane, M. G.; Kumar, A.; Zhang, D. C.; Rogers, J. A.; Hatalis, M.; Temple, D.; Moddel, G.; Eliasson, B. J.; Estes, M. J.; Kunze, J.; Handy, E. S.; Harmon, E. S.; Salzman, D. B.; Woodall, J. M.; Alam, M. A.; Murthy, J. Y.; Jacobsen, S. C.; Olivier, M.; Markus, D.; Campbell, P. M.; Snow, E. *Proc. IEEE* **2005**, *93*, 1239–1256.

(2) Tsutsui, T.; Fujita, K. *Adv. Mater.* **2002**, *14*, 949–952.

(3) Lee, S. Y.; Park, K. I.; Huh, C.; Koo, M.; Yoo, H. G.; Kim, S.; Ah, C. S.; Sun, G. Y.; Lee, K. J. *Nano Energy* **2011**, DOI: 10.1016/j.nanoen.2011.07.001.

(4) Cao, Q.; Kim, H. S.; Pimparkar, N.; Kulkarni, J. P.; Wang, C. J.; Shim, M.; Roy, K.; Alam, M. A.; Rogers, J. A. *Nature* **2008**, *454*, 495–500.

(5) Yu, W. J.; Lee, S. Y.; Chae, S. H.; Perello, D.; Han, G. H.; Yun, M.; Lee, Y. H. *Nano Lett.* **2011**, *11*, 1344–1350.

(6) Kwon, H. J.; Shim, H.; Kim, S.; Choi, W.; Chun, Y.; Kee, I.; Lee, S. *Appl. Phys. Lett.* **2011**, *98*, 151904–151906.

(7) Takei, K.; Takahashi, T.; Ho, J. C.; Ko, H.; Gillies, A. G.; Leu, P. W.; Fearing, R. S.; Javey, A. *Nat. Mater.* **2010**, *9*, 821–826.

(8) Abad, E.; Zampolli, S.; Marco, S.; Scorzoni, A.; Mazzolai, B.; Juarros, A.; Gomez, D.; Elmi, I.; Cardinali, G. C.; Gomez, J. M.; Palacio, F.; Cicioni, M.; Mondini, A.; Becker, T.; Sayhan, I. *Sens. Actuators, B* **2007**, *127*, 2–7.

(9) Rho, J.; Kim, S. J.; Heo, W.; Lee, N. E.; Lee, H. S.; Ahn, J. H. *IEEE Electron Device Lett.* **2010**, *31*, 1017–1019.

(10) Sekitani, T.; Yokota, T.; Zschieschang, U.; Klauk, H.; Bauer, S.; Takeuchi, K.; Takamiya, M.; Sakurai, T.; Someya, T. *Science* **2009**, *326*, 1516–1519.

(11) Cheng, C. H.; Yeh, F. S.; Chin, A. *Adv. Mater.* **2011**, *23*, 902–905.

(12) Chua, L. O. *IEEE Trans. Circuit Theory* **1971**, *18*, 507–519.

(13) Strukov, D. B.; Snider, G. S.; Stewart, D. R.; Williams, R. S. *Nature* **2008**, *453*, 80–83.

(14) Kim, K. *IEEE Tech. Dig. IEDM* **2010**, 1–4.

(15) Kim, S.; Choi, Y. K. *Appl. Phys. Lett.* **2008**, *92*, 223508–223510.

(16) Seo, J. W.; Park, J. W.; Lim, K. S.; Kang, S. J.; Hong, Y. H.; Yang, J. H.; Fang, L.; Sung, G. Y.; Kim, H. K. *Appl. Phys. Lett.* **2009**, *95*, 133508–133510.

(17) Jeong, H. Y.; Kim, Y. I.; Lee, J. Y.; Choi, S. Y. *Nanotechnology* **2010**, *21*, 115203–115208.

(18) Kang, B. S.; Ahn, S. E.; Lee, M. J.; Steftinovich, G.; Kim, K. H.; Xianyu, W. X.; Lee, C. B.; Park, Y.; Baek, I. G.; Park, B. H. *Adv. Mater.* **2008**, *20*, 3066–3069.

(19) Yun, J.; Cho, K.; Park, B.; Park, B. H.; Kim, S. *J. Mater. Chem.* **2009**, *19*, 2082–2085.

(20) Kim, J. J.; Cho, B.; Kim, K. S.; Lee, T.; Jung, G. Y. *Adv. Mater.* **2011**, *23*, 2104–2107.

(21) Jeong, H. Y.; Kim, J. Y.; Kim, J. W.; Hwang, J. O.; Kim, J. E.; Lee, J. Y.; Yoon, T. H.; Cho, B. J.; Kim, S. O.; Ruoff, R. S.; Choi, S. Y. *Nano Lett.* **2010**, *10*, 4381–4386.

(22) Cho, B.; Kim, T. W.; Song, S.; Ji, Y.; Jo, M.; Hwang, H.; Jung, G. Y.; Lee, T. *Adv. Mater.* **2010**, *22*, 1228–1232.

(23) Kim, T. W.; Choi, H.; Oh, S. H.; Wang, G.; Kim, D. Y.; Hwang, H.; Lee, T. *Adv. Mater.* **2009**, *21*, 2497–2500.

(24) Seo, J. W.; Baik, S. J.; Kang, S. J.; Hong, Y. H.; Yang, J. H.; Lim, K. S. *Appl. Phys. Lett.* **2011**, *98*, 233505–233507.

(25) Lee, M. J.; Lee, C. B.; Lee, D.; Lee, S. R.; Chang, M.; Hur, J. H.; Kim, Y. B.; Kim, C. J.; Seo, D. H.; Seo, S.; Chung, U. I.; Yoo, I. K.; Kim, K. *Nat. Mater.* **2011**, *10*, 625–630.

(26) Linn, E.; Rosezin, R.; Kugeler, C.; Waser, R. *Nat. Mater.* **2010**, *9*, 403–406.

(27) Hosono, H.; Nomura, K.; Ohta, H.; Takagi, A.; Kamiya, T.; Hirano, M. *Nature* **2004**, *432*, 488–492.

(28) Menard, E.; Lee, K. J.; Khang, D. Y.; Nuzzo, R. G.; Rogers, J. A. *Appl. Phys. Lett.* **2004**, *84*, 5398–5400.

(29) Ahn, J. H.; Kim, H. S.; Lee, K. J.; Jeon, S.; Kang, S. J.; Sun, Y. G.; Nuzzo, R. G.; Rogers, J. A. *Science* **2006**, *314*, 1754–1757.

(30) Jeong, H. Y.; Lee, J. Y.; Choi, S. Y.; Kim, J. W. *Appl. Phys. Lett.* **2009**, *95*, 162108–162110.

(31) Jeong, H. Y.; Lee, J. Y.; Choi, S. Y. *Appl. Phys. Lett.* **2010**, *97*, 042109–042111.

(32) Jeong, H. Y.; Lee, J. Y.; Ryu, M. K.; Choi, S. Y. *Phys. Status Solidi RRL* **2010**, *4*, 28–30.

(33) Viventi, J.; Kim, D. H.; Moss, J. D.; Kim, Y. S.; Blanco, J. A.; Annetta, N.; Hicks, A.; Xiao, J. L.; Huang, Y. G.; Callans, D. J.; Rogers, J. A.; Litt, B. *Sci. Transl. Med.* **2010**, *2*, 24ra22.

(34) Park, K. I.; Xu, S.; Liu, Y.; Hwang, G. T.; Kang, S. J. L.; Wang, Z. L.; Lee, K. J. *Nano Lett.* **2010**, *10*, 4939–4943.

(35) Rose, A. *Phys. Rev.* **1955**, *97*, 1538–1544.

(36) Many, A.; Rakavy, G. *Phys. Rev.* **1962**, *126*, 1980–1988.

(37) Bower, C. A.; Menard, E.; S., B. *Electronic Components and Technology Conference (ECTC), 2010 Proceedings 60th*; IEEE: Piscataway, NJ, 2010, pp 1339−1343.

(38) Streetman, B. G.; Banerjee, S. *Solid state electronic devices*, 6th ed.; Prentice Hall: Upper Saddle River, NJ, 2006; Chapter 6.

(39) Lee, M. J.; Park, Y.; Suh, D. S.; Lee, E. H.; Seo, S.; Kim, D. C.; Jung, R.; Kang, B. S.; Ahn, S. E.; Lee, C. B.; Seo, D. H.; Cha, Y. K.; Yoo, I. K.; Kim, J. S.; Park, B. H. *Adv. Mater.* **2007**, *19*, 3919–3923.

(40) Jo, S. H.; Chang, T.; Ebong, I.; Bhadviya, B. B.; Mazumder, P.; Lu, W. *Nano Lett.* **2010**, *10*, 1297–1301.

(41) Cho, B.; Song, S.; Ji, Y.; Kim, T. W.; Lee, T. *Adv. Funct. Mater.* **2011**, *21*, 2806–2829.

Supporting Information for:

Flexible Memristive Memory Array on Plastic Substrates

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1. Device Fabrication

Figure S1 shows schematics of the fabrication steps for a flexible 1T-1M NOR type RRAM. Patterned silicon nanomembranes were transferred from a SOI wafer onto a polyimide substrate (DuPont, Kapton) with a spin-cast PI precursor (Poly(amic acid), Sigma Aldrich) as an adhesive[1,2]. After transfer process, active regions of transistors were isolated by photolithography and SF_6 plasma etching. The PI precursor was fully cured at 250 °C for 1h in a nitrogen atmosphere [Figure S1a]. The gate dielectric layer, SiO_2 (~120 nm), was then deposited by PECVD at 300 °C. The source and drain contact were patterned by lithographic and buffered oxide etchant (BOE). Source, drain, and gate electrodes of Cr/Au (10nm/200nm) were deposited by a radio-frequency (RF) sputtering and defined in a single step by photolithography and wet etching [Figure S1b]. After formation of switching transistors, the Al bottom electrodes were formed at the drain regions using a radio-frequency (RF) sputtering and lift-off process [Figure S1c]. The *a*-TiO_2 (14 nm) was deposited by 270 cycles of plasma-enhanced atomic layer deposition (PEALD, ASM Genitech MP-1000) at a substrate temperature of 100 °C. Titanium tetra-iso-propoxide ($TI(OCH(CH_3)_2)_4$; TTIP) and O_2 plasma were used as Ti precursor and oxygen source, respectively [Figure S1d]. After deposition of the *a*-TiO_2 layer, the Al top electrodes were formed in the same way as the bottom electrodes [Figure S1e]. The bit lines, source lines, and word lines of Cr/Au (10nm/200nm) were patterned sequentially through a radio-frequency (RF) sputtering and wet etching [Figure S1f-h]. Spin-cast SU-8 thin layers with photo-lithographically opened interconnect access holes provided the interlayer dielectric between the metal layers.

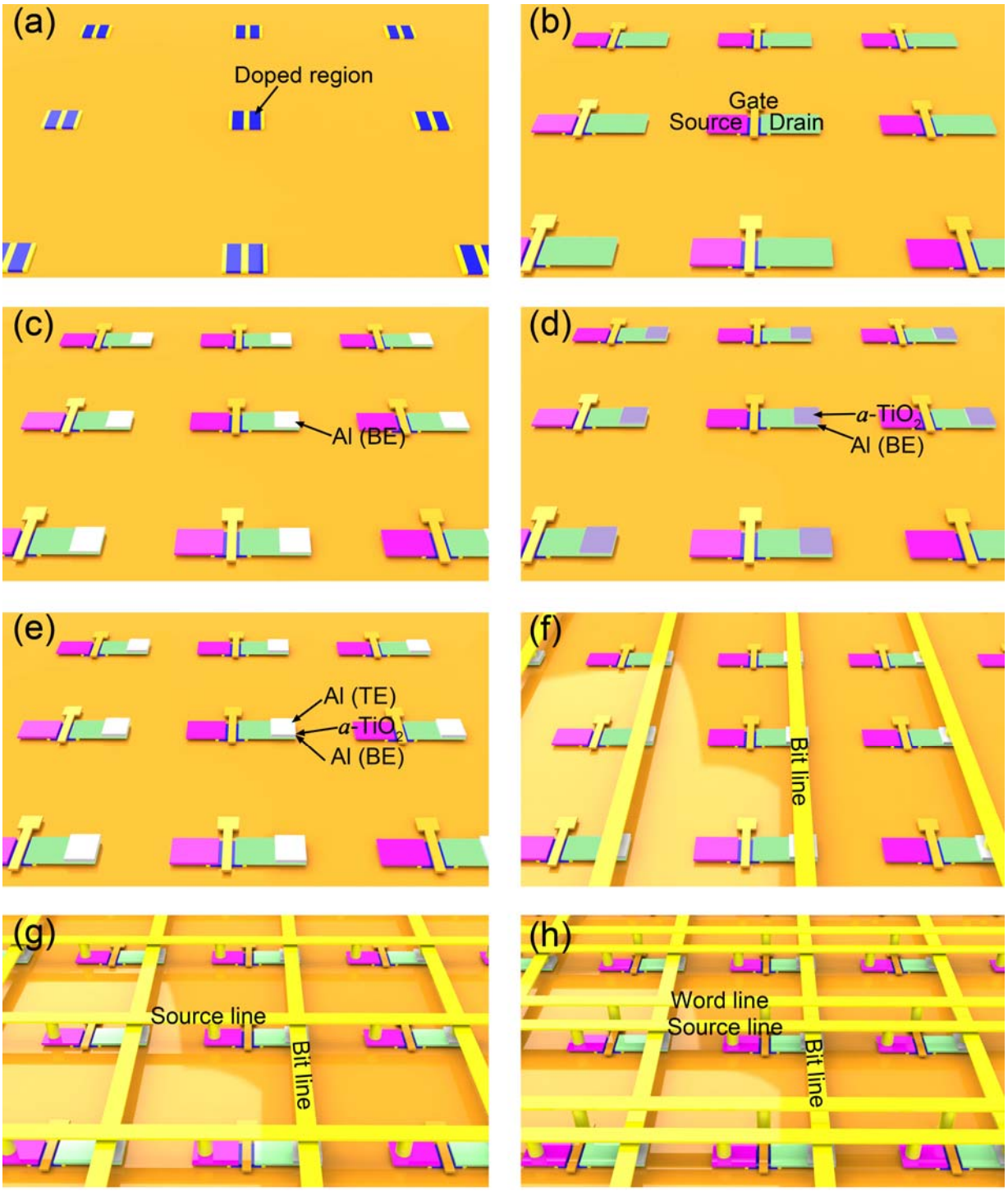

(a)
Doped region
(b)
Gate
Source
Drain
(c)
Al (BE)
(d)
a-TiO2
Al (BE)
(e)
Al (TE)
a-TiO2
Al (BE)
(f)
Bit line
(g)
Source line
Bit line
(h)
Word line
Source line
Bit line

Figure S1.

2. TEM analyses

A. ADF and BF image

The annular dark field (ADF) STEM image and BF STEM image were taken by using an aberration-corrected STEM (JEM -2100F) operated at accelerating voltage 200kV. As shown in Figure S2, a titanium oxide thin film could be clearly separated between two Al electrodes due to atomic z-contrast. From low magnification images, it can be seen that the titanium oxide thin film is uniformly deposited even on rough Al bottom electrode surface by atomic layer deposition process.

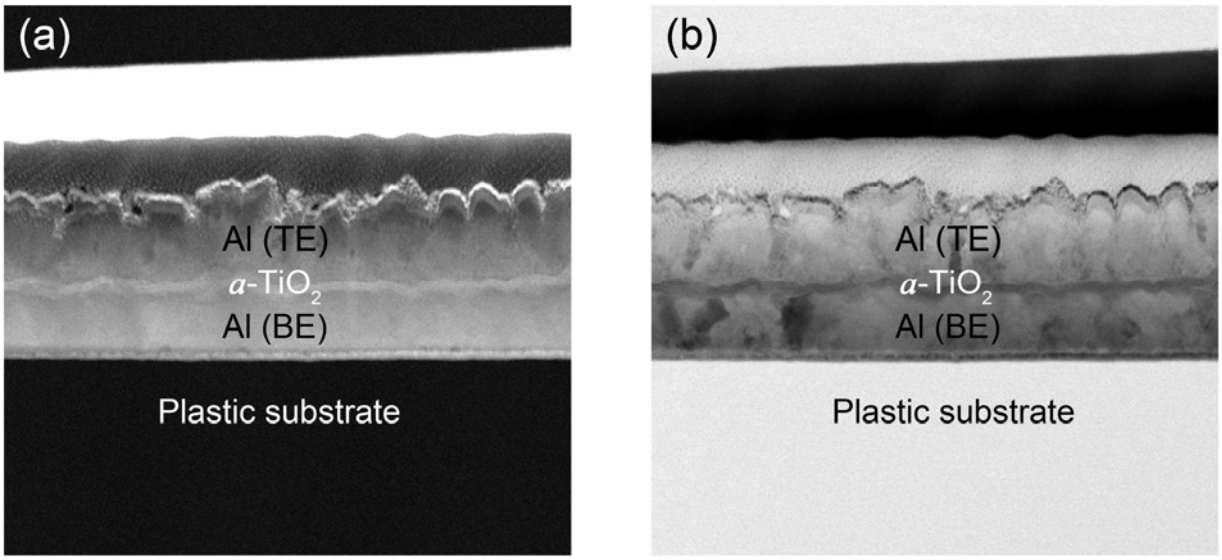


Figure S2.

B. TEM-EDS depth profile

Figure S3 shows the TEM-EDS line-scanned elemental profile between top and bottom electrodes. It is interesting that there exist a small decrease of oxygen concentration in the middle of amorphous titanium oxide region and an increase of oxygen concentration at the interface of top electrode and TiO_2. This indicates that another top interface layer (Al-Ti-O) was created by out-diffusion of oxygen ions from the *a*-TiO_2 layer[3]. These mobile oxygen ions can be attributed to the critical origin of the bipolar resistive switching of Al/*a*-TiO_2/Al memory element[4].

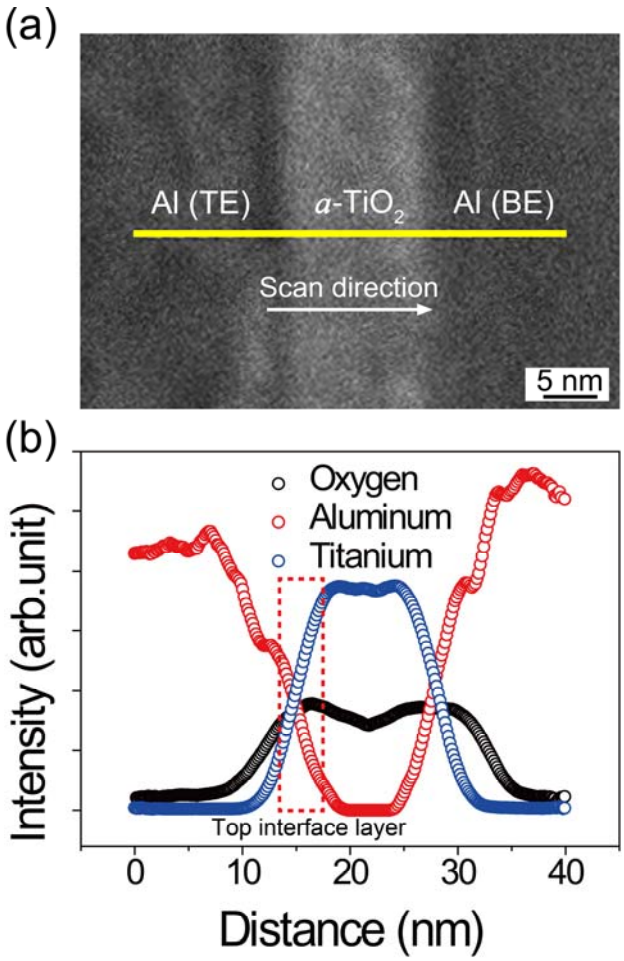


Figure S3.

3. Selection of the transistor turn-off voltage

To prevent the cross-talk interference, switching transistor components are necessary. A switching transistor should have sufficient output performance to drive memory in the ON state as well as enough resistance to remove leakage current paths in OFF state. Figure S4a-b depicts a schematic of switching Si MOS transistor on a flexible substrate and its corresponding I_D-V_D curves in negative gate/drain voltage region. From these I_D-V_D curves, the gate voltage of -4 V was selected for turning off a transistor.

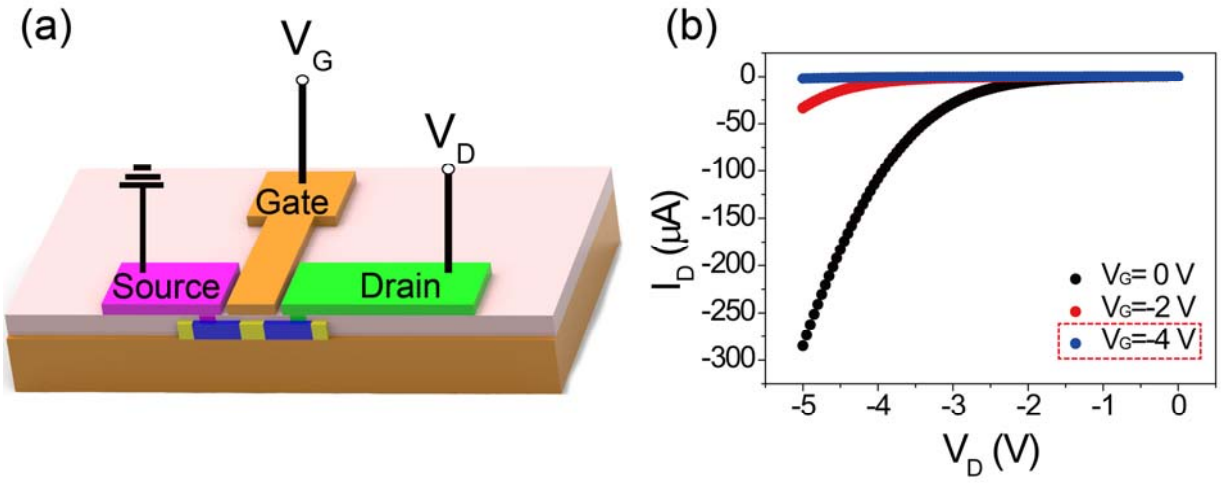
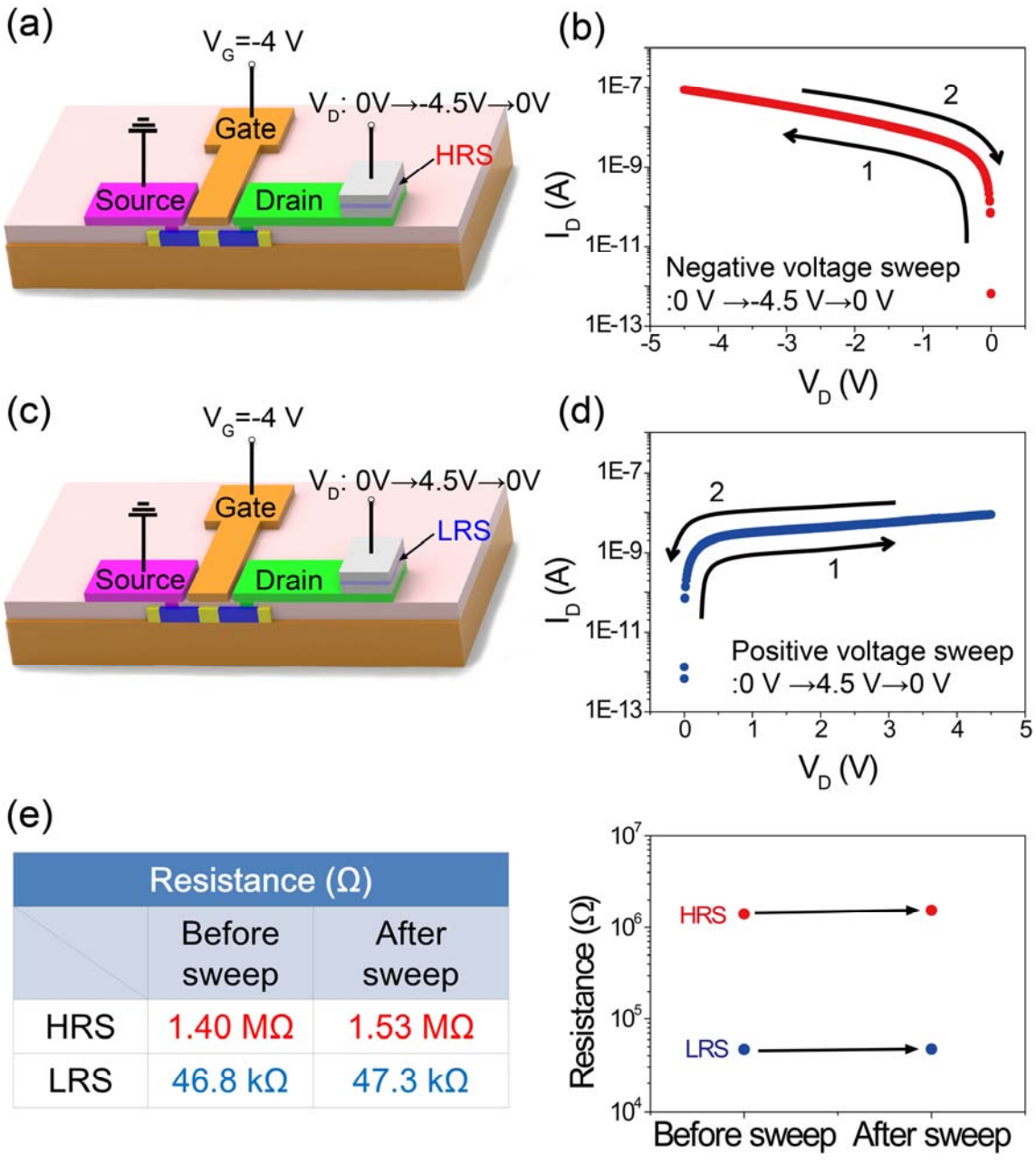


Figure S4.

4. Resistance behaviour in transistor OFF condition

Figure S5a shows a 1T-1M flexible memory cell where the negative voltage sweep (0 V → -4.5 V→ 0 V) is applied on the HRS memory element during transistor off condition and its corresponding I_D-V_D characteristics presents in Figure S5b. In contrast to memory cells with transistor on condition (V_G= 10 V) in Figure 2c, the resistance switching of HRS memory state was not observed during voltage sweep. Similarly, there is no resistance switching in a LRS memory cell during positive voltage sweep (0 V → 4.5 V→ 0 V) as shown in Figure S5c-d. Figure S5e presents that resistance changes, measured at a reading voltage condition of -0.5 V with 10 V of V_G, did not occur during negative/positive voltage sweeps.



(e)

Resistance (Ω)		
	Before sweep	After sweep
HRS	1.40 MΩ	1.53 MΩ
LRS	46.8 kΩ	47.3 kΩ

Figure S5.

5. The random access operation for 2 x 2 flexible RRAM cells

Figure S6 shows a schematic of 2 x 2 1T-1M RRAM cells (Figure S6a) and its corresponding circuit diagram (Figure S6b). The initial state of all memory cells was set to the HRS, represented in red (logic state "0").

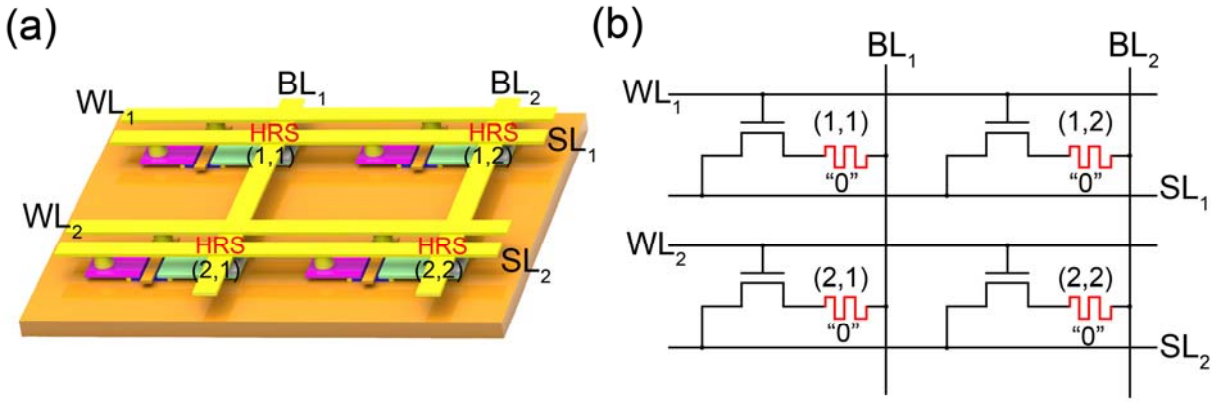


Figure S6.

A. Writing process

Figure S7 depicts the writing process of 2 x 2 flexible RRAM cells in a NOR type array. Figure S7-i shows that resistance state of the selected (1, 1) cell is converted from the HRS (logic state "0") to the LRS (logic state "1") while other memory cells maintain its original HRS states. The voltage pulse of 10 V, 50msec was applied on selected word line (WL_1) for turning on the transistor and the voltage pulse of -4 V, 50msec is applied on an unselected word line (WL_2) not only to suppress resistance change of unselected memory cells but also to remove leakage current paths. Initially, the 2.07 MΩ high resistance state of (1, 1) cell was read with the reading voltage pulse of -0.5 V, 50msec on a selected bit line (BL_1). To change the logic state of (1, 1) cell from HRS (logic state "0") to LRS (logic state "1"), the voltage pulse of -4.5 V, 50msec was applied

on a selected bit line. After switching logic state, the 86.8 kΩ low resistance state of (1, 1) cell was read with same reading voltage pulse. Similarly, logic states of other memory cells were sequentially converted from HRS "0" to LRS "1" in the order of (1, 2), (2, 1), (2, 2) through the writing process described in the above.

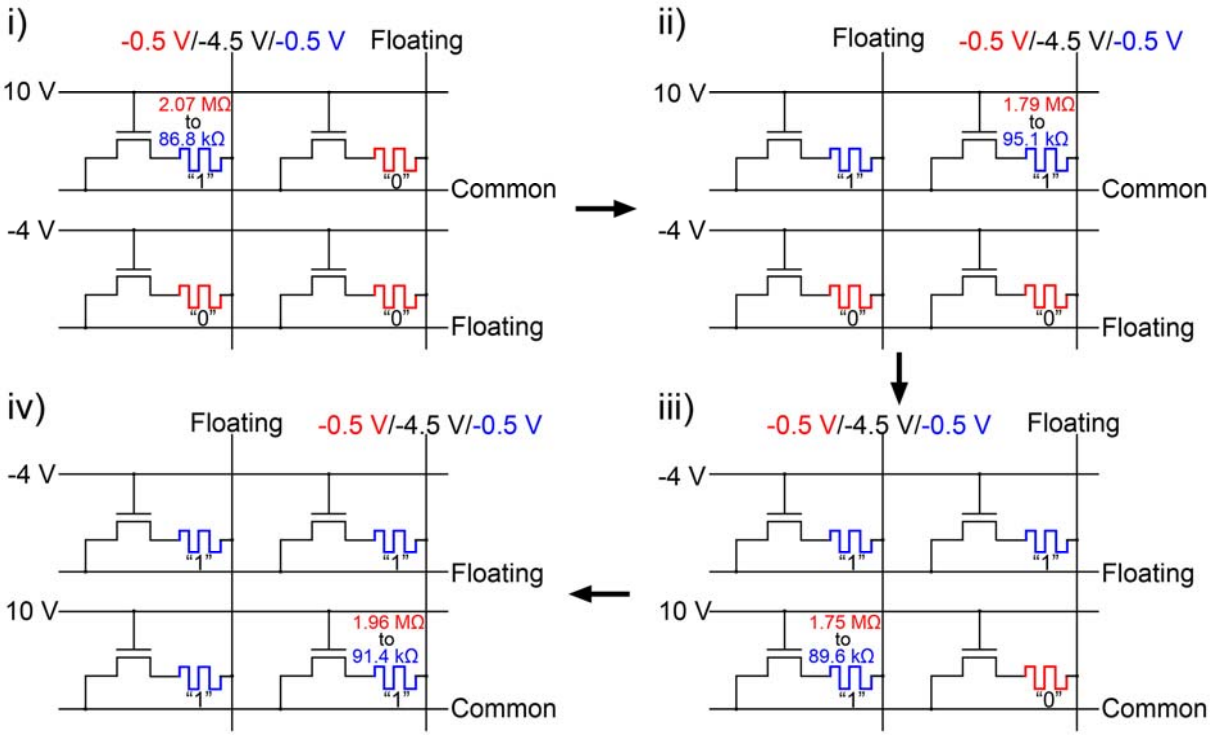


Figure S7.

B. Erasing process

Figure S8 shows the erasing process of 2 x 2 flexible RRAM cells in a NOR type array. Figure S8-i shows that resistance state of the selected (2, 2) cell is converted from the LRS (logic state "1") to the HRS (logic state "0") while other memory cells maintain its LRS states. To change the logic state of (2, 2) cell from LRS (logic state "1") to HRS (logic state "0"), the voltage pulse of 5.5 V, 50msec was applied on a selected bit line with the voltage pulse of 10 V, 50msec to WL_2 and -4 V, 50msec to WL_1. After switching logic state, the 1.60 MΩ high resistance state of (2, 2) cell was read with same reading voltage pulse. Similarly, logic states of other memory cells were sequentially converted from LRS "1" to HRS "0" in the order of (2, 1), (1, 2), (1, 1) through the erasing process described in the above.

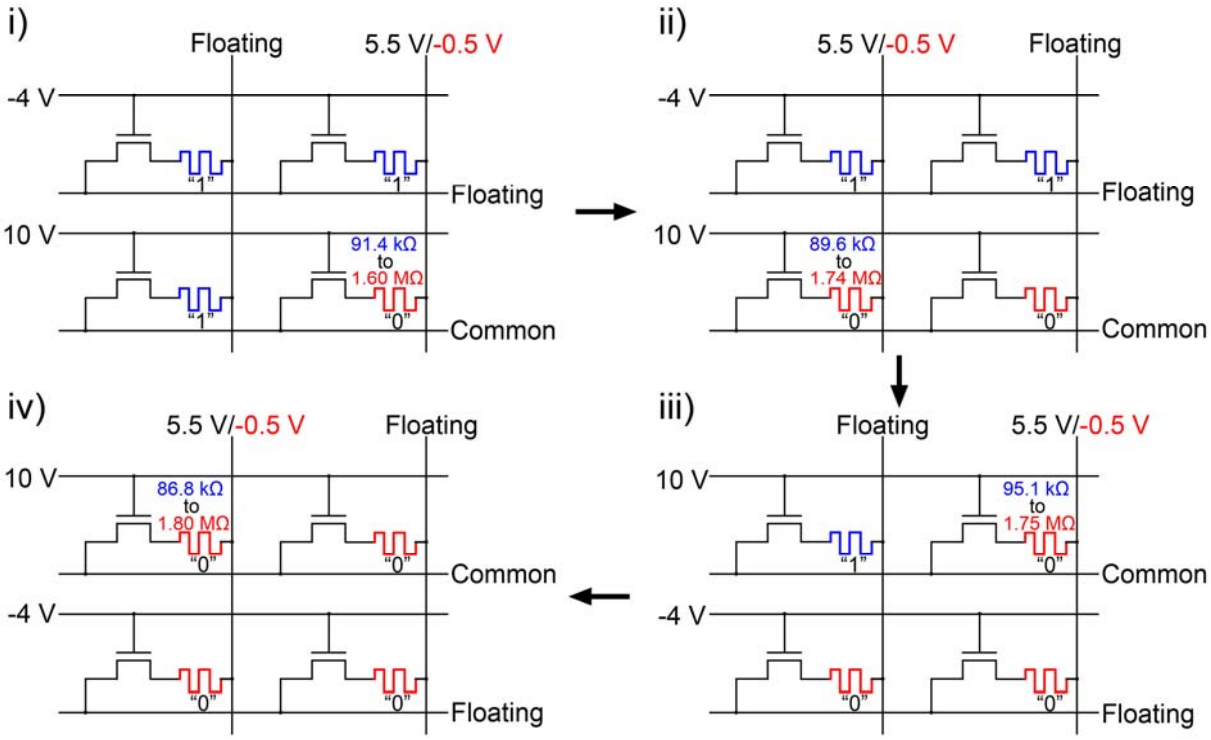


Figure S8.

REFERENCES

1. Lee, K.J. *et al.* Large-area, selective transfer of microstructured silicon: A printing-based approach to high-performance thin-film transistors supported on flexible substrates. *Adv. Mater.* **17**, 2332-2336 (2005).
2. Ahn, J.H. *et al.* Heterogeneous three-dimensional electronics by use of printed semiconductor nanomaterials. *Science* **314**, 1754-1757 (2006).
3. Jeong, H.Y., Lee, J.Y., Choi, S.Y. & Kim, J.W. Microscopic origin of bipolar resistive switching of nanoscale titanium oxide thin films. *Appl. Phys. Lett.* **95**, 162108-162110 (2009).
4. Jeong, H.Y., Lee, J.Y., Ryu, M.K. & Choi, S.Y. Bipolar resistive switching in amorphous titanium oxide thin film. *Phys. Status Solidi RRL* **4**, 28-30 (2010).

FIGURE CAPTIONS

Figure S1. Schematic illustration of the process for fabricating of flexible 1T-1M NOR type RRAM on a plastic substrate. (a) transfer-printing of silicon nanomembrane onto polyimide substrate. (b) Fabrication of switching transistors. (c) Deposition of Al bottom electrodes. (d) Deposition of *a*-TiO_2 using PEALD. (e) Deposition of Al top electrodes. (f)-(h) Interconnection of memory cells through word, source, and bit lines.

Figure S2. (a) ADF-STEM and (b) BF-STEM images of our Al/a-TiO_2/Al memristor on plastic substrate.

Figure S3. (a) Magnified ADF-STEM image and corresponding (b) EDS line elemental profile taken from the top Al electrode to bottom.

Figure S4. (a) Schematic structure of switching transistor (b) I_D-V_D curves of the switching transistor in negative gate/drain voltage region.

Figure S5. (a) Schematic structure of a RRAM unit cell in the HRS state. (b) I_D-V_D characteristics of a RRAM unit cell in the HRS state during negative voltage sweep (0 V → -4.5 V→ 0 V). (c) Schematic structure of a RRAM unit cell in the LRS state. (d) I_D-V_D characteristics of a RRAM unit cell in the LRS state during positive voltage sweep (0 V → 4.5 V→ 0 V). (e) Before and after resistance value. Any significant resistance changes do not occur.

Figure S6. (a) Schematic of 2 x 2 RRAM cells in a NOR type array. (b) Circuit diagram corresponding to Figure S6a. Red colour denotes the HRS (logic state “0”).

Figure S7. The writing process of 2 x 2 flexible RRAM cells in a NOR type array. Red color denotes the HRS (logic state “0”) and blue colour denotes the LRS (logic state “1”).

Figure S8. The erasing process of 2 x 2 flexible RRAM cells in a NOR type array. Red color denotes the HRS (logic state “0”) and blue colour denotes the LRS (logic state “1”).