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Interface Charge Induced p-Type Characteristics of Aligned $Si_{1-x}Ge_x$ Nanowires

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ABSTRACT

This study reports the electrical transport characteristics of $Si_{1-x}Ge_x$ ($x = 0-0.3$) nanowires. Nanowires with diameters of 50−100 nm were grown on Si substrates. The valence band spectra from the nanowires indicate that energy band gap modulation is readily achievable using the Ge content. The structural characterization showed that the native oxide of the $Si_{1-x}Ge_x$ nanowires was dominated by SiO_2; however, the interfaces between the nanowire and the SiO_2 layer consisted of a mixture of Si and Ge oxides. The electrical characterization of a nanowire field effect transistor showed p-type behavior in all $Si_{1-x}Ge_x$ compositions due to the Ge−O and Si−O−Ge bonds at the interface and, accordingly, the accumulation of holes in the level filled with electrons. The interfacial bonds also dominate the mobility and on- and off-current ratio. The large interfacial area of the nanowire, together with the trapped negative interface charge, creates an appearance of p-type characteristics in the $Si_{1-x}Ge_x$ alloy system. Surface or interface structural control, as well as compositional modulation, would be critical in realizing high-performance $Si_{1-x}Ge_x$ nanowire devices.

The downscaling of electronic devices is a critical issue in modern information industries. In this regard, semiconductor nanowires have drawn considerable attention as the building blocks for electronic devices downscaled to nanometer devices with superior performance.[1,2] Nanowires offer thermodynamically stable features and are typically defect-free and single-crystalline and thus have a number of advantages over thin films with respect to high-performance nanoscale devices.[3,4] Meanwhile, a large surface area to active channel volume ratio is accompanied by downscaling of devices. It is also well-known that the physical and chemical properties of nanomaterials, including nanowires, are dominated by their large surface area.[5−8] Thus, it is reasonable to assume that the performance of downscaled devices is significantly affected by the channel surfaces. Addressing the effect of the surface is crucial in achieving high-performance nanoscale electronic devices.

In the present work, we grew $Si_{1-x}Ge_x$ alloy nanowires ($x = 0-0.3$) and studied the electrical properties of the field effect transistors based on the nanowires. The $Si_{1-x}Ge_x$ system is attractive due to its compatibility with conventional complementary metal oxide semiconductor (CMOS) technology as well as band gap modulation between the end members of Si (1.1 eV) and Ge (0.7 eV).[9−11] Our study demonstrates that band gap modulation is readily achievable in single-crystalline $Si_{1-x}Ge_x$ nanowires. All nanowires exhibited p-type characteristics, and their mobility and on- and off-current ratio are decreased with Ge content. A high-resolution photoemission spectroscopy (PES) study indicated that these electrical properties are due to the interfacial Si−O−Ge or Ge−O bonds.

Compositionally controlled $Si_{1-x}Ge_x$ nanowires were synthesized using Au catalyst deposited silicon(111) substrates at 900−1000 °C in a horizontal hot-wall chemical vapor transport system. Figure 1a−c shows the scanning electron microscopy (SEM) images of the $Si_{1-x}Ge_x$ nanowires controlled for Ge content. The $Si_{1-x}Ge_x$ nanowires for $x = 0.05$, 0.15, and 0.3 were well-aligned on the substrates, and the diameter of these nanowires ranged from 50 to 100 nm. The composition of the aligned $Si_{1-x}Ge_x$ was varied by changing the growth temperature or the substrate distance from the Ge powder or both. Figure 1d shows a typical high-resolution transmission electron microscopy (HRTEM) image for the nanowires. The single-crystalline nature with a thin layer of native oxide can be seen in the HRTEM image. The selected

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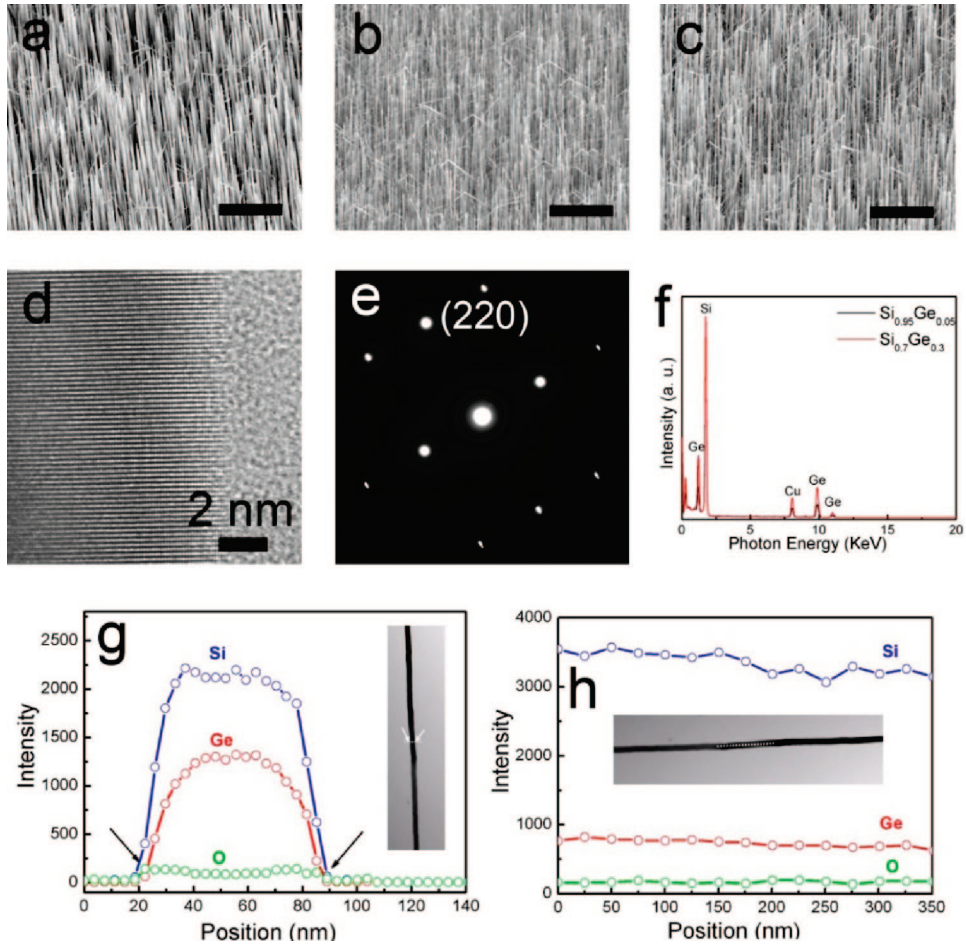

Figure 1. Synthesis and structural characterization of the $Si_{1-x}Ge_x$ nanowires. SEM images of $Si_{0.95}Ge_{0.05}$ (a), $Si_{0.85}Ge_{0.15}$ (b), and $Si_{0.7}Ge_{0.3}$ nanowires (c) well-aligned on the Si(111) substrates. The scale bar in the images is 15 μm. (d) Typical HRTEM image of controlled growth $Si_{1-x}Ge_x$ nanowires, showing the single-crystalline and defect-free nature. (e) SAED pattern, taken along the [001] zone axis that confirms the diamond structure of the wire with [110] growth direction. (e) Typical EDS spectra of $Si_{0.95}Ge_{0.05}$ and $Si_{0.7}Ge_{0.3}$ nanowires. EDS line profiles in both radial (g) and axial (h) directions of the nanowire with a diameter of 80 nm, showing that composition of native oxide is primarily SiO_x and any evidence of phase inhomogeneity is not found.

area electron diffraction (SAED) pattern recorded along the [001] zone axis, as shown in Figure 1e, indicates that the nanowires grew in the [110] direction. Figure 1f shows the relative composition of Si and Ge in the $Si_{1-x}Ge_x$ nanowires through an energy-dispersive spectroscopy (EDS) analysis, as representatively shown for the $Si_{0.95}Ge_{0.05}$ and $Si_{0.7}Ge_{0.3}$ nanowires. We observed compositional homogeneity for each nanowire with an EDS line scan. The profiles in both the radial and axial directions of the wire show that the composition of the native oxide is primarily SiO_x and any evidence of phase inhomogeneity was not found (Figure 1g,h); that is, no obvious Ge segregation within the nanowire was observed, as often found in thin film chemical vapor depositions.[12,13] This finding implies that the alloying of Si and Ge was appropriate, and it forms random substitutional alloy nanowires. The synchrotron X-ray diffraction (XRD) patterns of the aligned $Si_{1-x}Ge_x$ nanowires were indexed to a diamond structure (Supplementary Figure S01, Supporting Information). The shifts in the (111) Bragg peak to lower angles from that of the Si nanowires to that of the Ge nanowires were observed with an increasing Ge content in the $Si_{1-x}Ge_x$ nanowires. The valence band spectra for the $Si_{1-x}Ge_x$ nanowires indicated that the Fermi levels systematically shift toward the valence band maximum (VBM), from that of the Si nanowires to that of the Ge nanowires with an increasing Ge content (Supplementary Figure S02, Supporting Information). This indicates that band gap modulation of the $Si_{1-x}Ge_x$ nanowires between the Si and Ge nanowires is achieved by the Ge content.

To determine the electrical properties of the $Si_{1-x}Ge_x$ nanowires, we prepared nanowire-based field effect transistor (FET) structures. Figure 2a,b shows the current versus the gate bias voltage curves ($I-V_G$) of $Si_{0.95}Ge_{0.05}$ and $Si_{0.7}Ge_{0.3}$ nanowires, respectively. Although the Si nanowires exhibited an n-type gate response (not shown), the $Si_{1-x}Ge_x$ nanowires for $x = 0.05$ and 0.3 clearly showed a field effect response characteristic of a p-type semiconductor with conductance decrease under positive gate voltages, showing the achievement of the full depletion of the carriers. We also observed p-type behavior for the $Si_{0.85}Ge_{0.15}$ nanowires. The insets in Figure 2a,b show the SEM images of the nanowire transistor with a source−drain length of approximately 1 μm. Ge nanowires also clearly show the p-type gate response, seen as a conductivity decrease with a positively increasing gate

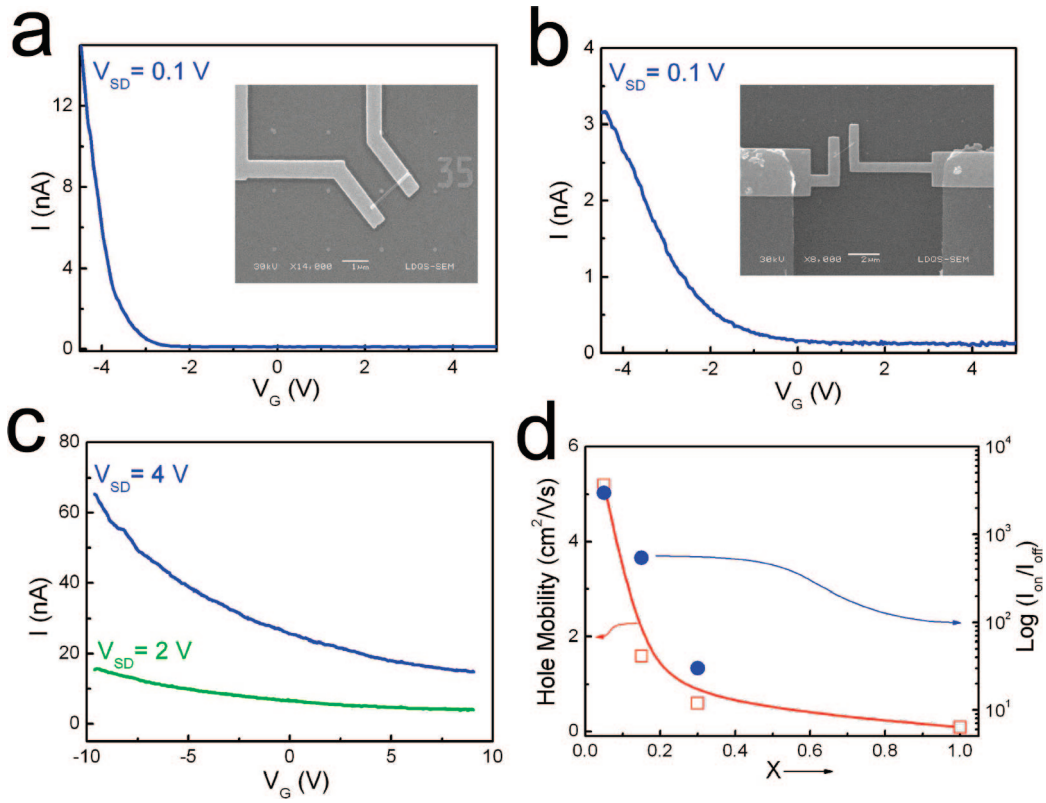

Figure 2. $I-V$ characteristics and their gate potential responsibility. Current versus gate voltage ($I-V_G$) curves of $Si_{0.95}Ge_{0.05}$ (a) and $Si_{0.7}Ge_{0.3}$ (b) nanowires. Insets in panels a and b are SEM images of an individual nanowire-based field effect transistor device with Ni/Au electrodes. (c) Current versus gate voltage ($I-V_G$) curves of a pure Ge nanowire. An individual Ge nanowire contacted with Ti/Au (60/50 nm) by evaporation. Prior to the metal-electrode deposition, the contact area of the nanowires was treated in buffered HF (3:1) to remove a thin oxide layer from the surface of the nanowire. To form stable electrical contacts between the nanowires and Ti/Au electrodes, the samples were annealed in an Ar atmosphere using rapid thermal annealing (RTA). (d) Average hole mobility and I_{on}/I_{off} of p-type $Si_{1-x}Ge_x$ nanowires as a function of Ge concentration.

voltage (V_G) (Figure 2c and Supplementary Figure S03, Supporting Information), resulting from the hole accumulation induced by trapped negative surface charges related to the surface.[14]

Next, we determine the mobility of the nanowire transistors. In general, the mobility is extracted in a linear regime of measured current−voltage characteristics by neglecting contact resistance.[15,16] However, the contact resistance in this study cannot be neglected because the electrical transport of the undoped $Si_{1-x}Ge_x$ nanowires shows that nonlinear behavior (Supplementary Figure 03, Supporting Information). We thus use an equation that reflects the non-negligible contact resistance to determine the mobility more precisely (Supporting Information).[17,18] We also measured the substantial channel length of the nanowire transistors. It has been reported that the active channel length of Si nanowire FET decreases with nickel silicide contact.[19] Accordingly, we have investigated the effect of annealing on the channel length of $Si_{1-x}Ge_x$ nanowire transistor by fabricating the transistors on the membrane and observing the contact region by transmission electron microscopy. Our results indicate that the channel length of the transistor is shortened by the formation of nickel silicides at the source and drain contact regime.[20] For example, a $Si_{0.95}Ge_{0.05}$ alloy nanowire transistor has a channel length (i.e., the distance between source and drain) of 1.5 μm; however, it shrinks to ~140 nm after annealing by the formation of nickel silicides. Similarly, the $Si_{70}Ge_{30}$ alloy nanowire device channel length shrank to ~420 nm. By the measurements, we can determine the rate of silicide formation in the nanowires for each composition and then reasonably estimate the substantial active channel lengths (Supplementary Table S01, Supporting Information). We measured the electrical transport from ten devices for each composition and confirmed the reproducibility.

Figure 2d shows the calculated hole mobility and the ratio of on- and off-current (I_{on}/I_{off}) of the p-type $Si_{1-x}Ge_x$ nanowires by considering the contact resistance and the substantial active channel length. As shown, the mobility and I_{on}/I_{off} decrease with Ge contents. The outcome indicates that the mobility is dominated by the oxygen component with Ge−O or Si−O−Ge bonds at the interfaces because they act as the surface trap levels (refer to Figure 3). Increase of the trapped negative surface states with Ge content decreases the electrical coupling between the gate and the nanowires and gives rise to a capacitance. The I_{on}/I_{off} is also dominated by the surface trap level and thus decreases with Ge content. The lower mobilities in the $Si_{1-x}Ge_x$ and Ge nanowires compared with those of bulk or planar devices may be due to the critical role of surface trap levels. Therefore, although composition-modulated alloy scattering with Ge content could not be excluded, it is believed that the trapped interface

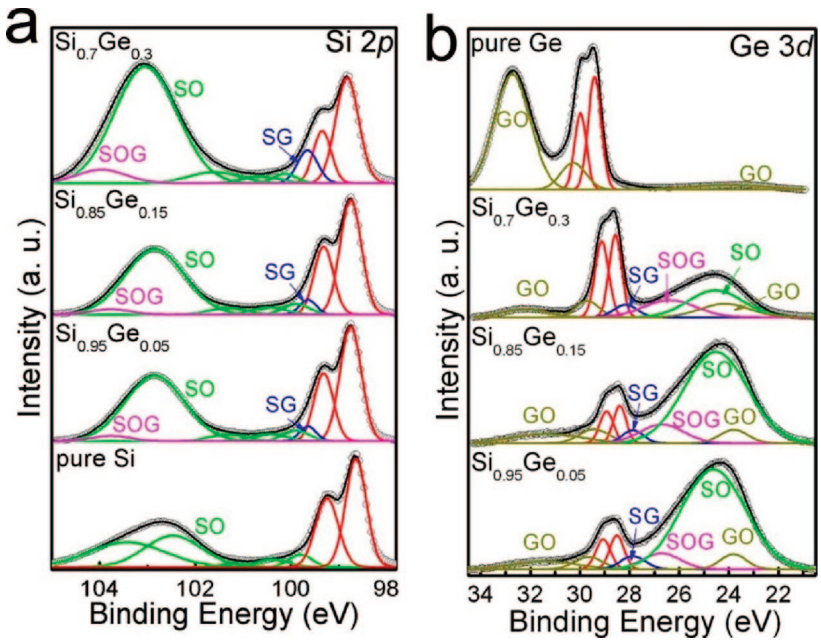

Figure 3. Surface distribution of $Si_{1-x}Ge_x$ nanowires from high-resolution PES. Si 2p (a) and Ge 3d (b) core level spectra of $Si_{1-x}Ge_x$ nanowires with Ge content. SG and SO denote Si−Ge bonds and four oxidation states (SO = Si^{1+} + Si^{2+} + Si^{3+} + Si^{4+}), respectively. GO and SOG mark GeO_x and Si−O−Ge bonds (mixture of Si and Ge oxides), respectively.

charges dominate the electrical transport in $Si_{1-x}Ge_x$ nanowire transistors.

Synchrotron radiation photoemission spectroscopy (SRPES) experiments were performed on $Si_{1-x}Ge_x$ nanowire mats to investigate the species on the nanowire surfaces. Figure 3a shows the Si 2p core-level spectra of the Si and $Si_{1-x}Ge_x$ nanowires with the native oxide. Spin−orbit splitting and area ratio values of 0.60 eV and 1:2 for the $2p_{3/2}$−$2p_{1/2}$ doublet were considered for each sample, as shown in the fitting curves. The peaks of the Si^0 2p spectra shift slightly toward higher binding energy with an increasing Ge content because the chemical state of the $Si_{1-x}Ge_x$ nanowires was changed by forming the small peak of the Si−Ge bonds (SG) at the interface regime. Each oxidation state (SO = Si^{1+} + Si^{2+} + Si^{3+} + Si^{4+}) is also characterized by its energy shift relative to Si^0. Four oxidation states (SO) of the pure Si nanowires can be found with chemical shifts in agreement with those reported for a classical, as-grown SiO_2/Si interface.[21,22] Increasing with the Ge content, an additional oxidation state SOG appears in the Si^{4+}, shifted to a higher binding energy relative to Si^{4+} as it increases with the Ge content. SOG is related to the Ge contribution to the Ge 3d spectra and is therefore assigned to Si−O−Ge bonds formed from the interfacial Si^{4+} oxidation states. With the Ge content, the level of GeO_x (GO) increases slightly, while the formation of SiO_2 increases dramatically. This means that the native oxide of the $Si_{1-x}Ge_x$ nanowires is dominantly related to SiO_2 (refer to the EDS line scan results). Importantly, the interface layer consisted of a mixture of Si and Ge oxides (SO, GO, and SOG), dependent on the Ge content. This finding is supported by O 2s (near 25 eV) peaks of the pure Ge and $Si_{1-x}Ge_x$ nanowires. The zero-valent Ge^0 states in the pure Ge nanowires peaked in the 3d spectrum between 29.8 and ~29.95 eV, and the GeO_x were between 32.7 and ~33 eV, indicating that the curve fittings reveal the spin−orbit splitting of Ge^0 and the native oxide peaks corresponding to the combinations of GeO and GeO_2. However, as shown in Figure 3b, the magnitude of the O 2s in the $Si_{1-x}Ge_x$ nanowires increases as the Ge content decreases, compared with that of the pure Ge nanowires. The amount of native oxide peaks in Ge 3d is consistent with that of O 2s. Interestingly, the level of SOG (Si−O−Ge) and GO (GeO_x) bonds decreases as the Ge content decreases, while formation of the SO (SiO_2) increases (fitting curves in Figure 3b). These results further confirm that the native oxide of $Si_{1-x}Ge_x$ nanowires is dominated by SiO_2 and the interface layer consisted of a mixture of Si and Ge oxides. The peaks of the Ge^0 3d spectra also shifted slightly toward the lower binding energy with a decreasing Ge content by forming a small peak of Si−Ge bonds (SG) at the interface regime. Meanwhile, the higher Pauling's electronegativity of the Ge relative to the Si yields an enhanced charge transfer from the Ge atom to the SOG bond at the $Si_{1-x}Ge_x$ nanowire interface, resulting in a shift of the Si 2p and Ge 3d core levels in the Si−O−Ge to a higher binding energy relative to the SiO_2.

Based on our observation, the carrier transport behaviors in the intrinsically as-grown $Si_{1-x}Ge_x$ nanowires can be explained by the formation of the Ge−O and Si−O−Ge bonds in the interface of the nanowire. Si nanowires show n-type characteristics through vacancy-related defects at the surface or in themselves, called the basic point defects in covalent semiconductors,[23] although the nanowires are typically single-crystalline and defect-free (Figure 4a). Meanwhile, the pure Ge nanowires exhibit the field effect response characteristics of p-type semiconductors. It is well-known that Ge tends to accumulate holes at the semiconductor surface as a result of the trapped negative surface charge.[24]

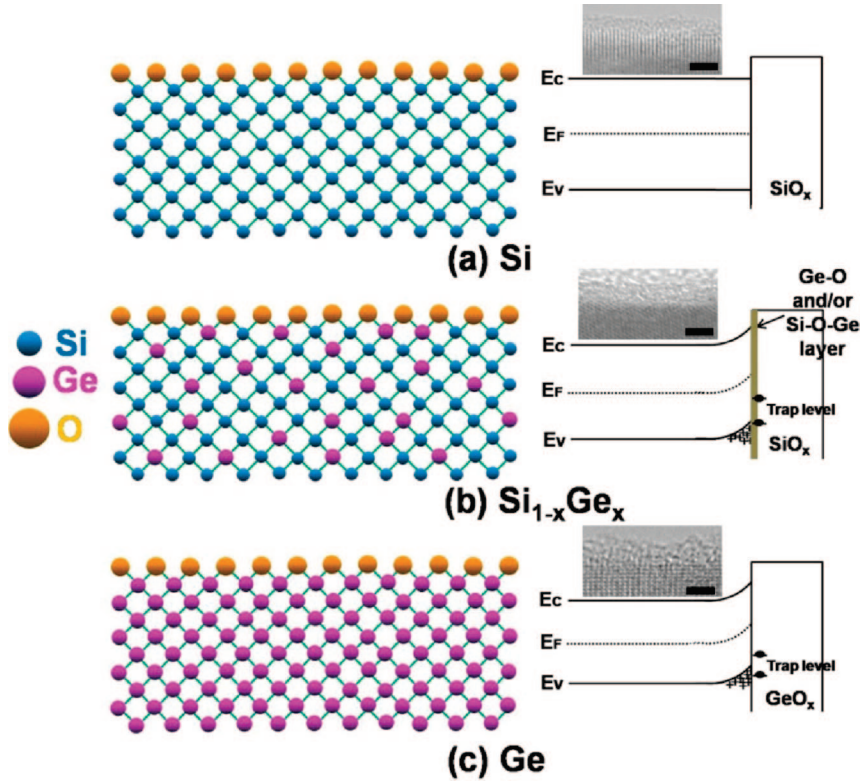

Figure 4. Schematic illustration of energy diagram. (a) Surface layer (left) and band structure (right) of pure Si with native oxides, showing n-type characteristics by vacancy-related defects in covalent semiconductors. (b) In the case of $Si_{1-x}Ge_x$ nanowires, the interface layer consists of a mixture of Si and Ge oxides, dependent on the Ge content (left). The oxygen component (Ge−O or Si−O−Ge bonds) acts as a trap for negative surface charge, resulting in hole accumulation by the interface charge, or upward band bending, to maintain charge neutrality by bending the valence and conduction bands up near the interface (right). (c) Surface layer of pure Ge (left) and band structure of Ge with available trap levels at the semiconductor surface (right). If the levels are lower than E_F, the trap level will be filled with electrons, resulting in a hole accumulation induced by trapped negative surface charge related to the surface. Insets are TEM images of the nanowires with native oxide. The scale bar in images is 1 nm.

As shown in Figure 4c, the Ge surface layer with a high density of surface states ($>10^{14}$ cm^2) has electron trap levels located ~0.15 eV below the middle of the band gap by GeO_x and a hole occurs in the level filled with an electron, resulting in p-type behavior by the trap level located below the Fermi level.[14,25] For the $Si_{1-x}Ge_x$ nanowires, increasing with the Ge content, the interface layer of the nanowire consists of a mixture of Si and Ge oxides (Si−O, Ge−O, and Si−O−Ge), dependent on the Ge content, while the native oxide is dominant relative to SiO_2 (left in Figure 4b). The formation of Ge−O and Si−O−Ge bonds at the interface may be critical for understanding the p-type behavior of the SiGe alloy system. The oxygen component in the interface acts as a trapped negative surface charge related to the Ge−O or Si−O−Ge bonds. The trap level is located below the Fermi level and then bends the valence and conduction bands near the interface (right in Figure 4b). The level is filled with an electron when the semiconductor Fermi level is higher than the trap level, resulting in hole accumulation via the interface charge, or upward band bending, to maintain the neutral charge in the nanowire. The interface induced hole accumulation creates an appearance of p-type semiconductor field effects intrinsic in the $Si_{1-x}Ge_x$ nanowires. The trap level at the interfaces also dominates the carrier transport characteristics such as mobility and on- and off-current ratio indicate that the large area of interfaces or surfaces has a dominant role in the electrical properties of the SiGe nanowires devices, and consequently, surface or interfacial structure control is critical in developing high-performance $Si_{1-x}Ge_x$ nanowire devices.

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Supporting Information Available: Experimental procedures, XRD scans, change of valence band spectra, $I-V_{SD}$ curves, and electric transport characteristics. This material is available free of charge via the Internet at http://pubs.acs.org.

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