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Toward Optimized Light Utilization in Nanowire Arrays Using Scalable Nanosphere Lithography and Selected Area Growth

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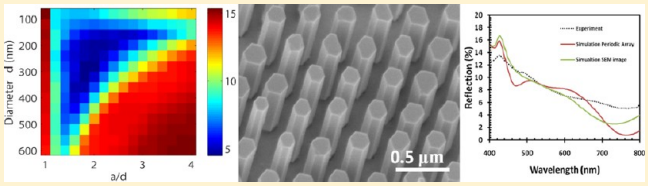
Supporting Information

ABSTRACT: Vertically aligned, catalyst-free semiconducting nanowires hold great potential for photovoltaic applications, in which achieving scalable synthesis and optimized optical absorption simultaneously is critical. Here, we report combining nanosphere lithography (NSL) and selected area metal−organic chemical vapor deposition (SA-MOCVD) for the first time for scalable synthesis of vertically aligned gallium arsenide nanowire arrays, and surprisingly, we show that such nanowire arrays with patterning defects due to NSL can be as good as highly ordered nanowire arrays in terms of optical absorption and reflection. Wafer-scale patterning for nanowire synthesis was done using a polystyrene nanosphere template as a mask. Nanowires grown from substrates patterned by NSL show similar structural features to those patterned using electron beam lithography (EBL). Reflection of photons from the NSL-patterned nanowire array was used as a measure of the effect of defects present in the structure. Experimentally, we show that GaAs nanowires as short as 130 nm show reflection of <10% over the visible range of the solar spectrum. Our results indicate that a highly ordered nanowire structure is not necessary: despite the "defects" present in NSL-patterned nanowire arrays, their optical performance is similar to "defect-free" structures patterned by more costly, time-consuming EBL methods. Our scalable approach for synthesis of vertical semiconducting nanowires can have application in high-throughput and low-cost optoelectronic devices, including solar cells.



KEYWORDS: *GaAs nanowires, selected area MOCVD, nanosphere lithography, light absorption, simulation*

Semiconductor nanowires have the potential to find applications in high performance electronic and optoelectronic devices. Various nanoscale devices such as logic gates,[1] light emitters,[2−4] and photodetectors[5] have been demonstrated using group IV and III−V nanowires. Vertically aligned nanowires have shown promising results when used to fabricate light emitters[6−10] and photovoltaic devices.[11−15] The small contact area between nanowires and substrate allows them to accommodate more strain than planar structures, thus minimizing the lattice-matching constraints in heteroepitaxy as compared to conventional thin film growth. In relation to photovoltaic applications, a vertically aligned periodic nanowire array structure has the potential to improve optical absorption.[16−18]

The majority of nanowires used in nanoelectronic devices are synthesized using the vapor−liquid−solid (VLS) growth method using metal catalysts.[19] Although this technique results in synthesis of a wide variety of nanowires, potential contamination by metal catalysts such as Au can produce midgap defects and hence be detrimental to the performance of the electronic device.[20]

Pioneering work has been done to demonstrate the controlled growth of catalyst-free III−V nanowires.[21−26] Techniques such as selected-area metal−organic chemical vapor deposition (SA-MOCVD) use a dielectric mask to produce nanowire growth at predetermined locations without the help of a catalyst. A recent comparative study between Au-assisted and Au-free grown GaAs nanowires showed a much superior minority carrier lifetime for the latter.[27]

The most common nanoscale patterning technique for the dielectric mask is electron beam lithography (EBL), which is a slow and expensive process. In contrast, nanosphere lithography (NSL) has emerged as a cost-effective, high throughput technique to pattern large areas.[28] NSL can be used to produce nanostructures with controlled shape, size, and interparticle spacing.[29,30] Previously, NSL has been used for VLS growth of semiconducting nanowires; the Au catalyst was deposited in the interstitial regions between self-assembled nanospheres. However, using this technique, the control over nanowire diameter is constrained to a small range, and the filling ratio (the ratio of the cross-sectional area of the nanowire to the area of the unit cell) is low.[31] A NSL technology that can offer both control over nanowire diameter and high filling ratio is therefore highly desired. Our paper combines NSL and catalyst-free SA-MOCVD for the first time for scalable synthesis of semiconductor nanowire arrays. Moreover, since NSL is known to produce patterns with a variety of defects, such as grain boundaries and line defects, it is important to understand how

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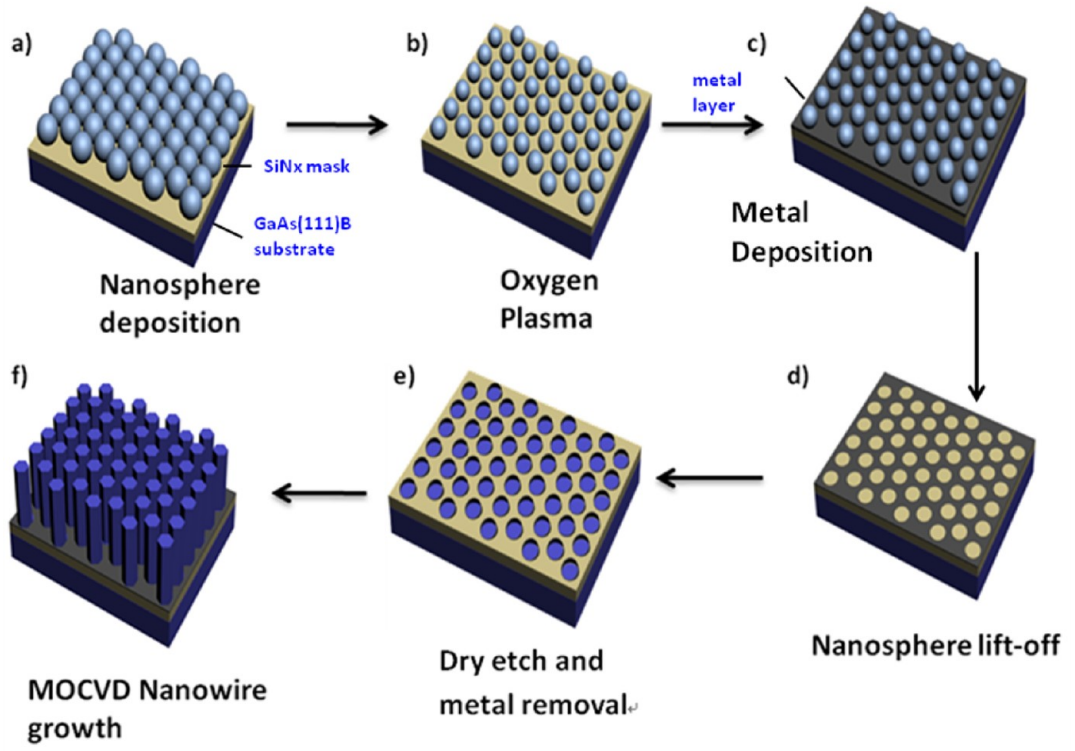

Figure 1. Schematic diagram of nanosphere lithography and nanowire growth. (a) Spin-coating nanospheres on the substrate. (b) Oxygen plasma to reduce the size of the nanospheres, which will determine the diameter of the nanowires after growth. (c) Metal (Al or Fe) deposition onto the nanospheres. (d) Dissolution of nanospheres in chloroform with the aid of sonication. (e) Transfer of the pattern to the underlying substrate by dry etching and removal of the metal mask by HCl wet etching. (f) Nanowire growth by SA-MOCVD.

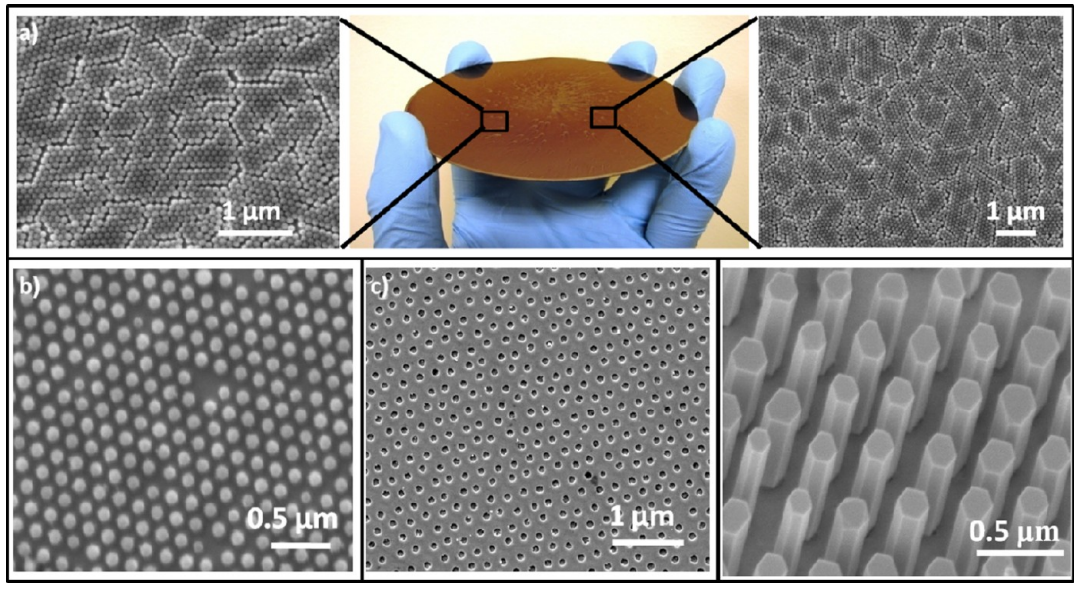

Figure 2. Demonstration of scalable GaAs nanowire synthesis on a GaAs substrate using NSL technique. (a) Photograph of the spin-coated polystyrene nanospheres on a wafer scale. SEM images of nanosphere assembly at two random locations on the wafer, showing monolayer assembly of the nanospheres. (b) SEM image of nanospheres after size reduction by oxygen plasma. (c) SEM image of the pattern after metal deposition, nanosphere lift-off, and dry etching, just before the nanowire growth. (d) Vertical GaAs nanowires grown on the NSL pattern showing a hexagonal cross section having six (110) side facets.

such defects affect the optical absorption of NSL-patterned nanowire arrays and their feasibility for solar cell applications.

Here we report the application of an adapted NSL technique to produce vertically aligned, catalyst-free GaAs nanowires on a large scale. We demonstrate precise control over nanowire diameter and achieve high filling ratio by combining, for the first time, the use of oxygen plasma to tune nanosphere size, pattern transfer, and SA-MOCVD growth. In addition, simulations have been performed to minimize the reflection of the array with respect to pitch and diameter. Experimental

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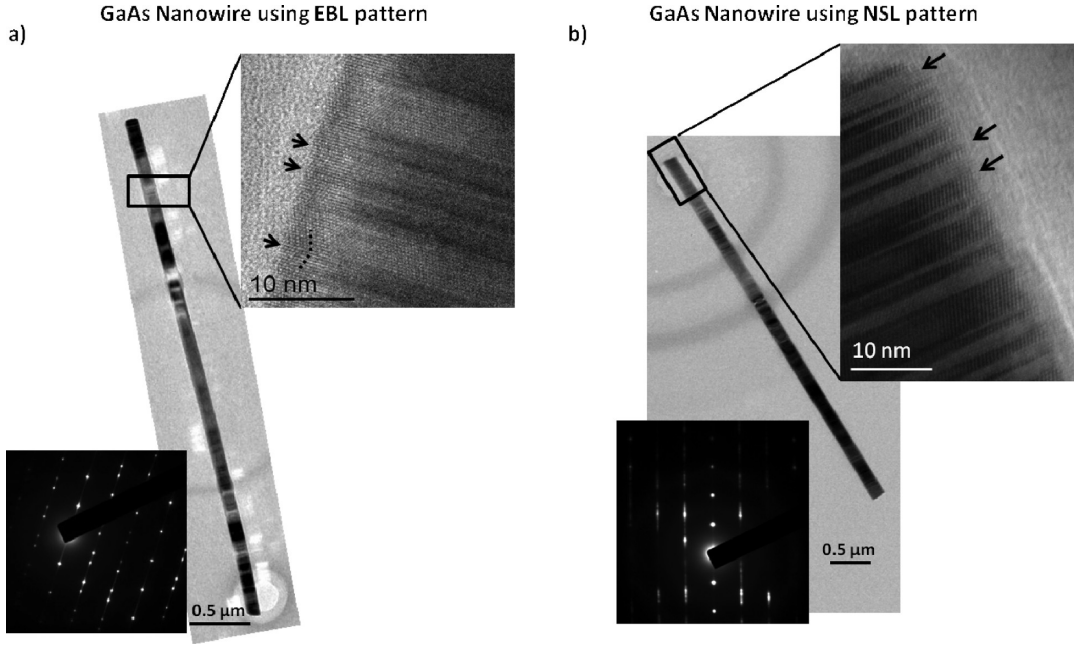

Figure 3. Structural quality comparison of GaAs nanowires grown using (a) electron beam lithography and (b) nanosphere lithography, using HRTEM. Inset in each case shows the twin planes and diffraction pattern corresponding to zinc-blende structure. Both images show similar distribution of twin planes and crystal structures. The arrow indicates the twin planes present in the nanowires.

data are found to be comparable to the simulated data. An array of GaAs nanowires with height as low as 130 nm grown on a GaAs (111) B substrate gives a reflection value <10% over the visible range of spectrum. We have measured structural properties of nanowires fabricated by NSL and EBL and found them to be comparable. Moreover, the optical properties of NSL-fabricated nanowires are comparable to perfectly periodic structures.

Figure 1 shows a schematic diagram of the scalable nanowire growth process, which includes nanopatterning using nanosphere lithography and nanowire growth using the SA-MOCVD technique. The detailed procedure of scalable catalyst-free growth of semiconducting nanowires begins with PECVD deposition of 30 nm of SiN (measured by ellipsometer) on a substrate of interest. The SiN acts as a mask for the selected area growth of nanowires. Next, the substrate/SiN is cleaned by oxygen plasma, making it hydrophilic. A 10 wt % aqueous solution of polystyrene nanospheres (Thermo Scientific) of desired size is spin-coated onto the hydrophilic substrate (Figure 1a). The spin speed was tuned to obtain uniform monolayer coverage of nanospheres on the substrate; higher spin speed resulted in islands of nanospheres, while lower spin speeds resulted in multilayer stacking of nanospheres. Next, the nanosphere size is reduced by dry etching with O_2 plasma. The power, partial pressure, and time of etching were optimized to obtain the desired size (Figure 1b). Aluminum or iron is then deposited on the SiN using the assembled nanospheres as a shadow mask (Figure 1c), and the nanospheres are dissolved in chloroform with the aid of sonication (Figure 1d). Finally, the pattern is transferred to the underlying substrate by dry etching SiN using CF4 plasma followed by removal of the metal mask using wet etching in hydrochloric acid (Figure 1e). The pattern is then ready for nanowire growth using MOCVD. Highly aligned vertical nanowires of desired length were obtained by controlling the growth conditions (Figure 1f).

We demonstrate this scalable nanowire synthesis approach by fabricating vertical GaAs nanowires on a GaAs (111) B substrate. The polystyrene nanospheres used in these studies were nearly monodisperse with a diameter of 100, 200, or 360 nm. Stable nanosphere suspensions in water (10 wt %, used as received) were spin-coated onto a hydrophilic GaAs/SiN wafer as shown in Figure 2a. As the solvent (water) evaporates, capillary forces draw the nanospheres together, and the nanospheres crystallize in a hexagonally close-packed pattern. The assembly of nanospheres was inspected with a scanning electron microscope (SEM), and images at two random locations are shown in Figure 2a. The images show monolayer assembly of the nanospheres, with ∼90% of the substrate successfully coated with large domains of defect-free nanosphere packings. As in all naturally occurring crystals, some regions include point defects (vacancies), line defects (slip dislocations), and polycrystalline grains. Typical domain sizes are in the 10−100 μm^2 range and increase with the size of the nanospheres. Figure 2b shows the SEM image of the nanosphere assembly after oxygen plasma, showing uniform reduction of the nanosphere size. Following size reduction, a thin film of 30 nm Fe is deposited by thermal evaporation from a source normal to the substrate through the nanosphere mask. After metal deposition, the nanosphere mask is removed by sonicating the entire sample in chloroform, leaving behind a meshlike pattern of Fe on the substrate. The pattern is then transferred to the underlying GaAs substrate by dry etching the SiN using CF_4 plasma, as shown in Figure 2c. GaAs nanowires are grown using SA-MOCVD and only form in the openings in the SiN (Figure 2d). Nanowires were grown both with and without a Fe mask (etched by HCl), and no difference in the morphology of the nanowires was observed.

Details of the nanowire growth are similar to those in ref 23. Briefly, nanowire growth was carried out in a vertical MOCVD system working at 0.1 atm pressure. Trimethylgallium (TMG) and arsine (AsH_3) were used as precursors. The partial pressure

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of TMG was 3.76118×10^{-7} atm, and that of AsH_3 was changed from 7.12×10^{-5} to 2.42×10^{-4} atm. The growth temperature was 700 °C. The total growth time was varied depending on the desired length of the nanowires. For nanowires shown in Figure 2d, the growth time was 50 min for 200 nm long nanowires. GaAs nanowires were grown in a (111) B (vertical) direction on the substrate. As shown in Figure 2d, the nanowires have a hexagonal cross section. From the symmetry, we conclude that the nanowires have six (110) side facets similar to the larger hexagonal structure.[32]

Our technique can be contrasted with other NSL methods for nanowire growth, in which the nanosphere pattern is used as a mask to deposit metal catalyst in the interstitial regions.[31] In that case, any area with defects in the nanosphere packing (vacancies, line defects, grain boundaries, etc.) is covered by metal, ultimately resulting in bulk material growth or a large distribution in nanowire diameter. In our case, the defect sites in the nanosphere pattern are covered by SiN and do not contribute to the growth of nanowires, only the areas which were initially covered with nanospheres resulted in nanowire growth. In principle, the method of scalable nanowire growth we propose is not restricted to GaAs nanowires on GaAs substrates and can be used to grow a variety of III−V nanowires on various semiconducting substrates.[21−26]

MOCVD nanowire growth is a complicated process involving migration of precursors which can be affected by the patterning defects at the grain boundaries in nanosphere lithography. As it has been shown that crystal structure of nanowires is closely correlated to growth conditions,[33−36] we believe it is important to compare the crystal structures and defects of nanowires using NSL and EBL. We used GaAs nanowires grown on GaAs (111) B substrates patterned by electron beam lithography to compare the structural quality of nanowires to those grown by NSL. High-resolution transmission electron microscopy (HRTEM) measurement was carried out on the nanowires using a JEOL 200 keV TEM. Nanowires were separated from the substrate by sonication in methanol and were dispersed onto carbon-supporting Cu grids. Figures 3a and 3b show the TEM images of the nanowires synthesized using electron beam lithography and nanosphere lithography, respectively. The bright and dark regions with 2−30 nm periods along the growth direction show that the nanowires contain many stacking defects. The insets in Figures 3a and 3b show the diffraction pattern for nanowires grown using EBL and NSL patterning, respectively. It consists of basic Bragg spots coinciding with the zinc-blende pattern observed from the $[1\bar{1}0]$ direction and additional spots which are line-symmetric to the basic ones with respect to the [111] axis. The crystal structure of the GaAs nanowire is thus a rotational twin of the zinc-blende type with a [111] twin axis. Therefore, the bright and dark regions in the TEM image in Figure 3 result from the difference in electron diffraction conditions on the two sides of the twin boundary. The density of these rotational twins was similar in nanowires produced by both NSL and EBL patterning.

In order to quantify the broadband antireflection property of the GaAs NW arrays, we evaluated the weighted reflection loss (ARL), defined as

$$\mathrm{ARL} = \frac{\int_{400\ \mathrm{nm}}^{\lambda_g} \frac{R_{TE}(\lambda) + R_{TM}(\lambda)}{2} I(\lambda)\lambda\ \mathrm{d}\lambda}{\int_{400\ \mathrm{nm}}^{4000\ \mathrm{nm}} I(\lambda)\lambda\ \mathrm{d}\lambda}$$

Here λ is wavelength, and λ_g is the wavelength corresponding to the band gap of GaAs (867 nm). $I(\lambda)$ is the ASTM AM1.5 direct and circumsolar solar irradiance spectrum,[37] and $R_{TE}(\lambda)$ and $R_{TM}(\lambda)$ are the surface reflectance for the TE and TM polarization, respectively. This figure of merit gives the loss in the ultimate efficiency[38] due to the reflection off the nanowire array. The ultimate efficiency is defined under the assumption that each absorbed photon with energy greater than the band gap produces one and only one electron hole pair with energy hc/λ_g.

The simulated structure is a vertically aligned GaAs nanowire array on top of a semi-infinite GaAs substrate, as shown in Figure 4a. The array consists of nanowires with diameter d and

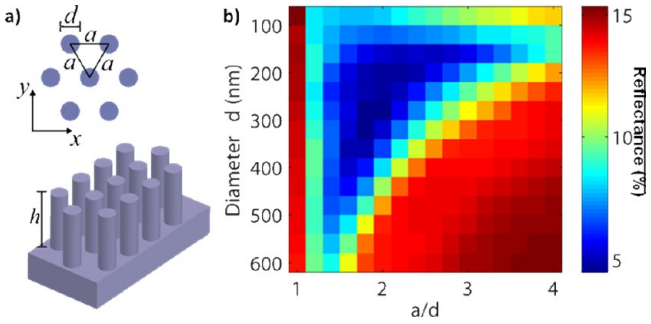

Figure 4. (a) Schematic of the GaAs nanowire array. (b) Calculated weighted reflection loss as a function of nanowire diameter and lattice constant−diameter ratio for GaAs nanowires of 130 nm in height. A range of optimum configurations can be extracted from the graph and used to fabricate GaAs nanowires using NSL.

lattice constant a arranged in a hexagonal lattice and surrounded by air. The nanowire height is 130 nm. The structure is illuminated by normally incident sunlight, modeled by the ASTM Air Mass 1.5 direct and circumsolar solar spectrum. The optical constants of GaAs used in the calculation are taken from ref 39. For GaAs solar cells, the wavelength range of interest is from 400 nm, where the solar irradiance is negligibly small, to 867 nm, the wavelength corresponding to the band gap of GaAs. We used the scattering matrix method implemented in the ISU-TMM simulation package[40,41] to calculate the average reflectance as a function of wavelength across the solar spectrum, defined as the average between the reflectance for the incidence light polarized along the ΓM direction and ΓK direction.

Figure 4b shows the weighted reflection loss as a function of nanowire diameter and the lattice constant−diameter ratio (a/d). Two trends can be observed. First, for fixed a/d, there exists an optimal range of nanowire diameters to minimize the reflection loss. Second, for fixed nanowire diameter, there exists an optimal range of lattice constants where the weighted reflection loss is minimal. For either small or large a/d, the reflection loss is very high. This trend can be qualitatively explained as follows. For small a/d (large filling fraction), the nanowires are almost touching each other and form a continuous film. The optical properties of the structure resemble those of a semi-infinite GaAs substrate and exhibit high reflection loss. On the other hand, for large a/d (small filling fraction), the nanowires are far apart from each other. Therefore, the incident light mainly interacts with the underlying substrate instead of the nanowires, also resulting in high reflection loss. There exists a fairly large region of parameter space, with a diameter of 150−400 nm and a/d of

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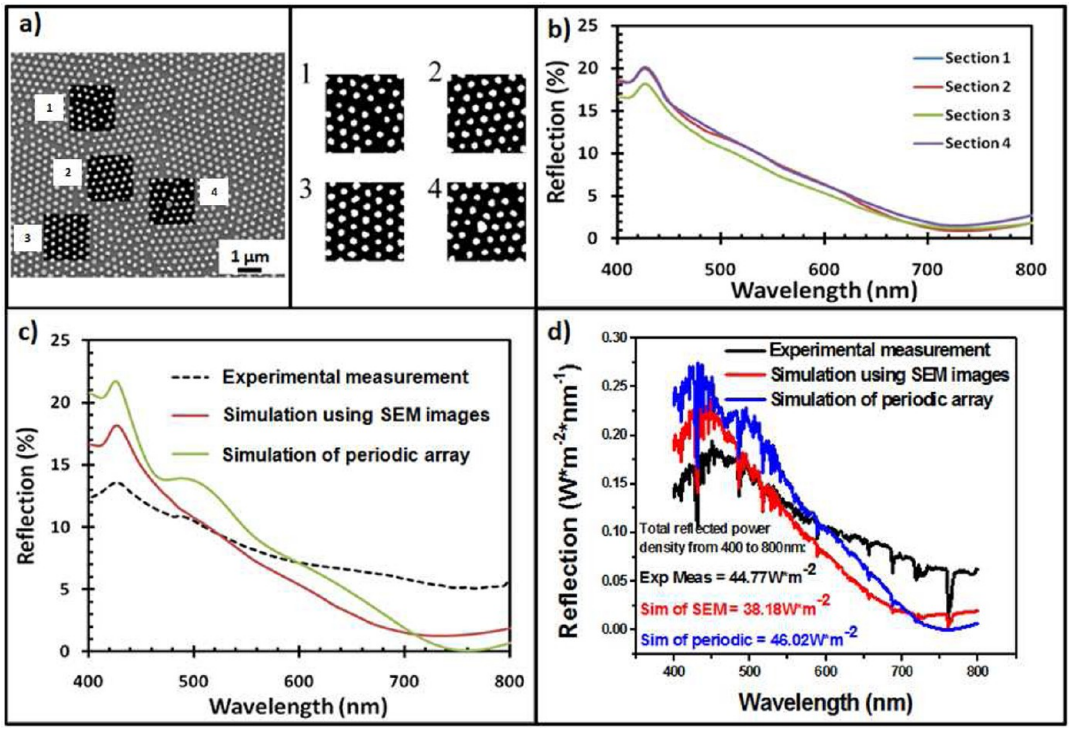

Figure 5. Comparison between experimentally measured and simulated reflectance spectrum for the as-fabricated GaAs nanowire array sample (a = 360 nm, d = 195 nm). (a) SEM image of the top view of the GaAs nanowires grown using NSL. Four regions extracted from the SEM image (1, 2, 3, and 4 shown in the inset) were selected to simulate the reflection profile across the visible spectrum. (b) Corresponding reflectance spectra using section 1, 2, 3, and 4. (c) Plot of reflectance spectra for GaAs nanowires grown on a GaAs substrate using NSL (experiment), simulated periodic nanowire array with a = 360 nm and d = 195 nm, and average of simulated nanowire arrays in (b). (d) Reflected power density under AM1.5 spectrum showing experimental measurement of the GaAs nanowire array grown on NSL patterned substrate, simulation of the periodic nanowire array, and simulation using nanowire arrays with SEM images in (a). The total integrated reflected power density is also calculated.

1.5−3, that can produce a reflection loss value of 7% or less with the minimum around $d \sim 300$ nm and $a/d \sim 1.9$.

In the simulation, we assumed that the nanowire array is a perfectly periodic structure with uniform spacing, diameter, and height. However, in reality, the fabricated sample always deviates from the ideal structure, due to variation in nanowire spacing, diameter, and height, as well as the finite grain size. In order to more accurately model the as-fabricated sample, we import the actual size, shape, and arrangement of nanowires in a 2 μm by 2 μm region of the sample from SEM pictures into the Lumerical FDTD solutions simulation package. We compare four different sections of the sample, as shown in Figure 5a. We use periodic boundary conditions in both X and Y directions and assume that the nanowires have a uniform height of 130 nm. Our simulations take into account the variation in the nanowire diameter and spacing and hence are more accurate than the simulation for the perfectly periodic structure. The simulated results are plotted in Figure 5b,c. We can observe in Figure 5b that the average reflectance spectra for the four different sections in the SEM picture are similar to each other, with only a slight difference in value. Furthermore, as we can see in Figure 5c, the experimentally measured spectrum (using a Perkin-Elmer Lambda 950 integrating sphere) shares similar features with the simulated spectrum for both the perfectly periodic structure and the as-fabricated structures, with slight differences in long wavelengths. We believe the deviation of simulation from experimental measurements is likely due to the fact that the simulation used a perfectly collimated incident light beam, while the incident beam for experimental measurements cannot be perfectly collimated. From Figure S2, the experimental spectra typically exhibit shallower and broader features than the theoretical spectra, which is consistent with a wider angular spread in the illumination angles. Figure 5d shows the reflection loss in the wavelength range between 400 and 800 nm under illumination of AM1.5 ASTMG173 spectrum, and the integrated reflection loss is 44.77 W/m^2 for our sample, which is close to that from a periodic array of nanowires with the same dimension and pitch (46.02 W/m^2). We have also used simulation to study the effect of height variation on reflection, which can be found in the Supporting Information.

We have also compared simulations and measurements of reflection for a nanowire array with larger pitch. The pattern for nanowire growth was fabricated using nanospheres with a diameter of 890 nm, which were reduced to 450 nm after assembly. This resulted in nanowires with a diameter of 450 nm and a pitch of 890 nm (as shown in Figure 6a). The height of the nanowires was ∼130 nm. According to Figure 3, we would expect more reflection from this nanowire array. As evident from the SEM image, the nanowires have more size and shape variation than those with 360 nm pitch shown in Figure 5. Figure 6b shows the simulated reflection spectra using three 5 μm by 5 μm sections from the SEM image of Figure 6a. The spectra are very similar to each other. In Figure 6c, we show the comparison between experimental measurements, simulated values from the periodic array (using a = 890 nm, d = 450 nm, and height = 130 nm), and the averaged simulated values in Figure 6b. The three quantities match closely, and again the integrated reflection loss of our sample (132.23 W/m^2) is very close to that from a periodic array of nanowires with the same

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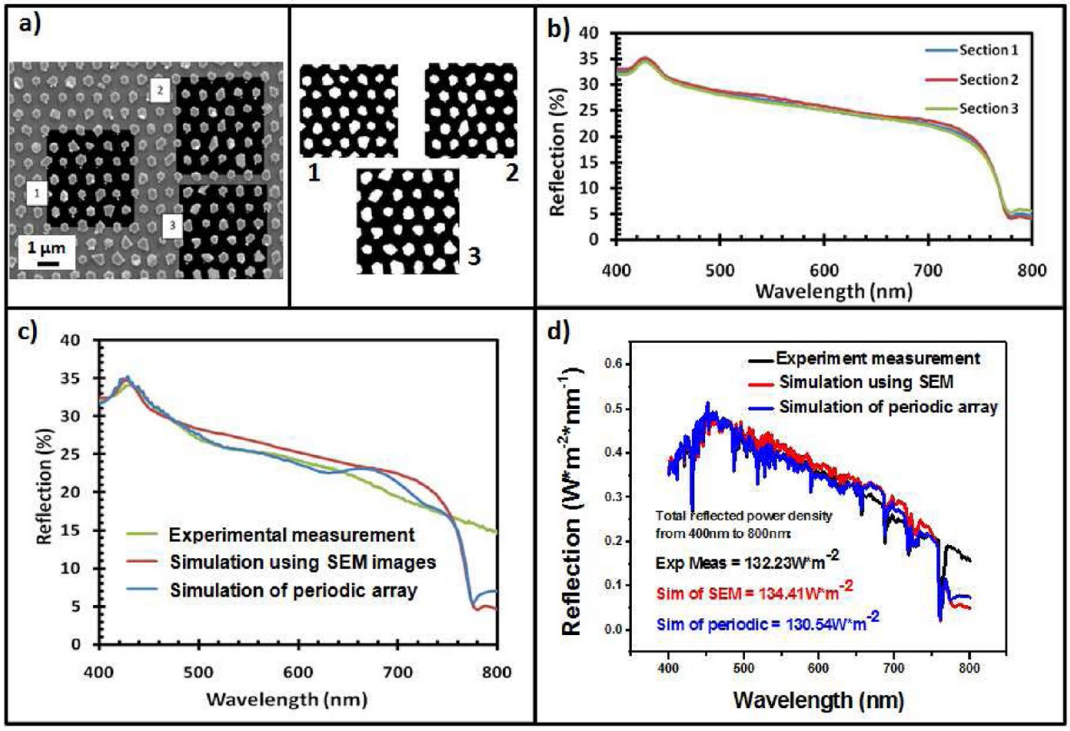

Figure 6. Comparison between experimentally measured and simulated reflectance spectrum for a GaAs nanowire array sample (a = 890 nm, d = 450 nm) fabricated using NSL. (a) SEM image of the nanowires (top view). Three regions extracted from the SEM image (labeled 1, 2, and 3) are shown in the inset, each with dimensions of 5 μm by 5 μm. (b) Corresponding reflectance spectra using section 1, 2, and 3. (c) Plot of reflectance spectra for GaAs nanowires grown on a GaAs substrate using NSL (experiment), simulated periodic nanowire array with a = 890 nm and d = 450 nm, and average of simulated nanowire arrays in (b). (d) Reflected power density under AM1.5 spectrum showing experimental measurement of the GaAs nanowire array grown on NSL patterned substrate, simulation of the periodic nanowire array, and simulation using nanowire arrays with SEM images in (a). The total integrated reflected power density is also calculated.

dimension and pitch (130.54 W/m^2) as shown in Figure 6d. As expected, reflection values are higher than those in Figure 5.

We have also compared simulations to experimental results for perfectly periodic arrays, patterned using EBL. We synthesized GaAs nanowires on EBL-patterned GaAs (111) B substrates with 360 and 890 nm pitch. Two sets of nanowires with growth times of 20 min (corresponding to a height of 500 nm for 360 nm pitch and 1350 nm for 890 nm pitch) and 30 min (corresponding to a height of 750 nm for 360 nm pitch and 1800 nm for 890 nm pitch) were produced. The experimental and simulated spectra along with corresponding SEM images are shown in Figure S2. The simulated and experimental curves show similar features, with slight variation in the absolute values. The results demonstrate that reliable and realistic predictions of reflection spectra can be obtained from simulation. Simulations can thus be used as a tool to predict optimum nanowire array designs and as guidance for nanowire fabrication and growth.

In summary, we report a versatile, scalable fabrication technique that used NSL patterning for synthesis of vertically aligned, catalyst-free nanowires using SA-MOCVD. The presence of defects in the assembled nanosphere pattern resulted in negligible effect on the optical properties of the array, as characterized by the reflection loss spectrum. There is thus "no need" to fabricate highly periodic structures in order to achieve good optical performance. As an alternative to costly, time-consuming patterning methods such as EBL, NSL will undoubtedly be a powerful technique to produce scalable nanowire arrays for photovoltaic applications.

■ ASSOCIATED CONTENT

Supporting Information

Size distribution of nanowires produced by NSL and effect of height variation on optical reflection in periodic array (S1); comparison between simulation and experiment results of GaAs nanowire arrays grown on EBL patterned GaAs (111) B substrate for S2 (a) 360 nm pitch and S2 (b) 890 nm pitch, for samples grown for 20 and 30 min, corresponding to two different nanowire heights. This material is available free of charge via the Internet at http://pubs.acs.org.

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Notes

The authors declare no competing financial interest.

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