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Scalable fabrication of self-aligned graphene transistors and circuits on glass

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Abstract

High frequency graphene transistors with the intrinsic cut-off frequency up to 300 gigahertz (GHz) have been demonstrated for radio frequency (RF) applications. However, functional graphene RF circuits such as frequency doublers and mixers operating in the gigahertz range is yet to demonstrated. Here we report a scalable approach to fabricate self-aligned graphene transistors and circuits that can operate in gigahertz regime. The devices are fabricated through a self-aligned aligned process on glass substrate using chemical vapor deposition (CVD) grown graphene and a dielectrophoretic assembled nanowire gate array. The self-aligned process allows to achieving unprecedented performance in CVD graphene transistors with a highest transconductance of 0.36 mS/μm. With the minimization of parasitic capacitance on insulating substrate, the resulting graphene transistors exhibit a record high extrinsic cut-off frequency (> 50 GHz) achieved in graphene transistors to date. The excellent extrinsic cut-off frequency readily allows configuring the graphene transistors into frequency doubling or mixing circuits functioning in the 1–10 GHz regime, a significant advancement over previous report (~20 MHz). The studies open a pathway to scalable fabrication of high speed graphene transistors and functional circuits, and represent a significant step forward to graphene based radio frequency devices.

Keywords

graphene transistors; self-aligned gate; cut-off frequency; RF mixers

Graphene exhibits many unique characteristics, including the highest carrier mobility and saturation velocity,[1–6] to make it an attractive material for ultra-high-speed electronics. Graphene transistors with the intrinsic cut-off frequency up to 150 GHz have been achieved through continued shrinking the channel length using conventional dielectric integration and electron beam lithography fabrication processes.[7–10] However, these processing steps can often introduce defects into the monolayer of graphene to degrade its performance. The recent development of a self-aligned approach using a physically assembled nanowire gate can minimize potential damage to the graphene lattice to preserve the high carrier mobility,[11] and allows precise positioning and alignment of source-gate-drain electrodes to

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Note added. As our manuscript was being considered by another journal, we became aware of a related work on graphene circuits by IBM group.

minimize the access resistance or parasitic capacitance. It has therefore enabled graphene transistors with intrinsic cut-off frequency in the range of 100–300 GHz.[12]

Additionally, channel length scaling studies projects that terahertz operation can be achieved in sub-70 nm transistors,[13] matching well with theoretical prediction by self-consistent quantum simulations,[14] which highlights that the self-aligned approach can enable graphene devices of nearly ideal performance. However, these initial studies employ mechanical peeled graphene and arbitrarily deposited nanowire gates, which complicates the scalable fabrication of graphene transistors or circuits. Additionally, all high-speed graphene transistors reported to date are fabricated on either highly resistive silicon or semi-insulating silicon carbide substrate with relatively large parasitic capacitance, which severely limits the extrinsic cut-off frequency to around 10 GHz or less.[7,9,10,12]

To address these critical challenges, here we describe a scalable approach to fabricate graphene transistor and circuits on glass substrate with chemical vapor deposition (CVD) grown graphene and dielectrophoretic assembled nanowire top gated arrays[15–19]. By minimizing the parasitic capacitance on insulating substrate, we demonstrate a record high extrinsic cut-off frequency in graphene transistors to date. The graphene device are further configured into frequency doubling or mixing circuits that can operate at 1–10 GHz regime, represensting a significant advancement over previous report (~20 MHz).[20]

The fabrication processing flow is shown in Figure 1. Briefly, single layer graphene is first grown by CVD approach and transferred onto a glass substrate (Figure 1a). The quality of the graphene is characterized using micro-Raman spectroscopy (Supplementary Figure S1a), suggesting continuous single layer graphene with few defects. Electrical transport studies of standard back gated devices on silicon/silicon oxide substrate show that the carrier mobility values of 1000–2000 $cm^2/V \cdot s$ are typically observed (Supplementary Figure S1b), demonstrating reasonable quality of the CVD grown graphene.

The graphene is then patterned using photolithography followed by oxygen plasma treatment to form isolated graphene blocks (Figure 1b). Next, pairs of electrodes are defined across each graphene block (Figure 1c), and a dielectrophresis assembly process is then used to precisely position the nanowire array on top of each patterned graphene block (Figure 1d). The dielectrophresis method is a self-limiting process allowing assembly of only a single nanowire on each pair of electrodes with high yield by controlling the hydrodynamic and electric field forces. Figure 2a shows 20 pairs of finger electrode array on the substrate, with each pair of electrodes bridged by a single nanowire. Standard lithography and metallization (Ti/Au, 70/50 nm) processes are then used to form the external source, drain and gate electrodes (Figure 1e). Lastly, a thin layer of Pt metal (10 nm) is deposited on top of the graphene across the nanowire, in which the nanowire separates the Pt thin film into two isolated regions that form the self-aligned source and drain electrodes adjacent to the nanowire gate (Figure 1f). Figure 2b shows an array of nine self-aligned graphene transistors, and Figures 2c and 2d shows zoomed-in picture of an individual self-aligned graphene transistor.

Figure 3 shows electrical performances of a typical graphene transistor with the gate nanowire diameter (channel length) of 170 nm. The I_{ds}-V_{ds} output characteristics at various gate voltages show that this device can deliver a significant on-current of about 1.26 mA/μm at V_{ds} = −1 V and V_{TG} = 0.0 V (Figure 3a). Interestingly, a slight current saturation is observed in this short channel device, which becomes more obvious when the channel length further increases to 240 nm (Supplementary Figure S2). The current saturation is desirable for power gain performance in RF graphene transistors, and has not been achieved in graphene transistors of such short channel. The observed current saturation can be

attributed to gate induced shifting of Dirac point due to the large gate-drain capacitance coupling[21–25]. The transfer characteristics (Figure 3b) show that the full current modulation can be achieved with a relatively small gate swing of about 1 V, from which the transconductance $g_m = \frac{dI_{ds}}{dV_g}$ can be derived. Significantly, a peak transconductance of 0.36 mS/μm can be obtained at V_{ds} = −1 V (V_g = 1.5 V) (Figure 3c), representing the highest value in CVD graphene transistors reported to date. The above discussions clearly demonstrate the self-aligned nanowire gate can allow us to achieve un-precedent DC performance in CVD graphene transistors.

An important benchmark of the transistor RF performance is the cut-off frequency f_T. To assess the RF characteristics of our self-aligned transistors, on-chip microwave measurements were carried out in the range of 50 MHz to 20 GHz using an Agilent 8722ES network analyzer. To accurately determine the intrinsic f_T values generally requires careful de-embedding procedures using the exact pad layout as “open” and “short” test structures. The scattering S-parameters that relate the AC currents and voltages between the drain and the gate of the transistor were first measured (Figure 3d). The de-embedded S parameters constitute a complete set of coefficients to describe intrinsic input and output behaviour of the graphene device and can be used to derive other important characteristic parameters such as gain. Figure 3e shows the small signal current gain |h21| derived from the measured S-parameters at V_{TG} = 1.6 V and V_{ds} = −1 V. The curve displays the typical *1/f* frequency dependence expected for an ideal FET. The linear extrapolation yields a f_T value of 72 GHz. To further confirm the accuracy our de-embedding process, we have used S-parameter measurements to extract all device component values based on the equivalent circuit (Figure 3f). Importantly, the device component values (including transconductance, parasitic capacitance, gate capacitance etc.) derived from the RF measurements are consistent with those obtained from the DC measurements or electrostatic simulations (Table 1). The observed f_T value of 72 GHz is comparable to that of the recent report of CVD graphene transistors (70 GHz for 140 nm device) with similar channel length,[10] but much smaller than that of the peeled graphene transistor (168 GHz for 182 nm device),[12] suggesting that the performance of this transistor is limited by the quality of the CVD graphene, and can be further improved upon improving the quality CVD graphene.

Although extraordinarily high intrinsic f_T up to 300 GHz has been reported from various types of graphene and/or device fabrication approaches, the high-speed graphene transistors reported to date typically have a rather low extrinsic cut-off frequency around 10 GHz or less. This dramatic difference between intrinsic and extrinsic f_T can be primarily attributed to the large ratio between parasitic pad capacitance and gate capacitance. These previous devices are typically fabricated either on highly resistive silicon or semi-insulating silicon carbide substrate with large parasitic capacitance, which has severely limited the achievable extrinsic f_T. Importantly, the component value analysis of our device (Table 1) reveals that the ratio between parasitic capacitance and gate capacitance is rather small, due to a greatly reduced parasitic capacitance with the use of insulating quartz substrate. The small parasitic/gate capacitance ratio achieved in our device suggests that excellent extrinsic f_T value may be achievable. Indeed, our measurement without the de-embedding procedures shows an extrinsic f_T value of 55 GHz, representing the highest extrinsic f_T achieved in any graphene transistors reported to date.

The achievement of such high extrinsic f_T is significant and can readily allow us to configure graphene transistor based RF circuits that can operate in the gigahertz regime. To this end, we have configured the graphene transistors into RF frequency doublers and mixers. Previous studies suggested the unique ambipolar transport properties of graphene transistors can allow the development of a new generation of nonlinear electronics for RF

signal-doubling applications.[20,26–28] Figure 4a and 4b show schematic circuit diagram of the graphene transistor based frequency doubler and the nearly symmetrical transfer characteristics of a graphene transistor around the Dirac point. Similar graphene frequency doubler has been reported previously but with an operation frequency merely up to 20 MHz due to the severe limitation of the low extrinsic f_T of the graphene transistors used. Importantly, with the excellent extrinsic f_T, the frequency doubler configured using the self-aligned graphene transistors shows a clear doubling function with the input signal frequency at 1.05 GHz (Figure 4c). Most of the output power is concentrated at the doubling frequency of 2.1 GHz. Spectrum analysis shows that the frequency-doubler device exhibits a high spectral purity in the output RF signal, with 90% of the output RF energy is at the doubling frequency (2.1 GHz) (Figure 4d). Together, this study clearly demonstrates for the first time a single graphene transistor based frequency doubler that can operate in the gigahertz regime with high output spectral purity.

We have further configured a single graphene transistor based RF mixer (Figure 5a) and performed two-tone measurements. The two tone signals with adjacent frequencies are applied to the gate through a power combiner to manipulate the transistor channel resistance. In general, the DC transconductance g_m and f_T of a graphene transistor strongly depends on the exact gate voltage. For the device shown in Figure 5b, as the gate voltage is varied, f_T follows the amplitude of g_m, with a maximum f_T of 34 GHz corresponding to the peak g_m of 3.0 mS at V_{TG} = 0.3 V. To explore the operation frequency limits of the graphene transistor based mixer, it is important to properly gate and bias the graphene transistors with optimized g_m and f_T. Figure 5c shows the output spectrum of the RF mixer with the RF input f_{RF} = 6.72 GHz and local oscillator f_{LO} = 2.98 GHz when the device is operating at V_{ds} = −1.0 V and V_{TG} = 0.3 V with a maximum extrinsic f_T = 34 GHz. The RF mixing function is clearly seen at intermediate frequency (IF) $f_{IF} = f_{RF} - f_{LO}$ = 3.74 GHz and $f_{IF} = f_{RF} + f_{LO}$ = 9.70 GHz. On the other hand, biasing the device at smaller V_{ds} = 0.2 V at the same gate voltage of 0.3V (extrinsic f_T~7 GHz), the output spectrum shows that power at all frequencies are greatly reduced, and $f_{IF} = f_{RF} + f_{LO}$ = 9.70 GHz disappeared (Figure 5d). Similarly, bias or gating at a different voltage with smaller g_m can generally result in a degradation of the output power ((Supplementary Figure S3 & S4). Together, these studies clearly demonstrating the importance to improve the g_m and extrinsic f_T for optimized power output at high frequencies.

The third-order intercept point (IP3) in a mixer is defined by the extrapolated intersection of the primary IF response with the two-tone third-order intermodulation IF product generated by $2f_1 \pm f_2$ or $2f_2 \pm f_1$. The IP3 is an important parameter to characterize the linearity of the RF mixer and is the most commonly used figure of merit to describe the intermodulation distortion of an RF mixer. Figure 4e shows the characterization of the third-order intermodulation product using two-tone measurements. The output power at IF and third-order intermodulation frequency (0.76 GHz) follows the theoretical 10- and 30-dB/dec dependences, respectively. A third-order intermodulation intercept (IIP3) of 13.5 dbm is achieved, comparable to 0.18 μm COMS mixers[29–32] and previously reported graphene mixer (operating at lower frequencies).[20]

It has also been suggested that the symmetrical transfer characteristics can suppress the harmful odd-order intermodulation distortions.[20] In order to take the advantage of this point, we need to gate the device near the Dirac point. Figure 5f shows the dependence of the signal power at intermediate frequency (IF) $f_{IF} = f_{RF} - f_{LO}$ = 0.75 GHz with the RF input f_{RF} = 1.26 GHz and f_{LO} = 2.01 GHz when the transistor operates near the Dirac point with V_{ds} = −1.0 V and V_{TG} = 1.0 V. Importantly, the output spectrum shows that there is no third-order intermodulation frequency when the transistor is gated near the Dirac point. In contrast, changing the V_{TG} away from the Dirac point (e.g. to the maximum

transconductance point, V_{TG} = 0.3 V), the third-order intermodulation frequency could be observed (Figure 5c, d). These studies clearly demonstrate that the odd-order intermodulations can be significantly suppressed in graphene transistor based mixers operating around Dirac point due to the ambipolar symmetrical transfer characteristics.

We noted that our frequency doubling or mixing circuits don't show an apparent conversion gain, but with a relative large conversion loss (~−30 dB at 1 GHz), which is also the case in previous reports of graphene or carbon nanotube based mixers operating at much lower frequencies (~ −35–43 dB at 20 MHz) under similar power input.[20,33] The loss can be largely attributed to the undesirable impedance mismatch and the non-ideal testing setup.[28] For example, signal input and output through a "short" test structure reveal that the loss increases significantly as the frequency increases (Supplementary Figure S5) (e.g. −28 dB at 500MHz, −40 to −50 dB at GHz), suggesting the testing equipment loss may contribute a major portion of the total loss in the gigahertz regime.

In summary, we have demonstrated a scalable process to fabricate self-aligned CVD graphene transistors array on glass with a nanowire gate by dielectrophoretic assembly process. With the minimization of parasitic capacitance on insulating substrate, the graphene transistors exhibit a record high extrinsic cut-off frequency (> 50 GHz), which therefore readily allows us, for the first time, to configure graphene transistor based frequency doubling and mixing circuits that could operate in the gigahertz regime. Our studies open a pathway to scalable fabrication of high speed self-aligned graphene transistors and functional circuits, representing a significant step forward to graphene based RF circuits.

Supplementary Material

Refer to Web version on PubMed Central for supplementary material.

Acknowledgments

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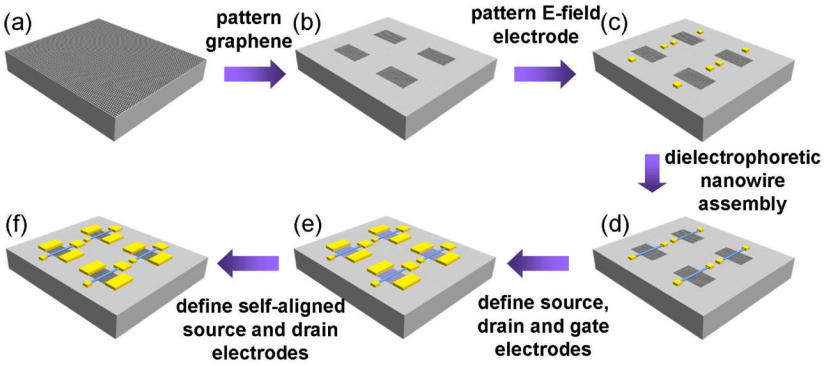

Figure 1.

Schematic illustration of the scalable fabrication of the top-gated graphene transistors with self-aligned nanowire gate. (a) Chemical vapor deposition grown graphene is transferred onto a glass substrate. (b) The graphene is patterned by photolithography. (c) The electric-field electrodes are patterned using photolithography. (d) The nanowires are assembled by dielectrophoresis. (e) The external source, drain and top-gate electrodes are fabricated using electron-beam lithography. (f) Deposition of 10-nm Pt metal film to form the source and drain electrodes self-aligned with the nanowire gate.

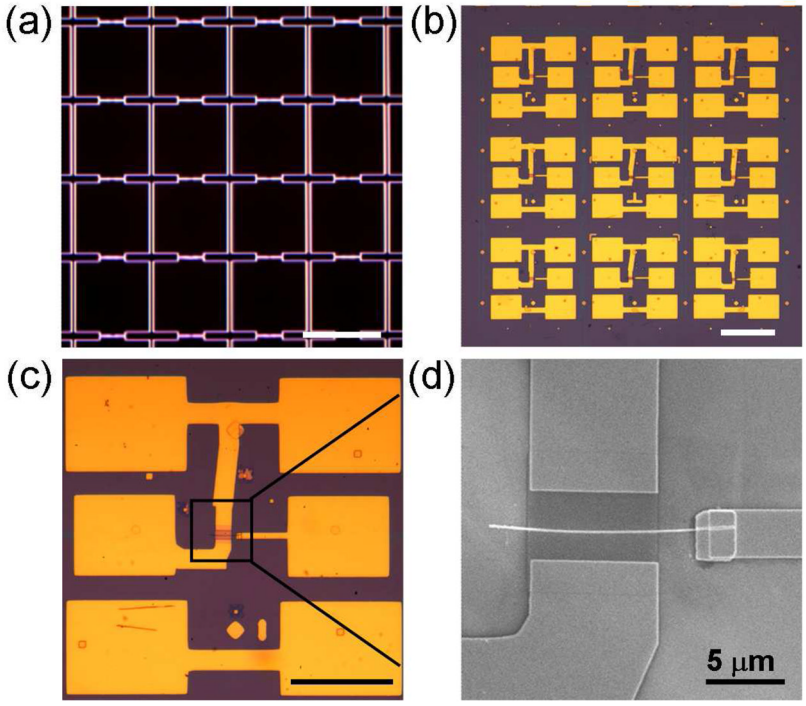

Figure 2.

The top-gated graphene transistors. (a) The dark-field optical image of dielectrophoretic assembled nanowire array, the scale bar is 50 μm. Each pair of electrodes is bridged by a single nanowire. (b) The optical image of self-aligned graphene transistors, the scale bar is 100 μm. (c) The optical image of an individual self-aligned graphene transistor, the scale bar is 50 μm. (d) The SEM image of a graphene transistor with a self-aligned nanowire gate.

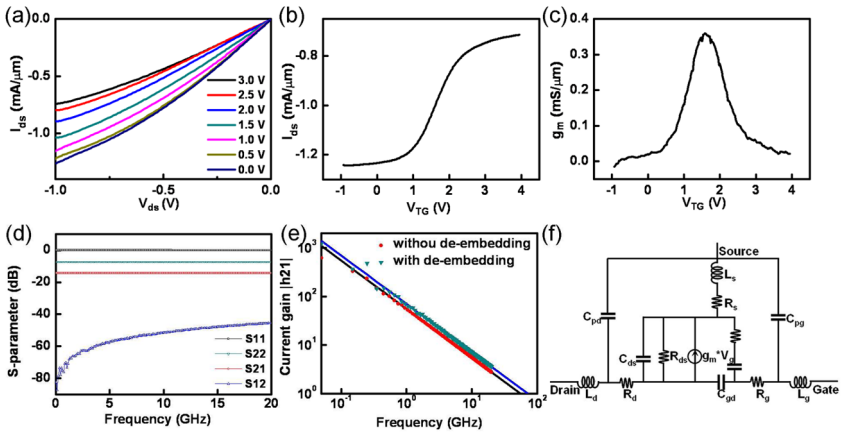

Figure 3.

Room temperature DC and RF characteristics of the self-aligned graphene transistor with 170 nm gate. (a) I_{ds}-V_{ds} output characteristics of device at various gate voltages. (b), I_{ds}-V_{TG} transfer characteristics at V_{ds} = −1 V. (c) Transconductance $g_m = \left|\frac{dI_{ds}}{dV_g}\right|$ at V_{ds} = −1 V as a function of top-gate voltage V_{TG}. (d) As-measured S parameters for the graphene RF transistor. (e) The small-signal current gain |h21| as a function of frequency f at V_{ds} = −1 V, highlighting an intrinsic cut-off frequency of 72 GHz, and an extrinsic cut-off frequency exceeding 50 GHz without de-embedding process. (f) The equivalent circuit topology.

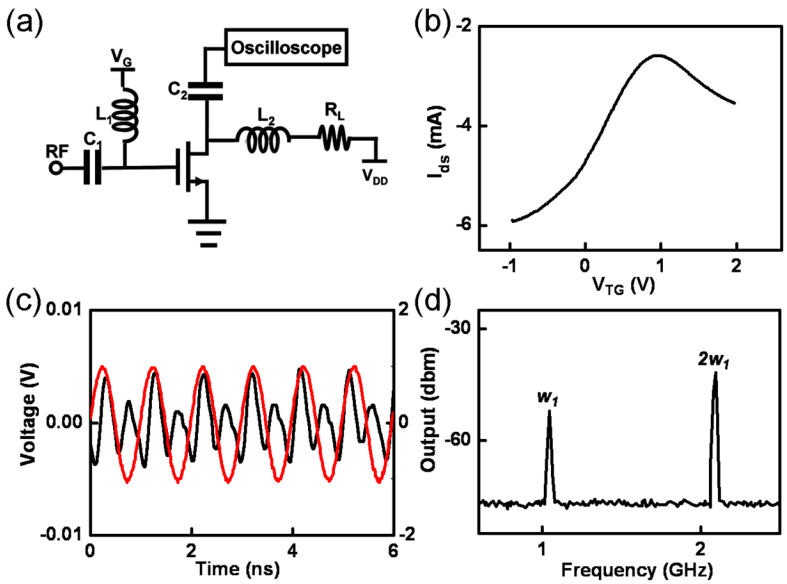

Figure 4.

Graphene transistor based RF doubler. (a) The circuit diagram of an RF doubler. (b) The I_{ds}-V_{TG} of an ambipolar graphene transistor shows nearly symmetrical behavior around the Dirac point. (c) Measured input and output signals of the frequency-doubling circuit when the graphene device is biased near the Dirac point, the input frequency is 1.05 GHz and the output frequency is 2.10 GHz. (d), Output spectrum with single RF input f_{RF} = 1.05 GHz. The frequency doubling is clearly visible. The signal power at $2f_{RF}$ = 2.1 GHz is about 10 dB higher than the signal power at f_{RF} = 1.05 GHz without filtering.

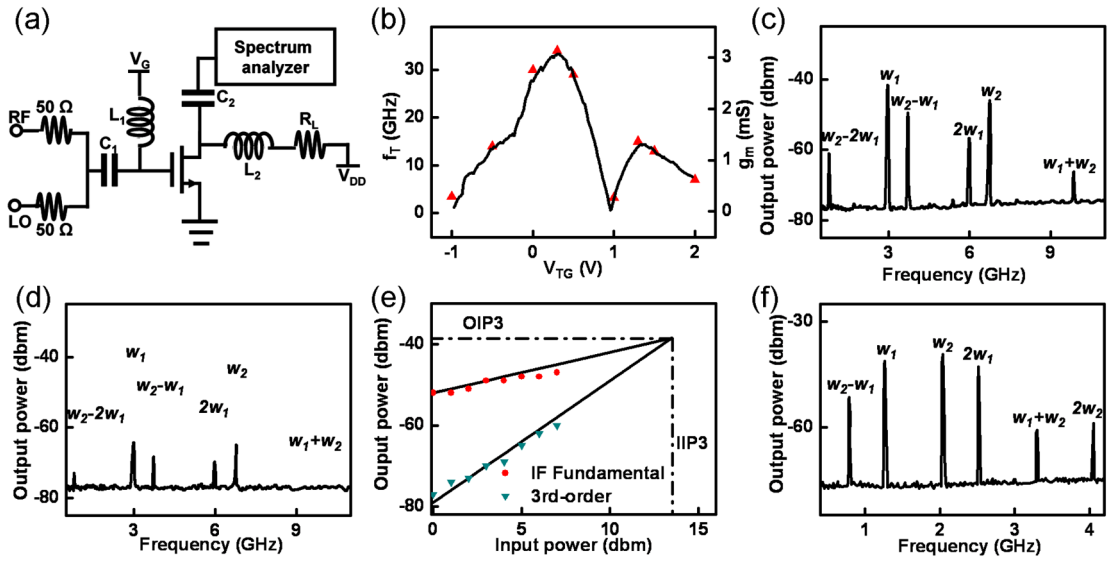

Figure 5.

Graphene transistor based RF mixer. (a) The circuit diagram of a graphene transistor based RF mixer. (b) Measured DC transconductance g_m (line) and f_T (triangle) as a function of gate voltage. (c) Output spectrum with LO input W_1 = 2.98 GHz and RF input W_2 = 6.72 GHz at equal power at V_{ds} = −1 V, and V_{TG} = 0.3 V. The presence of strong signal power at $W_2 - W_1$ and $W_1 + W_2$ clearly demonstrates mixing operations up to nearly 10 GHz. (d) Output spectrum with LO input W_1 = 2.98 GHz and RF input W_2 = 6.72 GHz at equal power at V_{ds} = −0.2 V, and V_{TG} = 0.3 V, in which $W_1 + W_2$ at 9.70 GHz disappears, demonstrating the RF mixer frequency limit depends strongly on the g_m and the extrinsic f_T of the device. (e) Output power of the fundamental and third-order intermodulation (W_2–$2W_1$) as a function of the input power to extract the IIP3 and OIP3. (f) Output spectrum with LO input W_1 = 1.26 GHz and RF input W_2 = 2.01 GHz at equal power (7 dbm) at V_{ds} = −1 V, and V_{TG} = 0.3 V. There is no third-order intermodulation frequency, which proves that odd-order intermodulation can be significantly suppressed in graphene transistor mixers operating near the Dirac point due to the symmetrical transfer characteristics.

Table 1

The component parameter values for the device shown in Figure 3.

C_{pg} (fF)	R_g (ohm)	R_{ds} (ohm)	g_{mo} (mS)	τ (ps)	R_i (ohm)	C_{ds} (fF)	C_{gs} (fF)	C_{gd} (fF)	L_d (pH)	L_g (pH)	L_s (pH)	R_s (ohm)	R_d (ohm)
1.9	390	124	2.7	0.6	235	0.5	5.5	0.6	54	130	11	4.7	11.6

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