Ambipolar to Unipolar Conversion in Graphene Field-Effect Transistors

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Ambipolar to Unipolar Conversion in Graphene Field-Effect Transistors

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ABSTRACT Typical graphene field-effect transistors (GFETs) show ambipolar conduction that is unfavorable for some electronic applications. In this work, we report on the development of unipolar GFETs. We found that the titanium oxide situated on the graphene surface induced significant hole doping. The threshold voltage of the unipolar p-type GFET was tunable by varying the density of the attached titanium oxide through an etching process. An annealing process followed by silicon nitride passivation was found to convert the p-type GFETs to unipolar n-type GFETs. An air-stable complementary inverter integrated from the p- and n-GFETs was also successfully demonstrated. The simple fabrication processes are compatible with the conventional CMOS manufacturing technology.

KEYWORDS: graphene · transistor · unipolar · p-to-n conversion · complementary inverter

Since the discovery of graphene in 2004, intensive research has been devoted to this two-dimensional (2D) carbon atom lattice arranged in a honeycomb structure of hexagons.[1−3] The 2D carbon sheet has a linear dispersion relation near the Dirac point. This causes electrons and holes to be massless Dirac fermions with extremely high mobilities[4−6] and makes graphene an ideal candidate for many nanoelectronic applications. Although the properties of this material have been intensively studied for several years, very little progress in the applications of graphene in complex and advanced functional logic circuits has been achieved. One of the main reasons is that the semimetallic nature of the pristine graphene sheet causes graphene (G) field-effect transistors (FETs) to exhibit ambipolar conduction.[4,7] Though several electronic applications have been demonstrated with the ambipolar characteristics of GFETs,[8,9] unipolar GFETs are required in complicated logic gates and circuits. Chemical molecule adsorption was found to shift the threshold voltages of the transfer curves of GFETs, but not to cause ambipolar-to-unipolar transition.[5,7] Nitrogen atoms were used to dope graphene and achieve unipolar n-type conduction.[10] However, the gaseous chemicals and high temperature involved in the CVD process make it impossible to selectively dope local areas in graphenes. Recently, GFETs with nickel and cobalt electrodes were found to show significantly asymmetric electron and hole conduction currents.[11,12] The observed distorted transfer curves were attributed to the weakened Fermi level pinning[13,14] in graphene underneath the electrode.[11] To the best of our knowledge, the present work represents the first experimental demonstration of unipolar p- and n-type GFETs consisting of large-area graphene channels. In addition, we also report a simple process to integrate such p- and n-type GFETs into complementary inverters. A reliable inverting operation at a low operating bias is demonstrated in air ambient at room temperature. The controllable threshold voltages of the unipolar GFETs, along with their CMOS-compatible fabrication processes, offer the promising advantages that could make large-scale fabrication of functional graphene-based logic gates and circuits feasible.

RESULTS AND DISCUSSION

As illustrated in Figure 1, a graphene flake was mechanically exfoliated from a piece of commercially available nature graphite with Scotch tape.[1] Optical microscopy and a Raman spectrum were used to confirm its monolayer nature. Subsequently, a 20-nm-thick titanium (Ti) layer was deposited on top of the flake. Optical lithography was used to pattern a rectangular stripe of photoresist on top of the Ti layer. The Ti film that was not covered by the photoresist was etched away chemically. Oxygen plasma etching was then performed to remove the exposed graphene and clean the wafer surface. A graphene flake passivated by the Ti stripe was obtained after removal of the photoresist (see Figure 1b). Afterward, standard lithography and lift-off processes were employed to fabricate the contact electrodes (Ti/Au). The Ti layer between the Au electrodes was then removed chemically (see Figure 1d). These fabrication processes have two advantages: (1) the Ti layer protects the graphene from any possible chemical contamination during the fabrication processes and (2) the Ti electrodes form intimate contacts with

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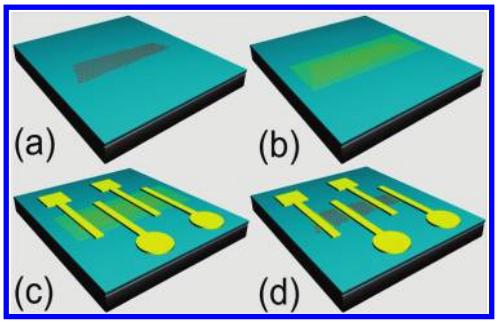

Figure 1. Schematic GFET fabrication processes. (a) A single-layer graphene flake is placed on the surface of a heavily doped silicon wafer capped by a 285-nm-thick SiO_2 layer. (b) The graphene flake is passivated by a 20-nm-thick Ti layer. (c) Ti/Au electrodes are formed on top of the graphene flake covered by the Ti layer. (d) The Ti layer between Au electrodes is removed using a wet etching process.

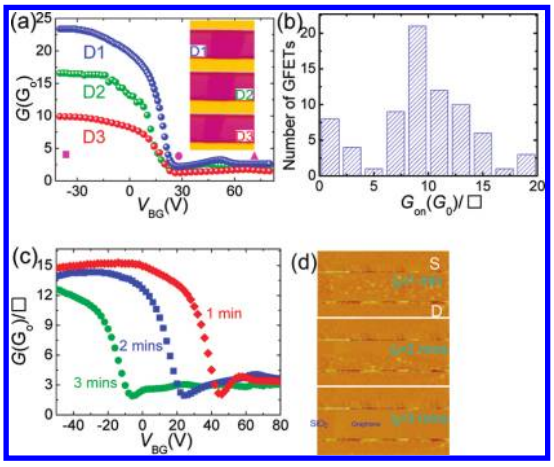

Figure 2. Unipolar p-GFETs. (a) Transfer characteristics of three typical GFETs from a single graphene flake (subjected to 2 min Ti etching). Inset: Optical microscopy images of the devices. (b) On-state conductance (per square) distribution of 75 GFETs. (c) Transfer characteristics of a GFET subjected to 1, 2, and 3 min Ti etching, respectively. (d) AFM images of the GFET after 1 (t_e = 1 min), 2 (t_e = 2 min), and 3 min (t_e = 3 min) Ti etching. The SiO_2 and graphene surfaces are on the left- and right-hand side, respectively.

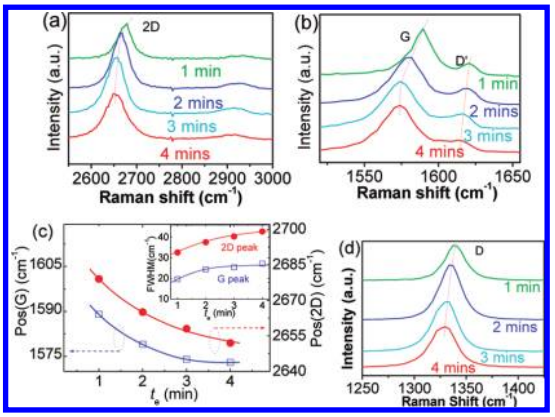

Figure 3. Raman spectra as a function of the etching time. All the Raman spectra are renormalized to the G peak. (a) 2D peak and (b) G and D′ peaks after 1, 2, 3, and 4 min etching, respectively. (c) Etching time-dependent position of G (POS(G)) and 2D peak (POS(2D)). Inset: fwhm of G and 2D peak as a function of etching time. (d) D peak after 1, 2, 3, and 4 min etching, respectively.

as-exfoliated fresh graphene surface without any process residues (*e.g.*, photoresist) in between. All of the *I*−*V* characteristics were obtained in air ambient at room temperature.

Figure 2a presents the transfer curves of three GFETs fabricated using the aforementioned processes on a single graphene flake (see the inset for optical images). These three GFETs have a similar threshold voltage (where the maximum transconductance occurs) of 20 V, but different on-state conductances (in units of quantum conductance $G_0 = e^2/h$). In contrast to the ambipolar conduction of a typical pristine graphene (without Ti decoration) FET with Ti/Au contacts (see Figure S1b of the Supporting Information), all the Ti-decorated GFETs exhibit very clear unipolar transfer characteristics. Figure 2b depicts a statistical summary of 75 devices fabricated under the same conditions, where 58 out of the 75 devices showed on-state conductance G_{on} between 7 and 15 G_0 per square, comparable to those of our pristine graphene FETs. Moreover, given the back-gate capacitance of 11.5 nFcm^{-2},[15] the field-effect mobilities of these Ti-decorated p-type GFETs are estimated to be around 1000−1400 cm^2 V^{-1} s^{-1}, suggesting little degradation in comparison with those of our pristine graphene FETs. More importantly, we found that the threshold voltages of these devices are tunable by varying the density of Ti adatoms through the wet etching process. For example, the threshold voltage decreases from 38 to −12 V when the etching time t_e increases from 1 to 3 min, as shown in Figure 2c. The corresponding atomic force microscopy (AFM) images in Figure 2d indicate that the density of the Ti adatoms does decrease with the increasing etching time. These observations suggest that the threshold voltages of the Ti-decorated GFETs depend on the density of the Ti adatoms.

In order to study the origins behind the dependence of threshold voltage on the Ti adatom density, we investigated the evolution of the Raman spectra as a function of t_e. The Raman spectra were excited with a 532 nm line at an incident power less than 1 mW (laser spot diameter of 500 nm) to avoid overheating the graphene. As displayed in Figure 3a, significant red-shift (27 cm^{-1}) and broadening of the 2D peak[16] can be seen as the density of Ti adatoms decreases. In other words, increasing the Ti adatom density results in a blue-shift and narrowing of the 2D peak. These observations are consistent with the effects of hole doping induced by applying an appropriate gate voltage (electrostatic doping)[17] and aromatic molecules (chemical doping), where blue-shift of the Raman 2D peak was observed.[18] Electrostatic doping obviously should not be the reason, as no gate voltage was applied during the Raman measurement here. The

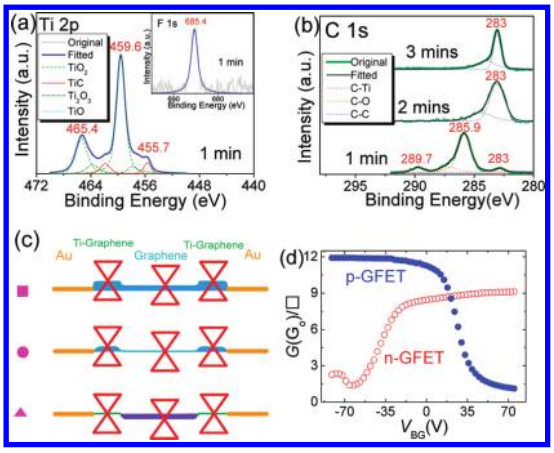

Figure 4. XPS spectra and transport mechanisms. (a) Measured and fitted Ti 2p XPS spectra after 1 min etching. Inset: Measured and fitted F 1s XPS spectra after 1 min etching. (b) Measured and fitted C 1s XPS spectra after 1, 2, and 3 min etching, respectively. The XPS spectra are renormalized to their main peaks. (c) Schematic energy band diagrams of the unipolar p-type GFETs at on-state (■), threshold point (●), and off-state (▲), respectively. (d) Transfer curves (at V_{DS} = 10 mV) of a typical GFET before and after Si_3N_4 passivation, respectively.

doping effect therefore could be attributed to the charge transfer between Ti adatoms and graphene.

The evolution of the G peak provides us with another insight. With increasing t_e, a red-shift of 16 cm^{-1} and the broadening of the G peak were observed (see Figure 3b). This may reflect that the hole doping effect weakens with decreasing Ti adatom density during the etching process, since both hole and electron doping move the Fermi level away from the Dirac point and result in a blue-shift of the G peak.[19,20] As summarized in Figure 3c, the shift of the G peak position POS(G) agrees well with that of 2D peak position POS(2D). In addition, the full-width at half-magnitude (fwhm) of both the G and 2D peaks increases with t_e, as depicted in the inset of Figure 3c. This observation suggests that E_f moves toward the Dirac point, leading to enhanced creation of electron−hole pairs excited by phonons. As a result, the phonon lifetime is decreased and the fwhm is increased.[19,21] It is also worth noting that the uniaxial tensile strain and the compressive stress typically result in a red-shift and blue-shift of the G peak in graphene, respectively. However, no significant peak width variation was observed.[22−24] In this sense, the observed variation in the Raman spectra here should not be induced by strain/stress. In addition, the presence of D′ (see Figure 3b) and D peaks (see Figure 3d) suggests a strong interaction between graphene and Ti adatoms.

The interaction between graphene and Ti adatoms was characterized using X-ray photoelectron spectroscopy (XPS).[25] Ti 2p XPS peaks for t_e = 1 min are shown in Figure 4a, while they were not detectable after 2 or 3 min etching. The main peaks at 459.6 and 465.4 eV can be attributed to TiO_2. The peaks at 457.9 and 463.7 eV are owing to Ti_2O_3, and the peak at 456.9 eV is due to TiO.[26−28] The two peaks at 455.7 and 461.9 eV ascribed to TiC suggest the direct interaction between Ti adatoms and graphene.[29,30] In fact, the charge transfer induced by the interaction between the Ti atom and graphite is still under argument.[29,31,32] Ramqvist *et al.* reported weak electron transfer from Ti to C atoms.[31] On the other hand, Ma and co-worker demonstrated negligible charge transfer between Ti and C atoms, as Ti adatoms interact with a pristine graphite surface through van der Waals forces in ultrahigh vacuum, and the interaction is catalytically enhanced by even a trace amount of oxygen.[32] The observed XPS peaks here suggest that the majority of Ti atoms react with O atoms, and only a small amount of Ti atoms form Ti−C bonds. A theoretical study showed that oxidized Ti atoms situated on a graphene π-electron network result in net hole transfer to graphene,[29] consistent with the observed p-type conduction here. This further confirms that Ti oxide plays a major role of hole doping.[33,34] In addition to Ti element, a small amount of fluorine (F) was also observed on graphene (inset of Figure 4a), as HF was used in the wet etching process. The F peak appears only at 685.4 eV, and it is clearly owing to HF, indicating that neither graphene nor Ti was fluorinated.

As shown in Figure 4b, the evolution of the C 1s XPS spectrum as a function of the etching time shows three notable features: (1) two peaks at 285.9 and 289.7 eV were observed for t_e = 1 min, but not for t_e = 2 and 3 min; (2) the dominant peak was situated at 283 eV for t_e = 2 and 3 min, while the peak at 285.9 eV dominated the spectrum for t_e = 1 min; and (3) the main peak at 283 eV became narrower for t_e = 3 min. The two peaks at 285.9 and 289.7 eV can be attributed to C atoms interacting with Ti oxide.[29,35] The Ti oxide-related C 1s peaks vanished, consistent with the disappearance of Ti 2p peaks, for t_e = 2 and 3 min. In contrast, the strong peak at 283 eV ascribed to the C−C sp^2 bond[36−38] suggests more pure graphene surface was obtained after wet etching for t_e = 2 and 3 min. Moreover, the narrower C−C peak for t_e = 3 min suggests that the disturbance of graphene electronic structure induced by C−Ti oxide interaction was significantly restored.[36]

We suggest that the graphene segments underneath the Au electrodes serve as doped contacts, while the center part of the channel becomes much less p-type after etching the Ti layer. Then, the device can be divided into three parts, *i.e.*, Ti/Au electrodes (orange color), doped graphene contacts (green color), and graphene channel (cyan color), as shown in Figure 4c, which illustrates the schematic energy band diagrams of the device at thermal equilibrium (see Figure 2a for the corresponding labels). At a large negative V_{BG} (■), the doped graphene contacts and channel are electrostatically doped to strong p-type, and the Fermi level is situated in the valence band of all

three segments of the graphene flake. The channel current is dominated by hole transport through two p^+-p junctions. Thus the device shows strong p-type conduction (see ■ in Figure 2a). At the threshold point (●), the Fermi level in the graphene channel is shifted upward to the Dirac point. As a result, the current channel consists of two p−i junctions. Owing to the reduced density of states (DOS) in the graphene channel, the conductance reaches the minimum. Similarly, another conductance minimum is expected when the Fermi level of the doped graphene contact regions reaches the Dirac point under an appropriate positive V_{BG} (▲). An alternative way to interpret the device performance is to view the entire system as two resistors connected in series; that is, the graphene channel is connected in series with the doped graphene contacts. The conductance G is proportional to the DOS of the graphene in the channel ($D_{ch}(E_F)$) and doped contact ($D_{co}(E_F)$) through $G \propto D_{ch}(E_F)D_{co}(E_F)/[D_{ch}(E_F) + D_{co}(E_F)]$. Thus, G reaches a valley when either $D_{ch}(E_F)$ or $D_{co}(E_F)$ reaches its minimum.[7]

The striking differences between the Ti-decorated and pristine graphene FETs could result from the atomic layers of Ti oxide existing between the Ti passivation layer and Ti/Au electrodes. In most cases, the charge density of pristine graphene underneath the electrodes is pinned by the metal.[13,39] Thus, DOS of the pristine graphene is not tunable by V_{BG}. On the contrary, the Ti oxide atomic layers in our GFETs could weaken the charge density pinning effect in the Ti-decorated graphene underneath Au electrodes and, hence, improve the controllability of the back-gate voltage on the DOS of the graphene. To address this issue, atomic layers of Ti oxide were introduced into pristine GFETs as control samples. The control samples did show expected unipolar p-type conductions (see Figure S1c of the Supporting Information). Moreover, the current saturation in the transfer curve could be attributed to the interfacial phonon scattering induced by the Ti adatoms.[40]

Unipolar n-type GFETs were obtained simply through annealing the p-type GFETs at 200 °C in nitrogen ambient for one hour and subsequently coating a 200-nm-thick Si_3N_4 passivation layer at 110 °C. Obviously, the annealing and Si_3N_4 deposition processes could cause (1) the desorption of oxygen on the Ti-decorated graphene channel and Ti/graphene contacts and (2) an intimate interaction between the graphene and Si_3N_4 layer. Si_3N_4 layer passivation does not induce doping effects in graphene,[41] while the adsorbed oxygen molecules on the surface of graphene can induce hole doping.[42] The aforementioned hole doping effect in p-type GFETs could result from both oxidized Ti atoms and adsorbed oxygen. Hole doping would be greatly decreased after oxygen was desorbed because the catalytically created reactive sites, where the interactions between Ti and carbon atoms occurred, became much less.[32] Thus, the influences of the annealing and Si_3N_4 deposition processes could be twofold: (1) to vary the doping in the graphene channel and (2) to shift

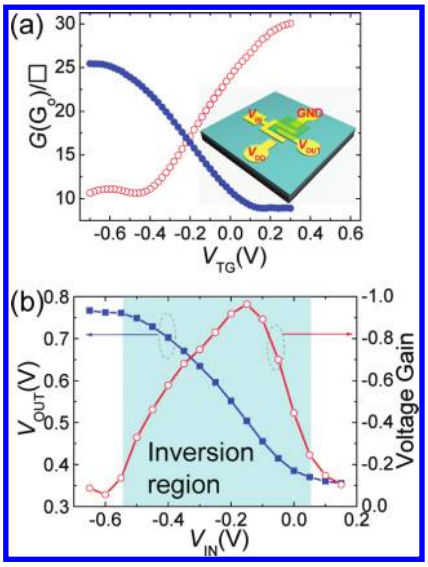

Figure 5. Complementary graphene logic inverter. (a) Transfer characteristics of a top-gated p- and n-GFET, respectively, at V_{DS} = 1 V. Inset: Schematic of a complementary graphene inverter. The Si_3N_4 passivation layer (green color) was introduced to have an n-type GFET. The input voltage, output voltage, bias voltage, and ground are labeled with V_{IN}, V_{OUT}, V_{DD}, and GND, respectively. (b) Output versus input characteristics and voltage gain of a complementary graphene inverter with operating bias V_{DD} = 1 V in air ambient at room temperature.

the work function of the contact electrode.[43] As discussed earlier (Figure 4c), the degree of doping would alter the charge concentration in the channel and then change the threshold voltage, while any variation in the contacts does not modulate the charge concentration in the channel and, thus, is not able to change the threshold voltage. Nevertheless, the threshold voltage decreases from 27 V (p-GFET) to −42 V (n-GFET) after Si_3N_4 layer passivation, as shown in Figure 4d. Therefore, we believe that the change in the degree of doping is the dominant reason for the p-to-n conversion and threshold voltage variation. Interestingly, the p-type characteristic of the GFET was restored after removal of the passivation layer (see Figure S2a of the Supporting Information). This confirms the important role of oxygen and/or water molecule desorption in the conduction-type conversion.

Top-gated p-GFETs were fabricated with 10-nm-thick Al_2O_3 (deposited using an electron-beam evaporator) as the gate dielectric, as shown in Figure 5a. The threshold voltage of the top-gated p-GFET is −0.1 V at V_{DS} = 1 V (solid circles). An annealing process at 200 °C in nitrogen ambient followed by a Si_3N_4 layer deposition was employed to convert the top-gated p-GFET to n-GFET with a threshold voltage of −0.3 V (open circles). A complementary graphene logic inverter was formed with a top-gated p-GFET and an n-GFET connected in series (see the inset of Figure 5a). The p-type characteristic was restored by selectively removing the Si_3N_4 layer above the p-GFET in the inverter. The graphene flake used for an inverter was etched into a rectangular stripe in order to have a good

matching of the electrical characteristics of the two transistors. As depicted in Figure 5b, the voltage gain at a bias voltage V_{DD} = 1 V is around unity, which is sufficient to drive the next stage component in a logic circuit. As the thin top-gate dielectric leads to the small threshold voltage, the inverter can function properly with the input voltage (V_{IN}) and bias voltage (V_{DD}) lower than 1 V in air ambient at room temperature. Previously reported graphene inverters, which were constructed from ambipolar GFETs with different Dirac points,[44−47] had nonsaturated output voltage outside the inversion region; that is, the output voltage V_{OUT} for the high (low) "state" decreased (increased) outside the inversion region, resulting in a weak reliability. Moreover, as the Dirac points of GFETs were very sensitive to the contaminants introduced in the fabrication or characterization processes,[5,7] the inverters required a vacuum environment for their stable inverting operations. It should be pointed out that V_{OUT} of our graphene inverter saturates outside the inversion region (cyan color), suggesting a much superior reliability in comparison with the ambipolar GFET-based inverters.

CONCLUSIONS

Unipolar p- and n-type GFETs have been successfully developed. Hole-doped graphene was achieved as a result of strong interactions between carbon atoms and titanium oxide. The degree of hole doping was well controlled by tuning the density of titanium adatoms on the graphene surface. Removal of oxygen and/or water molecules on the device surface resulted in p- to n-type conversion. Moreover, an air-stable complementary graphene inverter with operating bias as low as 1 V was successfully demonstrated.

METHODS

Graphene flakes were mechanically exfoliated from commercially available nature graphite using Scotch tape. Optical microscopy and a Raman spectrum were used to identify the monolayer graphene flakes. The monolayer graphene flakes on a SiO_2 (285 nm)/p-type silicon substrate were immediately transferred into an electron-beam evaporator, and a 20-nm-thick Ti layer was deposited. Optical lithography techniques were used to pattern a rectangular stripe of photoresist on top of the Ti film. The Ti film that was not covered by the photoresist was etched away using hydrofluoride (HF), hydrodioxide (H_2O_2), and deionized water with a volume ratio of 1:1:200 (the etch rate was around 20 nm/min). This was followed by oxygen plasma etching (20 sccm O_2 flow with rf power of 30 W) for 8 min to remove the exposed graphenes and clean the wafer surface. A graphene flake passivated by the patterned Ti film was obtained after removal of the photoresist. Afterward, standard optical lithography and lift-off processes were carried out to pattern the contact electrodes (Ti/Au). Lastly, the Ti passivation layer between the Au electrodes was removed using the wet etchant. The top-gate dielectric Al_2O_3 was deposited using an Edward electron-beam evaporation system. To convert a p-GFET to n-GFET, the device was annealed in nitrogen ambient at 200 °C for one hour, followed by a Si_3N_4 layer deposition in a plasma-enhanced chemical vapor deposition (PECVD) system at 110 °C. Saline (100 sccm) and ammonia (20 sccm), with nitrogen (600 sccm) as the background gas, were used as the reaction gas species. The rf power used for deposition was 20 W. The as-fabricated sample with "inverter" structure was annealed in nitrogen ambient at 200 °C for one hour, followed by a 600-nm-thick Si_3N_4 layer deposition at 110 °C. Then, a photoresist window was formed above the p-GFET using a standard lithography process. With the photoresist as the etching mask, the Si_3N_4 layer above the p-GFET was selectively etched away using HF and deionized water with a volume ratio of 1:20 (the etch rate was around 10 nm/s).

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Supporting Information Available: Illustration of the structure of the Ti-decorated sample (Figure S1a), transfer characteristic of a pristine graphene FET (Figure S1b), transfer characteristics of the two control samples (D1 and D2) (Figure S1c), p- and n-type transfer characteristics of the GFET with and without Si_3N_4 passivation, respectively (Figure S2a), schematic energy band diagrams of an n-type GFET (Figure S2b). This material is available free of charge *via* the Internet at http://pubs.acs.org.

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