Coplanar-Gate Transparent Graphene Transistors and Inverters on Plastic

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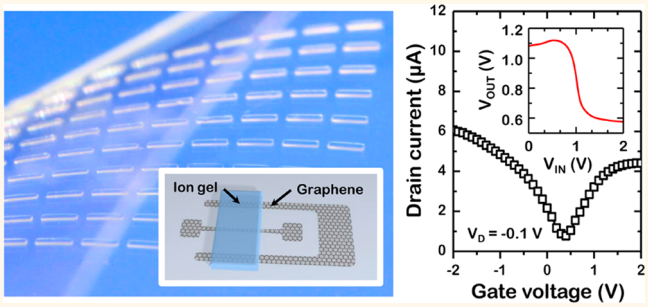
ABSTRACT



Transparent flexible graphene transistors and inverters in a coplanar-gate configuration were presented for the first time using only two materials: graphene and an ion gel gate dielectric. The novel device configuration simplifies device fabrication such that only two printing steps were required to fabricate transistors and inverters. The devices exhibited excellent device performances including low-voltage operation with a high transistor-on-current and mobility, excellent mechanical flexibility, environmental stability, and a reasonable inverting behavior upon connecting the two transistors.

KEYWORDS: graphene transistor · coplanar-gate configuration · transparent electronics · flexible electronics

Graphene has attracted significant attention due to its optical transparency, mechanical flexibility, and high carrier mobility.[1−6] To exploit these properties of graphene in large-area flexible electronics, a variety of printing methods of graphene and other device components have been developed. For example, assembling graphene-based thin-film transistors (TFTs) can be achieved using combinations of transfer-printing techniques applied to graphene films grown by chemical vapor deposition (CVD) or graphene oxide dispersion-based solution processes with various printing methods of gate dielectric and electrode, which have been investigated extensively in the field of organic electronics.[7−9]

From a practical perspective, the progress in printed graphene electronics could be further accelerated using a simpler TFT configuration that would require fewer printing steps.[10,11] Graphene is, in fact, an excellent material for use in TFTs with simplified configurations. As a single material, graphene features both semiconducting and metallic behavior and thus can function as a semiconductor channel as well as an electrode.[12−15] Therefore, the active channels and source/drain electrodes can be formed using a monolithic graphene layer *via* a single printing process.[16] Also, the use of electrical double layer capacitors as gate dielectrics can alleviate constraints on the positions of the gate electrodes.[17,18] Consequently, the development of graphene-based TFTs with unconventional and simple device configurations is highly promising.

To this end, we demonstrate the preparation of transparent flexible graphene transistors with a coplanar gate configuration based only on two materials, graphene and an ion gel gate dielectric. Moreover, flexible complementary graphene inverters prepared on a plastic substrate are presented for the first time by connecting two coplanar-gate graphene transistors. A single graphene transistor consists of a main graphene strip, a patch of graphene (with split arms) positioned away from the main strip, and an ion gel gate dielectric bridging the two components. The main strip of graphene functions as an active semiconducting channel and the source/drain electrodes, depending on its contact with the ion gel. The split arms, which are patterned to be coplanar with the main graphene strip, serve as the gate electrode. This unconventional device geometry with a coplanar-gate configuration dramatically simplifies the device fabrication such that only two printing steps were required to fabricate transistors and inverters. The resulting coplanar gate graphene transistors exhibit excellent device performances including low-voltage operation with a high transistor-on-current and mobility,

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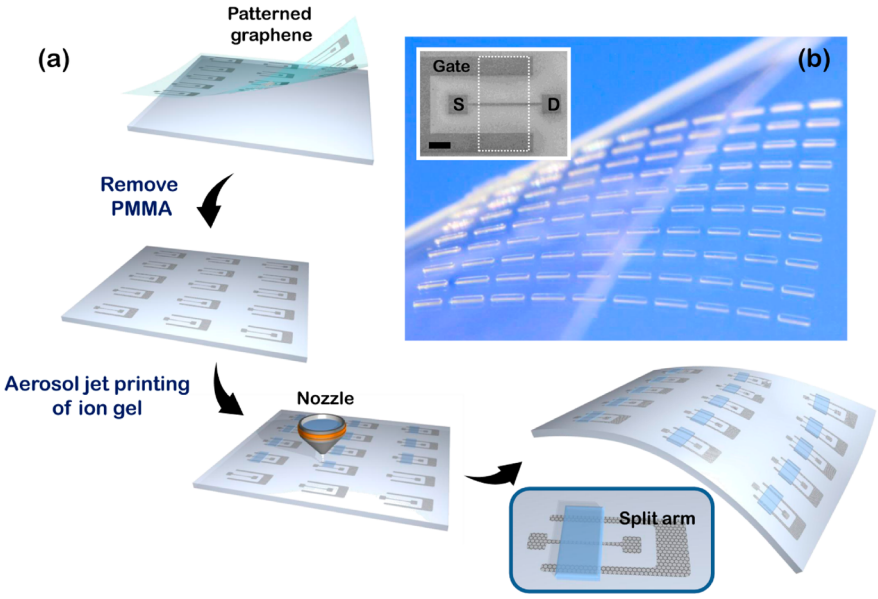

Figure 1. (a) Schematic diagram showing the fabrication of an ion gel-gated graphene transistor array in a coplanar gate configuration on a flexible plastic substrate. (b) Photograph of the coplanar-gate graphene transistor array. The inset shows an optical microscopy image of a coplanar-gate graphene transistor (scale bar: 200 μm).

excellent mechanical flexibility, environmental stability, and a reasonable inverting behavior upon connecting the two transistors. Accordingly, the coplanar-gate graphene transistors provide a novel and simple route to achieving low-cost printed flexible graphene electronics with a high device performance.

RESULTS AND DISCUSSION

Figure 1a illustrates the fabrication of coplanar gate graphene transistors with an ion gel gate dielectric on a plastic substrate. To begin with, high-quality monolayer graphene was synthesized *via* CVD over a large-area Cu foil, as described previously.[19] Multiple strips and split arms of graphene were then formed on the Cu foil by photolithography and oxygen plasma etching. The distance between the split arms and the graphene stripes was 300 μm. Note that we introduced the split arms gate electrode instead of a single arm structure to achieve more uniform charge accumulation across the width of channel. A supporting polymer layer used for transfer-printing was spin-coated onto the graphene patterns on the Cu foil, and the Cu foil was removed by electrochemical etching. The graphene patterns were then transfer-printed onto a polyethylene terephthalate (PET) substrate, and the supporting layer was removed. Subsequently, an ion gel gate dielectric consisting of poly(styrene-methyl methacrylate-styrene) (PS-PMMA-PS) triblock copolymer and 1-ethyl-3-methylimidazolium bis(trifluoromethylsulfonyl)-imide ([EMIM][TFSI]) ionic liquid was printed across the split arms and a portion of the graphene stripe using an aerosol jet printing technique. Note that the long-range polarizability of the ion gel gate dielectrics enabled the gate electrode (split arms) to be offset completely from the channel (main strip)[20] and positioned to be coplanar with the channel. The graphene strip segment in contact with the ion gel functioned as the channel of the transistor with a conductance that could be tuned by the bias applied at the split arms gate electrode, while the remainder of the strip formed the source/drain electrodes. The length (L) and width (W) of the channel were 500 and 10 μm, respectively. A photograph of the as-prepared coplanar-gate graphene transistor array is displayed in Figure 1b. The coplanar gate graphene transistors also exhibit good optical transparancy. Figure 2 displays the transmittance of the layered films over the visible and near-infrared spectral range. The transparency of a neat PET film depended weakly on the wavelength and was approximately 92%, for example, at 550 nm. The overall transparency was reduced after transferring a graphene monolayer onto PET and slightly more after patterning the ion gel on the graphene layer but was still above 80% (84% optical transparency at 550 nm).

Typical drain current (I_D)−drain voltage (V_D) characteristics of a coplanar-gate graphene transistor at five different gate voltages (V_G) are plotted in Figure 3a, demonstrating reasonable gate modulation. Note that large drain currents were obtained at low drain and gate voltages ($I_D \approx 30$ μA at $V_G = -2$ V and $V_D = 0.5$ V with a L/W ratio of 50). These results were attributed to the very large capacitance of the ion gel gate dielectrics. A specific capacitance of 8.1 μF/cm^2 was obtained at 10 Hz from a metal/insulator/metal test structure in a coplanar electrode configuration [Figure 3b].[21] I_D is also displayed in Figure 3c as a function of V_G at a given V_D. Clear ambipolar behavior was observed in the gate dependence of I_D, where

positive and negative V_G regions represent electron and hole transport, respectively. Devices show the low operation voltages (<2 V) and the charge neutrality point (Dirac point) around 0 V. The operating speed of these devices, which is unavoidably associated with the relatively slow motion of ions under gate field, is under investigation.

Estimating the mobility (μ) of the devices required a more rigorous calculation to treat the monolithic nature of the graphene devices. It is worth emphasizing that the resistivity of the source and drain electrodes (the portion of the graphene strip not covered with the ion gel) exceeds that of the channel (the portion of the graphene covered with the ion gel) when the device is turned on. These properties differ from those of conventional transistors in which the resistivity of an electrode is, in general, much lower than that of a channel. As a result, accurate estimates of the channel resistance ($R_{channel}$) should consider subtracting the electrode resistance ($R_{electrode}$) from the total resistance (R_{total}) obtained directly from the raw $I-V$ characteristics; $R_{channel} = R_{total} - R_{electrode}$; $R_{electrode}$ could be measured from a separate metal–graphene–metal test structure constructed with the dimensions used for the graphene transistors, as shown in Supporting Information, Figure S1. Accordingly, the channel conductivity ($\sigma_{channel}$), obtained from $R_{channel}$, can be displayed as a function of the carrier density (n) at a given V_G, as shown in the inset of Figure 3c, using the channel dimensions and the following relation,[22,23]

$$|V_G - V_{G,min}| = \frac{h\nu_F\sqrt{\pi n}}{e} + \frac{ne}{C_{EDL}}$$

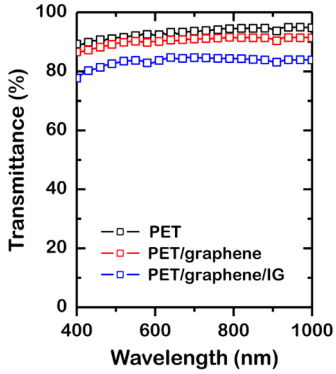

Figure 2. Transmittance of a PET substrate (black) with graphene (red) and an ion gel layer (blue).

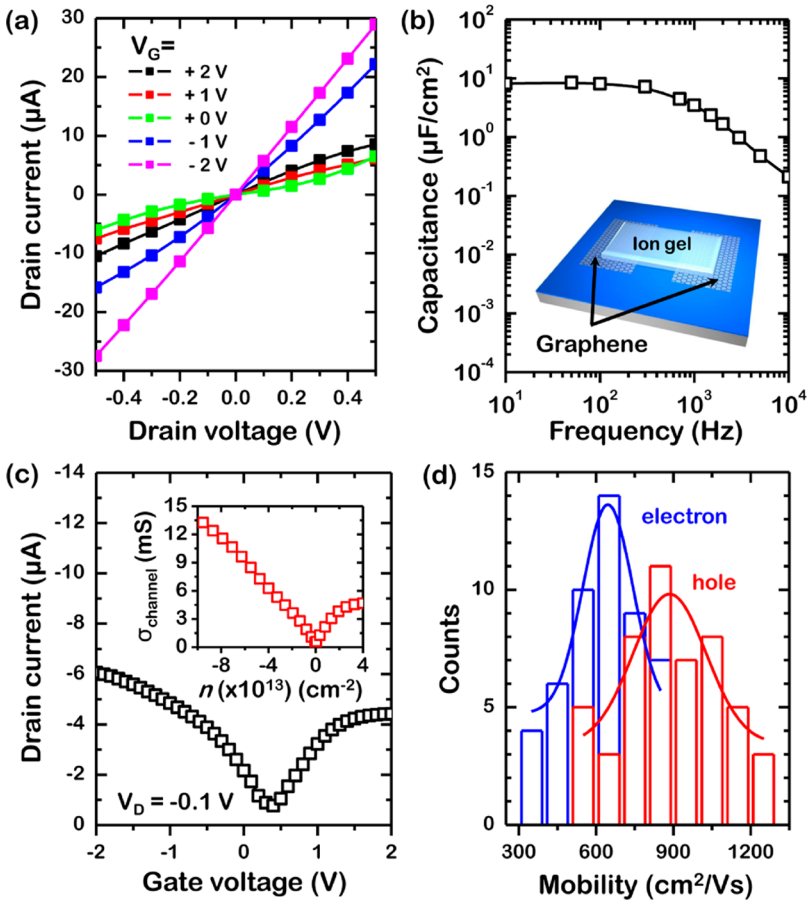

Figure 3. (a) Output characteristics (I_D vs V_D) of a coplanar-gate graphene transistor at five different V_G values. (b) Frequency dependence of the specific capacitance of the ion-gel capacitor in graphene/ion–gel/graphene coplanar configuration. (c) Transfer characteristics (I_D vs V_G) of a coplanar-gate graphene transistor at $V_D = -0.1$ V and the corresponding $\sigma_{channel}$ *vs* n plot (inset). (d) Distribution of the hole and electron mobilities from 50 coplanar-gate graphene transistors.

where h is the reduced Planck's constant, v_F is the Fermi velocity (1.1×10^6 m/s), and C_{EDL} is the electric double layer capacitance.[24] Finally, the carrier mobility is calculated according to $\mu = (d\sigma_{channel}/dn)/e$. Figure 3d displays the distributions of the hole and electron mobilities of 50 devices that are randomly selected among coplanar-gate graphene transistors fabricated from different batches. A Gaussian fit indicates that the hole and electron mobilities were centered on 892 ± 196 and 628 ± 146 $cm^2/(V \cdot s)$, respectively. Moreover, the overall device yield is greater than 95%; this is typical for many batches we have examined. Note that these estimated values (excluding the influence of electrode resistance) determine the upper bound of the nominal mobility values (including the influence of electrode resistance which may be practical for integrated circuit design).

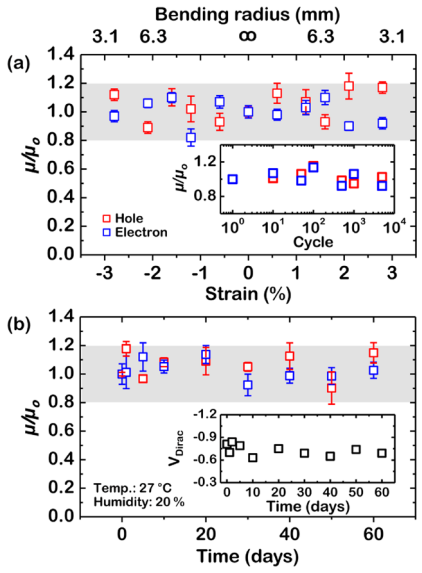

Figure 4. (a) The normalized hole/electron mobilities (μ/μ_o) as a function of strain induced by bending. The inset shows the changes in μ/μ_o after multiple bending cycles at a tension strain up to 2%. (b) Ambient air stability of graphene transistors. The insets show changes in the Dirac point during the stability test.

The mechanical flexibility, robustness, and air stability of the coplanar-gate graphene transistors were investigated. Figure 4a shows the changes in the effective hole and electron mobilities, measured in forward and backward bending tests and normalized by the corresponding mobilities from the unbent state (μ/μ_o). Negative and positive strains corresponded to tension and compression, respectively. Strains within ±2.8% yielded only a 20% change in the hole and electron mobilities. Fatigue tests were also performed on the graphene transistors. The inset of Figure 4a shows μ/μ_o after five thousand cycles of bending, which introduced tension strains between 0% and 2%. The values of μ/μ_o changed relative to the initial values by only 20% after 5000 cycles. Finally, the device stability under ambient conditions was tested. As shown in Figure 4b, almost no appreciable degradation in the device performance was observed, even after storing the devices under ambient conditions for more than one month. Overall, the bending tests, fatigue tests, and air stability tests demonstrated the stable and reliable operation of the flexible graphene transistors.

Finally, complementary inverters were prepared by connecting two coplanar-gate graphene transistors on a plastic substrate; one of the transistors was connected to the supply voltage (V_{DD}), the other was connected to the ground, and the two transistors shared an input gate terminal and an output terminal, as shown in Figure 5a. The circuit diagram of an inverter is displayed in Figure 5b. It should be noted that these devices were fabricated in two simple steps, including transfer printing of graphene and aerosol printing of the ion gel. Details of the inverter operation based on two identical ambipolar transistors, unlike those of complementary inverters based on separate *n*- and *p*-channel transistors, are thoroughly described in refs 25−27. Briefly, the effective channel potential applied to the two identical transistors varies respectively due to the drain potential superposition effect upon sweeping an input signal (V_{IN}) under a constant V_{DD}.[25−27] As a conseqence, their channel resistances

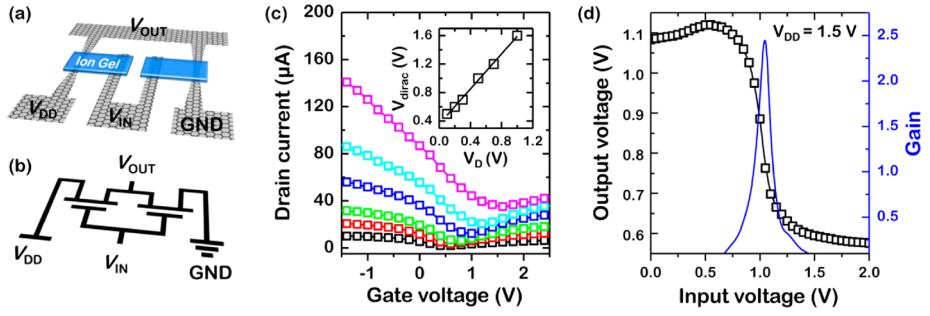

Figure 5. (a) Schematic diagram of a complementary inverter based on two coplanar-gate graphene transistors. (b) Circuit diagram of the inverter. (c) Transfer characteristics (I_D *vs* V_G) of a coplanar-gate graphene transistor at different V_{DS} (from 0.1 to 1 V), demonstrating that the channel resistance at a given gate field can vary if the effective channel potential (drain field) varies. The inset shows V_{dirac} *vs* V_D plot. (d) Input−output voltage characteristic and corresponding gain of a complementary inverter based on coplanar-gate graphene transistors.

(R_1 and R_2) [Figure 5c] and the resulting output signal (V_{OUT}), which follows $V_{OUT} = V_{DD}[(R_2/(R_1 + R_2)]$, change accordingly to yield an inverted signal between the input and the output. As an example, Figure 5d shows a typical $V_{OUT} - V_{IN}$ relation of an inverter based on the coplanr-gate transistors at V_{DD} of 1.5 V. Differing from a typical CMOS inverter, the output voltage did not saturate to zero or V_{DD} due to the zero band gap of graphene.[28,29] $V_{OUT} - V_{IN}$ relations at different values of V_{DD} are displayed in Supporting Information, Figure S2. The signal inversion could be obtained at both positive and negative V_{DD} values due to the ambipolar nature of the constituent transistors. The gain values of these inverters at different V_{DD} values are displayed in Figure S2. A maximum gain of 2.6 was estimated at V_{DD} of 1.5 V, which is sufficient to drive a next stage component in a logic circuit.

CONCLUSIONS

We describe the preparation of transparent flexible graphene transistors and inverters in coplanar-gate configurations based on graphene and an ion gel gate dielectric. Owing to the simple device structure and the unique properties of the materials, the entire device fabrication could be carried out in two steps: transfer of the graphene layer followed by printing of the ion gel. Despite the simple fabrication procedure, these devices exhibited excellent mechanical flexibility and environmental stability. The simple fabrication of coplanar-gate graphene transistors will advance further applications of graphene in printable, transparent, flexible electronics.

EXPERIMENTAL SECTION

High-quality monolayer graphene films were prepared on a Cu foil (thickness 25 μm, 99.8%) *via* CVD, as described previously (Supporting Information, Figure S3).[19] The graphene patterns, including multiple strips and split arms, were defined by photolithography (AZ 1512 and AZ 500 MIF developer) and oxygen plasma etching (~2 s) of the graphene layers on the Cu foil. Poly(methyl methacrylate) (PMMA) supporting layer was spin-coated at 3500 rpm for 30 s onto the graphene patterns on the Cu foil, and the Cu foil was electrochemically etched using an aqueous 0.1 M ammonium persulfate solution. The graphene patterns were then transfer-printed onto a PET substrate (thickness of 188 μm) attached to a glass slice for easy handling. Finally, the supporting layer was removed by dipping in the hot acetone (~60 °C) for 30 min.

The ion gel gate dielectrics were patterned using a commercial aerosol jet printing technique under room temperature. An ion gel ink consisting of PS-PMMA-PS triblock copolymer and [EMIM][TFSI] ionic liquid in ethyl acetate solvent (weight ratio of 0.1:0.9:9) was printed onto the patterned graphene. The ion gel was patterned across the split gate and a portion of the graphene stripe. Upon solvent evaporation, the PS-PMMA-PS triblock copolymer in the [EMIM][TFSI] ionic liquid formed a well-defined physical gel through noncovalent association of PS components that were insoluble in the ionic liquid. The graphene region in contact with the ion gel served as the active channel (L = 500 μm and W = 10 μm), whereas the other region functioned as the source/drain electrodes. In some devices, a layer of Au (50 nm) was patterned onto the portion of graphene that functioned as the source/drain electrodes. These Au layers visually guided the position of the transparent graphene source/drain electrodes during electrical measurements.

Conflict of Interest: The authors declare no competing financial interest.

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Supporting Information Available: Electrical characteristics of a graphene electrode; input−output voltage curves of the inverter devices; Raman spectra of CVD-grown monolayer graphene. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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