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# Axial Diffusion Barriers in Near-Infrared Nanopillar LEDs

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# Axial Diffusion Barriers in Near-Infrared Nanopillar LEDs

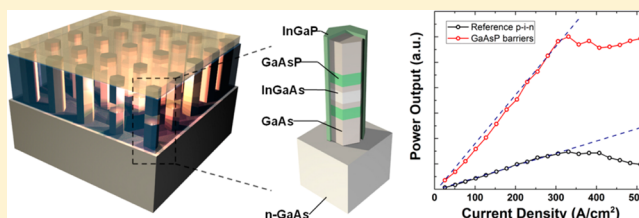
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**S** Supporting Information

**ABSTRACT:** The growth of GaAs/GaAsP axial heterostructures is demonstrated and implemented as diffusion current barriers in nanopillar light-emitting diodes at near-infrared wavelengths. The nanopillar light-emitting diodes utilize an *n*-GaAs/*i*-InGaAs/*p*-GaAs axial heterostructure for current injection. Axial GaAsP segments are inserted into the *n*- and *p*-GaAs portions of the nanopillars surrounding the InGaAs emitter region, acting as diffusion barriers to provide enhanced carrier confinement. Detailed characterization of growth of the GaAsP inserts and electronic band-offset measurements are used to effectively implement the GaAsP inserts as diffusion barriers. The implementation of these barriers in nanopillar light-emitting diodes provides a 5-fold increase in output intensity, making this a promising approach to high-efficiency pillar-based emitters in the near-infrared wavelength range.

**KEYWORDS:** Nanopillar, diffusion barrier, light-emitting diode



Semiconductor nanowires (NWs) and nanopillars (NPs) have been the subject of intense research because of their promise in new nanoscale electronic and optoelectronic devices. Much of their potential is derived from the ability to form complex axial and radial heterostructures that are either impossible or not easily attained using planar epitaxy. Different combinations of axial and radial heterostructures have been implemented in light-emitting diodes,<sup>1–3</sup> lasers,<sup>4,5</sup> photo-detectors,<sup>6,7</sup> and solar cells.<sup>8</sup> In terms of light-emitting devices, the predominant application of NWs has been in the visible wavelength range for future solid-state lighting, with only a few examples of devices operating in the near-infrared.<sup>9–14</sup> Being less developed, the near-infrared devices are missing one of the key components to making a high internal efficiency emitter: an axial high band gap barrier to limit diffusion of carriers past the active region.

In planar GaAs-based emitters, the typical choice for the diffusion barrier layer is Al<sub>x</sub>Ga<sub>1–x</sub>As, as it is lattice-matched for any composition *x*. For GaAs NW- or NP-based emitters, the use of AlGaAs as a barrier has been demonstrated, but the propensity of Al to adhere to the surrounding substrate and NP sidewalls limits the use of AlGaAs to core–shell-type heterostructures.<sup>15</sup> These core–shell-type emitters require a radial current injection scheme, placing the active region in close proximity to the metal contact, which can be highly detrimental to device performance because of band-bending and recombination at the semiconductor/metal interface. For many applications, an axial current injection scheme is necessary in order to maintain separation between the active region and contacts<sup>16,17</sup> while at the same time having a wide-bandgap shell for surface passivation.<sup>11</sup> If an axial current injection scheme is used, then axial heterostructures must also be used to form the diffusion barriers.

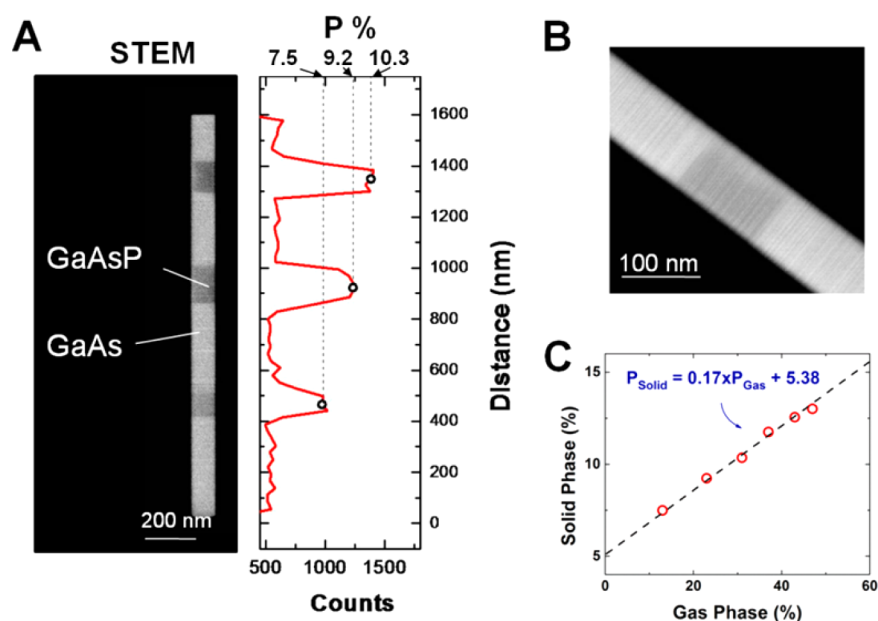
In this work, we demonstrate the growth and application of axial GaAsP diffusion barriers in GaAs NPs. In NP devices, the greatly reduced lattice matching requirements of axial heterostructures<sup>18,19</sup> opens up the possibility of using alternative materials to AlGaAs, making GaAsP a strong candidate for the choice of barrier material as it contains no Al. While in planar devices GaAsP is typically used in strain-compensating layers<sup>20</sup> and strained-layer superlattices<sup>21</sup> with critical thicknesses on the order of 40 nm for 20% phosphorus,<sup>22</sup> compositions of GaAsP with phosphorus below 20% can be completely strain relaxed for NPs with diameters below 100 nm following refs 15 and 16.

In order to properly implement the axial GaAsP heterostructures in any device, a detailed study of the material growth and electronic properties is necessary. With planar structures this characterization would normally be accomplished with a combination of photoluminescence and capacitance–voltage measurements. In NPs, however, the impact of the three-dimensional geometry makes it either difficult or impossible to deconvolve the nonideal effects of the surfaces and interfaces on these measurements. Therefore, an alternate set of measurements and characterization is needed to circumvent these effects. In this case, we implement energy-dispersive X-ray (EDS) measurements and temperature-dependent current–voltage characteristics to determine the compositional dependence on growth conditions and the electronic band-offsets, respectively.

The NP arrays and devices used in this study were grown by selective-area metal–organic chemical vapor deposition with

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**Figure 1.** (a) STEM image of a GaAs NP with multiple GaAsP inserts with EDS data of phosphorus composition as a function of distance along the length of the NP. (b) Magnified STEM image of one of the GaAsP inserts showing the abrupt transition between materials. (c) Plot of solid phase vs gas phase composition of GaAsP extracted from EDS data from the axial GaAsP inserts.

nanopatterned SiO<sub>2</sub> on GaAs (111)B substrates. The SiO<sub>2</sub> selective-area growth mask was deposited by e-beam evaporation to a thickness of 20 nm and subsequently patterned by electron-beam lithography using ZEP-520A as the resist and reactive-ion etching in CHF<sub>3</sub>/Ar plasma. Following resist stripping and O<sub>2</sub> plasma cleaning of the samples, the NP growth was carried out in an Emcore D-125 vertical-flow metal–organic chemical vapor deposition (MOCVD) reactor. The NP growth is divided into two segments. The GaAs, GaAsP, and InGaAs axial heterostructures are grown at a temperature of 720 °C, followed by the growth of the InGaP shell at 600 °C. Further details of the growth and selective-area mask patterning process are described in more detail elsewhere.<sup>23</sup>

To accurately characterize and apply the GaAsP axial barriers using the aforementioned techniques, three different types of NP structures were grown: (i) NPs with multiple i-GaAsP inserts in i-GaAs with varied phosphorus composition, (ii) NP arrays with single n-GaAsP inserts in n-GaAs with InGaP passivation, and (iii) axial n-GaAs/i-InGaAs/p-GaAs NP light-emitting diodes with and without GaAsP barriers. The first type of NP structure, GaAs NPs with multiple GaAsP inserts, is used to characterize the growth of the axial GaAsP segments by scanning transmission electron microscopy (STEM) and EDS. An example NP and data from these measurements is shown in Figure 1. Three samples, each with three GaAsP inserts of varying composition, were used to relate the gas phase composition of arsenic and phosphorus with the solid phase composition and observe any relevant structural changes or defects. In order to maintain simplicity in the growth, the GaAsP inserts were formed only by the addition of tertiary-butyl-phosphine to the gas mixture while the temperature, trimethyl-gallium, and tertiary-butyl-arsenic flow rates were all held constant.

Following growth, the NPs were scraped and deposited on TEM grids for measurement. An STEM image of a NP from the first of the three samples is shown in Figure 1A, where the

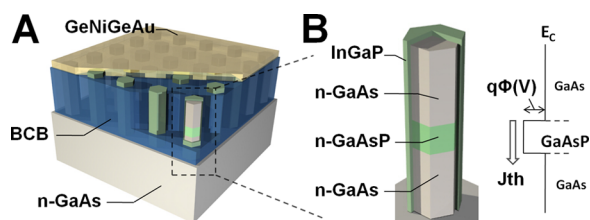
image contrast shows the GaAsP segments as darker regions along the length of the NP. A close-up image of one of the inserts is in Figure 1B, showing the abrupt transition from GaAs/GaAsP. In all three growths a 10 min GaAs segment is grown followed by alternating 2 min GaAsP and 2 min GaAs segments, where a noticeable decrease in growth rate is observed for GaAsP, likely due to the increase in column V overpressure.<sup>24</sup> For the growth represented in Figure 1A, the phosphorus gas phase composition used in the GaAsP segments was varied from 13% to 31% as calculated from the gas flow rates into the chamber. By using the P/(As + P) method, the phosphorus composition as a function of position along the NP was extracted from an EDS scan as shown plotted adjacent to the STEM image in Figure 1A, and the overall composition of each segment was taken to be the average of the EDS data points.

The imaging and composition measurements were repeated for the second and third growths, with the collective data of gas phase vs solid phase composition shown in Figure 1C. For the range of gas phase compositions between 7% and 50%, the incorporation of phosphorus into the solid is linear, as shown by the fitting in Figure 1C. At higher gas phase compositions from 60% to 80%, the GaAsP segments transition from an axial to a core–shell heterostructure. In this composition range, the strain fields are noticeable in TEM images, and the uniformity of the NP arrays decreases, as the NPs have different oblong cross sections rather than hexagonal cross sections. The images show that even for the highest phosphorus composition only small strain fields are observed. Even at this composition, the strain fields show a relaxation of the crystal without defect formation. Additional details of these effects and corresponding TEM images are included in the Supporting Information.

While different temperature and gas flow ratios may impact the phosphorus incorporation rate into the solid, we limit the present work to a fixed set of growth conditions for both GaAs and GaAsP to make device applications of the GaAsP barriers more practical. In this case, the presented data show an upper

limit of about 13% phosphorus in the solid phase while maintaining an axial heterostructure with high-uniformity NP arrays. This composition corresponds to a band gap of 1.58 eV. This energy is 165 meV greater than the band gap of GaAs, which is sufficient for significant blockage of carrier diffusion at room temperature, given an appropriate conduction and valence band offset of the two materials.

In order to determine the relative band-offset between the axial GaAsP and GaAs, a series of temperature-dependent current–voltage measurements must be performed to extract the barrier height from thermionic emission. To accomplish this task, NP devices with the second type of structure described above were grown and fabricated as illustrated in Figure 2A. In this case, arrays of  $\sim 50\,000$  NPs are planarized



**Figure 2.** (a) Schematic of the device structure used to measure the conduction band offset of the GaAsP inserts. (b) Detailed view of the NP heterostructure and (c) conduction band-edge diagram illustrating the thermionic emission limited current flow through the device.

with bisbenzocyclobutene (BCB) and contacted at their tips so that a sufficiently large current is measurable over a wide range of temperature and bias. The NP heterostructure shown in Figure 2B consists of an n-GaAs/n-GaAsP(100 nm)/n-GaAs axial structure with  $\text{In}_{0.5}\text{Ga}_{0.5}\text{P}$  shells ( $\sim 5\text{--}8$  nm) for surface passivation. After planarization, the exposed InGaP at the tips of the NPs is selectively etched in  $\text{HCl}:\text{H}_3\text{PO}_4$  in order to directly contact the n-GaAs core. The contacts to the n-GaAs substrate and n-GaAs top segment of the NP are ohmic Ge/Ni/Ge/Au, so that the band structure of the device is simply the GaAsP barrier with a height equal to the conduction band offset as shown in Figure 2C.

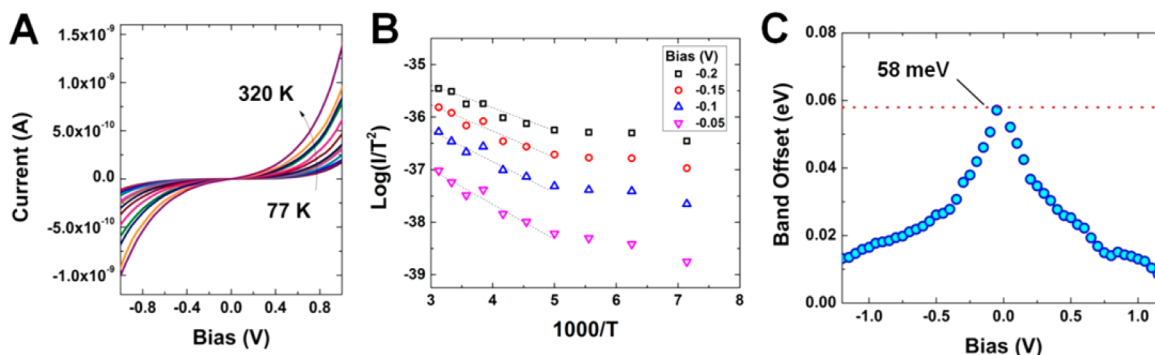
In unipolar devices such as these with a single barrier, the current is limited by thermionic emission of electrons according to  $I \propto T^2 \exp\{-q\phi(V)/kT\}$ , with the barrier height  $q\phi(V)$  being a function of voltage. To extract the zero-bias barrier height corresponding to the conduction band offset, the current–voltage characteristic is acquired over a range of

temperatures as shown in Figure 3A. This allows the barrier height to be extracted at each bias point via a Richardson plot. Figure 3B shows this method for several bias points where the barrier height is extracted for temperatures between 225 and 320 K, below which the thermionic emission is shows little change with temperature.

The barrier height in eV as a function of bias is shown in Figure 3C over a range of  $-1$  to  $1$  V. The bias-dependent height shows a typical inverse u-shape characteristic, where the effective height increases with decreasing bias. From this curve, the zero-bias barrier height corresponding to the conduction band offset can be extracted. In this case the conduction band offset of the single GaAsP insert is shown to be approximately 58 meV. Given the 10.5% phosphorus composition of the inset as determined from prior EDS measurements, this corresponds to a band-offset ratio  $dE_c/dE_v$  of 0.8, making the axial GaAs/GaAsP a type-I heterostructure.

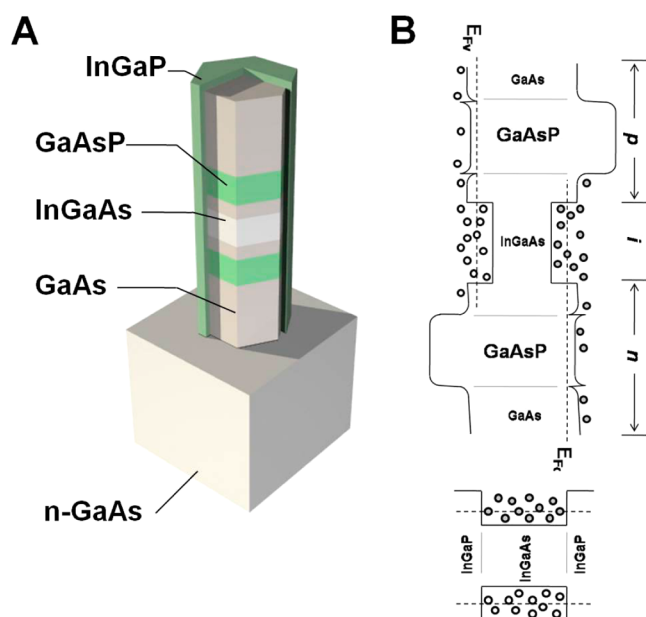
Having performed characterization of the material composition and electronic band offset of the GaAsP inserts, they can be properly implemented in light-emitting diodes to demonstrate their functionality as diffusion barriers. The device design used to test this effect is shown in Figure 4. The basic NP-LED design is a composite axial/core–shell NP heterostructure consisting of n-GaAs/i- $\text{In}_{0.25}\text{Ga}_{0.75}\text{As}$ /p-GaAs segments for current injection with an  $\text{In}_{0.5}\text{Ga}_{0.5}\text{P}$  shell ( $\sim 5\text{--}8$  nm) for surface passivation. The NP arrays are planarized with BCB and contacted with indium–tin–oxide, allowing electroluminescence to be collected vertically from the samples. Further details of the device fabrication and design are reported elsewhere.<sup>11</sup>

In order to quantify the impact of the GaAsP barriers on device performance, NP-LEDs were grown and fabricated with and without the GaAsP barriers. The LEDs with GaAsP were grown with the addition of phosphorus to the n-GaAs and p-GaAs segments with a short 30s break in phosphorus flow both before and after the i- $\text{In}_{0.25}\text{Ga}_{0.75}\text{As}$  emission region, making the complete axial heterostructure n-GaAs/n-GaAsP(100 nm)/n-GaAs/i- $\text{In}_{0.25}\text{Ga}_{0.75}\text{As}$  (200 nm)/p-GaAs/p-GaAsP(100 nm)/p-GaAs. The resulting NPs were  $1.2\text{--}1.3\ \mu\text{m}$  in height for both samples. For consistency with the band offset measurements, the same phosphorus flow rate corresponding to a composition of 10.5% was used for both GaAsP segments. During the GaAsP growth, the dopant flow rates for both Sn and Zn were increased by a factor of 2 in order to shift the barrier to predominantly block minority carriers on either side of the junction as illustrated in Figure 4B. This combination of axial



**Figure 3.** (a) Temperature dependent  $I$ – $V$  curves ranging from 77 K to 320 K. (b) Richardson plot of the current as a function of temperature for several bias points and linear fitting used to calculate band offset. (c) Extracted band offset as a function of bias voltage and extrapolated zero-bias band offset of GaAsP with 10.5% phosphorus.





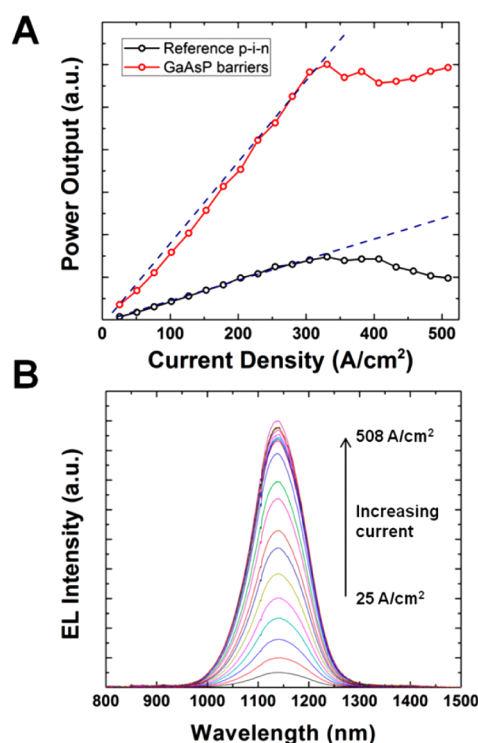
**Figure 4.** (a) Schematic of the device structure used in the NP-LEDs to demonstrate the application of GaAsP inserts as diffusion current barriers and (b) intended electronic band-edge diagrams of the NP in the axial and radial directions under forward bias conditions.

diffusion barriers with InGaP shells provides a complete three-dimensional confinement of carriers to the InGaAs emission region as shown in Figure 4B.

The NP-LEDs with and without GaAsP barriers were measured at room temperature using a 50× magnification long focal length objective lens with a monochromator and liquid-nitrogen cooled InGaAs detector. Electroluminescence was produced from the devices by using a source-meter operating in constant current mode. The results of these measurements are shown in Figure 5. At each current point, the total electroluminescence intensity and spectra were collected as shown in Figure 5A and B, respectively. The LEDs with GaAsP inserts exhibit a significant increase in output intensity at each drive current compared to those without the insets, indicating the effectiveness of the diffusion barriers. The increase in quantum efficiency of the NP-LEDs with the diffusion barriers is nearly 5-fold over the normal LEDs as extracted from the linear fitting of the  $L$ – $I$  curves.

While the NP-LEDs with diffusion barriers exhibit a dramatic increase in output, both devices have an output power saturation at approximately 300 A/cm<sup>2</sup>. Using the  $\Delta V/I$  method, the measured series resistances of the devices are 221  $\Omega$  and 341  $\Omega$  for the NP-LED without and with GaAsP barriers, respectively. The higher series resistance of the NP-LED with GaAsP barriers is expected due to either the abrupt band-offset creating a thin potential barrier or inaccurate doping of the GaAsP segment leading to nonideal band-alignment. In both NP-LEDs the series resistance is an order of magnitude higher than typical planar GaAs devices, which is likely the reason why the output power saturates at relatively low current densities.

The characterization and application of axial GaAsP diffusion barriers in NPs enables many design possibilities beyond the enhancement of electroluminescence in NP-LEDs. With the introduction of an axial barrier, other devices such as detectors and photovoltaics can also benefit. For example, the simple introduction of a diffusion barrier can reduce dark current in



**Figure 5.** (a) Comparison of the  $L$ – $I$  characteristics of the NP-LEDs with and without the GaAsP diffusion barriers and (b) electroluminescence spectra of the NP-LEDs with GaAsP barriers as a function of input current.

photodetectors or serve as a second band gap material for tandem solar cells. Furthermore, the switching of the column V precursor yields highly abrupt interfaces between GaAs and GaAsP. This fact could be exploited to circumvent issues in producing quantum heterostructures with mixed column III elements, which in prior reports have been shown to suffer from compositionally graded interfaces.<sup>25</sup>

## ■ ASSOCIATED CONTENT

### Supporting Information

High phosphorus composition GaAsP inserts, uniformity degradation at high phosphorus composition, Figures S1–S2. This material is available free of charge via the Internet at <http://pubs.acs.org>.

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### Notes

The authors declare no competing financial interest.

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