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ABSTRACT We demonstrate a room temperature processed ferroelectric (FE) nonvolatile memory based on a ZnO nanowire (NW) FET where the NW channel is coated with FE nanoparticles. A single device exhibits excellent memory characteristics with the large modulation in channel conductance between ON and OFF states exceeding 10^4, a long retention time of over 4×10^4 s, and multibit memory storage ability. Our findings provide a viable way to create new functional high-density nonvolatile memory devices compatible with simple processing techniques at low temperature for flexible devices made on plastic substrates.

KEYWORDS Semiconductor nanowires, nonvolatile memory, ferroelectric nanoparticles

Diverse functionalities of semiconducting nanostructures offer the enormous potential for creation of novel field-effect transistors (FETs) serving as the basis for integrated electronic memory and switching devices that go beyond the inherent limitations of conventional semiconducting devices.[1−8] Numerous devices based on one-dimensional (1D) nanostructures have been realized recently demonstrating unique capabilities for next-generation electronic systems.[9−16] In particular, ZnO nanowire (NW) FETs are attracting significant interest as key components for logic circuits and memory devices because of the ability to precisely modulate channel conductance and threshold voltages of FETs through the surface engineering of a ZnO NW.[17,18] This controllability provides a promising route to a range of functionalized memory devices based on a simple low temperature fabrication process that in turn allows for applications on flexible plastic substrates.

Ferroelectric (FE) FETs have attracted great attention because they offer nondestructive memory readout, low-power consumption, good retention, and fast response time, making them promising nonvolatile memory components for widespread use in portable electronic devices such as mobile phones, digital cameras, MP3 players, and smart debit cards.[19−21] Their memory functionality arises from the modulation of the channel conductance by switching the polarization of the FE electrically, which induces charges in a semiconducting channel. Despite these attractive features and favorable architectures with a high-density integration capability, there still remain problems in the fabrication of an acceptable nonvolatile memory device, such as imperfec-

tions and thermal instability at the FE−semiconductor interface, resulting in device performance deterioration due to the high-temperature processing required to obtain high-quality films of inorganic FEs.[19−21] Furthermore, although all-organic FE FETs are highly desirable for easy fabrication, flexibility, and low temperature processes,[20] they also suffer from several problems, which need to be solved, such as an insufficiently low polarization value to effect a high conductance change, air-unstable semiconducting channels, and low retention time and on/off ratios compared to their inorganic counterparts. Thus, a combination of a stable ZnO NW as a semiconducting channel, which is beneficial for tuning and controlling channel conductance due to the large surface to volume ratio, and inorganic FE nanoparticles (NPs) as the gate dielectric surrounding the channel surface can be considered as a viable strategy. These can be processed with simple and inexpensive methods at room temperature. Compared to a conventional film type channel, another benefit with using a nanostructured material is to make it easier to adjust the balance between carriers in the semiconducting layer and FE induced charges for achieving large ranges of modulation in channel conductance and threshold voltages. This allows for various FEs with a wide range of polarization magnitudes. In addition to the issues of flexible, transparent, and low temperature processes for the development of the FE FET memory, the creation of a new functionality such as the multibit nonvolatile memory ability of a single device utilizing beneficial properties of nanostructures is also of particular interest for an ultrahigh density memory. Here, we report a novel nonvolatile memory FET with multibit storage ability using a ZnO NW functionalized with FE NPs as shown schematically in Figure 1. Compared to a conventional FE film based FET, controllable and
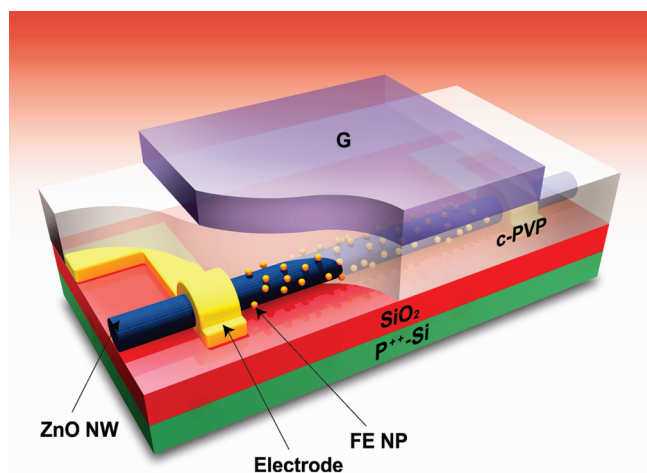
FIGURE 1. A schematic view of a top-gate FET based nonvolatile memory device. For a top-gate ZnO NW FET where a ZnO NW is incorporated with FE NPs, cross-linked poly(4-vinylphenol) (c-PVP) was used as a gate dielectric.
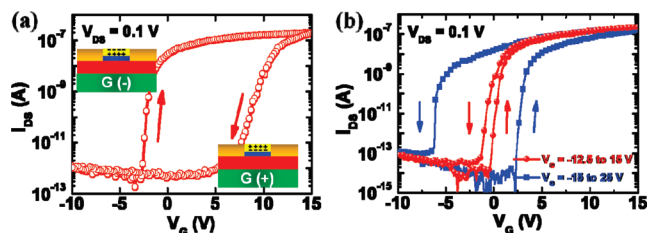

FIGURE 2. Electrical characteristics of a FE NP-coated NW FET. (a) A hysteretic behavior for a back-gate ZnO NW FET after coating FE NPs on the NW surface. The inset shows a schematic view of a back-gate FET. Positive or negative polarization is induced on a semiconducting NW depending on gate voltage sweep directions as shown in the inset of Figure 2a, causing modulation in channel conductance and threshold voltages. (b) Hysteresis behaviors of a top-gate NW FET as a function of the sweep range of gate voltages. Compared to the hysteretic behavior of a back-gate FET with a clockwise hysteresis loop, devices with the top-gate structure show a counterclockwise hysteresis loop, confirming that the origin of such hysteretic behaviors is due to the polarization of FEs. Arrows indicate gate voltage sweep directions.

tunable remnant polarization of FE NPs associated with orientation of dipole moments in the direction of the gate field causes variable and controllable electrical behaviors of ZnO NW FETs, such as channel conductance and threshold voltages.

The ZnO NWs employed in this study were grown on a-plane sapphire substrates with Au catalysts by the vapor phase transport process reported in detail elsewhere (see also Supporting Information).[17,22] ZnO NWs with typical diameters of 100–120 nm were first dispersed by sonication in isopropyl alcohol and then transferred onto a silicon substrate by dropping a liquid suspension of ZnO NWs from a pipet. A 100 nm thick silicon oxide layer was employed as a gate oxide layer on a heavily doped p-type silicon substrate used as a global back gate. Source and drain electrode patterns were defined by conventional photolithography followed by electron-beam evaporation of Ti (80 nm)/Au (40 nm) electrodes on a ZnO NW and lift-off processes. The separation of source and drain electrodes was ~3 μm. Then FE $BaTiO_3$ NPs with an average diameter of 14 nm were coated on the ZnO NW using spin coating with a standard deviation of 4 nm, and the surface density of FE NPs was estimated to be ~5 × 10^{11} cm^{-2} from transmission electron microscopy images (not shown here). The preparation of FE NPs was previously reported.[23] For the top-gate ZnO NW FETs, cross-linked PVP (acting as a dielectric layer) was coated on the prepared substrate with source and drain electrodes, followed by a curing step. The 200 nm thick cross-linked PVP dielectric layer was prepared by mixing PVP (10 wt % of solvent) with additive poly(melamine-*co*-formaldehyde) methylated (5 wt % of solvent) in propylene glycol monomethyl ether acetate (PGMEA).[24,25] Top-gate electrodes were made by electron-beam evaporation of a 50 nm thick Al layer on the PVP layer using a shadow mask.

In order to address whether the FE polarization can affect the electrical transport in a semiconducting channel, we performed transfer measurements with a conventional back-gate FET device structure by sweeping gate voltages from −10 to +15 V and back to −10 V with a sweep rate of 0.2 V/s at V_{DS} = 0.1 V in an ambient environment. Figure 2a shows the hysteretic behavior of back-gate FETs (see Figure S1a in the Supporting Information) after coating FE NPs on the ZnO NW surface. Before FE NPs were added, negligible hysteresis was observed in a conventional back-gate FET exhibiting the typical electrical behavior of an n-channel ZnO NW FET (see Figures S1b and S1c in the Supporting Information), what hysteresis there was being caused by uncontrolled chemical species adsorbed on the ZnO NW when exposed to ambient air.[10,15,26] Noticeably, a considerable increase in hysteresis width was observed after the incorporation of FE NPs into a ZnO NW FET, which was attributed to the polarization of the FE. As the gate voltage was swept from a negative (positive) value, the positive (negative) polarization was induced on the NW surface (the inset of Figure 2a) and thus caused the enrichment (depletion) of electrons in the channel. Consequently, this resulted in an increase (decrease) in the channel conductance at a more negative (positive) value than for a conventional FET, resulting in a clockwise hysteresis loop. These results indicate that a large hysteresis is strongly dependent on the induced charges by the FE.

To examine further the origin of a large hysteresis and the feasibility to modulate the channel conductance and threshold voltages, which define various different states of a memory device, we investigated electrical transport characteristics of FE NP-coated NW FETs with gate voltages being swept from −10 to +15 V as a function of applied gate voltage pulses. We clearly observed reversible, reproducible shifts of transfer curves with a large change in the channel conductance (more than 5 orders of magnitude) and threshold voltages (more than about 11 V) in the same back-gate FET device (see Figure S2a in the Supporting Information), which were measured subsequently after the application of

1 s gate pulses. The transfer curve was shifted toward the positive gate voltage direction when a positive gate pulse (+15 V) was applied. Its initial state was completely recovered from the shifted position after applying a negative gate pulse (−15 V). Furthermore, a significant dependence of transfer characteristics on values of applied gate pulses was also observed (see Figure S2b in the Supporting Information). That is, larger positive shifts in transfer curves from the initial position were induced by applying larger values of positive gate pulses before starting the gate voltage sweeping. Interestingly, a complete recovery of the initial state after various shifts in transfer curves was always achieved by applying a gate pulse of −15 V, indicating that the quantity of polarized charges on the surface of the channel determined by values of applied gate pulses plays a significant role in the channel modulation. These results suggest that large hysteresis and the controllable shifts of threshold voltages mainly originate from the nature of the FE polarization, not surface traps arising from undesirable chemical species adsorbed on the NW surface.[10,15,26] Here, note that conductance and threshold voltages of FE NP-coated NW FETs can be precisely tuned, which is of fundamental importance not only to demonstrate logic circuits with less power consumption and a desirable switching behavior but also to realize memory devices with multilevel storage ability.

To demonstrate the practical memory function of a FE FET based on a combination of a ZnO NW and FE NPs, we fabricated a top-gate FET (Figure 1), which is an attractive architecture to allow the favorable polarization of FEs inducing a more effective field effect on the channel for a nonvolatile memory and to minimize the parasitic capacitance for high-performance devices. Transfer characteristics of FE NP-coated NW FETs with a top gate structure were measured by sweeping gate voltages from different negative values to +15 V and from different positive values to −15 V, respectively (see Figure S3 in the Supporting Information). We clearly observed a strong dependence of threshold voltages on the sweep range of gate voltage as well as sweep directions, as expected. That is, threshold voltages were shifted toward more positive directions with sweeping gate voltages from more negative values, while more negative shifts in threshold voltages were caused as the gate voltage was swept from more positive values. Similar to the dependence of threshold voltage shifts on gate voltage sweep ranges and directions, we observed that a larger gate voltage sweep range led to a larger hysteresis as shown in Figure 2b. Here, an interesting finding is that, unlike the hysteretic behavior of back-gate FETs, a counterclockwise hysteresis loop was observed. This is in good agreement with the nonvolatile memory effect we expect, originating from the polarization switching of FEs. These electrical characteristics of FETs with different configurations, causing the opposite polarization states, clearly indicate that the threshold voltages and hysteresis width are modulated by the polarization
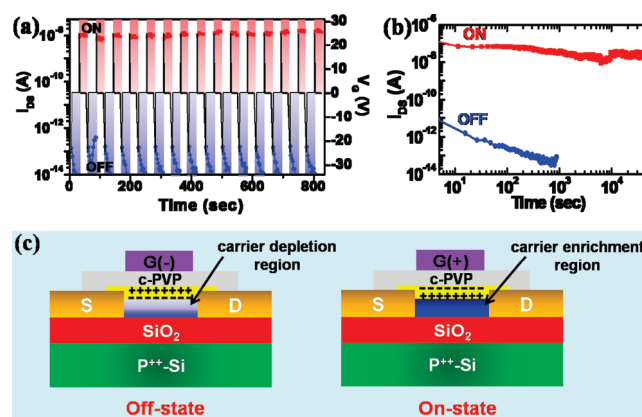

FIGURE 3. Memory properties and switching mechanism of a FE NP-coated NW FET based memory. (a) Reversible, reproducible ON and OFF switching of a device with a top gate structure. (b) Retention times for the ON and OFF states of FE NP-coated NW FETs measured at V_{DS} = 0.1 V and V_G = 0 V after a device was switched ON and OFF using +25 V writing and −25 V erasing pulses, respectively. (c) Schematic views of n-type FE FETs for a simplified field effect model.

of FEs due to the field effect, which induces positive or negative charges in the semiconducting channel according to the polarity sign of applied gate voltages and thus causing the channel modulation.

The reversible switching of the two different conductance states, defined as the ON (high conductance) and OFF (low conductance) states of a memory from a counterclockwise hysteresis, is demonstrated in Figure 3a. The two stable states were continuously measured at V_{DS} = 0.1 V and V_G = 0 V and reproducibly switched with a write and an erase gate voltage pulse of +25 and −25 V, respectively. Remarkably, a large conductance change of ~10^5 (i.e., from ~10 to ~0.001 nA) was observed and completely stable for 70 switching cycles between ON and OFF states of a memory without any device performance degradation. Figure 3b shows retention characteristics of the ON and OFF states of FE NPs-coated NW FETs measured at V_{DS} = 0.1 V and V_G = 0 V after applying a write and an erase gate voltage pulse, respectively. A large change in conductance between ON and OFF states exceeded over 10^4 and was retained over 4 × 10^4 s (>11 h), although the initial ON-current state decayed slowly until the device reached a steady state (~6 × 10^3 s). Li et al. have reported that the physisorption of molecules on the FE surface is strongly and reproducibly polarization dependent.[27] Liao et al. have also reported that charge traps such as water and related molecules at the NW/SiO$_2$ interface give non-negligible effects on the memory endurance of FE FETs.[28] Thus, we believe that the reduction in the initial value of the drain current is attributed to uncontrolled chemical species caused by ex situ deposition of NWs and FE NPs as well as performing the measurements in ambient air (see Figure S1b in the Supporting Information). However, the storage stability of our FE NPs-coated NW FET is comparable to or longer than recently reported memory devices based
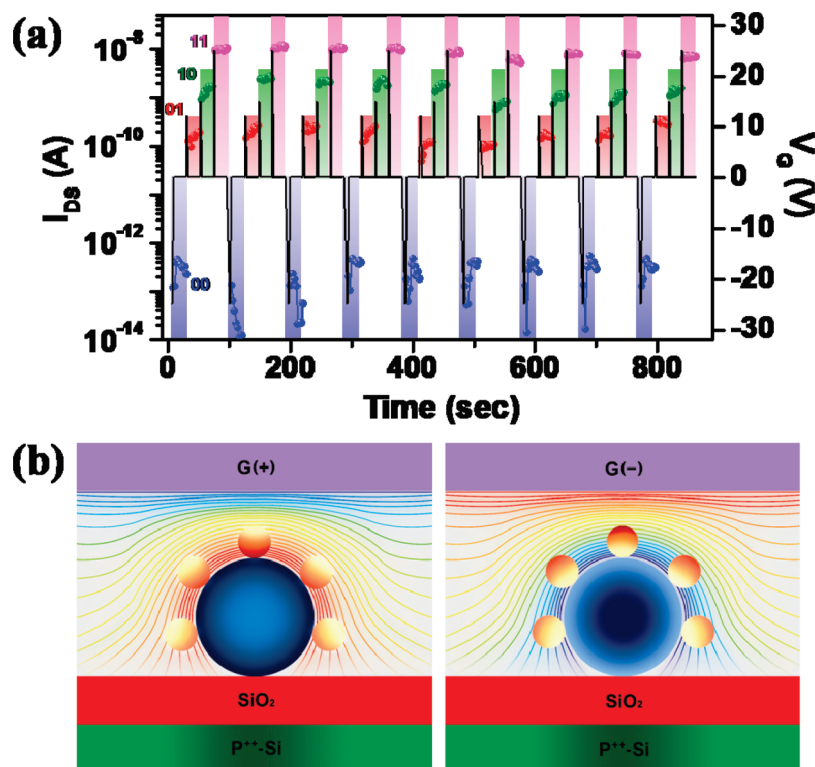
FIGURE 4. Multibit memory operation of a FE NP-coated NW FET. (a) Switching characteristics of a device with a top gate structure measured with $V_{DS} = 0.1$ V and $V_G = 0$ V, clearly showing that a FE FET functions as a two-bit memory with four different conductance states defined as "00", "01", "10", and "11" after the application of gate voltage pulses of -25, $+12$, $+15$, and $+25$ V, respectively. (b) A schematic view of a simplified polarization model for FE NPs surrounding a NW. The lines show the electric field distribution between a ZnO NW and a gate electrode. Electric dipole moments are reoriented along electric field lines, resulting in different polarization states according to the gate electric field strength. Furthermore, more dense equipotential lines around the upper part of a NW easily induce more polarized charges at the FE–NW interface, resulting from more amounts of reoriented electric dipole moments. Thus, different conductance states result from different net amounts of reoriented electric dipole moments dependent on the applied gate electric field strength.

on nanoscale building blocks such as molecules, carbon nanotubes, and semiconducting NWs.[10,28–30]

Here, we propose the following model to elucidate that the memory effects we observed are explained by the reversible switching between two stable polarization states. When a positive gate pulse is applied, the polarization of FEs is effectively rearranged in the direction of the FE–semiconducting NW interface, causing the buildup of positive charges on the NW surface as shown in Figure 3c. Subsequently, this leads to accumulation of electrons and thus a high conductance state, that is, the ON state in an n-channel FE FET. Conversely, when a negative gate pulse is applied, the negative remnant polarization causes the depletion of electrons and leads to a low conductance state, corresponding to the OFF memory state. Thus, a FE NP-coated NW FET clearly functions as a nonvolatile memory device because of two stable remnant polarization states, which persist after the removal of gate voltage pulses.

The ability to store multibit information in a single memory enables us to achieve a nonvolatile memory device with ultrahigh integration density, which is important to overcome the scaling method limitations of the current semiconducting technology. To this end, we investigated the multilevel switchability of a FE NP-coated

NW FET for a multibit nonvolatile memory. Figure 4a shows switching characteristics of a two-bit memory with four different conductance states defined as "00", "01", "10", and "11" by the application of gate voltage pulses of -25, $+12$, $+15$, and $+25$ V, respectively. Similar to our one-bit memory, we find that the erase state of a memory can be easily recovered by applying a -25 V gate pulse. Although the exact mechanism for multibit memory operations is still unclear, we suggest that different states of the memory are attributed to differing degrees of reoriented electric dipole moments in the direction of gate electric field as shown in Figure 4b. Higher gate bias is expected to polarize more FE NPs and thus bring correspondingly more net polarized charges at the FE–NW interface, modulating the channel conductance. This model is supported by results of transfer characteristics showing that channel conductance and threshold voltages are strongly related to the starting value of sweeping gate voltages as well as sweep ranges in Figure 2 (also see Figures S2 and S3 in the Supporting Information).

Unlike a conventional FE film based memory device, the electrically variable behavior of a FE NP-coated ZnO NW FET reported herein will be of great importance in realizing a flexible, functional nonvolatile memory with multibit memory

storage ability and excellent memory performance as well as with the advantage of simplicity where only a few device fabrication steps and low-temperature fabrication processing are required. This approach is expected to be an attractive potential strategy, providing the high possibility of implementing synapse-like devices, requiring electrically variable properties.

Supporting Information Available. A description of experimental methods and figures showing electrical characteristics of back-gate field effect devices and transfer characteristics for FE NP-coated NW FETs. This material is available free of charge via the Internet at http://pubs.acs.org.

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