CMOS Compatible Nanoscale Nonvolatile Resistance Switching Memory

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ABSTRACT

We report studies on a nanoscale resistance switching memory structure based on planar silicon that is fully compatible with CMOS technology in terms of both materials and processing techniques employed. These two-terminal resistance switching devices show excellent scaling potential well beyond 10 Gb/cm^2 and exhibit high yield (99%), fast programming speed (5 ns), high on/off ratio (10^3), long endurance (10^6), retention time (5 months), and multibit capability. These key performance metrics compare favorably with other emerging nonvolatile memory techniques. Furthermore, both diode-like (rectifying) and resistor-like (nonrectifying) behaviors can be obtained in the device switching characteristics in a controlled fashion. These results suggest that the CMOS compatible, nanoscale Si-based resistance switching devices may be well suited for ultrahigh-density memory applications.

Resistance switching behavior has been observed and studied in amorphous silicon (a-Si) devices since the 1980s.[1−6] A typical device consists of two metal layers sandwiching an a-Si layer serving as the storage medium and result in a metal/a-Si/metal (M/a-Si/M) layered structure. The resistance switching behavior was explained in terms of metal filament formation (elimination) inside the a-Si matrix at positive (negative) applied voltages.[3−5] Such M/a-Si/M devices, however, need to go through a high-voltage forming process in which a long voltage pulse is applied at a value over 10 V.[3−5] The forming process is generally not well-controlled, and permanent damage to the device may occur after initial filament formation, which severely limits the device yield and application potential. It is also not clear whether such devices can be scaled down to the sub-100 nm range, as micrometer-sized filaments were typically observed after forming.[2,5,6] As a result, few studies have been attempted on a-Si resistance switching devices as ultrahigh-density memories. Inspired by recent work on nanowire-based memory devices,[7] we studied a nanoscale a-Si resistance switching structure in a planar silicon platform and show here that high-performance, nonvolatile resistance switching memories using solid-state silicon as the storage medium may be readily implemented through CMOS compatible, conventional processing processes.

Our device structure consists of a top metal electrode, the active a-Si layer, and a heavily doped p-type crystalline-silicon (p-Si) layer as the bottom electrode (Supporting Information). The device fabrication involves standard CMOS processes only, with the exception that the active device area is defined with electron-beam lithography to test the smallest devices. The cross-sectional image of a fabricated device is shown in Figure 1a, illustrating the M/a-Si/p-Si layered structure at the active device region. Because of the highly resistive a-Si layer, the as-fabricated devices show high resistance and negligible current between the top and bottom electrodes. When a voltage V is applied on the top metal electrode, repeatable resistance switching is observed as V is varied, as shown in Figure 1c: the resistance of the device is suddenly reduced, and the device is turned on when V is increased beyond a certain positive threshold voltage V_{th1}; the device can be switched back into the high-resistance state, i.e., turned off when a negative voltage is applied beyond a threshold V_{th2}. We note that qualitatively similar switching behaviors were observed on all devices, insensitive to the fabrication method of the a-Si layer (e.g., Figure 1c and Figure 4 for devices fabricated by the plasma-enhanced chemical vapor deposition (PECVD) and low-pressure chemical vapor deposition (LPCVD) processes, respectively) or the metal used as the top electrode (Supporting Information). The threshold voltages V_{th1} and V_{th2} depend on the deposition method of the a-Si layer and the choice of metal used as the top electrode but show narrow distributions for a specific set of device parameters. For example, V_{th1} is tightly centered at 3.5 V with a standard deviation of 0.3 V for devices fabricated with the PECVD method with Ag top electrodes (Figure 1d). The off-state

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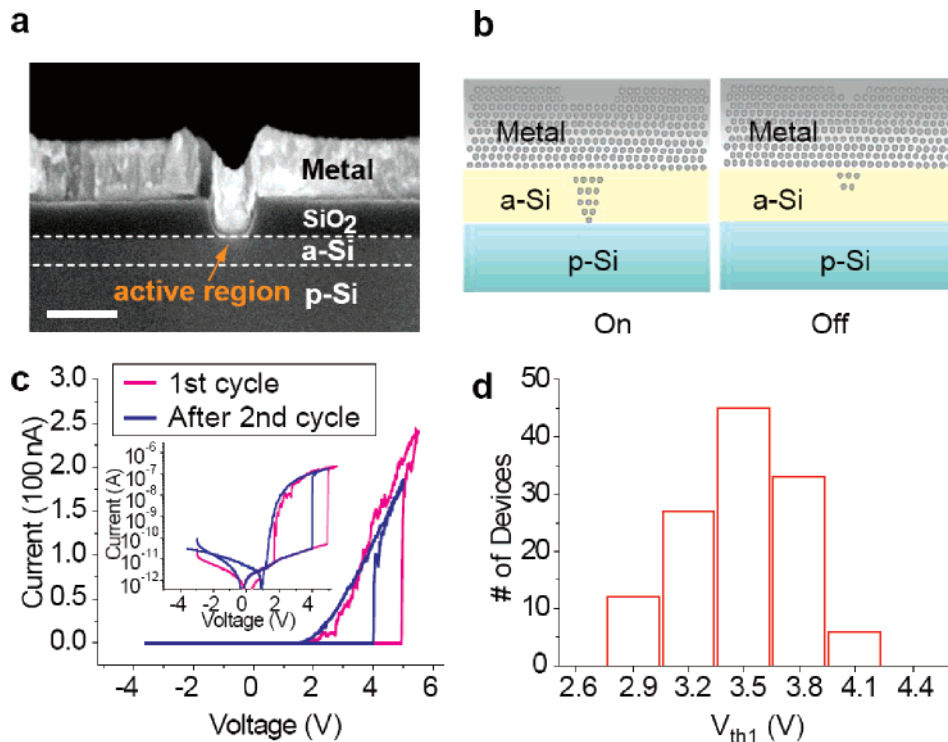† Department of Electrical Engineering and Computer Science, the University of Michigan.

Figure 1. Device structure and DC characterization. (a) Cross-sectional SEM image of a device showing the M/a-Si/p-Si structure. The regions outside the active area are protected by a SiO_2 layer. Scale bar: 100 nm. (b) Schematics of the formation and retraction of filaments in the on and off states. (c) Resistance switching characteristics of a device fabricated by the PECVD method. The device has a Ag top electrode, a 80 nm a-Si layer, and a 50 nm × 50 nm active area. Inset: switching characteristics of the same device in log scale. (d) Histogram of the Off/On threshold (V_{th1}) for over 120 devices fabricated using the PECVD method. V_{th1} was measured after the initial forming cycle and shows a tight distribution with mean ± 1 standard deviation of 3.5 ± 0.3 V.

resistance is comparable to the resistance of as-fabricated devices, while the on-state resistance is several orders of magnitude lower. The resistance ratio, R_{off}/R_{on}, ranges from 10^3 to 10^7 depending on the device type (e.g., PECVD vs LPCVD devices) and growth conditions. If V is between V_{th1} and V_{th2}, the state of the device is not affected and such intermediate voltage levels are used to read out the on or off device state.

Compared with phase-change memory devices, which show no polarity dependence,[8] and conductive-bridge devices based on electrochemical reactions that depend crucially on the electrode material,[9,10] the polarity dependence (i.e., devices can only be written with a positive voltage and erased with a negative voltage) and insensitivity to the choice of electrode material of the M/a-Si/p-Si devices suggest that the observed resistance switching behavior is caused by a filament formation process, as was studied previously in conventional microscale metal/a-Si/metal (M/a-Si/M) devices[1−6] and consistent with recent observations on nanowire-based devices.[7] Briefly, a positive voltage ($> V_{th1}$) on the top metal electrode generates a high electric field that drives metal (e.g., Ag) ions into the a-Si matrix and form a conducting filament inside the a-Si layer.[1−7] The metal filament creates a conductance pathway for electrons and results in a much lower on-state resistance compared to the off-state in which the filament is not formed. When a negative voltage $< V_{th2}$ is applied, the Ag ions are retracted from the a-Si layer and the high resistance off-state is recovered (Figure 1b). The status of the filament is not

affected at intermediate voltages or when the voltage source is removed, thus ensuring nonvolatile operation. As in the nanowire-based devices,[7] high-voltage forming treatment is not required in the planar M/a-Si/p-Si devices and forming, if needed at all, is much more controllable. As shown in Figure 1c, even for the smallest devices tested (active area of 50 nm × 50 nm), only a slightly higher write voltage was needed for the as-fabricated device compared to that for subsequent cycles. Once formed, V_{th1} and V_{th2} show little dependence on the number of write/erase cycles. The reduced forming voltage compared with M/a-Si/M devices may be partly explained by the fact that high electrical fields can be readily generated inside the a-Si region because the metal/a-Si/p-Si device effectively forms a reverse-biased Schottky junction at positive bias. The reverse-biased Schottky junction may also help limit damage to the device after filament formation in terms of heating or electromigration, hence improving the device yield. Our control experiments further show that devices fabricated on n-type substrates do not exhibit resistance switching behavior. By eliminating the high voltage forming process, we were able to obtain a much higher device yield compared to conventional M/a-Si/M structures (of the more than 300 devices examined, only two devices were found not to exhibit resistance switching.) As a comparison, our control experiments showed that M/a-Si/M devices with otherwise identical structures still require forming voltages >10 V, with a device yield <40%.

The M/a-Si/p-Si device structure shows excellent scalability that makes it suitable for ultrahigh-density memory
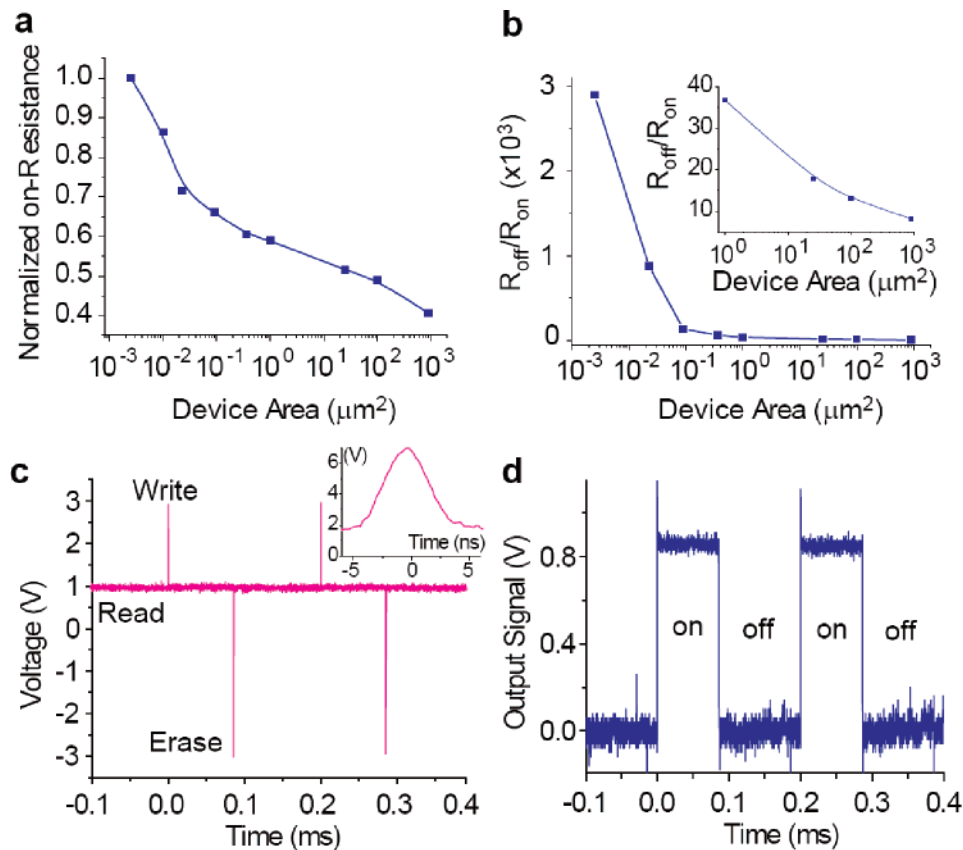
Figure 2. Scaling and switching speed tests of the M/a-Si/p-Si devices. (a) Dependence of the on resistance on the active device area. The on resistance was normalized to that of the device with the smallest active area. The a-Si layer (120 nm thick) in these devices was deposited by PECVD at 260 °C. (b) Dependence of off/on resistance ratio on the active area for the same devices shown in (a). Inset: blowup for devices with active area $>1 \mu m^2$. (c) Representative programming signal used for the switching speed test. Inset: blow-up of the write pulse. (d) The corresponding output signal measured on the sensing resistor R_s. The device in (c) and (d) has a 40 nm thick a-Si layer deposited by LPCVD.

applications. We have tested devices with active areas ranging from 1×10^3 to $2.5 \times 10^{-3} \mu m^2$ (50 nm × 50 nm), and no sign of device degradation was observed down to 50 nm × 50 nm. The dependence of the on-state resistance on the active device area was plotted in Figure 2a. The on-resistance increases only 2.5 times when the active device area is reduced by 6 orders of magnitude. This observation indicates that the conducting filament is formed locally and the formation of the first conducting filament (combined with series resistances at the contacts or in the p-Si layer) reduces the electric field across the a-Si layer and prevents other filaments from being completed. This observation is consistent with earlier studies on voltage-programmed resistance switches, which show area-independent off-current,[2] and in contrast to slow current programmed switches in which multiple filaments may be formed, resulting in a linear dependence of the on-current on device area.[11] Furthermore, because the off-state resistance is limited by leakage and is inversely proportional to the device area, the R_{off}/R_{on} ratio is in fact improved in smaller devices (Figure 2b). Unlike previous studies on M/a-Si/M devices in which micrometer-scale filaments were observed and the devices were limited to $>10 \mu m$,[2,5,6] the high device yield and continued improvement of R_{off}/R_{on} at the smallest device scales indicate the filament size in the M/a-Si/p-Si devices is in fact much

smaller than the 50 nm × 50 nm metal electrode size (limited by the lithography process). This observation is consistent with that observed on nanowire-based devices[7] and arguably put the a-Si system in the same class of molecular memory devices in terms of practical scaling as the cell size in both cases is limited by the smallest electrodes that can be practically fabricated rather than the active medium. We note the existing 50 nm × 50 nm structure already corresponds to a density of 10 Gbit/cm² using a cell size of $4F^2$, where F is the electrode width in this case.[12] The reduction of the conducting filament size in the M/a-Si/p-Si system compared to M/a-Si/M systems[2,5,6] studied earlier is likely related to the reduced programming voltages. However, more detailed experimental and theoretical studies will be needed to quantitatively explain this dramatically improved device behavior.

We have carried out a series of measurements to test the potential of the planar silicon-based nanoscale M/a-Si/p-Si structures as nonvolatile devices, namely the speed, endurance, and retention of the memory devices. Unless specified otherwise, devices of 50 nm × 50 nm in size with Ag electrodes were used. In a typical setup, the device state was read out at a low voltage by measuring the voltage across a sensing resistor in series and short voltage pulses were used to write and erase the device. In general, the switching speed
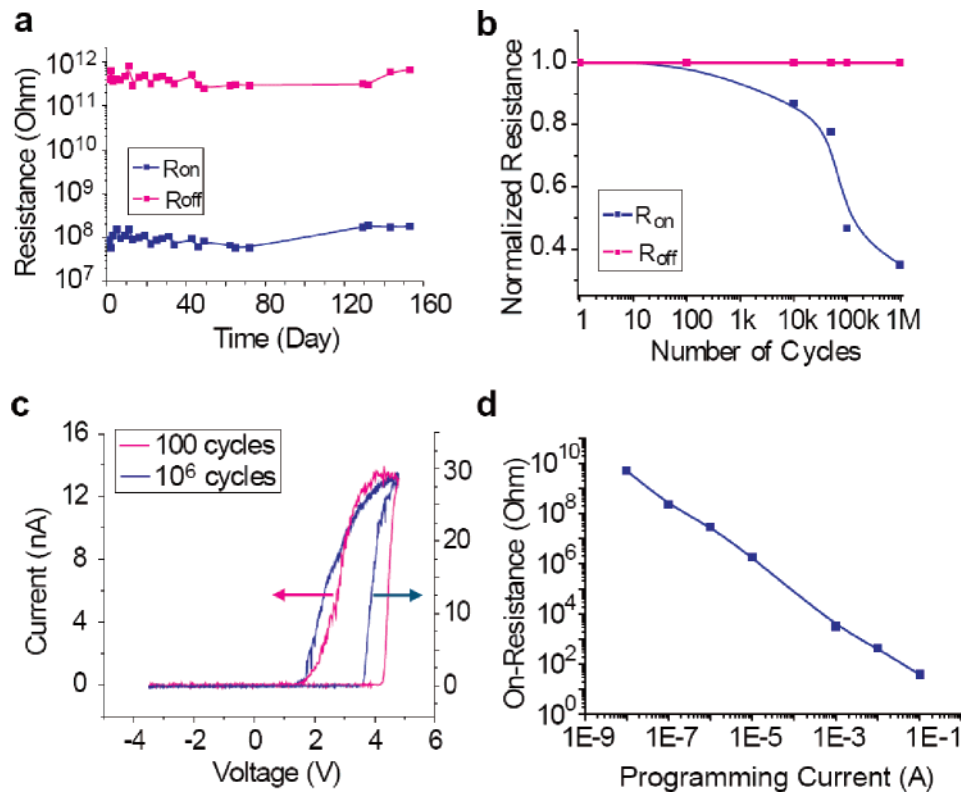
Figure 3. Retention, endurance, and multi-bit capabilities. (a) Retention test of a device prepared by PECVD with an active area of 150 nm × 150 nm. (b) Dependence of the on and off resistances on the number of programming cycles for a similar device as in (a). The on and off resistances were normalized to those obtained before the cycling test for clarity. (c) Switching characteristics of the device in (b) after 10^2 and 10^6 cycles of write/erase operations, showing excellent switching characteristics and on/off ratio after 10^6 cycles. (d) Dependence of the on resistance on the programming current, demonstrating the multilevel bit capability. The device was fabricated with LPCVD with 40 nm thick a-Si.

also depends on the amplitude of the write/erase signal. A write/read/erase/read sequence consisting of a 5 ns write pulse at 6.5 V, 10 ns erase pulse at −6.5 V, and a 1 V read voltage is shown in Figure 2c, along with the corresponding output signal shown in Figure 2d. The device was off at the beginning of the cycle, and the voltage measured across the sensing resistor (corresponding to the current through the device) was low. When the write pulse was supplied, the device was turned on and a higher sensing voltage was recorded in the following read period. Finally, the erase pulse turned the device off and the cycle was repeated. Switching speed faster than 5 ns (e.g., Figures 2c,d) was routinely obtained for LPCVD devices for devices with on-resistance below 200 Ω. We note the programming speed is several orders of magnitude faster than those reported on molecular devices and is comparable to the best values reported in other emerging memory devices.[13−16] The switching speed for PECVD prepared devices was limited to ~150 ns due to the higher intrinsic resistance R_{in} (typically >1 MΩ) and may be improved by reducing R_{in} through adjustment of the growth conditions (e.g., Figures 4a,b) or by reducing the parasitic capacitance using on-chip sensing amplifiers to reduce the RC delay in the circuit.

After the device was written on or off, little degradation of the stored information was observed for more than 5 months at room temperature in air ambient, as shown in Figure 3a. It is likely that data can be stored even longer in

such devices, as retention times of more than a year have been observed in conventional M/a-Si/M structures.[17] Endurance of the memory devices was tested by repeatedly running the programming cycles. For devices with a low programming current (~10 nA during the write process), we observed a slow increase of the on-state conductance (equivalently, on-current) as the number of write/erase cycles was increased, while the off-current remained below the equipment limit (Figure 3b). As illustrated in Figure 3c, reliable switching persisted in the device even after 10^6 programming cycles, which is already comparable to flash memory devices.[14] The endurance is generally less robust when the programming current is high. For example, the R_{off}/R_{on} ratio starts to decrease after 10^4 cycles and decrease to <10^4 after 10^5 cycles for a device with a write programming current of 10 mA (Supporting Information). The decrease in R_{off}/R_{on} was mainly caused by the increase in off-current and may be explained by semipermanent formation of metal islands inside the a-Si matrix after repeated application of large drive currents.

The capability of storing multiple levels in one storage element is another important criterion in accessing emerging memory technologies. We have tested multilevel bit capability of the M/a-Si/p-Si devices by controlling the maximum write programming current using a series resistor setup. The dependence of the on-state resistance on programming
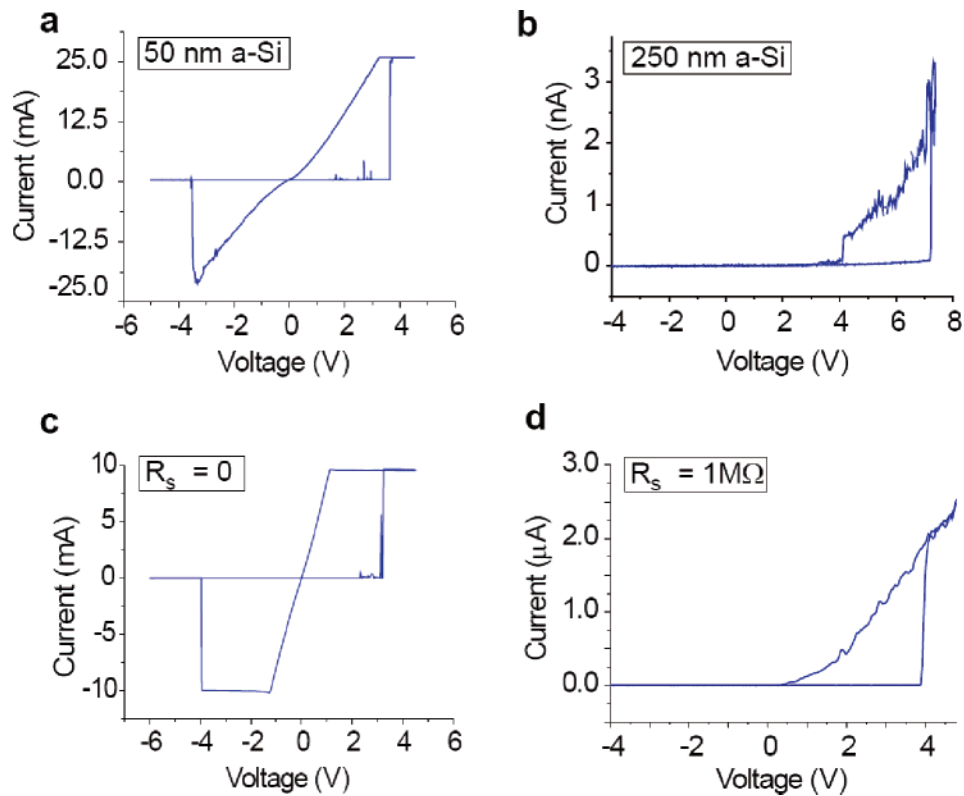
Figure 4. Control of the rectifying and nonrectifying behaviors. (a,b) Switching characteristics of devices with 50 nm thick a-Si (a) and 250 nm thick a-Si (b) deposited by LPCVD. (c) Switching characteristics of another device with 40 nm thick a-Si deposited by LPCVD without series resistors. (d) Switching characteristics of the same device with a 1 MΩ series resistor.

current is shown in Figure 3d and clearly demonstrates the multibit potential of the M/a-Si/p-Si devices.

Finally, we note that two different types of switching behavior, rectifying (diode-like) and nonrectifying (resistor-like), can be obtained in the M/a-Si/p-Si devices at the on-state (e.g., Figure 1c and Figure 4). In the rectifying case, the device at on-state exhibits a much higher current level at a positive bias compared to that at a negative bias (when the bias is still below V_{th2}) (Figure 1c), i.e., the device at on-state behaves like a diode. In the nonrectifying case, the device shows a symmetric $I-V$ curve at on-state and behaves as a resistor (Figure 4a,c). The rectifying behavior is beneficial to the elimination of crosstalk in crossbar devices[18] and was observed only recently on the nanowire-based devices.[7] In general, we observed that devices with a-Si grown by the PECVD method showed rectifying switching behavior, and devices with a-Si grown by the LPCVD method showed nonrectifying behavior. The different behaviors correlate well with the different on-state resistances R_{in} in the two types of devices: R_{in} is much higher in the PECVD prepared devices (Figure 1c, the rectifying case) compared to that of the LPCVD prepared devices (Figure 4a,c, the non-rectifying case). Further studies confirmed the role of R_{in} in the switching behavior. By adjusting the thickness of the a-Si layer during LPCVD growth, we were able to adjust R_{in} systematically and observed the transition from nonrectifying (Figure 4a) to rectifying behavior (Figure 4b) as the thickness of a-Si, hence R_{in} was increased. Furthermore, rectifying behavior can be obtained on existing low-R_{in} LPCVD devices by adding a series resistor R_s, as

demonstrated in Figure 4c,d. In general, we observed that if the on-current is smaller (greater) than ~10 μA (measured at V_{th1} for devices with active area of 50 nm × 50 nm), the switching characteristics is likely rectifying (nonrectifying). The nonrectifying behavior, like the retention dependence, may be related to the more permanent changes in the a-Si matrix[7] at large write currents. In the meantime, the large range of R_{in} that can be systematically obtained in the a-Si memory devices offers the potential to tune the device parameters to suit specific requirements. For example, high-resistance PECVD devices offer rectifying on-state and ultralow write current (the 10 nA write current in Figure 3c is 5 orders of magnitude lower than that required in state-of-the-art phase-change devices[19]) with excellent retention and endurance, while low resistance LPCVD devices offer even faster speed with compromise in write current and endurance. We expect these key performance factors will be further improved with continued studies in the device structure.

In summary, we have developed a nanoscale M/a-Si/p-Si resistance switching memory structure in a planar silicon platform that show excellent scalability and close to 100% device yield. The device is fully compatible with CMOS processing techniques and exhibits key performance metrics comparable to the best results from other emerging technologies,[13−16] suggesting it may be a strong candidate for future nonvolatile memory applications. Looking into the future, the two-terminal M/a-Si/p-Si devices may be ideally suited for ultrahigh-density memory and logic applications using the crossbar and hybrid Nano/CMOS architectures.[20−25]

Further improvement of the device structure will include the addition of a bottom metal layer to reduce potential series-resistance problem in large scale arrays and replacing e-beam lithography with nanoimprint lithography[26−28] or interference lithography[29] to improve the throughput.

Supporting Information Available: Device fabrication and characterization, metal dependence on the switching behavior, and retention and endurance test results on the low resistance (high I_{on}) LPCVD devices. This material is available free of charge via the Internet at http://pubs.acs.org.

References

(1) den Boer, W. *Appl. Phys. Lett*. **1982**, *40*, 812.
(2) Lecomber, P. G.; Owen, A. E.; Spear, W. E.; Hajto, J.; Snell, A. J.; Choi, W. K.; Rose, M. J.; Reynolds, S. *J. Non-Cryst. Solids* **1985**, *77−78*, 1373.
(3) Owen, A. E.; Lecomber, P. G.; Hajto, J.; Rose, M. J.; Snell, A. *Int. J. Electron*. **1992**, *73*, 897.
(4) Jafar, M.; Haneman, D. *Phys. Rev. B* **1994**, *49*, 13611.
(5) Avila, A.; Asomoza, R. *Solid-State Electron.* **2000**, *44*, 17.
(6) Hu, J.; Branz, H. M.; Crandall, R. S.; Ward, S.; Wang, Q. *Thin Solid Films* **2003**, *430*, 249.
(7) Dong, Y.; Yu, G.; McAlpine, M. C.; Lu, W.; Lieber, C. M. *Nanoletters* **2008**, *8*, 386.
(8) Hudgens, S.; Johnson, B. *MRS Bull*. **2004**, *29*, 829.
(9) Terabe, K.; Hasegawa, T.; Nakayama, T.; Aono, M. *Nature* **2005**, *433*, 47.
(10) Kund, M.; Beitel, G.; Pinnow, C.-U.; Rohr, T.; Schumann, J.; Symanczyk, R.; Ufert, K.; Muller, G. *IEDM Tech. Dig*. **2005**, 754.
(11) Hu, J.; Jackson, W.; Ward, S.; Stradins, P.; Branz, H. M.; Wang, Q. *Mater. Res. Soc. Proc*. **2003**, *762*, A18.3.1−6.
(12) DeHon, A. *IEEE Trans. Nanotechnol*. **2003**, *2*, 23.
(13) Goronkin, H.; Yang, Y. *MRS Bull.* **2004**, *29*, 805.
(14) Muller, G.; Happ, T.; Kund, M.; Gill, Y. L.; Nagel, N.; Sezi, R. *IEDM Tech. Dig*. **2004**, 567.
(15) Chen, A.; Haddad, S.; Wu, Y-C.; Fang, T-N.; Lan, Z.; Avanzino, S.; Pangrle, S.; Buynoski, M. R.; Cai, W.; Tripsas, N.; Bill, C.; VanBuskirk, M.; Taguchi, M. *IEDM Tech. Dig*. **2005**, 746.
(16) Waser, R.; Aono, M. *Nat. Mater*. **2007**, *6*, 833.
(17) Owen A. E.; Le Comber, P. G.; Spear, W. E.; Hajto, J. *J. Non-Cryst. Solids* **1983**, *59−60*, 1273.
(18) Scott, J. C. *Science* **2004**, *304*, 62.
(19) Lee, S. H.; Hwang, Y. N.; Lee, S. Y.; Ryoo, K. C.; Ahn, S. J.; Koo, H. C.; Jeong, C. W.; Kim, Y.-T.; Koh, G. H.; Jeong, G. T.; Jeong, H. S.; Kinam, K. *Tech. Dig. VLSI Symp.* **2004**, 20.
(20) Heath, J. R.; Kuekes, P. J.; Snider, G. S.; Williams, R. S. *Science* **1998**, *280*, 1716.
(21) Chen, Y.; Jung, G. Y.; Ohlberg, D. D. A.; Li, X.; Stewart, D. R.; Jeppesen, J. O.; Nielsen, K. A.; Stoddart, J. F.; Williams, R. S. *Nanotechnology* **2003**, *14*, 462.
(22) Lu, W.; Lieber, C. M. *Nat. Mater*. **2007**, *6*, 841.
(23) Strukov, D. B.; Likharev, K. K. *Nanotechnology* **2005**, *16*, 888.
(24) Snider, G. S.; Williams, R. S. *Nanotechnology* **2007**, *18*, 035204.
(25) Wang, W.; Liu, M.; Hsu, A. *J. Comput. Sci. Technol*. **2006**, *21*, 871.
(26) Green, J. E.; Choi, J. W.; Boukai, A.; Bunimovich, Y.; Johnston-Halperin, E.; DeIonno, E.; Luo, Y.; Sheriff, B. A.; Xu, K.; Shin, Y. S.; Tseng, H-R.; Stoddart, J. F.; Heath, J. R. *Nature* **2007**, *445*, 414.
(27) Chou, S. Y.; Krauss, P. R.; Renstrom, P. J. *Science* **1996**, *272*, 85.
(28) Guo, L. J. *Adv. Mater.* **2007**, *19*, 495.
(29) Brueck, S. R. J. *International Trends in Applied Optics*; SPIE Press: Bellingham, WA, 2002.

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