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Solution-Based Stoichiometric Control over Charge Transport in Nanocrystalline CdSe Devices

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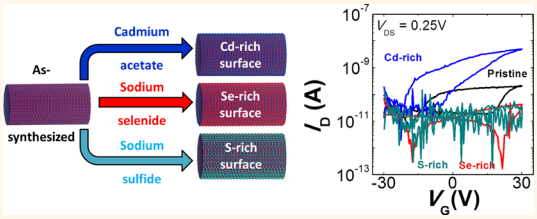
ABSTRACT Using colloidal CdSe nanowire (NW) field-effect transistors (FETs), we demonstrated the dependence of carrier transport on surface stoichiometry by chemically manipulating the atomic composition of the NW surface. A mild, room-temperature, wet-chemical process was devised to introduce cadmium, selenium, or sulfur adatoms at the surface of the NWs in completed devices. Changes in surface composition were tested for by energy dispersive spectroscopy and inductively coupled plasma-atomic emission spectroscopy and through the use of the vibrational reporter thiocyanate. We found that treatment with cadmium acetate enhances electron currents, while treatment with sodium selenide or sodium sulfide suppressed them. The efficacy of doping CdSe NWs through subsequent thermal diffusion of indium was highly dependent on the surface composition. While selenium-enriched CdSe NW FETs were characterized by little to no electron currents, when combined with indium, they yielded semimetallic devices. Sulfur-enriched, indium-doped devices also displayed dramatically enhanced electron currents, but to a lesser extent than selenium and formed FETs with desirable $I_{ON}/I_{OFF} > 10^6$. The atomic specificity of the electronic behavior with different surface chalcogens suggested indium was bound to chalcogens at the NW surface, indicating commonalities with and implications for indium-containing CdSe nanocrystal films. Low temperature measurements of indium-doped CdSe NW FETs showed no evidence of impurity scattering, further supporting the existence of an indium–chalcogen interaction at the surface rather than in the core of the NW.



KEYWORDS: cadmium selenide · remote dopant · colloidal nanowire · nanocrystals · inorganic salts

Colloidal semiconductor nanocrystals (NCs) are of fundamental scientific interest and present tremendous advantages for technological applications, as they exhibit profound differences from their bulk counterparts. Notably, quantum confinement restricts the available electronic states and provides the unique opportunity to tailor the optical and electronic properties of NC materials by changing their physical dimensions. Colloidal dispersibility makes them amenable to scalable, low-cost, solution-based fabrication. These properties have proven valuable in a variety of electronic and optoelectronic devices (*e.g.*, field-effect transistors,[1] integrated circuits,[2] solar cells,[3] and light-emitting diodes[4]). NC materials also possess an extraordinarily high surface-to-volume ratio, and consequently dangling bonds, surface adsorbates and stoichiometric imbalance strongly influence their electronic properties.[1,5−13] The complexity of the NC surface has typically been considered a drawback. However in this study we build on previous work[12−14] to demonstrate that, in particular, the NC surface composition can instead be exploited as a powerful tool to control trap density and charge-carrier doping. In this respect, intentional engineering of NC surface stoichiometry promises an alternative route to both traditional doping strategies, where impurity atoms are introduced into the core of nanostructured materials,[15−19] and to ligand manipulation[1,5,6,8,9] as means to engineer carrier statistics.

From foundational work on bulk and thin-film semiconductors, in particular on II–VI and IV–VI compounds, it is well-known that adsorbed atmospheric gases[20,21] and

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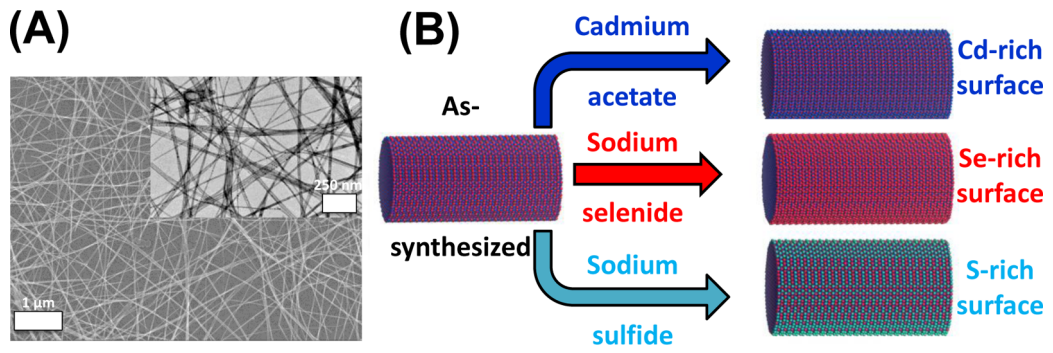

Figure 1. (A) SEM and TEM (inset) images of as-synthesized colloidal CdSe NWs. (B) Schematic of chemical modification introducing surface adatoms.

nonstoichiometry, at the surface, at grain boundaries and in the interior,[22−27] drastically change the carrier type and concentration. These perturbations introduce electronic states in the bandgap that when shallow, act as dopants, and when deep in the gap, act as traps. Early quantum chemical calculations on CdSe NCs suggested that surface selenium atoms contribute states deep in the bandgap, creating traps,[28] in agreement with early experiments on closely related CdS NCs.[29] These findings suggest that precise stoichiometric control of the surface in nanocrystalline materials offers a particularly promising route to control doping and traps. Recent synthetic advances[7,10−12,14,30,31] are providing new opportunities to test this hypothesis.

To directly probe charge-carrier transport engineered through intentional nonstoichiometry in nanocrystalline CdSe, here we utilized a simple platform consisting of arrays of single crystalline, colloidal CdSe nanowires (NWs) assembled to form the semiconductor channel of field-effect transistors (FETs). Wet-chemical methods akin to selective ion layer adsorption and reaction (SILAR)[32,33] or so-called "colloidal atomic layer deposition" (c-ALD)[34] were used to introduce surface adatoms. We show that we could modify the CdSe NW stoichiometry after device fabrication by exposing them to inorganic, cadmium- or selenium-containing salt solutions, to either enhance or suppress the electron current, respectively. In addition to manipulating the electron currents directly, changes in surface composition altered the efficiency of subsequent doping steps. In this work, we found that the doping efficiency of the well-studied CdSe dopant, indium,[35−38] depends on the NW surface composition with atomic specificity: untreated and cadmium acetate-treated NW FETs exhibited modest increases in current with indium doping compared with large increases in current in sodium selenide-treated and sodium sulfide-treated devices, doped with indium. In the case of the selenide with indium, the highest currents were observed, while a greatly enhanced ON/OFF ratio was seen in the case of the sulfide with indium. We show that surface modification using metal salt solutions in the solid state allowed the doping of nanocrystalline materials to be engineered in an integrated device, akin to ion implantation in bulk semiconductors and their devices.

Temperature-dependent charge transport measurements were utilized to probe the physics and mechanism of doping. NWs provide a particularly simple case, allowing for unambiguous interpretation. Unlike examples in many polycrystalline and NC thin films, in which scattering at grain boundaries,[39,40] trapping at defects, and hopping between particles[1,41,42] *may* give rise to thermally activated transport, single crystal NWs display band transport.[43] Temperature-dependent transport measurements of NWs allow one to separate perturbations in the core, which give rise to impurity scattering at low temperature, from those at the surface, which act remotely and do not introduce scattering that would otherwise degrade carrier mobility at low temperatures. Sulfur and selenium enriched and indium-doped CdSe NW FETs show a monotonic increase in mobility with decreasing temperature, similar to our previous studies on PbSe NW FETs,[43,44] suggesting that the thermally diffused indium dopants reside at the surface of the nanostructure, rather than in the core. We present a model of remote, surface doping of CdSe nanostructures, highlighting its promise as a route to engineer transport in nanostructures without introducing impurity scattering.

RESULTS AND DISCUSSION

Nanowire Synthesis and Surface Manipulation. Crystalline CdSe NWs 10 nm in diameter were synthesized *via* solution−liquid−solid synthesis [Figure 1(A)].[45] The NWs were deposited by drop-casting for structural and analytical characterization, and by electric-field alignment across prefabricated device electrodes for electrical characterization. To remove the organic surfactants present after synthesis and provide a bare surface for subsequent treatments, the NW samples were immersed in a 50 mM solution of ammonium chloride in anhydrous methanol for 10 min followed by pure methanol. In this step, 76 ± 6% of the organic ligands were removed, as measured by Fourier transform infrared spectroscopy (FTIR) [Supporting Information Figure S1]. We modified the surface stoichiometry

of the CdSe NWs in a simple, wet-chemical step after the NWs were deposited on solid surfaces and integrated in device structures as follows. NWs on a substrate were immersed in solutions of cadmium acetate (blue), sodium selenide (red), or sodium sulfide (cyan) in methanol to enrich the surface with cadmium, selenium or sulfur, respectively [Figure 1(B)]. We used energy dispersive X-ray spectroscopy (EDS), inductively coupled plasma-atomic emission spectroscopy (ICP-AES) and FTIR to quantify the surface enrichment. EDS data showed an excess of cadmium over selenium in the as-synthesized samples. The ratio was further increased by treatment with cadmium acetate and diminished by sodium selenide; however, the changes were small and comparable to the magnitude of the experimental uncertainty [Figure 2(A)]. Treatment with sodium sulfide preserved the cadmium to selenium ratio and showed a similar increase in overall chalcogen-to-cadmium ratio as that of sodium selenide treatment. ICP-AES, performed on treated NWs, exhibited the same trends but with an even higher ratio of cadmium to selenium throughout [Table 1]. In this case, the size of the measured changes upon sodium selenide treatment were significant relative to the experimental uncertainty, while the changes due to cadmium acetate treatment were again in the expected direction, but statistically uncertain. The observation that the cadmium to selenium ratio was never less than 1 may be the consequence of either or both of two possibilities: (1) unreacted cadmium oxide impurities that were never completely separated from the NWs, which were less prominent in the EDS experiments because large impurities were identified by their morphology and intentionally avoided; (2) selenium bound less strongly to the surface, resulting in incomplete reaction of all possible binding sites or subsequent partial erosion of excess selenium under later wash steps.

We also sought to test these more established methods of measuring atomic composition against a method we recently introduced that measures the relative excess of cations on NC surfaces. As-synthesized, cadmium-treated and selenium-treated NWs on a silicon substrate were immersed in a solution of ammonium thiocyanate and washed in pure acetone, leaving the anionic thiocyanate specifically bound to positively charged cadmium sites on the nanocrystalline surface.[46] We compared the integrated area of the CN-stretching region of the bound thiocyanate as a measure of the total surface-exposed cadmium content of the three samples. The broad, asymmetric peak characteristic of thiocyanate bound to surface cadmium was observed to increase in total integrated area after treatment with cadmium acetate [Figure 2(B) and Table 1]. This corroborated that the increases in cadmium content measured by EDS and ICP-AES were not due to contamination with molecular cadmium species, which exhibit a narrower CN stretching transition when combined with SCN to form a complex,[46] and were instead incorporated as adatoms on the NW surface.

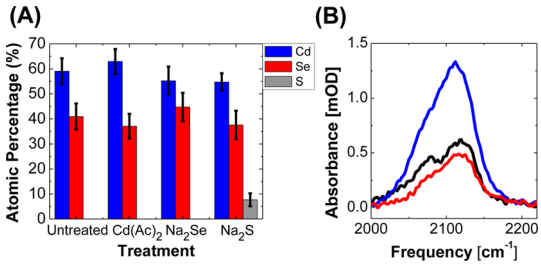

Figure 2. (A) Energy-dispersive X-ray spectroscopy of CdSe NWs treated with inorganic salts of cadmium acetate, sodium selenide, or sodium sulfide in methanol. (B) Surface enrichment using the vibrational reporter thiocyanate to quantify the increase in available surface sites of Cd for pristine NWs (black), treated with cadmium-acetate (blue) and sodium selenide (red).

TABLE 1. Excess Cadmium Measured by EDS, ICP-AES and FT-IR

	[Cd]/[Cd+Se]			
	model[a]	EDS	ICP-AES	FT-IR[b]
as synthesized	0.50	0.59 ± 0.05	0.69 ± 0.01	–
cadmium acetate	0.52	0.63 ± 0.05	0.71 ± 0.01	0.68 ± 0.13[b]
sodium selenide	0.48	0.55 ± 0.06	0.59 ± 0.01	0.56 ± 0.02[b]

[a] Model is based on a 10 nm diameter wurtzite NW. 8.1% of the atoms are surface atoms, consisting of equal parts Cd and Se. The number of adatoms was calculated by assuming each surface atom of one type can bind exactly one surface atom of the opposite type. [b] Relative changes in the cadmium excess were estimated from the integrated area of the CN stretch of adsorbed thiocyanate, as described in the text. This was converted to an absolute number by multiplying the relative change by the EDS-measured value for excess cadmium as synthesized.

While the error is significant when probing small compositional changes by any single measurement, the enrichment of the NWs toward either cadmium or selenium was observed universally by EDS, ICP-AES and FT-IR spectroscopy, providing strong evidence that the desired changes in surface stoichiometry were achieved with the metal salt treatments. It should be noted that the data above does not indicate how much residual sodium, acetate or chlorine is left bound to the surface after sodium chalcogenide, cadmium acetate or ammonium chloride treatments, respectively. XPS measurements on PbSe NCs treated after film deposition with sodium sulfide show sodium is effectively removed by washing in methanol,[47] whereas treatment of PbS NCs with bromide salts show evidence for bromide bound to the NC surface,[48] and similar processes may operate here. We return to the question of the role of the counterion in the context of the electronic measurements below, and find it to be negligible.

Effects of Surface Composition on Charge Transport. With a simple, low-temperature, solution-based process to manipulate the atomic composition of the NW surface in the solid-state, we investigated how the surface properties in turn control charge transport before and after surface modification in FET devices. In an inert glovebox, CdSe NWs were aligned with a DC

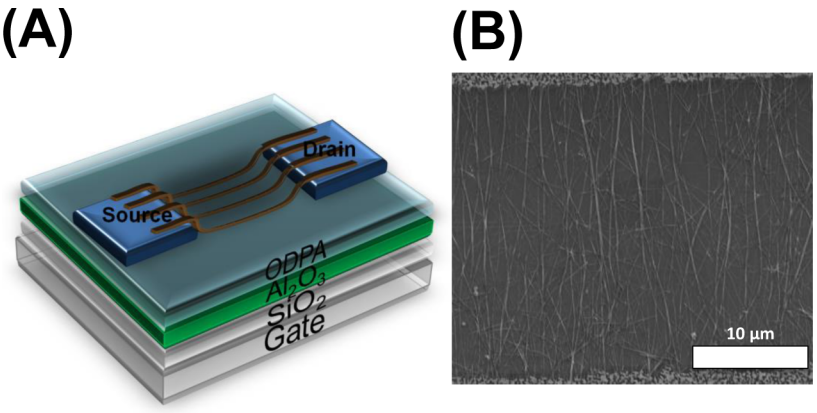

Figure 3. (A) Schematic of CdSe NW FETs atop an ODPA/Al_2O_3/SiO_2 dielectric stack. (B) SEM image of electric-field aligned CdSe NWs.

electric field[44,49] across gold electrodes deposited on top of an octadecylphosphonic acid (ODPA) self-assembled monolayer[12,49]/aluminum oxide (Al_2O_3)/silicon oxide (SiO_2) dielectric stack, with a degenerately doped silicon substrate acting as the back gate [shown schematically in Figure 3(A)]. A dense mat of NWs spanning approximately 5% of the channel width was controllably deposited [Figure 3(B)], presenting a high surface-to-volume ratio for subsequent surface modification. We exposed the NW FETs to solutions of inorganic salts, with or without subsequent thermal treatments. As a control, leakage currents, measured between the source and gate and drain and gate electrodes, were confirmed to be small and unchanged with the different NW surface and heat treatments (Supporting Information Figure S2), indicating that these processes introduced no significant effects on the integrity of the dielectric stack.

Representative I_D-V_{DS} [Supporting Information Figure S3(A), black] and I_D-V_G [Figure 4(A), black] characteristics for CdSe NW FETs, stripped of their long ligands used in synthesis, but otherwise untreated, exhibited n-type behavior typical of CdSe with low mobilities ($1.43 \pm 0.8 \times 10^{-5}$ cm^2 V^{-1} s^{-1}). The hysteresis made a true mobility extraction difficult, but to give an idea of trends, forward scans were used to extract values in the linear regime. The electron mobility was calculated based on the channel width defined by the electrode dimensions, so the mobility values quoted in the text should be considered a conservative estimate, since only 5% of the channel width is covered with NWs. Significant hysteresis ($\Delta V_T = 38.3 \pm 4.2$ V) was seen between forward and reverse sweeps in the I_D-V_G curves, attributed to traps states. Evidence of contact resistance was observed in the closely spaced I_D-V_{DS} curves at low voltages, which are consistent with significant barriers to electron injection due to the energy band misalignment between the Fermi level of the gold contacts and the lowest unoccupied molecular orbital (LUMO) level of CdSe. Using cadmium acetate [Figure 4(A), blue] to cadmium-enrich the NW surface led to enhanced electron currents, as cadmium is an effective n-type dopant in CdSe,[11,50] and to smaller hysteresis ($\Delta V_T = 27.2 \pm 1.9$ V), consistent with passivation of NW surface trap states, analogous to our report of Pb-enrichment of PbSe NCs.[12] Despite the enhanced currents and higher mobilities ($2.2 \pm 1.2 \times 10^{-4}$ cm^2 V^{-1} s^{-1}), the device still suffered from significant contact resistance, as seen in the device I_D-V_{DS} curves [Supporting Information Figure S3(B), blue]. If devices were instead treated with cadmium chloride, a qualitatively similar change was observed (Supporting Information Figure S4), suggesting that any effects of the anionic counterion are secondary to the principle effect of the cadmium cation. In contrast, treatment with sodium selenide [Figure 4(A), red] led to complete electron current suppression and no evidence of hole transport in both I_D-V_G and I_D-V_{DS} characteristics [Supporting Information Figure S3(C), red]. This is unlike lead chalcogenides, which have been reported to exhibit p-type transport with even small stoichiometric increases in surface selenium.[22−24] However, this is consistent with previous reports on crystalline CdSe, which have shown that while cadmium enrichment readily increases the free electron concentration, it is very difficult to increase the free hole concentration with selenium enrichment. The asymmetric band structure of CdSe gives rise to an ionization energy for selenium acceptors that is significantly higher (at least 200 times larger) than that for cadmium donors,[50] and holes have a lower mobility than electrons. p-type CdSe has been accomplished only rarely, by utilizing selenium vapors.[26,27] In addition to these properties of the semiconductor itself, it may be difficult to create a Cd:Se ratio less than 1 using our solution-based methods [Table 1].

We also fabricated CdSe NW FETs with indium-containing electrodes [titanium/gold/indium (2 nm/10 nm/10 nm)]. The FETs exhibited the same trends, with the modest electron currents of an untreated device [Figure 4(B), black], giving way to an increase in electron current after cadmium acetate treatment [Figure 4(B),

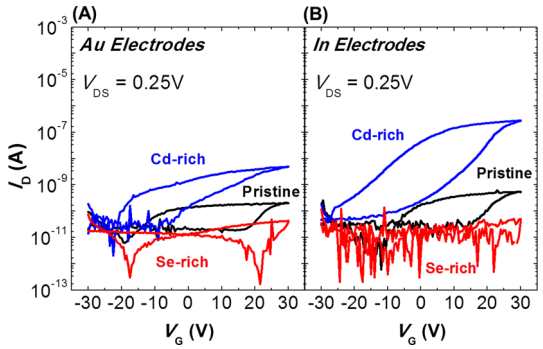

Figure 4. I_D-V_G characteristics of electric-field aligned colloidal CdSe NW field-effect transistors that were not heated, with bottom contact (A) gold electrodes and (B) indium electrodes atop an ODPA/Al_2O_3/SiO_2 gate dielectric stack. NWs were pristine (black), or treated with inorganic salts of cadmium acetate (blue) or sodium selenide (red).

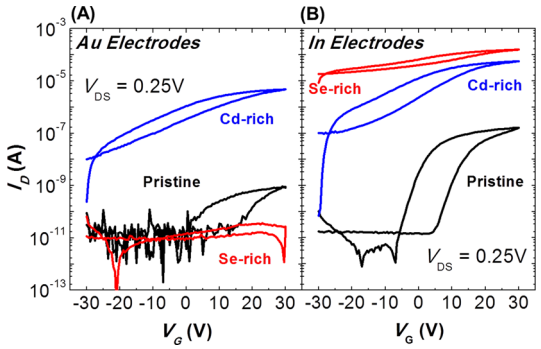

Figure 5. I_D-V_G characteristics of electric-field aligned colloidal CdSe NW field-effect transistors heated at 250 °C for 2 min with bottom contact (A) gold electrodes and (B) indium electrodes atop an ODPA/Al_2O_3/SiO_2 dielectric stack. NWs were pristine (black), or treated with inorganic salts of cadmium-acetate (blue) or sodium selenide (red).

blue] and complete suppression of electron current upon sodium selenide treatment [Figure 4(B), red]. We note that, compared to gold electrodes [Figure 4(A)], higher current levels were observed in both the pristine CdSe NW FETs and the cadmium acetate treated FETs, as transistors with indium electrodes displayed much reduced contact resistances [Supporting Information Figure S3(E, F), blue]. The energy band alignment of the LUMO of CdSe with indium (4.12 eV) is much more favorable than that of gold (5.1 eV), giving rise to a much smaller injection barrier for electrons.[51] It should be noted that the workfunction of indium is typically attributed to high purity, clean indium under an ultrahigh vacuum. Since bottom contacts were used, we should expect the indium electrodes to become contaminated and their workfunction to be altered, because the NWs were drop-cast from solvent in a glovebox. Again, sodium selenide treated devices displayed no current [Supporting Information Figure S3(G), red]. Treating the NWs with sodium sulfide depressed the FET electron currents for both gold and indium contact devices [Supporting Information Figure S3(D, H), cyan]. This is expected, since both selenium[25,26] and sulfur[52−54] act as acceptors in CdSe and CdS, respectively. The use of sodium sulfide will be explored in more detail in the following section.

Effect of Surface Composition on Thermal Diffusion of Indium. Indium serves as an n-type dopant in polycrystalline and nanocrystalline CdSe,[35−38] and annealing cadmium chalcogenides in the presence of metallic indium is thought to activate its diffusion into the film along grain boundaries.[35,38,55] It remains an interesting question whether, in colloidal NC and NW systems, the doping action occurs with the dopant situated at the nanocrystalline surface (remote doping) or if the dopant is incorporated into the nanocrystalline lattice. To address this question, we exploited the synergistic interactions between metal and chalcogen surface enrichment and thermally diffused indium metal.

As a control to measure the effect of heat alone in the absence of indium, samples with gold electrodes were heated at 250 °C for 10 min. I_D-V_{DS} curves [Supporting Information Figure S5(A), black] of untreated CdSe NW FETs exhibited a small improvement in the contact resistance, similar current levels and higher mobility values ($7.4 \pm 5.9 \times 10^{-3}$ cm^2 V^{-1} s^{-1}). The I_D-V_G curves [Figure 5(A), black] show reduced hysteresis (ΔV_T = 19.9 V ± 7.6 V), similar to prior observations in PbSe NW FETs[49] and CdSe NC FETs[56] where it was concluded that the reduction in hysteresis was due to residual solvents and water being driven out of the device with heat. Devices treated with cadmium acetate [Figure 5(A), blue] showed a drastic increase in electron current of about 2 orders of magnitude, increased mobility ($2.2 \pm 1.5 \times 10^{-2}$ cm^2 V^{-1} s^{-1}) and reduced hysteresis ($\Delta V_T = 16.8 \pm 5.5$ V). We speculate that this is due to a combination of water and residual solvents being driven out of the device, as well as the availability of the thermal energy required for surface reorganization and dopant activation.[28] However, the FETs still showed significant contact resistance [Supporting Information Figure S5(B), blue]. Even devices treated with sodium selenide began to show some marginal current and weak gate modulation after heat treatment [Figure 5(A) and Supporting Information Figure S5(C), red].

We applied the same annealing protocol to FETs with indium electrodes [Figure 5(B), black], allowing for thermal diffusion of indium into the NW channel (note that under these conditions there is no bulk flow of indium; the electrodes retain their shape and only atomic indium diffuses into the channel region).[35] All of the annealed indium electrode devices showed superior, low-contact resistances in comparison to analogous gold electrode devices, evident from the I_D-V_{DS} curves [Supporting Information Figure S5(E−H)]. Untreated devices [Figure 5(B), black] showed improved mobilities (2.0 ± 1.0 cm^2 V^{-1} s^{-1}) and 2 orders of magnitude higher currents due to indium doping than reference FETs with gold electrodes, and reduced hysteresis (ΔV_T = 15.4 ± 2.7 V). Cadmium acetate-treated devices [Figure 5(B), blue] also displayed an increase in

TABLE 2. Hysteresis and Mobility Values for Various Treatments of CdSe NW FETs

		gold		indium	
metal salt treatment		unheated	heated	unheated	heated
untreated	μ [cm^2 V^{-1} s^{-1}]	$1.4 \pm 0.8 \times 10^{-5}$	$7.4 \pm 5.9 \times 10^{-3}$	$3.1 \pm 1.4 \times 10^{-4}$	2.0 ± 1.0
	Hysteresis [V]	38.3 ± 4.2	19.9 ± 7.6	29.6 ± 2.3	15.4 ± 2.7
cadmium acetate	μ [cm^2 V^{-1} s^{-1}]	$2.2 \pm 1.2 \times 10^{-4}$	$2.2 \pm 1.5 \times 10^{-2}$	$2.5 \pm 1.2 \times 10^{-2}$	4.1 ± 2.3
	hysteresis [V]	27.2 ± 1.9	16.8 ± 5.5	24.0 ± 3.5	13.4 ± 2.4
sodium selenide	μ [cm^2 V^{-1} s^{-1}]	N/A	N/A	N/A	23.9 ± 5.8
	hysteresis [V]				12.4 ± 2.6
sodium sulfide	μ [cm^2 V^{-1} s^{-1}]	N/A	N/A	N/A	13.4 ± 4.0
	hysteresis [V]				10.8 ± 5.4

current levels and mobility (4.1 ± 2.3 cm^2 V^{-1} s^{-1}) when compared to gold electrode devices, and smaller hysteresis values ($\Delta V_T = 13.4 \pm 2.4$ V). Enriching the surface with cadmium serves to n-dope CdSe NWs similar to indium, as both cadmium[50] and indium[57] are low-lying donors in CdSe. However, CdSe NW FETs treated with sodium selenide show a dramatic difference in conductivity: from insulating, either unannealed with indium electrodes [Figure 4(B) and Supporting Information Figure S3(G), red] or annealed with gold electrodes [Figure 5(B) and Supporting Information Figure S5(C), red], to nearly semimetallic behavior upon annealing with indium-containing electrodes to allow its diffusion [Figure 5(B), red]. Sodium selenide-treated, indium-diffused devices yield current levels and mobilities (23.9 ± 5.8 cm^2 V^{-1} s^{-1}) that far exceed other inorganic salt treatments, with smaller hysteresis values ($\Delta V_T = 12.4 \pm 2.6$) [Figure 5(B) and Supporting Information Figure S5(G), red]. While selenium enrichment using sodium selenide strongly suppresses electron currents, indium and sodium selenide together act synergistically to yield the highest observed electron currents. The interaction between the selenium enriched *surface* and the indium dopant is one indicator that the doping mechanism involves adatoms at the surface, rather than indium incorporation into the lattice. Full device statistics for different metal salt treatments, electrodes and heat treatments are summarized (Table 2).

We further explored the diversity in metal-chalcogen interactions by introducing an alternate chalcogen, sulfur, at the surface with the inorganic salt sodium sulfide. Sodium sulfide treated FETs displayed drastically reduced electron current, [Figure 6(A), gray, and Supporting Information Figures S3(D, H) and S5(D), cyan], almost to the same extent as for selenium-enrichment [Figure 4 and 5(A), Supporting Information Figures S3(C, G) and S5(C), red]. Reduced electron currents are consistent with sulfur acting as an acceptor, as it does in CdS.[52,53] However, upon annealing sulfur-enriched CdSe NW FETs with indium-containing electrodes, again a dramatic change in electronic behavior was observed [Figure 6(A), cyan]: devices displayed high mobilities (13.4 ± 4.0 cm^2 V^{-1} s^{-1}), currents, and I_{ON}/I_{OFF} ratios (>10^6), and low hysteresis ($\Delta V_T = 10.8 \pm 5.4$ V). Like selenium-enriched and indium-doped NWs created upon annealing, sulfur-enriched, indium-doped NWs have higher currents compared to pristine and cadmium-enriched FETs upon indium-doping. The striking difference between sulfur *versus* selenium treatments, when coupled with indium diffusion, was the higher current and the interrelated lower current modulation of sodium selenide treated devices. It is worth highlighting again that the EDS measurements [Figure 2(A)] showed that the total percent change in chalcogen content, either with sodium selenide or sodium sulfide, is similar and that the number of chalcogen sites for indium to react with on the surface should be approximately the same. Given an equivalent number of sites, the observation of drastically different electrical behaviors strongly suggests a direct indium−chalcogen interaction on the NW surface. We hypothesize that due to the greater electronegativity of sulfur and the mismatched geometry of the Cd−S bond compared to a CdSe lattice, indium-bound sulfur would require greater activation energy to donate an electron to the NW than indium-bound selenium. The lower doping efficiency of indium−sulfur at the NW surface necessitates larger gate fields to raise the Fermi energy toward the NW LUMO and increase the free carrier density, in agreement with the electrical differences.

The behavior of the NW FETs parallels that of CdSe NC FETs, suggesting that the NW FETs provide an apt model system for interrogating surface modification in colloidal nanomaterials in general. We compared the values of the critical parameter, I_{ON}/I_{OFF}, observed in sulfide enriched, indium-doped (>10^6) and selenide-enriched, indium-doped (>10) CdSe NWs with three examples of annealed NC FETs: $In_2Se_4^{2-}$-capped (10^4),[58] sulfide-capped, indium-doped (>10^5)[11] and thiocyanate-capped, indium-doped (>10^6) CdSe NCs.[35,46] The combination of selenium and indium at the surface of NCs or NWs resulted in high currents both in the ON and OFF states in all cases. In contrast, examples where sulfur and indium are present at the surface yield higher I_{ON}/I_{OFF}, a necessary characteristic for many device applications. For this comparison we grouped

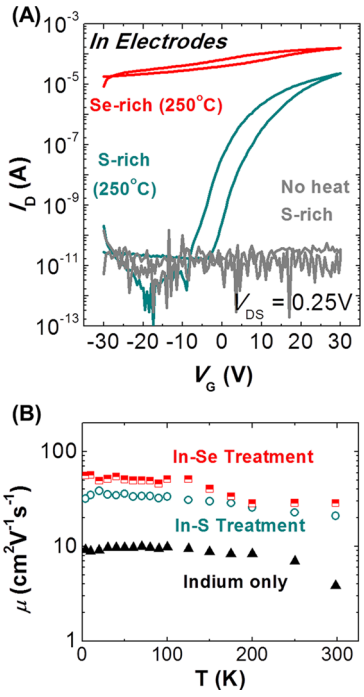

Figure 6. (A) I_D-V_G characteristics of electric-field aligned colloidal CdSe NW field-effect transistors heated at 250 °C for 10 min with bottom contact indium electrodes atop an ODPA/Al_2O_3/SiO_2 dielectric stack. NWs were treated with metal salts sodium selenide and annealed (red) and sodium sulfide before (gray) and after annealing (cyan). (B) Low-temperature mobility measurements of annealed CdSe NW FETs with indium electrodes that were pristine (black), treated sodium selenide (red) or with sodium sulfide (cyan).

the thiocyanate-capped NC-FETs with those that were sulfide enriched because thermal decomposition of the thiocyanate ligand is understood to result in sulfide formation.[59] In support of this grouping, we found that thiocyanate-treated NW devices yield similar electronic behaviors as that of sodium sulfide treated NW transistors [Supporting Information Figure S6].

While our observed synergy of indium doping and surface stoichiometry manipulations indicate that the indium should be interacting with the NW surface, we wanted to further test the model of indium doping. To date, scanning tunneling microscopy (STM),[16] magnetic circular dichroism (MCD) and electron paramagnetic resonance (EPR) of Mn atoms[18] with ZnSe NCs have been some of the techniques to distinguish if impurity atoms have been incorporated into the bulk or are on the surface. More recently, electron energy loss spectroscopy with annular dark-field scanning transmission electron microscopy (ADF-STEM)[60] was used to detect Mn inside ZnSe. However, many impurities are magnetically passive, limiting the use of MCD, and EPR depends on the hyperfine interaction with the ^{55}Mn nuclear spin (I = 5/2) and cannot be used to image other types of dopants. STM and ADF-STEM require specialized equipment and, as with any single-object measurement, are not guaranteed to accurately reflect an ensemble. We previously used low-temperature transport measurements to demonstrate that excess Pb and oxygen can "remote dope" the surface of nanostructures without introducing scattering in single-crystalline PbSe NWs.[43]

Here, we performed temperature-dependent transport measurements, between 4.5 K and room temperature, on CdSe NW FETs [Figure 6(B)]. We show the temperature-dependent mobility for CdSe NW FETs employing indium electrodes, untreated and surface-modified with sodium sulfide or sodium selenide, and annealed at 250 °C for 10 min. The electron mobility as a function of temperature was extracted in the saturation regime because contact resistance increased significantly at lower temperatures. As stated previously, the mobility values should be considered a conservative estimate (noting that it is the temperature dependence of the mobility and not the precise values that tells the key physics). Indium-doped CdSe NW FETs that were not treated with metal salts show a rise in mobility with decreasing temperature at high temperatures with a $\sim T^{-0.7\ \text{to}-0.9}$ power-law dependence on mobility (although transmission electron microscopy (TEM) images of colloidal CdSe NWs suggest the presence of stacking faults, the energy barriers presented by these imperfections are sufficiently small [Supporting Information Figure S7]), similar to the $T^{-0.5\ \text{to}-0.83}$ values[61−63] reported for various single crystals of CdSe and typically attributed to bulk acoustic phonons. The mobility plateaus at temperatures below 100 K. This is in contrast to measurements performed on many polycrystalline films, where scattering at grain boundaries and defects give rise to thermally activated transport over the whole temperature range. It is also in contrast to transport measurements of cobalt-doped CdSe single-crystals, where mobility similarly increases from room temperature down to 100 K, but impurity scattering gives rise to a decrease in mobility below 100 K.[63] These results are consistent with our previous report on single-crystalline PbSe NW FETs, where (1) at high temperatures the mobility increases with decreasing temperature with a power law akin to that in the bulk and (2) at low temperatures the mobility plateaus, showing no evidence of impurity scattering, even as excess Pb or oxygen were introduced on the surface, acting as remote dopants.[43]

Samples treated with sodium sulfide and sodium selenide, prior to then introducing indium through diffusion, exhibited the same rise and plateau in mobility with decreasing temperature as untreated CdSe NW FETs. At high temperatures >100 K, CdSe NW FETs treated with sodium sulfide and sodium selenide had power law dependencies of $\sim T^{-0.4\ \text{to}\ -0.6}$ and $\sim T^{-0.5\ \text{to}\ -0.7}$, respectively, again consistent with acoustic phonon scattering in single crystal CdSe. The difference observed in the low temperature mobility (<100 K) is akin to what is observed in modulation-doped semiconductors. In modulation-doped semiconductors, the mobility rises with a power law characteristic of the

crystal's acoustic phonons and plateaus with a maximum mobility typically limited by native, amphoteric defects.[64] In our NW devices, we hypothesize that the surface introduces similar defect states, setting an upper limit for the mobility at low temperature. Enriching the surface in chalcogen increases the number of indium binding sites at the NW surface, passivating NW surface states and increasing the low temperature mobilities for sulfide and selenide treated, indium-doped CdSe NW FETs. We hypothesize the small difference in mobility between the different chalcogens may again arise from their different electronegativities and atomic radii, and the greater effectiveness of selenium-bound sulfur in doping and removing trap states from the NW bandgap, than sulfur-bound indium. The surface-sensitive indium–chalcogen electrical behavior of the NWs is consistent with indium incorporation at the NW surface and surface indium acting as a "remote dopant", enhancing carrier transport and passivating surface trap states in CdSe NWs.

CONCLUSIONS

In summary, we have demonstrated the pronounced sensitivity of charge transport behavior in CdSe NWs to surface composition. In FET measurements, selenium and sulfur enrichment on their own led to suppressed electron currents, while cadmium enrichment, especially in conjunction with annealing, yielded greatly enhanced electron currents and lower hysteresis values, indicative of effective doping and surface trap passivation. In this study, cadmium was introduced in its preferred 2^+ oxidation state, leaving it with no free carrier to impart to the NW. Thus we attributed the observed trap reduction and doping effect to compensation of cadmium vacancies and contribution of selenium vacancies, respectively, at the NW surface, in analogy to the role these imperfections play in bulk CdSe. When combined with another dopant, indium, currents could be increased slightly for cadmium enriched NWs, but dramatically for selenium and sulfur enriched NWs. While the combination of indium and selenium enrichment exhibited the highest currents of all devices measured, indium with sulfur enrichment demonstrated the best I_{ON}/I_{OFF} ratio, shedding light on recent observations in CdSe NC FETs.[11,35,65] Low-temperature data for indium-doped CdSe NW FETs show no evidence of impurity scattering, and the surface-sensitive indium–chalcogen behavior is consistent with indium incorporation at the CdSe NW surface as a "remote dopant." The simple wet-chemical methods introduced here for manipulating the atoms at the NW surface after FET fabrication represents a practical approach to optimizing device characteristics independently from the synthesis and processing conditions. With further exploration, this approach may prove applicable to a wide variety of compound semiconductor nanostructures.

METHODS SECTION

Materials for CdSe Nanowire Synthesis. HMDS, octadecene (90%), and butyl lithium (1.6 M solution) were purchased from Acros. Trioctylphosphine oxide (90%), trioctylphosphine (90%), selenium shot (99.99%), oleic acid (90%), bismuth chloride (99.999%), cadmium oxide (99.99%), and hexadecylamine (90%) were purchased from Sigma-Aldrich. All solvents were either purchased anhydrous or dried by standard methods.

Synthesis of Bismuth Precursor. Following a published procedure and using air-free Schlenk techniques:[66] 4.25 mL of HMDS, cooled using an ice bath was treated slowly with 12.5 mL of *n*-butyl lithium solution (1.6 M in hexanes). The flask was allowed to stir for 1 h and slowly warm to room temperature, and then it was held under a vacuum for 2 h to remove volatile solvent, leaving a white crystalline solid, $Li(N(SiMe_3)_2)$. The solid was redissolved in 20 mL of ether and cooled with an ice bath. To this solution was slowly added a suspension of 1.057 g of $BiCl_3$ in 20 mL of ether and 5 mL of THF. The mixture was stirred and slowly warmed to room temperature for 1 h, turning yellow. Vacuum was applied for 1 h to remove volatile species, and the solid was dissolved in 30 mL of pentane and filtered through a medium porosity frit. A yellow powder solid, $Bi(N(SiMe_3)_2)_3$, was isolated after application of a vacuum to remove pentane.

Synthesis of Bismuth Nanocrystals. Bismuth nanocrystals were prepared following literature procedure and using air-free Schlenk techniques:[67] 20 g of hexadecylamine was degassed under a vacuum at 100 °C for 1 h and then heated to 130 °C under nitrogen. 140 mg of $Bi(N(SiMe_3)_2)_3$ and 170 mg of $Li(N(SiMe_3)_2)$, made as described above, were dissolved in 2 mL of toluene and injected rapidly into the reaction flask. The reaction was quenched after 15 s with the injection of 20 mL of dry toluene and application of a water bath. 1.0 mL of dry and degassed oleic acid was added to the reaction solutions to aid in the long term stability of the colloids. The bismuth particles were isolated by precipitation with ethanol, redispersed in chloroform, precipitated again with acetone, then hexanes/acetone, and finally dispersed into toluene.

Synthesis of CdSe Nanowires. A scale-up of literature procedure was followed for the synthesis of SLS-grown CdSe nanowires:[45] 24.0 g of trioctylphosphine oxide, 200 mg of cadmium oxide, and 5.0 mL of oleic acid were combined in a 25 mL 3-neck flask and heated under a vacuum to 120 °C for 1 h and then to 330 °C for injection. An injection solution of ~2 mg of bismuth particles in 50 μL of dry toluene with 1.4 mL of octadecene and 0.20 mL of 1 M trioctylphosphine selenide was rapidly injected. The reaction was maintained on a heating mantle for 1 min after injection and then removed and cooled. The nanowire product was washed successively with chloroform/ethanol(2×), toluene/acetone, and butanol and then dispersed into 10.0 mL of chloroform.

Electrode and Dielectric Fabrication. Devices were fabricated on a degenerately *n*-doped Si wafer with 250 nm thermally grown SiO_2 from Silicon, Inc. The Si wafers were treated with UV-Ozone for 30 min before deposition of the Al_2O_3 dielectric. A Cambridge Nanotech Savannah 200 system was used to deposit 20 nm of atomic layer deposited Al_2O_3 at 250 °C using trimethylaluminum and water precursors. Next, the Al_2O_3 device was prepared with a self-assembled monolayer following a previously reported procedure.[49,68] Al_2O_3 devices were submerged in 0.005 M octadecylphosphonic acid (ODPA) (PCI Synthesis) in isopropyl alcohol solution over 16 h to treat the Al_2O_3 surface. The substrates were then rinsed thoroughly with isopropyl alcohol, submerged in a fresh bath of isopropyl alcohol, rapidly dried with a nitrogen gun and then heated at 70 °C for 10 min. Bottom contact electrodes were fabricated by evaporating metal through a shadow mask made of silicon nitride membranes with very fine channel lengths of 30 μm and widths of 1260 μm. To make bottom contact gold electrodes,

2 nm of chromium and then 20 nm of gold were evaporated. To make bottom contact indium electrodes, 2 nm of chromium, 10 nm of gold and then 10 nm of indium were evaporated.

Nanowire Solution Preparation and DC Electric-Field Alignment. 30.0 μL of stock CdSe nanowire originally in chloroform (approximately 2 mg/mL) was added to 10.0 mL of anhydrous octane:nonane at a 1:1 (vol:vol) ratio with 15.0 μL of 10 wt % solution hexadecane-graft-polyvinylpyrrolidinone (HD-PVP) copolymer (M_n = ~7300), which was used to improve the nanowires' dispersibility. The presence of HD-PVP is absolutely critical to preventing the nanowires from aggregating and precipitating out of solution.[44,49] Without the use of HD-PVP, nanowires "crash out" of solution and will align as mats of densely clumped nanowires. Nanowire solutions were dropcast under DC electric fields (10^4 to 10^5 V/cm) to align nanowire arrays across prefabricated bottom electrodes. The density of aligned NWs was highly dependent on the dropcast solution volume and concentration, which we optimized at 1 μL and approximately 6 μg/mL, respectively. Nanowire devices were then washed in both ethanol and chloroform to remove excess ligands, namely, the ligands used in nanowire synthesis and the HD-PVP used to aid nanowire dispersion. Removing surface-bound ligands improved FET transport characteristics, whereas insufficient washing led to very poor FET current modulation. Electric-field directed assembly was carried out in an MBraun nitrogen glovebox, and all solvents used were distilled and anhydrous. An Agilent 4156C parameter analyzer in combination with a Karl Suss PM5 probe station mounted in the nitrogen glovebox was used to measure device characteristics. The source was grounded, and the highly *n*-doped silicon wafer was used as a back gate electrode. When hysteresis was significantly large, a true mobility extraction was difficult, but to give an idea of trends, forward scans were used to extract values in the linear regime. The electron mobility was calculated on the basis of the channel width defined by the electrode dimensions, so the mobility values quoted in the text should be considered a conservative estimate.

Inorganic Salt Treatment. CdSe NWs were deposited on a substrate and then immersed in a 50 mM solution of ammonium chloride in anhydrous methanol for 10 min to remove 76% of the ligands, as verified by Fourier transform infrared spectroscopy (FTIR). The substrates were then submerged in a bath of fresh methanol to rinse off excess nonsurface bound ammonium chloride. Substrates with ligand-free NWs were submerged for 10 min in solutions of inorganic salts at 50 mM concentrations of cadmium acetate, sodium selenide or sodium sulfide in anhydrous methanol to build a layer of cadmium, selenium, or sulfur, respectively. The samples were then rinsed in a fresh bath of methanol to remove excess, nonspecifically bound cadmium acetate, sodium selenide or sodium sulfide.

Energy Dispersive X-ray Spectroscopy Measurements and ICP Measurements. Concentrated solutions of CdSe NWs were dried atop 300 mesh SiO-coated copper TEM grids, cleaned with ammonium chloride and then treated with different inorganic salts, as described above. Grids were subsequently measured to verify that the inorganic salt treatment changed the Cd:Se ratio. Scanning electron microscopy (SEM) images and energy dispersive X-ray spectroscopy (EDS) spectra were recorded on a JEOL JSM7500F equipped with an Oxford X-stream EDS detector. EDS spectra were recorded at 10 kV and were analyzed with Oxford's INCA software. Samples for inductively coupled plasma optical emission spectroscopy (ICP-OES) were prepared by dissolving with concentrated nitric acid and diluting with ultrapure water and were measured on a Spectro Genesis ICP-OES.

FT-IR Spectra. A concentrated NW solution in octane was spin-cast on to 1" square pieces of double polished Si coated with a monolayer of mercaptopropyltrimethoxysilane to promote NW adhesion.[69] The 1" pieces were broken into smaller fragments and either treated directly with thiocyanate or treated with different inorganic salts, as described above, and then thiocyanate. Thiocyante treatment was performed as follows: fragments were immersed in 1% ammonium thiocyanate in acetone for 2 min, followed by immersion in pure acetone to wash. The transmission spectrum was taken on a Thermo Scientific 6700 FT-IR spectrometer. Three independently prepared samples were measured for each treatment and averaged to make the composite spectra shown.

Low-Temperature Measurements. For measurements down to 4.5 K, samples were sealed with a glass coverslip using epoxy (ITW Devcon). When using the epoxy method, either top contact gold electrodes had to be fabricated over the bottom contact electrodes to maintain electrical connectivity between the electrodes and nanowire at lower temperatures, or the device had to be coated with 20 nm of Al_2O_3 using atomic layer deposition. The gold top contact was fabricated according to a modified literature method.[44,49] All e-beam resists and developers were degassed and used inside an MBraun nitrogen glovebox. An e-beam resist bilayer of 495 PMMA A4 (MicroChem) and 950 PMMA A4 (Microposit) was spincast and baked under nitrogen at 180 °C for 2 min for each layer. The PMMA coated device was secured in a jar under nitrogen in the glovebox and taken to the e-beam lithography tool, where the top contact pattern was exposed. After exposure, the sample was developed in the glovebox with methyl isobutyl ketone in isopropyl alcohol (MIBK: IPA 1:3, Honeywell Burdick and Jackson). E-beam evaporation of the 50 nm gold contact layer was carried out in a nitrogen glovebox with an integrated evaporator, followed by lift-off with anhydrous acetone. ALD coatings were carried out in a Cambridge Nanotech Savannah 200 system to deposit 20 nm of atomic layer deposited Al_2O_3 at 200 °C using trimethylaluminum and water precursors. Encapsulating in Al_2O_3 maintained good connectivity between the metal contacts and nanowire and does not require the use of top contact gold electrodes. Both methods maintained good connectivity between the metal contacts and NW and the devices remained largely unchanged throughout the fabrication process [Supporting Information Figure S8]. The sample was transferred to the Lakeshore Cryotronics vacuum, cryogenic probe station. Once under a high vacuum, the epoxy seal was broken upon cooling to low temperature (around 200 K), and the device was kept under a vacuum for all reported measurements. Measurements were performed under a high vacuum (at least 10^{-6} Torr) and at varying temperatures between 4.5 and 298 K by introducing liquid helium. Because of increasing contact resistances at lower temperatures, mobility values were calculated in the saturation regime, where $V_{DS} > V_G - V_T > 0$ [Supporting Information Figure S9].

Conflict of Interest: The authors declare no competing financial interest.

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Supporting Information Available: Detailed FET output characteristics and FTIR data of inorganic salt treated CdSe NWs. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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