Circuit Fabrication at 17 nm Half-Pitch by Nanoimprint Lithography

ARTICLE *in* NANO LETTERS · APRIL 2006

Impact Factor: 13.59 · DOI: 10.1021/nl052110f · Source: PubMed

NANO LETTERS

2006
Vol. 6, No. 3
351−354

Circuit Fabrication at 17 nm Half-Pitch by Nanoimprint Lithography

Gun-Young Jung,[†,‡] Ezekiel Johnston-Halperin,[§] Wei Wu,[†] Zhaoning Yu,[†] Shih-Yuan Wang,[†] William M. Tong,[†,||] Zhiyong Li,[†] Jonathan E. Green,[§] Bonnie A. Sheriff,[§] Akram Boukai,[§] Yuri Bunimovich,[§] James R. Heath,[§] and R. Stanley Williams*[,†]

Hewlett-Packard Laboratories, 1501 Page Mill Road, Palo Alto, California 94304, Division of Chemistry and Chemical Engineering, California Institute of Technology, Pasadena, California 91125, and Advanced Materials & Processes Labs, Technology Development Operations, Hewlett-Packard Company, 1000 Circle Boulevard, Corvallis, Oregon 97330

Received October 26, 2005; Revised Manuscript Received January 6, 2006

ABSTRACT

High density metal cross bars at 17 nm half-pitch were fabricated by nanoimprint lithography. Utilizing the superlattice nanowire pattern transfer technique, a 300-layer GaAs/AlGaAs superlattice was employed to produce an array of 150 Si nanowires (15 nm wide at 34 nm pitch) as an imprinting mold. A successful reproduction of the Si nanowire pattern was demonstrated. Furthermore, a cross-bar platinum nanowire array with a cell density of approximately 100 Gbit/cm^2 was fabricated by two consecutive imprinting processes.

The cross-bar architecture has been adopted by many as a leading candidate architecture for post-CMOS nanoelectronic circuits[1] because of its scalability down to the molecular scale, addressability of each cross point cell with a demultiplexer, its reconfigurability to tolerate defects in the circuit,[2] and its manufacturability at a reasonable cost with nanoimprint lithography.[3,4] We have previously demonstrated an 8 × 8 nanoscale electronic circuit using molecules as functional elements in the junction of the metal cross bar fabricated by nanoimprint lithography at 65 nm half-pitch (hp).[5] Since then, we have successively scaled the nanoimprint process down to 50 nm[6] and further to 30 nm hp[7] by using molds that were fabricated using electron beam lithography (EBL). However, severe proximity effects on neighboring features during e-beam exposure has made it extremely challenging to produce molds with dense wires smaller than 30 nm hp at the present time.[8]

Our need for patterning metal nanowires with 17 nm hp drove us to seek alternatives to EBL for mold fabrication. One solution was to perform a spatial frequency-doubling process on an existing e-beam generated mold.[9] An alternative approach was to use a mold patterned by the superlattice nanowire pattern transfer (SNAP) method, which could create high aspect ratio arrays of metal[10] or semiconductor[11] nanowires at dimensions down to 8 nm hp from the selectively etched edges of the superlattice. In this Letter, we report on the combination of the SNAP patterning method with the nanoimprinting replication method to fabricate metal nanowire arrays and cross-bar circuits at a feature half-pitch (hp) of 17 nm. This approach should enable high throughput manufacturing of ultra-high-density metal and semiconductor nanowire circuits for memory,[12] logic,[2,13] sensing,[14] optoelectronic,[15] and other applications.[16]

Features in a superlattice structure with a less than 15 nm hp have been previously patterned on a polymer resist by nanoimprint lithography.[17] However, transferring such patterns from the imprinted resist to the substrate as metal wires is far more difficult and until now has not been reported. Imprinting ultradense patterns poses several additional challenges. For example, issues such as the thickness of the imprinting resist, resist adhesion to the mold features, composition of the resist material and the selectivity of various etching processes, etc., all require higher levels of control than are needed for less demanding replication tasks. In this paper, we will briefly review the procedure for fabricating a silicon mold with features at 17 nm hp from a superlattice and focus on describing a UV-based imprinting process for replicating the 17 nm hp pattern from the silicon mold to metal wires on a glass substrate.

The silicon molds used in this study were fabricated with the previously reported SNAP techniques[10,11] with a slight

* Corresponding author: e-mail, stan.williams@hp.com; phone, (+1)-650-857-6586; fax, (+1)650-236-9885.
† Hewlett-Packard Laboratories.
‡ Current address: Department of Materials Science and Engineering, Gwangju Institute of Science and Technology (GIST), Gwangju, Republic of Korea.
§ Division of Chemistry and Chemical Engineering, California Institute of Technology.
|| Advanced Materials & Processes Labs, Technology Development Operations, Hewlett-Packard Co.

10.1021/nl052110f CCC: $33.50
Published on Web 02/04/2006

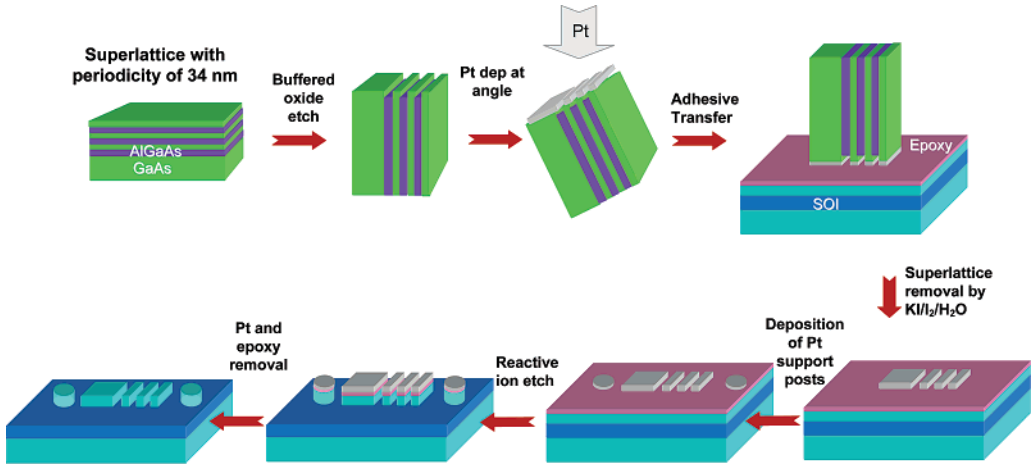

Figure 1. SNAP process procedure for transferring nanoscale features from a cleaved superlattice to a flat substrate.

variation, as summarized in Figure 1. Briefly, GaAs/Al_xGa_{1-x}As superlattice was prepared by epitaxial deposition on a GaAs wafer. The wafer was cleaved and then diced into a number of small (3 mm long) pieces. By chemically selective etching of the GaAs layers, the edge of each piece became the initial nanowire template. After a self-aligned shadow mask deposition of metal onto the exposed $Al_xGa_{1-x}As$ ridges, metal nanowires were formed along the top of the $Al_xGa_{1-x}As$ planes in which the spacing, alignment, and width were determined by the periodicity of the original epitaxy (with typically sub-monolayer thickness control).

Typically, those metal wires transferred to a substrate served as an etch mask for defining nanowires in the underlying material (in this case a commercial silicon-on-insulator wafer from Ibis Tech. Corp., consisting of 35 nm of silicon on 150 nm of oxide). In this experiment an additional array of platinum disks was deposited over the entire substrate using a shadow-mask evaporation just prior to pattern transfer to silicon layer by reactive ion etching. The result was an array of silicon posts, 400 μm wide at 1.4 mm spacing with heights exactly matched to that of the nanowire array. These posts served as standoffs during the imprinting process, and their function was to ensure that the mold and substrate were kept as parallel as possible during the imprinting process and the imprinting pressure was evenly distributed over the entire contact area. Finally, a section of silicon nanowires with the best transfer results was selected from the full length of the array (typically a 20 μm section from a 2−3 mm array), and the excess silicon nanowires were removed using a combination of electron-beam lithography and dry-etching (not shown in Figure 1).

Figure 2 illustrates the process procedure to fabricate the metal patterns by nanoimprint lithography and subsequent lift-off process. Optimizing the aspect ratio (i.e., height/width) of the features on the mold is important in terms of mold lifetime and the following lift-off process. Features with a high aspect ratio are likely to collapse during the imprinting process. Conversely, features with a small aspect ratio can cause major difficulties during metal lift-off. This is especially true for a single-layer imprint resist structure. A commonly adopted solution is to utilize a bilayer resist

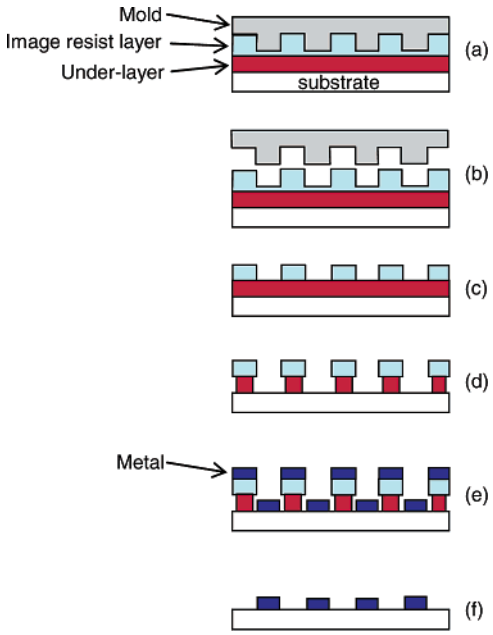

Figure 2. Schematic diagram of process flow: (a) application of mold to resist; (b) mold separation from the imprinted resist; (c) residual layer etching; (d) pattern transfer to the underlayer; (e) metal deposition; (f) metal lift-off.

structure, in which the imprinted patterns in the image resist layer are transferred to the underlayer by selective reactive ion etching (RIE, Figure 2d). It not only leads to an enhanced aspect ratio of the overall resist structure after etching through the underlayer but also creates a lateral resist undercut in the underlayer which separates the metal deposit on the substrate from the sidewall of the trench and greatly improves the metal lift-off process (Figure 2f). The use of an underlayer in addition to the image resist layer, however, adds a significant amount of complexity to the total process.

Several requirements for the image resist layer need to be considered for successful nanoimprinting lithography. First, a high mechanical strength after curing, typically achievable by cross-linking of the imprint resist, is needed to counter the separation force during mold detachment from the imprinted image resist. Second, a low viscosity is required to promote spreading of the resist solution under imprinting

pressure. Third, good adhesion to and compatibility with the underlayer are required such that the coating of the image resist layer will neither peel from nor dissolve into the underlayer. Fourth, the image resist layer should have a strong resistance to oxygen plasma dry-etching which is used to transfer the imprinted patterns to the underlayer with the image resist layer as an etching mask.

The underlayer also has several requirements. It should adhere to the glass substrate, preferably through covalent chemical bonding, and at the same time it should firmly hold the overlaying image resist layer during the mold separation. It should be easily dissolved with solvents to facilitate metal lift-off. Finally, it should serve as a planarizing layer to cover the substrate topolograpgy and to distribute the imprinting pressure evenly over the entire sample, thus minimizing damage to the mold.

On the basis of the above considerations, we used the following major components to engineer the image resist: UV-curable poly(dimethylsiloxane) material (Gelest, 87%), radical initiator (Irgacure 184, Ciba, 3%), and cross-linker (ethylene glycol dimethacrylate, Aldrich, 10%). LOL 1000 (Shipley Ltd.) was selected as the underlayer material.

The successful fabrication of metal wires at 17 nm hp relied on the delicate balance of thickness control of each layer and the etching process. For the image resist layer, the initial spin-coated layer thickness determined the residual layer thickness under the trenches after imprinting. A thick film resulted in a significant residual layer under the trenches, which required a long etching step of Figure 2c to remove it before pattern transfer to the underlayer. This may lead to significant line edge roughness for the imprinted wires. Typically, the initial image resist layer thickness was closely matched with the feature height (~35 nm in this experiment) on the mold itself.

For the underlayer, a thin underlayer was required to enable rapid pattern transfer. A thicker film requires a longer etching time for the pattern transfer (Figure 2d), which will lead to more lateral resist loss and to the collapse of the resist structure. A thin underlayer, on the other hand, may not allow sufficient undercut to enable the metal lift-off process.

With all these considerations in mind, the LOL layer was spin-coated on a borofloat glass substrate (Precision Glass & Optics, Santa Ana) and baked in an oven at 90 °C for 30 min. The thickness was modified with an oxygen plasma treatment to reach 25 nm. Subsequently, 35 nm of the UV-curable resist was spin-coated on top of the LOL layer.

After the mold was treated with a releasing material in the vapor phase as previously described,[18] it was brought into contact with the UV-curable resist layer. When the substrate and the mold were pressed together in a vacuum, the fluidlike UV-curable resist layer spread evenly over the entire contact area. The resist layer was then cured for 15 min by UV irradiation through the glass substrate at an imprinting pressure of 80 psi in a purpose-built UV-based imprinting machine (Figure 2a).

Parts A and B of Figure 3 are scanning electron microscopy (SEM) images of the SNAP-generated silicon nanowire mold at 17 nm hp and the corresponding nanoimprinted pattern on the image layer resist after mold separation, respectively. The mold was readily detached from the resist film with negligible separation force (Figure 2b). The imprinted patterns showed that the structure of the high-density nanowire arrays was transferred to the resist film with high fidelity.

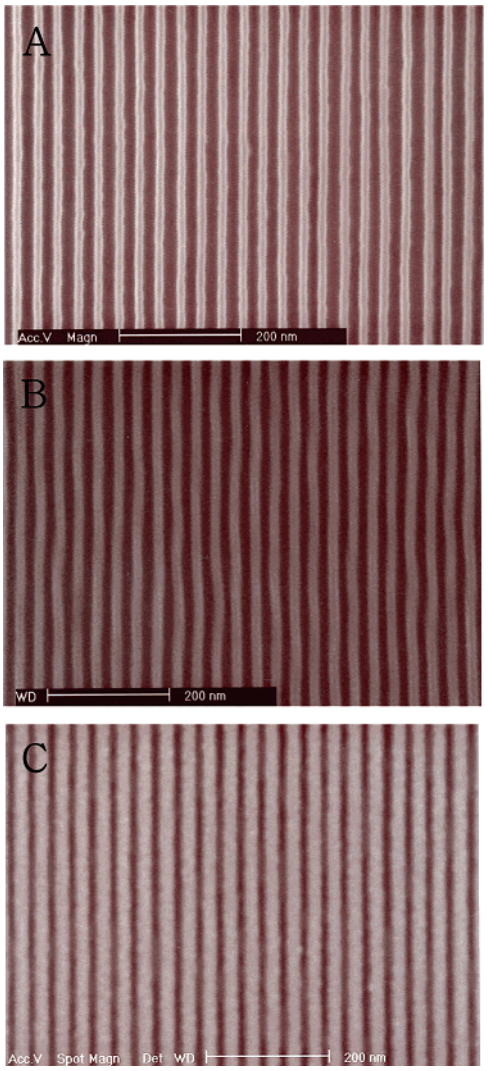

Figure 3. SEM images of (A) the SNAP-generated 17 nm hp silicon nanowire mold, (B) the corresponding nanoimprinted pattern in resist, and (C) final metal nanowires on glass substrate. The scale bars in A, B, and C are 200 nm.

We used a gentle reactive ion etching (CF_4; 7 W at 2 mTorr for 20 s; Cambridge, Inc., Plasmalab system 100) to etch any residual layer under the trenches (Figure 2c). The etch rate under such conditions was measured to be 0.3 nm/s for the image resist layer. The imprinted image patterns were then transferred to the LOL layer with an O_2 plasma treatment (50 W at 20 mTorr for 25 s). The etch rate under O_2 plasma was 1.3 nm/s for the LOL underlayer, which was 22 times faster than that of the image layer, 0.06 nm/s. With such a selective etching process, pattern transfer to the underlayer was accomplished without destroying the imprinted patterns on the image resist layer.

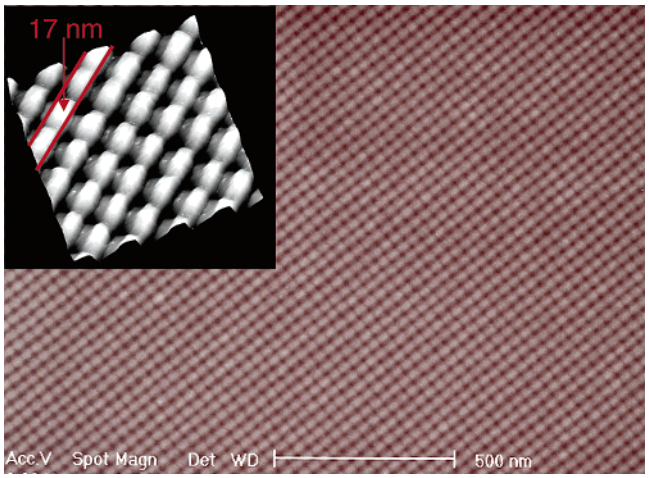

Figure 4. A scanning electron micrograph of the central region of a 13 000 junction metal cross-bar structure. This circuit was generated by carrying out two consecutive nanoimprinting processes. The same mold was employed for both. The inset shows an AFM image of a magnified region of the cross bar.

Following the O_2 plasma etch, titanium (4 nm) and platinium (5 nm) were deposited by electron-beam evaporation (CHA, Fremont) at a deposition rate of 0.03 nm/s (Figure 2e). The metal lift-off process was performed by soaking the sample in a polymer remover (1165, Shipley Ltd.) at 110 °C for 30 min followed by ultrasonic agitation for 1 min to produce the isolated metal nanowires at 17 nm hp as shown in Figure 3C.

A cross-bar structure was produced by repeating the same nanoimprinting process at 90° with respect to the first imprinting. A conventional mask aligner (Canon, PLA-501F) was used to align the top nanowire imprint process with the bottom layer of metallic nanowires. Figure 4 shows an SEM image of the imprinted 34 nm pitch metal cross-bar structure with an equivalent cell density of approximately 100 Gbit/cm^2. The inset of Figure 4 is an atomic force microscopy (AFM) image of this cross-bar structure collected with a carbon nanotube tip, showing clearly that one set of metal nanowires runs over the other.

High-density silicon nanowire arrays generated by the SNAP technique were utilized as a mold for generating 17 nm hp metal nanowires. To faithfully reproduce small features from the mold, a carefully engineered bilayer resist structure was used for the nanoimprint lithography. Nanowire patterns at 17 nm hp were successfully transferred to the underlayer by selective RIE without collapsing the resist patterns. As a demonstration, an array of 150 separated platinum nanowires was produced using the nanoimprinting process, and a corresponding cross-bar structure was fabricated by repeating the imprinting process with the same mold and a 90° rotation. A molecular memory device, based on such a cross-bar structure, is currently under investigation. Such a circuit could potentially push the limits of electronically addressable memory density toward 100 Gbit/cm^2. The SNAP process has already been demonstrated as capable of producing nanowire arrays at 8 nm hp, and it is likely that even smaller pitch nanowire arrays can be generated. This demonstration shows that the SNAP process can in principle be coupled with nanoimprint to create a manufacturable process; molds with a large number of nanowire fields may be produced as daughters of an original SNAP mold by a step and repeat process. Such techniques may lead to a manufacturing approach that can generate electrical circuits at near molecular scales.

Acknowledgment. This research was supported in part by the Defense Advanced Research Projects Agency (DARPA) and through a subcontract from Mitre Corp.

Note Added after ASAP Publication. Changes were required in the author affiliation line and the related footnote on the title page and in the third paragraph of the third page in the version published ASAP February 4, 2006; the corrected version was published ASAP February 9, 2006.

References

(1) Heath, J. R.; Kuekes, P. J.; Snider, G. S.; Williams, R. S. *Science* **1998**, *280*, 1716.
(2) Kuekes, P. J.; Williams, R. S.; Heath, J. R. US Patent 6 128 214, 2000.
(3) Chou, S. Y.; Krauss, P. R.; Renstrom, P. J. *Science* **1996**, *272*, 85.
(4) Colburn, M.; Johnson, S.; Stewart, M.; Damle, S.; Bailey, T.; Choi, B.; Wedlake, M.; Michaelson, T.; Sreenivasan, S. V.; Ekerdt, J.; Willson, C. G. *Proc. SPIE* **1999**, *3676*, 379.
(5) Chen, Y.; Jung, G. Y.; Ohlberg, D. D. A.; Li, X.; Stewart, D. R.; Jeppesen, J. O.; Nielsen, K. A.; Stoddart, J. F.; Williams, R. S. *Nanotechnology* **2003**, *14*, 462.
(6) Jung, G. Y.; Ganapathiappan, S.; Ohlberg, D. A. A.; Olynick, D. L.; Chen, Y.; Tong, W. M.; Williams, R. S. *Nano Lett.* **2004**, *4*, 1225.
(7) Jung, G. Y.; Wu, W.; Wang, S. Y.; Tong, W. M.; Williams, R. S. *J. Polym. Sci. Technol.* **2005**, *18*, 565.
(8) Kyser, D. F. *J. Vac. Sci. Technol., B* **1983**, *1*, 1391.
(9) Yu, Z.; Wu, W.; Olynick, D. L.; Jung, G. Y.; Straznicky, J.; Li, Z.; Li, X.; Tong, W. M.; Wang, S. Y.; Williams, R. S. Nanoimprint and Nanoprint Technology (NNT), 20-P-5-30, Nara, Japan, 2005.
(10) Melosh, N. A.; Boukai, A.; Diana, F.; Gerardot, B.; Badolato, A.; Petroff, P.; Heath, J. R. *Science* **2003**, *300*, 112.
(11) Beckman, R. A.; Johnston-Halperin, E.; Melosh, N. A.; Luo, Y.; Green, J. E.; Heath, J. R. *J. Appl. Phys.* **2004**, *96*, 5921.
(12) Collier, C. P.; Mattersteig, G.; Wong, E. W.; Luo, Y.; Beverly, K.; Sampaio, J.; Raymo, F. M.; Stoddart, J. F.; Heath, J. R. *Science* **2000**, *289*, 1172. Collier, C. P.; Jepsen, J. O.; Luo, Y.; Perkins, J.; Wong, E. W.; Heath, J. R.; Stoddart, J. F. *J. Am. Chem. Soc.* **2001**, *123*, 12632.
(13) Huang, Y.; Duan, X.; Cui, Y.; Lauhon, L. J.; Kim, K. H.; Lieber, C. M. *Science* **2001**, *294*, 1313. Duan, X.; Huang, Y.; Lieber, C. M. *Nano Lett.* **2002**, *2*, 487.
(14) Cui, Y.; Wei, Q.; Park, H.; Leiber, C. M. *Science* **2001**, *293*, 1289.
(15) Duan, X.; Huang, Y.; Cui, Y.; Wang, J.; Lieber, C. M. *Nature* **2001**, *409*, 66. Huang, M.; Mao, S.; Feick, H.; Yan, H.; Wu, Y.; Kind, H.; Weber, E.; Russo, R.; Yang, P. *Science* **2001**, *292*, 1897. Svensson, C. P. T.; Seifet, W.; Larsson, M. W.; Wallenberg, L. R.; Stangly, J.; Bauer, G.; Samuelson, L. *Nanotechnology* **2005**, *16*, 936.
(16) Karnick, R.; Castelino, K.; Fan, R.; Yang, P.; Majumdar, A. *Nano. Lett.* **2005**, *5*, 1638.
(17) Austin, M. D.; Ge, H.; Wu, W.; Li, M.; Yu, Z.; Wasserman, D.; Lyon, S. A.; Chou, S. Y. *Appl. Phys. Lett.* **2004**, *84*, 5299.
(18) Jung, G. Y.; Li, Z.; Wu, W.; Chen, Y.; Olynick; Wang, S. Y.; Tong, W. M.; Williams, R. S. *Langmuir* **2005**, *21*, 1158.

NL052110F