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Growth of Stacking-Faults-Free Zinc Blende GaAs Nanowires on Si Substrate by Using AlGaAs/GaAs Buffer Layers

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ABSTRACT Vertical GaAs nanowires on Si (111) substrate were grown by metal organic chemical vapor deposition via Au-catalyst vapor–liquid–solid mechanism. Stacking-faults-free zinc blende nanowires were realized by using AlGaAs/GaAs buffer layers and growing under the optimized conditions, that the alloy droplet act as a catalyst rather than an adatom collector and its size and composition would keep stable during growth. The stable droplet contributes to the growth of stacking-faults-free nanowires. Moreover, by using the buffer layers, epitaxial growth of well-aligned NWs was not limited by the misfit strain induced critical diameter, and the unintentional doping of the GaAs nanowires with Si was reduced.

KEYWORDS GaAs, nanowires, Si, zinc blende, stacking faults

Growth of high quality III–V compound semiconductors on Si substrate has applications in novel optoelectronic devices and optoelectronic integrated circuits. However, for the growth of GaAs epilayer on Si, there are three major problems, that is, the large lattice-mismatch (4.1 %), the large thermal expansion coefficient mismatch (55 %), and the formation of antiphase domain.^{1–3} Free-standing nanowires (NWs) grown in a bottom-up manner show considerable promise of resolving these problems, due to their small lateral dimensions.^{4–7}

Recently, epitaxial growth of GaAs NWs on Si substrate has been investigated by using selective-area growth,⁸ self-catalyzed growth,⁹ or Au-assisted vapor–liquid–solid (VLS) growth.^{10–15} However, a large amount of stacking faults were observed in the GaAs NWs,^{8–12,15} and growth along the nonvertical $\langle 111 \rangle$ equivalent directions normally occurred.^{9–11,13,14} Moreover, for Au-assisted VLS growth, there exists a critical diameter (~ 100 nm) limitation for epitaxial growth of well-aligned GaAs NWs on Si substrate due to the large lattice mismatch,^{7,15,16} and an unintentional doping of GaAs NWs and Si substrate with Si and Au atoms from the Au–Si alloy droplet, respectively.^{13,14}

In this letter, Au-catalyst VLS growth of stacking-faults-free zinc blende GaAs NWs on Si (111) substrate was realized by using AlGaAs/GaAs buffer layers. Moreover, epitaxial growth of vertically aligned NWs was not limited by the critical diameter, and the unintentional doping of the GaAs NWs with Si was not observed.

The epitaxy was performed by metalorganic chemical vapor deposition (MOCVD) with a Thomas Swan CCS-MOCVD system at a pressure of 100 Torr. Trimethylgallium (TMG), trimethylaluminum, and arsine were used as the precursors. Growth of the GaAs NWs on Si substrate was carried out as the following steps. (1) The Si (111) substrate was chemically cleaned with a final treatment in HF/NH₄F/H₂O (1:5:6) solutions to remove the native oxide and form a hydrogen-terminated surface.¹² (2) The AlGaAs/GaAs buffer layers, which consist of a 5 nm AlAs nucleation layer, a 15 nm Al_{0.5}Ga_{0.5}As nucleation layer and a 100 nm GaAs buffer layer, were grown on the Si substrate via a two-step growth, as described in our previous publication.³ (3) A 2.5 nm Au layer was deposited on the substrate by magnetron sputtering. Then the Au-coated substrate was loaded into the MOCVD reactor and annealed in situ at 645 °C in arsine and hydrogen ambient for desorption of surface contaminants and formation of Au-semiconductor alloy droplets as catalyst. (4) After ramped down to the desired temperature, GaAs NWs were grown via a two-temperature^{17,18} or a single-temperature procedure for Sample A and Sample B, respectively. For Sample A, the NWs growth was initiated at 510 °C for 60 s and then proceeded at 440 °C for 10 min, and the TMG was switched off during temperature changing from 510 to 440 °C. For Sample B, the NWs were grown at a constant temperature of 440 °C for 10 min. The V/III ratio was kept constant at 70 during the NWs growth.

In Step 2, the growth initiated at low temperature tend to form the (111)B-oriented surface, which favors the vertical growth of NWs.⁸ In Step 4, the low-temperature growth can reduce planar defects and lateral overgrowth,^{12,17} and the growth conditions including growth temperature and V/III ratio were previously optimized.

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Received for review: 08/31/2009

Published on Web: 12/15/2009

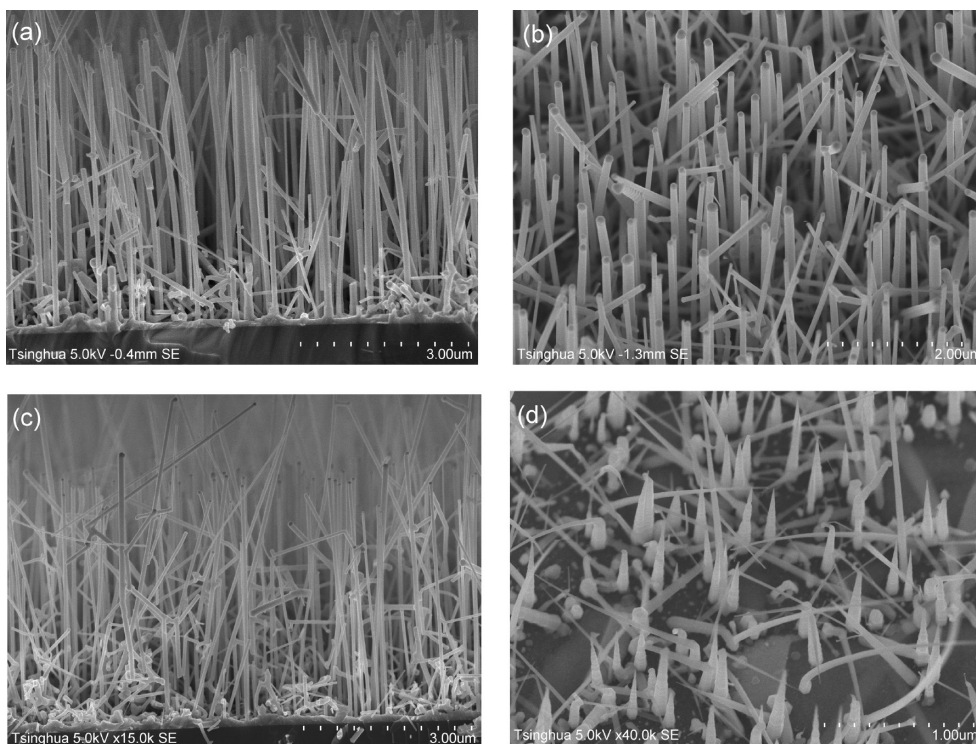


FIGURE 1. SEM images of (a) Sample A with a cross-sectional view of the cleaved sample, (b) Sample A with a 20° view from surface normal direction, (c) Sample B with a cross-sectional view of the cleaved sample, and (d) Sample C with a 20° view from surface normal direction.

To investigate the influence of the AlGaAs/GaAs buffer layers on the grown NWs, Sample C without the buffer layer was prepared by carrying out Step 1, Step 3, and Step 4 as aforementioned. In Step 4, Sample C was grown via the two-temperature procedure.

NWs were characterized by field-emission scanning electron microscopy (SEM) and transmission electron microscopy (TEM). SEM images were obtained with an accelerating voltage of 5.0 kV. TEM analyses were performed by using a FEI TECNAI F30 instrument operating at 300 KV, and the specimens were prepared by ultrasonicing the samples in ethanol for 5 min, followed by spreading drops from the suspension onto holey carbon/Cu grid.

Figure 1a,c,d shows the SEM image of Sample A, Sample B, and Sample C, respectively. A tilted SEM image of Sample A is shown in Figure 1b. The average length of NWs in Sample A, Sample B, and Sample C is 5.0, 4.5, and 0.92 μm , respectively, and the corresponding growth rate is 8.3, 7.5, and 1.5 nm/s. For Sample A, the average diameter of the NWs was about 110 nm, and the density of the NWs is about 10^9 cm^{-2} .

As shown in Figure 1d, about 70 % of the NWs in Sample C are perpendicular to the Si (111) substrate (in other words these wires are epitaxially grown) and are highly tapered without clear observation of Au—Si alloy droplet at the sharp tip. By contrast, in Sample A, the NWs grown under the same conditions are uniform in diameter as shown in Figure 1(a). Thus, for Sample C, the high tapering was not likely to be

induced by the growth model such as lateral overgrowth.¹⁹ Moreover, as reported by Dick et al.¹⁴ and Joyce et al.,¹⁷ uniform GaAs NWs can be obtained by growth on native oxide covered Si substrate or GaAs substrate, so it can be concluded that the droplet size should be keep constant and few or no Au atom diffuse into the GaAs NWs during growth. It is clear that the droplet became smaller or even disappeared during NWs growth due to diffusion of Au atom away from the droplet to the Si substrate. As reported by Dick et al.,¹⁴ a clean and deoxidized Si surface can act as a reservoir for Au atom, so the high tapering should mainly result from the shrinking of the droplet. In comparison with Sample A, the much slower growth rate of the taper NWs in Sample C should also result from the shrinking of the droplet due to the Gibbs—Thompson effect. For Sample A, the diffusion of Au atom to Si substrate can be blocked by the AlGaAs/GaAs buffer layers grown on the Si substrate, so uniform NWs can be obtained.

As shown in Figure 1a,c, Sample A appears to have higher yield of straight and vertical NWs than Sample B. For Sample A, about 80 % of the NWs are perpendicular to the Si substrate as shown in Figure 1b. It is clear that an initial brief step of high-temperature growth is useful in obtaining straight and well-aligned epitaxial NWs. Similar result has been reported for a two-temperature growth of vertically aligned GaAs NWs on GaAs (111)B substrate by Joyce et al.¹⁷ It was supposed that a planar nanoparticle—substrate interface, which contributes to the vertical growth, can be

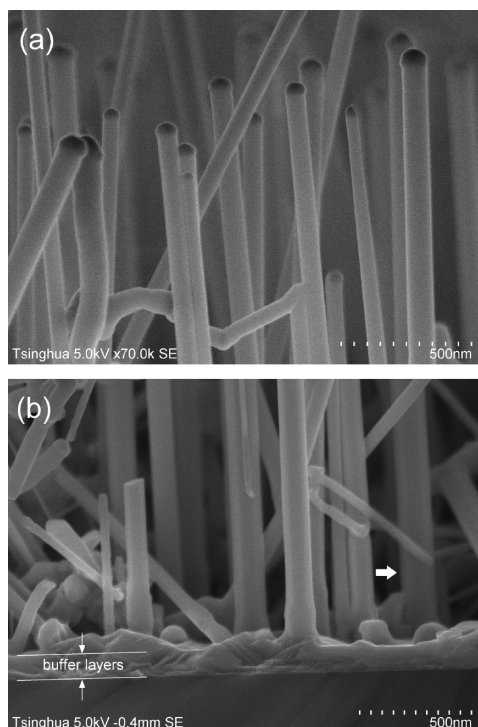


FIGURE 2. SEM cross-sectional view images of (a) the top and (b) base section of the GaAs NWs in Sample A.

established by an initial high-temperature growth.¹⁷ We believe that increasing supply of Ga at initial growth step would be helpful in establishing the planar interface because the pyrolysis efficiency of TMGa increases with temperature in the range from 430 to 500 °C.²⁰ Moreover, the yield of vertical GaAs NWs also has a relationship with the AlGaAs/GaAs buffer layer. Currently, the influence of crystal quality, thickness, and smoothness of the buffer layers on the yield of vertical NWs is still unclear and needs further investigations.

As reported by Chuang et al.¹⁶ and Cirilín et al.,¹⁵ well-aligned GaAs wire can be grown on Si substrate if and only if its diameter is smaller than the critical diameter (~ 100 nm), beyond which the lateral relaxation of the wire cannot accommodate the misfit strain between GaAs NWs and Si substrate, and then defects and kinks are induced by the strain.^{13,15,16} However, for Sample A vertical wire with diameter of 157 nm (as indicated by the arrow in Figure 2b), which is much larger than the critical diameter (~ 100 nm), can be grown successfully, because the misfit strain can be accommodated via generating dislocations in the AlGaAs/GaAs buffer layers.³ Thus, by using the AlGaAs/GaAs buffer layers, thick GaAs NWs can be epitaxially grown on Si substrate without the critical diameter limitation.

For VLS growth, there are two major contributions, that is, direct impingement of the precursors onto the alloy droplet and adatom diffusion from the sidewalls and substrate surface to the top.^{4,5,19–21} It has been demonstrated that the adatom diffusion will result in lateral overgrowth and tapering when the wire length is longer than the diffusion

length of adatom.^{19,22–24} As shown in Figure 1a and Figure 2, two remarkable phenomena can be observed in Sample A. (1) Lateral overgrowth and tapering of the NWs do not occur because the wire has a constant diameter from base to top and its diameter is slightly smaller than that of the alloy particle; and (2) the NWs length is nearly diameter independent and is about $5.0\ \mu\text{m}$, which is much longer than the diffusion length of Ga adatom (the diffusion length is about 10 nm for MOCVD growth at 440 °C²¹ and about 160 nm for MBE growth at 420 °C²⁴). Thus, for Sample A, it can be concluded that the NWs were grown with negligible contribution from the Ga adatom diffusion and almost all contribution from catalytic pyrolysis of the precursors impinging on the alloy droplet. In other words, the droplet acts as a catalyst rather than a collector of adatom.

Figure 3 shows the TEM analyses of a wire with a diameter of 98 nm from Sample A, and the TEM images were taken with $\langle 01\text{-}1 \rangle$ direction of the electron beam incidence. As shown in Figure 3a, the selected-area diffraction (SAD) indicated pure zinc blende structure, and no stacking faults was observed in the wire. High-resolution TEM (HRTEM) images of the top and middle section of the wire were shown in Figure 3b,c, respectively. The HRTEM images and the corresponding Fourier transform confirmed the pure zinc blende structure of the wire. Moreover, no Si signal was detected along the wire by the energy dispersive X-ray analysis (EDX) (not shown). As reported by Bakkers et al.,¹³ Si incorporation in the III–V nanowires, which grown directly on Si substrate, was detected by EDX clearly. It can be concluded that the unintentional doping of the GaAs NWs with Si can be reduced by using the AlGaAs/GaAs buffer layers.

Figure 4 shows the TEM analyses of a wire with a diameter of 21 nm from Sample A, and the TEM images were taken with $\langle 01\text{-}1 \rangle$ direction of the electron beam incidence. A HRTEM image of the middle section of the wire was shown in Figure 4b. The HRTEM image and the corresponding Fourier transform indicated pure zinc blende structure of the wire, and no stacking fault was observed.

For Sample A, the NWs growth conditions such as the two-temperature procedure, the high growth rate (8.3 nm/s), and the relatively high V/III ratio (70) may all contribute to the reducing of planar defects such as stacking faults and twins in the NWs.^{17,25} Moreover, fluctuations in the composition and/or size of the droplet would also result in stacking faults or twins in the wire due to the change of tension and supersaturation in the droplet.^{19,26–28} Fluctuation in composition and size of the droplet can be induced by the Ga adatom diffusion from the sidewall and substrate surface, because the amount of adatom diffusing into the droplet varies with lateral overgrowth as well as wire length.^{21,24} Thus, for Sample A, the droplet would keep stable during growth without contribution from the Ga adatom diffusion and that also contributes to growth of stacking-faults-free NWs.

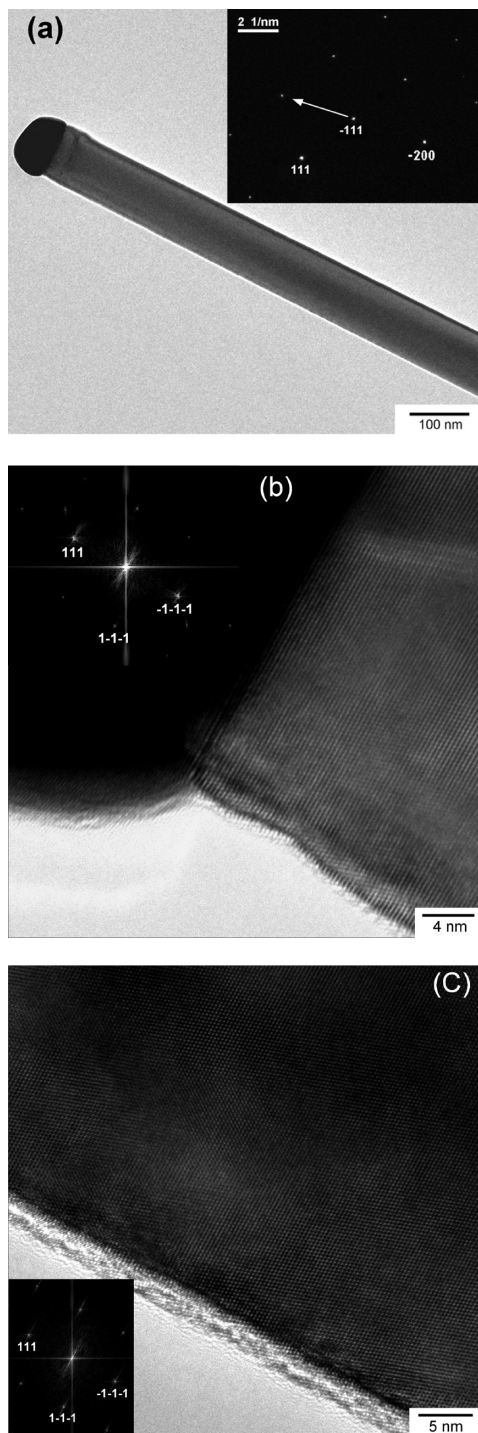


FIGURE 3. TEM analyses of a wire with a diameter of 98 nm from Sample A. (a) Bright field TEM image of the wire with an Au–Ga alloy particle at the tip (the corresponding SAD was shown as an inset and the growth direction was indicated by an arrow), where the contrast is due to bend contours; (b) HRTEM image of the alloy particle capped wire tip; (c) HRTEM image of the middle section of the wire. In (b,c), the corresponding Fourier transform of the structure was shown as an inset.

In conclusion, GaAs NWs were grown under the optimized conditions of selective pyrolysis of the precursors at the droplet. The AlGaAs/GaAs buffer layers and the opti-

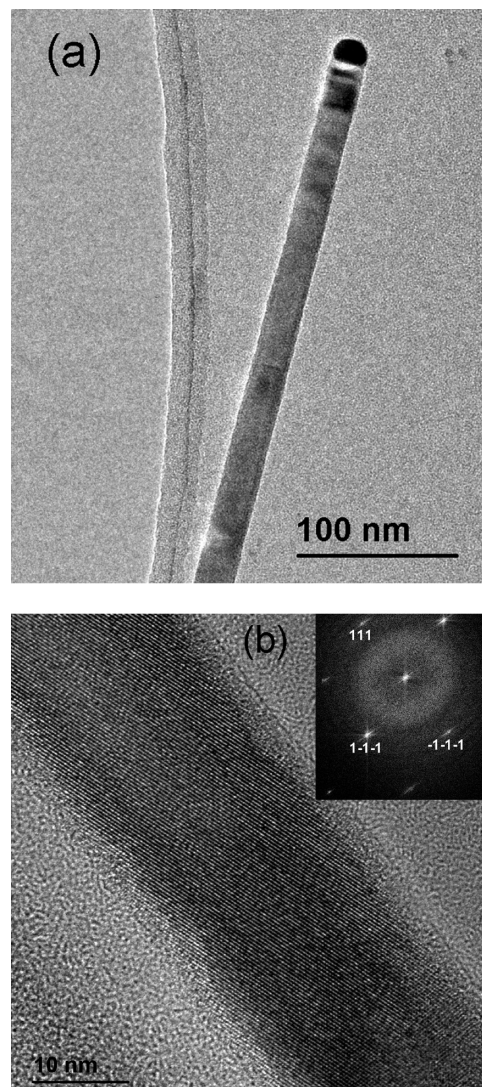


FIGURE 4. TEM analyses of a wire with a diameter of 21 nm from Sample A. (a) Bright field TEM image of the wire with an Au–Ga alloy particle at the tip, where the contrast is due to bend contours; (b) HRTEM image of the middle section of the wire with the corresponding Fourier transform as an inset.

mized growth conditions would make the droplet remain stable during NWs growth due to eliminating diffusion of Au atom away from the droplet and Ga adatom to the droplet. The stable droplet as well as the high growth rate (8.3 nm/s) and the high V/III ratio (70) contribute to the growth of stacking-faults-free NWs. Moreover, epitaxial growth of vertically aligned NWs was not limited by the critical diameter due to relaxation of the misfit strain between GaAs NWs and Si via the buffer layers.

Acknowledgment. This research was supported by grants from National Basic Research Program of China (2010CB327601), New Century Excellent Talents in University of China (NCET-05-0111), National Natural Science Foundation of China (60576018 and 90201035), National High Technology R&D Program of China (2006AA03Z416

and 2007AA03Z418), New Star Science and Technology Project of Beijing (2006A46), Changjiang Scholars and Innovative Research Team in University of China (IRT0609), 111 Program of China (B07005), and Program of Key International Science and Technology Cooperation Project (2006DFB11110). The authors thank V.G. Dubrovskii (Ioffe Physical Technical Institute of the Russian Academy of Sciences) for fruitful collaborations.

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