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High Volumetric Capacity Silicon-Based Lithium Battery Anodes by Nanoscale System Engineering

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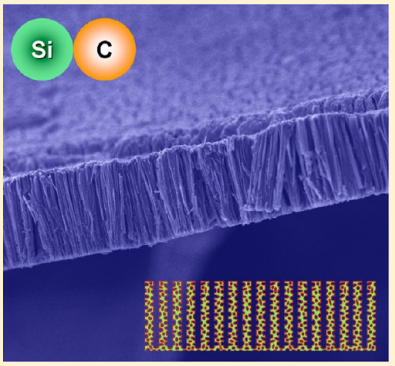
Supporting Information

ABSTRACT: The nanostructuring of silicon (Si) has recently received great attention, as it holds potential to deal with the dramatic volume change of Si and thus improve lithium storage performance. Unfortunately, such transformative materials design principle has generally been plagued by the relatively low tap density of Si and hence mediocre volumetric capacity (and also volumetric energy density) of the battery. Here, we propose and demonstrate an electrode consisting of a textured silicon@graphitic carbon nanowire array. Such a unique electrode structure is designed based on a nanoscale system engineering strategy. The resultant electrode prototype exhibits unprecedented lithium storage performance, especially in terms of volumetric capacity, without the expense of compromising other components of the battery. The fabrication method is simple and scalable, providing new avenues for the rational engineering of Si-based electrodes simultaneously at the individual materials unit scale and the materials ensemble scale.



KEYWORDS: *Silicon nanowire, graphene, volumetric capacity, nanoscale system engineering, lithium ion battery*

There is a steadily increasing demand for making lithium ion batteries smaller and lighter, namely, with higher volumetric capacity and gravimetric capacity, for various technological applications, including portable electronics, medical implants, electric vehicles, and smart grids.[1−6] Silicon (Si) has been touted as one of the most promising anode materials for next generation lithium ion batteries due to its relatively low working potential, abundance in nature, and more importantly highest known theoretical gravimetric (specific) capacity (3579 mAh g^{-1} for $Li_{15}Si_4$ at room temperature)[7,8] which is almost ten times that of commercialized graphite anodes. However, the Si experiences a dramatic volume change (more than 300%) during the lithiation and delithiation processes.[9] This causes pulverization and loss of electrical contact, as well as formation and propagation of an unstable solid electrolyte interphase (SEI)[10] on the Si surface, both of which result in rapid capacity fading of the battery.[5] Compared with Si bulk films and/or micrometer-sized Si particles, the nanostructuring of Si represents a very popular tactic to deal with the volume change-induced instability issues of Si, as well as has led to a quantum leap in the lithium storage properties in terms of gravimetric capacity, rate capability, and/or cycling stability.[11−13] So far, diverse exciting nanostructured Si paradigms, integrated with and without a second phase (e.g., carbon), have been extensively designed and exploited, some of which include nanoparticles,[14−18] nanowires,[11,19−26] nanotubes,[27,28] thin films,[29−31] and three-dimensional porous nanostructures.[32] Unfortunately, such transformative nanoscale materials design principle has generally been plagued by the relatively low tap (packing) density of Si, which first lowers volumetric capacity reflecting volumetric energy density, and second increases the use of other auxiliary components (e.g., binder, conductive carbon, foils) of the battery capable of reducing the gravimetric capacity and hence gravimetric energy density, fatally limiting the implementation of Si in a viable lithium ion battery.[2,13,33−36]

In principle, because the Si, regardless of its dimension and morphology, has to expand to exert its markedly high lithium storage capability, the adoption of a satisfactory void space is absolutely required; otherwise the electrode structure and cell/battery pack configuration can be deformed and even disintegrated by such a substantially large volume expansion. Given a ~300%[37] volume change of Si during full charge/discharge cycling, the essential void size can be speculated to be two times larger than the original volume of Si, which rather defines the maximum tap density of Si to be 0.8−0.9 g cm^{-3} of the electrode volume (see Supporting Information). In this regard, a major challenge is to build an energetic electrode architecture that can address the aforementioned volume change-induced problems and simultaneously realize the trade-off between the increase of the Si tap density and the incorporation of the required void space. We believe that the similar situation holds inevitably for other emerging electrode materials subject to large volume changes.

As schematically shown in Figure 1a, in this contribution we propose and develop a novel electrode configuration where the

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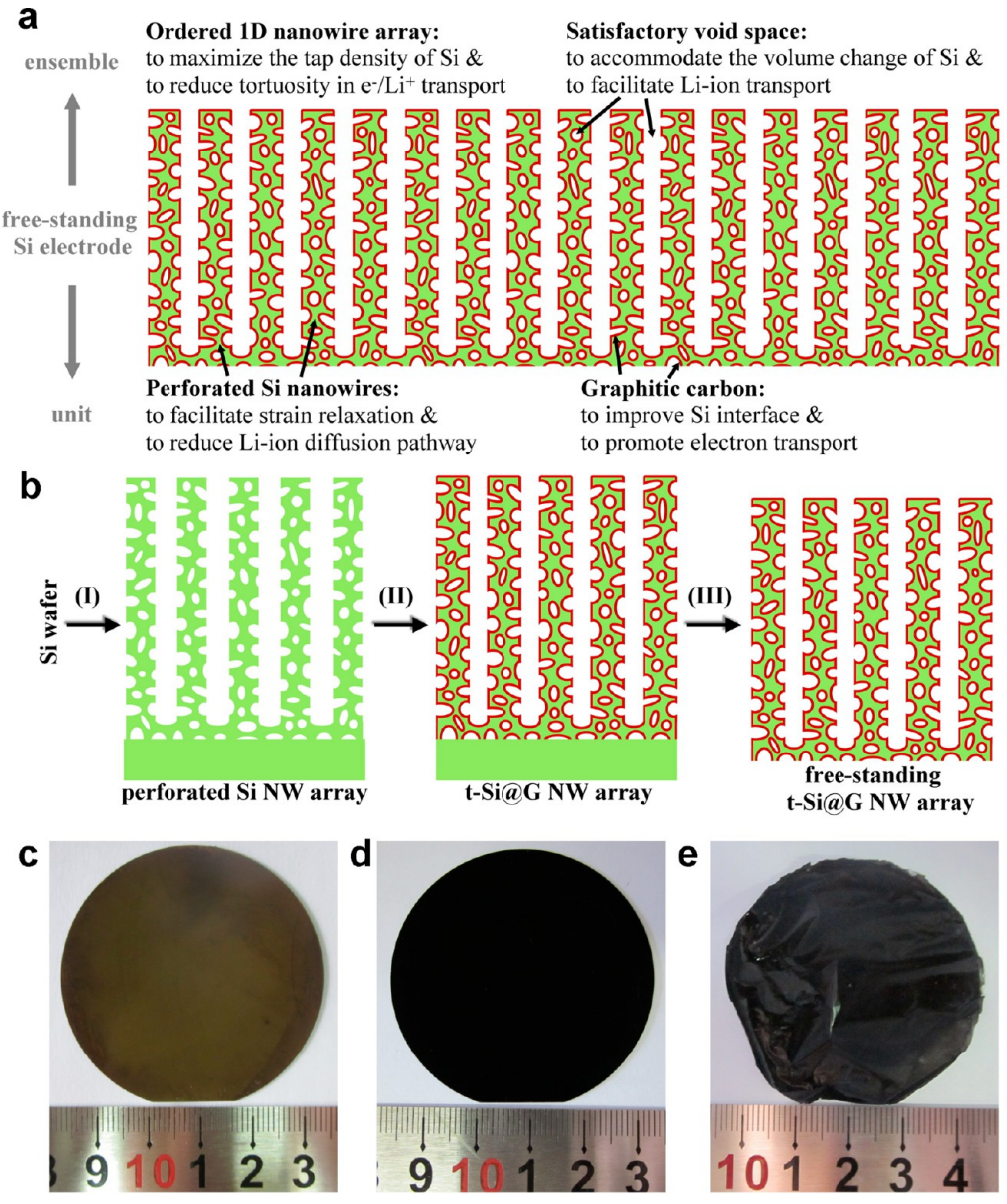

Figure 1. Electrode design and fabrication. (a) Cross-sectional view of a proposed textured silicon@graphitic carbon nanowire (t-Si@G NW) array electrode configuration with advantageous features at both the individual materials unit scale and the materials ensemble scale, designated in the schematic. (b) Schematic of the fabrication process of a t-Si@G NW array, consisting of (I) chemical etching of a Si wafer to synthesize perforated silicon nanowire array, (II) graphitic carbon coating to create the t-Si@G NW array, and (III) delaminating the t-Si@G NW array from the silicon wafer. (c–e) Photographs showing (c) perforated silicon nanowire array on the wafer, (d) t-Si@G NW array on the wafer, and (e) free-standing t-Si@G NW array, respectively. In this study, commercial Si wafers with 2 in. diameter are used.

well-ordered perforated Si nanowires are conformally coated with the graphitic carbon sheets (G) and interconnected through an underlying hinging layer, thus forming a mechanically robust, free-standing textured silicon@graphitic carbon nanowire (namely, t-Si@G NW) array. Such a unique electrode structure has been designed simultaneously at the individual materials unit scale (perforated Si nanowires and graphitic carbon coating) and the materials ensemble scale (ordered nanowire array and satisfactory void space of the whole electrode), namely, based on a nanoscale system engineering strategy, as discussed in greater detail below. As a result, the resultant t-Si@G NW array electrode exhibits unprecedented lithium storage performances, especially in terms of volumetric capacity. To the best of our knowledge, this is the first time that a binder-free silicon-based lithium ion battery anode with both high gravimetric capacity and high volumetric capacity has been designed and exploited from the viewpoint of both materials unit and whole electrode (materials ensemble).

The performance of designed t-Si@G NW array electrodes can be attributed to harmonious integration of several distinct advantages via the nanoscale system engineering formula. First, at the materials ensemble scale the ordered one-dimensional (1D) nanowire array allows for a substantially high tap density of Si. The concept of using an ordered 1D nanostructure array to maximize the tap density of active materials has been demonstrated with carbon,[38] silicon,[39,40] and others. Besides, the ordered 1D nanowire arrays reduce tortuosity in electronic and ionic transport and hence improve the rate capability, consistent with previous studies on other ordered 1D

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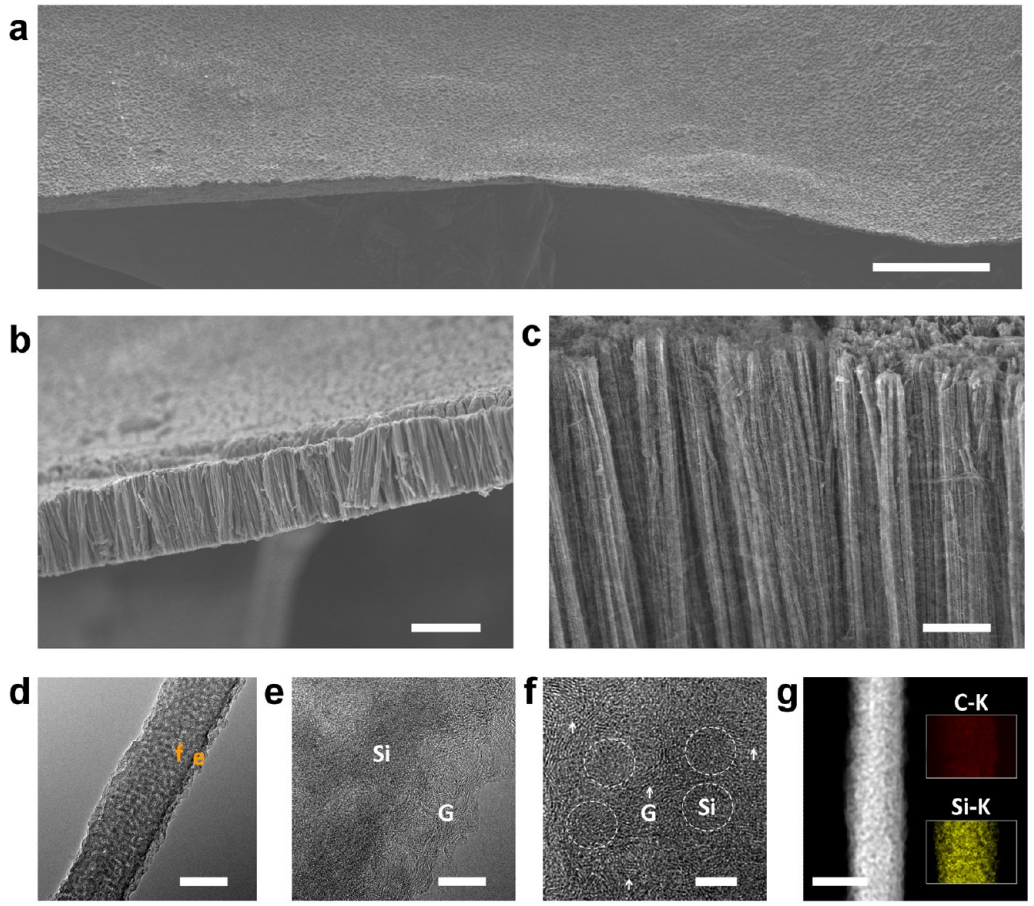

Figure 2. Microstructure of t-Si@G NW arrays. (a–c) SEM images of a t-Si@G NW array. (a) Scale bars, 200 μm. (b) Scale bar, 10 μm. (c) Scale bar, 2 μm. (d) TEM image of an individual t-Si@G NW. Scale bar, 100 nm. (e,f) High-magnification TEM images of the areas labeled in (d). Arrows in (f) indicate graphitic carbon sheets while the circles show crystal silicon as the pore wall. (e) Scale bar, 10 nm. (f) Scale bar, 5 nm. (g) Carbon and silicon elemental mapping of a selected area of an individual t-Si@G NW. Scale bar, 100 nm.

nanostructure arrays.[41−44] Second, the void space, being incorporated uniformly within the whole array to accommodate the volume change of Si, is gauged to be around two times the Si volume, so as to avoid the failure of the electrode structure and cell configuration due to the inherent volume expansion of Si, as well as to avert the excessive incorporation of the void space at the cost of compromising the tap density of Si. At the individual materials unit scale, the importance of managing the void space has been highlighted in previous materials design strategies, for example, for the second phase-encapsulated void-involved Si electrode materials.[5,45,46] Third, at the individual materials unit scale, each perforated Si nanowire is composed of interconnected pore walls with an average thickness of ∼8 nm, which facilitates strain relaxation and enhances tolerance to the volume change of Si, thereby ensuring the structural integrity of materials units upon cycling. This is in agreement with recent studies that have suggested a critical size (∼10 nm) with which the silicon is structurally stable in terms of exhibiting the optimal electrochemical performance.[16,17,23,25] Fourth, the graphitic carbon coating mimics the modality of Si completely, thus improving the Si interface with the electrolyte. In addition, the graphitic carbon inside and outside the Si nanowires is interconnected by an underlying hinging layer, thus affording efficient pathways to promote lateral electron transport from/to each nanowire. More importantly, such a thin carbon coating enables the construction and direct utilization of free-standing t-Si@G nanowire arrays without the addition of any other additives or substances. This scenario is quite different from previous studies on binder/conductive additive-involved,[13,47] polymer-impregnated,[40] and/or metallic collector-embedded Si anodes,[42,43] in which the substantial need of extra substances really dilutes the lithium storage performance in terms of both volumetric capacity and gravimetric capacity because the total electrode weight and volume must be considered from a practical point of view.

The fabrication of such a proof-of-concept electrode prototype was realized by (I) synthesizing perforated silicon nanowire (Si NW) arrays by metal-assisted chemical etching of silicon wafers,[48] (II) depositing graphitic carbon sheets through in situ decomposition of methane, and (III) delaminating the resultant silicon/carbon hybrid membrane by hot sodium hydroxide (NaOH) treatment (Figure 1b). As displayed in Figure 1c–e, the fabrication method is applicable to full-size Si wafers (2 in. diameter in this study), which can be easily scaled up to industrial production only depending on the size of the used Si wafers. More strikingly, the resultant membranes are mechanically robust and free-standing, allowing for their direct utilization as lithium ion battery electrodes without any auxiliary components.

Figure 2 shows the morphology and structure of as-produced t-Si@G NW array membranes. Typically, the thus-produced hybrid membrane comprises a nanowire array interconnected with an underlying thin layer as a hanging base (Figures 1b, 2b, and Supporting Information Figure S1). The presence of such a

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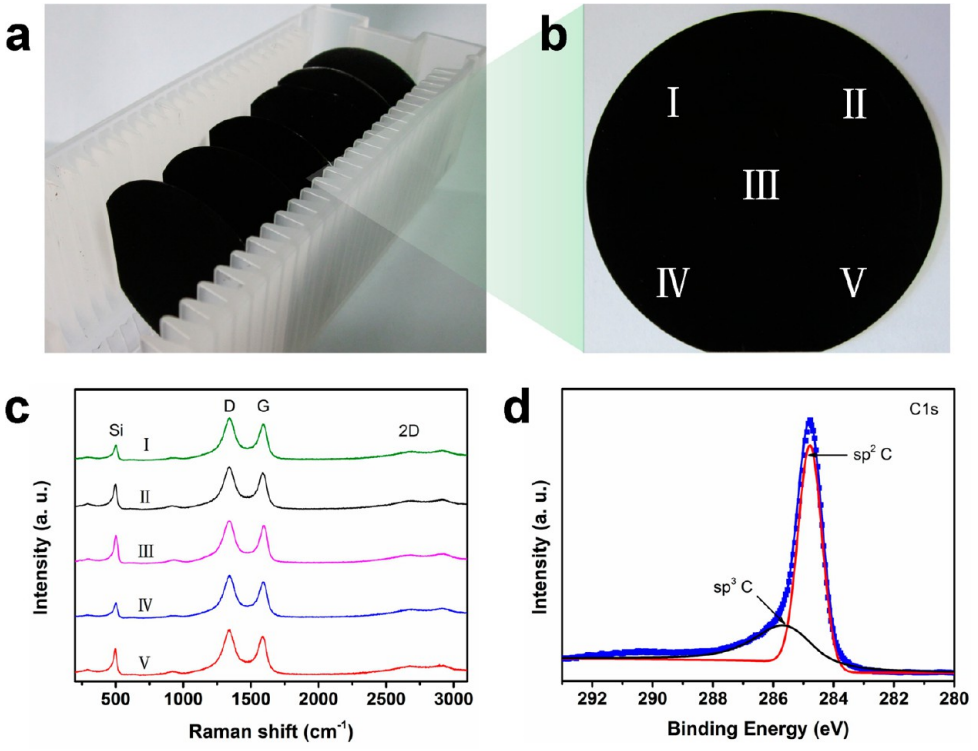

Figure 3. Uniformity and component analysis of t-Si@G NW arrays. (a,b) Photographs of (a) a box of 2 in. diameter Si wafers with t-Si@G NW arrays and (b) a single Si wafer with t-Si@G NW array. (c) Raman spectra of t-Si@G NW array collected from different positions as labeled in (b), indicating the uniformity over the whole array. (d) Typical C1s XPS spectrum of t-Si@G NW array.

hanging layer is suggested to be vital for maintaining the mechanical robustness and electrical connectivity of the membrane. As exhibited in Figure 2b,c, the nanowires in the membrane are well aligned and densely packed with an average diameter of ∼150 nm and a typical length (and consequent membrane thickness) of ∼10 μm. It is noteworthy that the membrane thickness is mainly dependent on the length of pristine silicon nanowires and thus can be facilely tuned by adjusting the etching duration for Si wafers (Supporting Information Figure S2). Notably, both scanning electron microscopy (SEM) and transmission electron microscopy (TEM) images (Figure 2c,d) show a highly porous structure of the nanowires. The high-magnification TEM images (Figure 2e,f) further reveals that each nanowire in the hybrid membrane, consisting of interconnected pore walls with an average thickness of ∼8 nm, is intimately coated with very thin graphitic carbon sheets (average thickness: less than 3 nm) from the outer surface to the pores. That is, the introduced G coating replicates the modality of pristine perforated silicon nanowires (Supporting Information Figure S3), thereby forming a well-textured Si@G nanowire structure. The elemental mapping images (Figure 2g) further disclose that this special silicon/carbon texturing is highly uniform along the nanowire length. After a prolonged hot sodium hydroxide treatment (5% NaOH, 20 h) to remove silicon completely, the TEM characterization shows that the resultant nanowires are composed of numerous randomly arranged, highly curled graphitic carbon sheets (Supporting Information Figure S4), confirming that the introduced graphitic carbon mimics the modality of perforated silicon nanowires perfectly. It should be mentioned that the content of G is determined to be around 10 wt % by measuring the weight change after depositing the graphitic carbon. Furthermore, by optimizing the etching protocol for perforated silicon nanowires, deposition condition for the graphitic carbon, and delamination process for the hybrid membrane, the typical tap density of Si relative to the membrane volume can be 0.8−0.9 g cm^{-3} in this study, which renders the total free void space involved in the membrane with approximately two times the original volume of Si considering that the introduced graphitic carbon occupies a negligible portion (∼5%) given its density similar to that of graphite. Overall, the fabrication approach has enabled the simple and scalable production of well-textured Si@G nanowire array membranes from commercial silicon wafers, rather than via complicated and energy-consuming apparatuses and/or complex and costly synthesis processes.

The uniformity of membrane electrodes is critically important for their direct use in lithium ion batteries. In this regard, different batches of t-Si@G NW arrays were randomly characterized by Raman spectroscopy, X-ray photoelectron spectroscopy (XPS), and powder X-ray diffraction (XRD) (Figure 3). Typically, we picked up five positions for each membrane array to perform the above-mentioned measurements (Figure 3b, I−V). As exhibited in Figure 3c, Raman spectra are nearly the same for all the measured positions, suggesting a very high degree of uniformity throughout the whole array (2 in. diameter in this work). As the peak appearing at ca. 500 cm^{-1} originates from silicon, two peaks at ∼1360 and ∼1580 cm^{-1} correspond to the disordered band (D band) and the graphitic band (G band) from the graphitic carbon sheets, respectively. The ratio of the D band to the G band is estimated to be around 1.05 in all cases, which is mainly associated with the defects and partially disordered structures of the graphitic carbon sheets.[49] This result is consistent with XPS analyses as well (Figure 3d). While the dominant peak at ca. 284.7 eV corresponds to sp^2 C in the graphitic carbon sheets, a small

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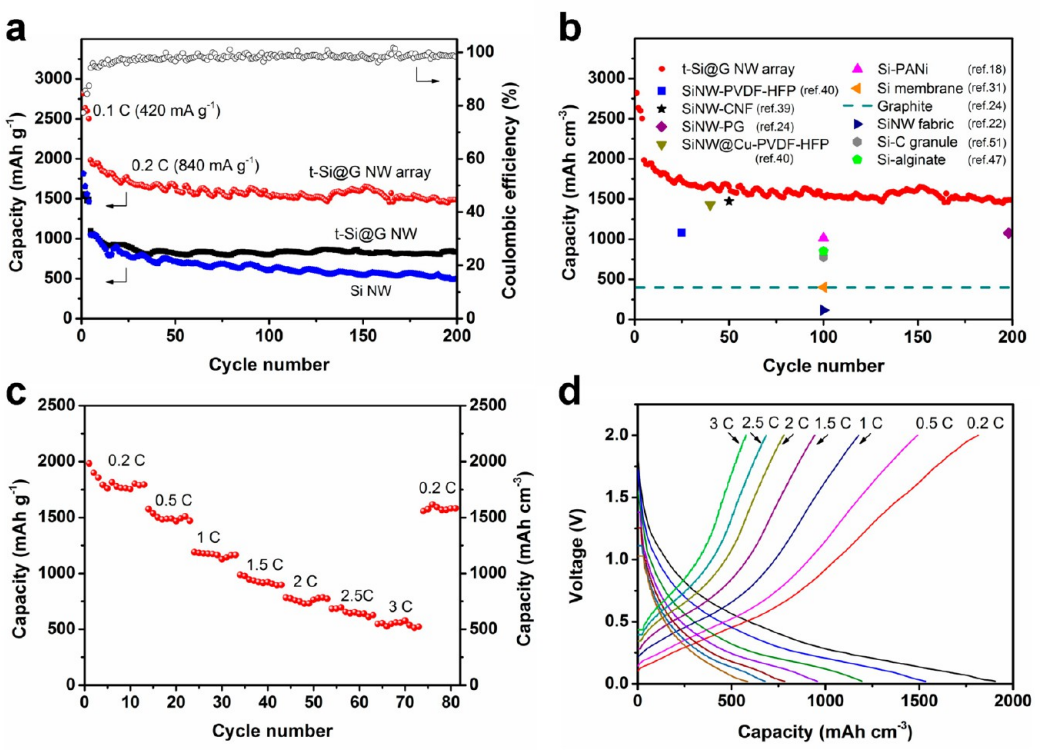

Figure 4. Electrochemical performance of t-Si@G NW arrays. (a) Electrochemical cycling performance and Coulombic efficiency of the t-Si@G NW array electrodes under charge/discharge cycles from 2 to 0.02 V. Cycling performances of control electrodes (Si NW and t-Si@G NW) are compared in the figure. (b) Volumetric capacities versus cycle number of the t-Si@G NW array electrode. The achieved capacity values at the highest cycle number reported for graphite and some representative Si-based electrodes are also superimposed for comparison. A detailed comparison is tabulated in Supporting Information Table S1. (c) Reversible capacity and (d) voltage profiles of the t-Si@G NW array electrode cycled at various current rates from 0.2 to 3 C. All the capacities reported are on the basis of the whole electrode.

peak at ca. 285.6 eV, assignable to sp^3 C, can originate from defects of the graphitic carbon sheets. Furthermore, the XRD results (Supporting Information Figure S5) show that perforated silicon nanowires retain a crystal structure after experiencing the graphitic carbon coating process, consistent with those reported elsewhere.[25]

Two-electrode coin-type cells (2032) with metallic lithium counter electrodes were used to evaluate the electrochemical performance of the electrode comprising a t-Si@G NW array, as well as two polyvinylidene fluoride (PVDF)-enabled control electrodes (Si NW and t-Si@G NW, see Methods in Supporting Information). One molar $LiPF_6$ in 1:1 (v/v) ethylene carbonate/diethyl carbonate (EC/DEC) was used as the electrolyte. In the t-Si@G NW array electrode (typically, 10 μm thick), the mass loading and mass fraction of Si were ~0.9 mg cm^{-2} and 90%, respectively. For balancing the specific capacity and capacity retention, in all control electrodes the mass loading and mass fraction of silicon were reduced to be around 0.15 mg cm^{-2} and 60%, respectively, both of which are yet among the ranges widely used for existing silicon anode materials.[5,18,23,45] Unless otherwise noted, the specific capacity values reported were calculated on the basis of the total weight of the electrodes. Figure 4a shows the cycling performance of these electrodes at 0.1 C (420 mA g^{-1}) for initial four cycles and then 0.2 C (840 mA g^{-1}) for subsequent 200 cycles. It can be observed that the Si NW control electrode exhibits gradual capacity fading and bears a specific capacity of ~500 mAh g^{-1} after 200 cycles. In comparison, the cycling stability of the t-Si@G NW control electrode is significantly enhanced and exhibits an increased capacity of ~800 mAh g^{-1} at the end of 200 cycles. The excellent cycling stability can be mainly ascribed to the high structural stability of Si ensured by harnessing perforated silicon nanowires to facilitate strain relaxation,[23,25] as well as the improved electrical conductivity and Si interface enabled by the graphitic carbon coating mimicking the modality of Si. Herein, it should be mentioned that the optimization of binders can be an alternative approach to significantly improving the cycling stability of the electrode.[47] This tactic has been demonstrated recently by Zhou et al.[23] to improve the performance of perforated silicon nanowires at a mass loading of silicon (0.3 mg cm^{-2}) similar to that of the Si NW control electrode. Interestingly, the greatly enhanced cycling stability can be readily achieved for the electrode composed of a t-Si@G NW array, even at a much higher loading level and without any binders. The marked difference is that the stable specific capacity of the t-Si@G NW array is observed to be very high at 1500 mAh g^{-1}, being nearly two times that of the t-Si@G NW control electrode and four times that of commercial graphite anodes.[50] We believe that high specific capacity and outstanding cycling stability of the t-Si@G NW array mainly stem from its designed architecture as discussed before, which allows for the exertion of each counted t-Si@G NW as the lithium storage materials unit even at a relatively high mass loading and mass fraction of Si. It should be noted that the Coulombic efficiency is relatively low in the first four cycles (78% for the first cycle, Supporting Information Figure S6), which can be related to the SEI formation especially around some defects, pinholes, and/or imperfections in the graphitic carbon sheets. After that, nevertheless, the Coulombic

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efficiency can rapidly increase and stabilize at around 99% in subsequent cycles.

The volumetric capacity is another critically important concern for commercialization of Si anodes, dependent in large part on the tap density of active materials. For our t-Si@G NW array, the electrode architecture affords high specific capacity on the basis of the total electrode weight by promoting the electrochemical utilization of every individual materials unit (t-Si@G NW) during cycling, and the tap density of Si (~0.9 g cm^{-3}) reaches a maximum acceptable value with a small variation being attributed to the processing variations and measurement errors. Thus, the volumetric capacity is expected to be competitive. Figure 4b displays the volumetric capacity of the t-Si@G NW array derived from its specific capacity shown in Figure 4a (see Methods in Supporting Information), which is superimposed with some available representative results of the existing Si-based and commercial graphite electrodes for comparison. It can be seen that the volumetric capacity remains a quite high value of ~1500 mAh cm^{-3} after 200 cycles, which is nearly four times that of the commercial graphite anodes.[24] Notably, the achieved volumetric capacity and capacity retention is also comparable to or even better than the best results for the previously reported Si-based electrodes,[18,22,24,31,39,40,47,51] which is further detailed in Supporting Information Table S1. We note that there is still large room for increasing the capacity values of the t-Si@G NW array, for example, by optimizing the array structure further and engineering the test conditions elaborately (e.g., addition of electrolyte additives and control of cutoff voltages).[13]

In addition, the graphitic carbon inside and outside of each perforated silicon nanowire, which is interconnected by an underlying hanging layer, provides channels for fast electron transport and consequently, the t-Si@G NW array should afford excellent rate capability. Figure 4c shows specific and volumetric capacities of the t-Si@G NW array versus cycle number at different charge/discharge rates ranging from 0.2 to 3 C (12.6 A g^{-1}). Notably, even at a high current rate of above 10 A g^{-1}, the volumetric capacity of more than 500 mAh cm^{-3} is delivered, which is still much higher than that of commercial graphite anodes.[24] As exhibited in Figure 4d, at different charge/discharge current rates the voltage profiles are similar and in good agreement with the behavior of amorphous silicon,[45] which is also verified by cyclic voltammetry (Supporting Information Figure S7). Clearly, lithium ions can rapidly reach the Si active material even at high charge/discharge rates, reflecting the effectiveness of the t-Si@G NW array electrode in promoting ionic transport and diffusion. This is also the case for t-Si@G NW array electrodes with various thicknesses ranging from 7 to 20 μm (Supporting Information Figure S8).

The ultimate principle of engineering electrode materials is to boost the lithium storage performance of materials without compromising other components of a cell and consequent battery pack/module. Since an acceptable degree of volume change for a commercialized lithium ion battery electrode is about 10%,[52,53] the volume variation of a viable Si electrode itself must be controlled as far below this limit. In view of this consideration, we further dissembled and characterized our electrodes after cycling (Supporting Information Figures S9–S11). As shown in Supporting Information Figure S9, the cycled t-Si@G NW array maintains an integrated membrane structure and the array height (that is, electrode thickness) remains almost the same as the initial one (~10 μm). From the viewpoint of the whole electrode, the built-in void space, involving voids between nanowires and the pores inside nanowires, is around two times the initial Si volume and hence allows for better accommodation of the volume change of Si, thus offering an explanation for the maintenance of the electrode thickness observed. Notably, this scenario enabled by the nanoscale system engineering is in stark contrast to the t-Si@G NW control electrode that shows increased thickness by 2.8 times after 100 cycles (Supporting Information Figure S10), as well as other traditional slurry-involved Si electrode geometries that have recently been observed to commonly suffer from a significant electrode thickness increase upon cycling (up to more than 160%) even with the materials nanostructuring and surface-engineering.[24,54] Moreover, the modality of individual t-Si@G nanowires remains even after 200 cycles as confirmed by TEM and elemental mapping images (Supporting Information Figure S11), which reflects the structural and interfacial stability of the designed material unit, contributing to the exceptional lithium storage performance achieved.

In conclusion, we have designed and developed a t-Si@G NW array electrode to strike a balance between maximizing the Si tap density and incorporating the satisfactory void space, while addressing the structural and interfacial instability issues of Si. On the basis of the nanoscale system engineering formula, we have demonstrated its direct use as a high-performance anode with high volumetric capacity on the basis of the whole electrode, competing rate capability, and excellent cycling stability (e.g., 1500 mAh cm^{-3} after 200 cycles). These performance parameters are achieved without the expense of disturbing other components of the battery, attributing to the incorporation of an indispensible void space at the whole electrode scale. Coupled with a simple and scalable production protocol, the electrode architecture developed represents a significant advance in developing Si-based electrodes practically applicable to next-generation lithium ion batteries. More importantly, the nanoscale system engineering formula highlighted could also be extended to other emerging high-capacity anode and cathode materials that undergo large volume expansion.

■ ASSOCIATED CONTENT

Supporting Information

Additional information for detailed synthesis and characterization of t-Si@G NW arrays and control samples and Figures S1–S11. This material is available free of charge via the Internet at http://pubs.acs.org.

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Notes

The authors declare no competing financial interest.

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