

Gate-Defined Confinement in Bilayer Graphene-Hexagonal Boron Nitride Hybrid Devices

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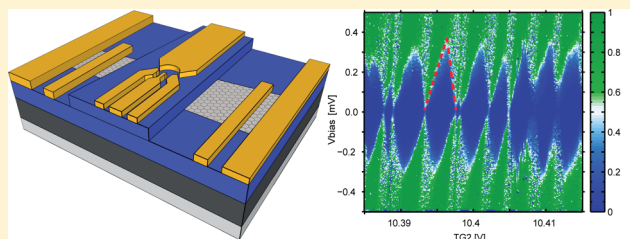
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S Supporting Information

ABSTRACT: We report on the fabrication and measurement of nanoscale devices that permit electrostatic confinement in bilayer graphene on a substrate. The graphene bilayer is sandwiched between hexagonal boron nitride bottom and top gate dielectrics. Top gates are patterned such that constrictions and islands can be electrostatically induced. The high quality of the devices becomes apparent from the smooth pinch-off characteristics of the constrictions at low temperature with features indicative of conductance quantization. The islands exhibit clear Coulomb blockade and single-electron transport.

KEYWORDS: Graphene, bilayer graphene, hexagonal boron nitride, confinement, coulomb blockade, quantized conductance



Confinement of charge carriers in graphene has been heavily investigated since graphene flakes on a substrate were first measured.^{1,2} Nanopatterning graphene into nanoribbons or small islands has been a widely used strategy for both zero- and one-dimensional confinement.^{3–7} Unfortunately, as a result of the etching process that is used for nanopatterning, the edges of the devices are very rough. This edge disorder, aggravated by substrate-induced disorder, leads to rather irregular device behavior. For instance, no quantized conductance was observed in etched constrictions, the transparency of barriers varied nonmonotonously with gate voltage, no atom-like shell-filling has been observed in quantum dots, and in many cases quantum dots fell apart into multiple islands.

Last year, suspended single layer graphene sheets narrowed by current induced heating showed quantized steps in conductance of $2e^2/h$ as the Fermi wavelength was varied.⁸ Presumably, these constrictions were not only narrow but also short, as observed in recent transmission electron microscope measurements,⁹ reducing the effects of edge disorder. However, the formation of these constrictions is hard to control, making it difficult to reproduce these results. Clean ribbon edges can be obtained reproducibly by unzipping carbon nanotubes, and a well-behaved quantum dot formed in such a nanoribbon was recently reported.¹⁰ Barriers were formed at metal Schottky contacts, but such barriers are not tunable, limiting follow-up work. Moreover, as the ribbons are not obtained lithographically but are dispersed from solution, they face many of the limitations of the carbon nanotube they originate from.

The ideal device would confine charge carriers in the bulk, far from (disordered) edges, have well-controlled tunnel barriers, and enjoy all the design freedom offered by lithography. All these requirements can be satisfied using patterned electrostatic gates,

provided a band gap is present. This calls for the use of bilayer graphene¹¹ rather than monolayer graphene, as in bilayers a band gap can be induced by an electric field perpendicular to the layers.^{12–14} An additional requirement for clean confinement is to minimize substrate-induced disorder. Substrate disorder can be eliminated in suspended devices with suspended top gates, as shown in recent work by Allen et al.¹⁵ However, it would be highly desirable to realize devices of comparable quality on a substrate, as this would facilitate integration of complex devices. Currently the cleanest gate dielectric available for graphene devices is hexagonal boron nitride (hBN), and mobilities reported on such substrates approach those of suspended devices.¹⁶

Here we report on the first realization of electrostatic confinement devices in bilayer graphene on a substrate. The bilayer graphene is encapsulated in hBN top and bottom dielectrics via successive transfer steps. The devices have split top gates and a global back gate, which we bias so that a gap is opened in the graphene bilayer. The Fermi level is tuned inside the gap in the regions below the top gates so that they become insulating. We demonstrate the potential of this new device platform by confining charge carriers in one-dimensional (1D) channels and zero-dimensional islands.

A schematic and atomic force microscopy (AFM) image of a device is shown in Figure 1. We first deposit a 14 nm thick hBN flake by mechanical exfoliation on a silicon wafer coated with a silicon oxide (SiO_2) layer of thickness $t_{\text{SiO}_2} = 285$ nm. On top of

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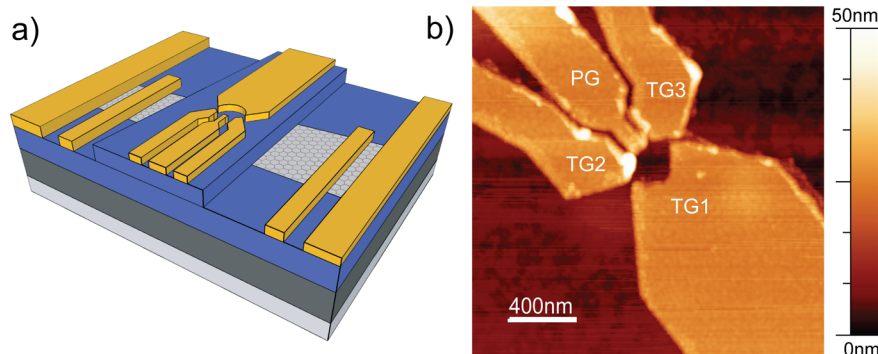


Figure 1. (a) Schematic layout of the sample. The light gray area indicates the heavily p-doped silicon wafer, dark gray shows the SiO₂ backgate dielectric, blue indicates the hBN dielectrics, and yellow shows Cr/Au electrodes and gates. In the actual sample, several top gate structures are present in between the contacts. (b) AFM height image of device A with labeled top gates. Note that the plunger gate (PG) was not connected for device A.

the hBN, we transfer a bilayer graphene flake ($\sim 22 \mu\text{m}$ long and $\sim 3 \mu\text{m}$ wide, its bilayer nature was confirmed by Raman spectroscopy) using a dry transfer method following the protocol of ref 16 (at a temperature of 100°C to remove any water absorbed on the surface of the graphene and hBN flakes). The sample was subsequently annealed in an oven at 400 and 450°C (Ar 2400 sccm, H₂ 700 sccm) to remove residues induced by the transfer process. Cr (5 nm)/Au (95 nm) electrodes are fabricated using electron-beam lithography (EBL). We annealed the samples again (same flow rate as the first annealing step, $T = 300, 350$, and 440°C) to remove fabrication residues. This did not give the desired sample quality. Hence we applied the recently developed mechanical cleaning technique¹⁷ followed by dry transfer of a 50 nm thick hBN flake partly covering the bilayer graphene flake. This hBN flake will act as top gate dielectric. In a two-step EBL process, we deposited Cr/Au top gates. We defined several gate patterns between the contacts on this flake and report here on two “quantum dot” top gate structures, one with a lithographic diameter of 320 nm (device A) and one of 250 nm (device B). The separation between the top gates that together define a barrier is less than 30 nm. For device B, TG1 and TG2 were unintentionally connected.

This specific graphene sample was cooled down multiple times. The maximum field effect mobility measured at $T = 35 \text{ mK}$ was $\sim 36\,000 \text{ cm}^2/(\text{V s})$ (four-terminal configuration; both covered and uncovered graphene are in between the voltage probes, see Supporting Information Figure 1, so the measured mobility averages over both as well). The field-effect mobility measured during the last cool-down was much lower ($\sim 6000 \text{ cm}^2/(\text{V s})$, two-terminal configuration). Presumably, this degradation of electronic quality was caused by deposition of amorphous carbon on the uncovered graphene induced by exposure to an electron beam during imaging in a scanning electron microscope. Nevertheless, we expect that the graphene sandwiched in hBN retained high mobility.

We set the back gate to a large negative voltage and tune the top gate to a voltage that compensates for the doping induced by the back gate. For typical values $V_{\text{BG}} = -50 \text{ V}$ and $V_{\text{TG}} = 9 \text{ V}$, the displacement field is $D \sim 0.6 \text{ V/nm}$, which translates into a theoretically predicted band gap of $\sim 50 \text{ meV}$.^{12,18,19} As in earlier work, the transport gap is substantially smaller^{13,20} but still large enough to realize quantum confinement, as we will see.

In Figure 2a, we show a top gate trace at a large negative back gate voltage, taken at low temperature. Clearly visible is a region of suppressed conductance with a minimum conductance of the order of a conductance quantum. The fact that conduction is not

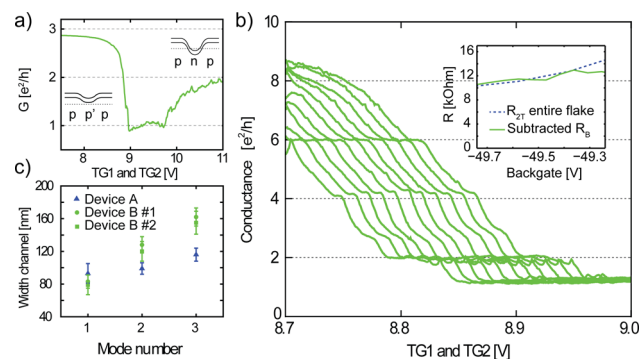


Figure 2. (a) Conductance (G) versus the voltage on TG1 and TG2 (device B, $T = 35 \text{ mK}$, $V_{\text{bias}} = 0.5 \text{ mV}$, $V_{\text{BG}} = -49.74 \text{ V}$). The other top gates of the device are set to 5 V , far from pinch-off, so that we are dealing with only one constriction. All measurements presented in this paper are conducted in two-terminal DC voltage bias configuration. The conductance has been corrected for filter resistance and current amplifier input resistance. In the inset, we show cartoons of the bandstructure for pp'p and pnp measurement regimes. Solid lines indicate valence and conduction band edges and dashed line the position of the Fermi level. (b) Top gate traces for device B at back gate voltages from -49.26 V (leftmost) to -49.74 V (rightmost) in 10 equal steps ($V_{\text{bias}} = 0.5 \text{ mV}$, $T = 35 \text{ mK}$). The solid green line in the inset is the subtracted R_b . The dashed blue line is the two-terminal resistance of the graphene flake with all top gates at ground. (c) Channel width W_n for modes $n = 1, 2$, and 3 for device A (blue triangles) and for two measurements on device B (green circles and squares). The widths are calculated in the square-well potential approximation $W = (n/2)\lambda_F$. The Fermi wavelength at the n -th plateau is estimated via $\lambda_F = (2\pi)/(\pi C_{\text{TG}} \Delta V_{\text{TG},n}/e)^{1/2}$. C_{TG} is the top gate capacitance per unit area, extracted from the slope of the position of the $\nu = 4$ plateau in top gate voltage against magnetic field (Figure 3b). $\Delta V_{\text{TG},n}$ is the difference between the top gate voltage in the middle of the n -th plateau and the top gate voltage at charge neutrality.

fully pinched off seems reasonable given the small induced band gap and the small dimensions of the gates near the constriction. Importantly, the top gate trace shows a remarkably clean transition region on the hole side. A somewhat less clean transition and lower conductance is seen on the electron side. This asymmetry can be expected since the leads are p-doped by the backgate, and a pnp-junction is formed on the electron side. The pnp-junction decreases the transparency of the device as the charge carriers have to Zener tunnel through the induced band gap. On the hole side, the conductance suppression with top gate voltage is very smooth and well behaved. This is in strong contrast to similar top gate sweeps for graphene nanoribbons,

which exhibit very irregular pinch-off characteristics when the Fermi energy is swept into the transport gap.^{4,5,7}

Zooming in on the steep flank of the pinch-off curve, we observe several plateaus in conductance, with a value that is independent of V_{BG} (Figure 2b). The traces have been corrected for filter resistance, current amplifier input resistance, and for a background resistance (R_B) consisting of contact resistance, Maxwell spreading resistance²¹ and graphene lead resistance. The background resistance is slightly dependent on back gate voltage. In Figure 2b, for each value of V_{BG} we subtracted a value of R_B comparable to the two-terminal resistance (R_{2T}) of the graphene flake with all top gates at ground (see inset), fine-tuning R_B such that the conductance G at the upper plateau is $6e^2/h$ (other possible assignments are discussed in the Supporting Information).²² The other two plateaus consequently appear at $G = 4e^2/h$ and $G = 2e^2/h$. The same sequence of steps was observed for device A (see the Supporting Information Figure 2b). In device B, a less well-developed feature can be seen just below $G = 3e^2/h$, which does not appear in device A. This feature suggests that despite the encapsulation in hBN and the overall cleanliness of the pinch-off characteristics, there is some residual disorder. This analysis of the data suggests transport through 2-fold degenerate one-dimensional ballistic channels and the formation of a quantum point contact.^{23,24}

The $2e^2/h$ steps in conductance, also reported in ref 15 are surprising given that there is both spin and valley degeneracy in bulk bilayer graphene, which would give $4e^2/h$ steps. What mechanism lifts the degeneracy is an open question that calls for further exploration. Increasing the temperature to 440 mK did not change the general behavior. Lowering the bias to 50 μV (lock-in measurement with an AC excitation of 10 μV) did not change the appearance of the plateaus either. Both a larger bias and a higher temperature smoothened out aperiodic conductance fluctuations, as can be expected.

We can estimate the width of the constriction from the position of the plateaus in top gate voltage with respect to the conductance minimum (Figure 2c). We see that as subbands become occupied, the width of the constriction increases from $W_1 \sim 90$ nm to $W_3 \sim 120$ nm for device A and from $W_1 \sim 80$ to $W_3 \sim 160$ nm for device B, which is characteristic of a smooth confining potential (with W_n the constriction width for the n -th subband). The lithographically defined separation between the respective top gates was less than 30 nm for both devices. This implies that the channel extends below the top gates, which can be expected given the modest band gap induced underneath.

In Figure 3a, we explore the influence of a perpendicular magnetic field on the 1D channels (device B). In the low-field regime, the plateau at $6e^2/h$ quickly disappears, but the plateaus at $4e^2/h$ and $2e^2/h$ remain visible. At large fields, pronounced plateaus in conductance develop at $4e^2/h$ ($\nu = 4$) and $8e^2/h$ ($\nu = 8$), typical values for the quantum Hall effect in bilayer graphene.²⁵ This transition from size confinement to magnetic confinement occurs when the cyclotron radius (r_c) is equal to or smaller than $W_n/2$.²⁶ By extrapolating the positions of the plateaus for $n = 2$ and $\nu = 4$, we can determine a crossover magnetic field of 0.9 ± 0.2 T and estimate the size of the constriction based on r_c (Figure 3b). This gives $W_2 = 76 \pm 18$ nm. The agreement with the estimate based on the plateau positions (~ 120 nm) is better than a factor two.

When we induce two barriers by appropriate gate voltages, the device behavior changes drastically. Figure 4a shows a gate voltage scan of TG2 while TG1 and TG3 are also biased (device A). We see sharp conductance peaks separated by

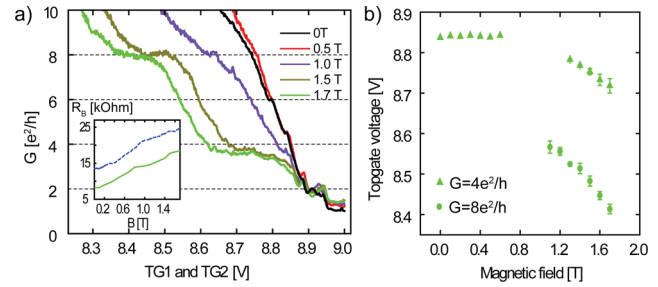


Figure 3. (a) Conductance versus TG1 and TG2 voltage for device B at different magnetic fields (see legend, $T = 440$ mK, $V_{bias} = 150$ μV , $V_{BG} = -49.74$ V, V_{PG} and $V_{TG3} = 5$ V). The inset shows as a function of magnetic field the background resistances that we subtracted (solid green line) and the two-terminal resistance with all top gates at ground (dashed blue line, measured at $V_{bias} = 500$ μV). In the low-field regime, the background resistance was determined by aligning the plateaus near $G = 4e^2/h$ and in the high-field regime by aligning the plateaus near $G = 8e^2/h$ (b) Extracted top gate voltages at the plateau centers versus magnetic field. By fitting a linear curve to the large field data we obtain $C_{TG1\&2} = [(4e^2/h)/h][(dB)/(dV_{TG,\nu=4})] \sim 1.04$ F/m². The value for $C_{TG1\&2}$ extracted from the $\nu = 8$ data is very similar.

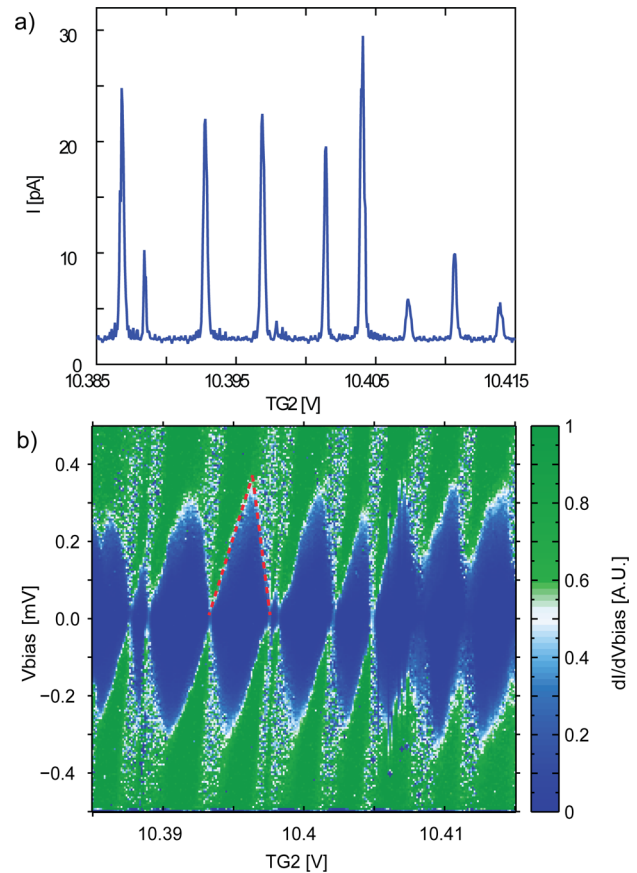


Figure 4. (a) Current versus the voltage on TG2 (device A, $V_{TG1} = V_{TG3} = 10.1546$ V, $V_{BG} = -49.5$ V and $V_{bias} = 50$ μV). (b) Differential conductance plotted in color scale versus gate voltage and source-drain bias (device A, $V_{TG1} = V_{TG3} = 10.1546$ V, $V_{BG} = -49.5$ V). The red dashed lines indicate the outline of a diamond as used for the analysis of the capacitances. The tiny diamond in the middle is not included in the analysis.

regions of strongly suppressed conductance, which is characteristic of Coulomb blockade.²⁷ As expected for Coulomb peaks, their position on one gate voltage axis varies smoothly (linearly)

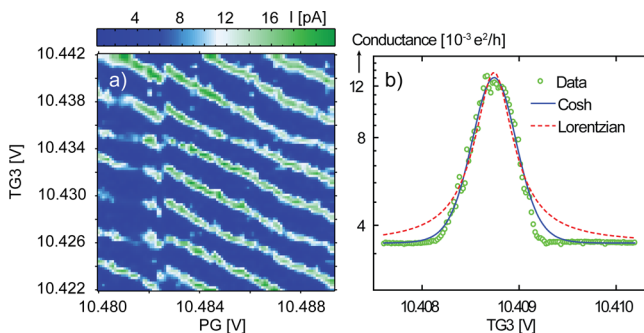


Figure 5. (a) Current plotted in color scale versus the voltage applied to PG and TG3 (device B, $V_{\text{TG1\&2}} = 10.2548$ V, $V_{\text{BG}} = -49.38$ V and $V_{\text{bias}} = 50$ μ V). Occasionally shifts occur such as the one at $V_{\text{PG}} \sim 10.4825$ V, which we attribute to a rearrangement of background charges in the substrate. (b) Zoom-in on a conductance peak plotted on a logarithmic scale along with fits by a Lorentzian and hyperbolic cosine function (device B, $V_{\text{TG1\&2}} = 10.1907$ V, $V_{\text{PG}} = 10.3880$ V, $V_{\text{BG}} = -49.86$ V and $V_{\text{bias}} = 50$ μ V). Fit formulas are $G \propto \cosh^{-2}[\alpha(V_{\text{TG}} - V_{\text{TG,offset}})/(2.5kT)]$ where $\alpha = (2E_{\text{C}})/(\Delta V_{\text{TG}})$ (the factor 2.5 assumes temperature exceeds level spacing) and $G \propto \Gamma/[(\alpha(V_{\text{TG}} - V_{\text{TG,offset}})/\hbar)^2 + (\Gamma/2)^2]$, where Γ is the coupling strength to the leads.

when another gate voltage is swept (Figure 5a). We note that the resistance in Coulomb blockade is orders of magnitude larger than the sum of the two barrier resistances, which saturates around h/e^2 (Figure 2), indicating each gate couples to both barriers. Coulomb blockade is confirmed further by the diamond-shaped regions of suppressed conductance seen in a color plot of conductance versus gate voltage and bias voltage (Figure 4b).

The Coulomb peak spacing exhibits a standard deviation of 1.4 mV, compared to an average peak spacing of 4 mV (device B). In principle, irregular peak spacings can originate from quantized level spacing contributions.²⁷ However, no excited state features are visible in the Coulomb diamonds so it is not clear that level spacing is responsible for the peak spacing variation. Instead the reason may be the breakdown of the constant-interaction model, for instance, due to disorder-induced variations in the island size or position as charge carriers are added one by one, or a second island capacitively coupled to the main island.

From the Coulomb diamonds and peak spacing, we can obtain information on the dimensions and location of the island. For the data set of Figure 4b (device A), the addition energy E_{add} is 0.35 ± 0.02 meV. When we neglect orbital energies, $E_{\text{add}} = 2E_{\text{C}}$, where E_{C} is the charging energy. Using $E_{\text{C}} = e^2/(2C_{\Sigma})$, we can calculate the total capacitance of the dot, $C_{\Sigma} = 0.46 \pm 0.03$ fF. From the slope of the Coulomb diamond edges, we find that C_{Σ} is dominated by the source and drain capacitances ($C_{\text{s}} = 0.10 \pm 0.024$ fF, $C_{\text{d}} = 0.30 \pm 0.033$ fF), which makes it difficult to estimate the island size from E_{add} and C_{Σ} .

Instead, we compare the measured top gate capacitances with top gate capacitances simulated using a 3D Poisson equation solver (Ansoft Maxwell). From the average Coulomb peak spacing ΔV_{TG2} , we extract a capacitance $C_{\text{TG2}} \sim 45$ aF. C_{TG3} , C_{TG1} , and C_{PG} are comparable. The calculated capacitance between a circular island of 320 nm in diameter and a metal plate with a 320 nm hole, 50 nm above the island, is 40 aF, about as large as each measured top gate capacitance by itself. We thus infer that the island is formed in the central region uncovered by the top gates and extends underneath all the gates. This is consistent with the quantum point contacts extending underneath the split gates as discussed above (see also ref 15).

Presumably lateral confinement is less tight in these devices than in GaAs split gate devices, due to the much smaller band gap.

Finally, we investigate whether the dot is weakly or strongly tunnel coupled to the leads by inspecting the line shape of the Coulomb peaks at low bias voltage. In Figure 5b, we overlay on the data a fit by a hyperbolic cosine function and by a Lorentzian function. The former fits the data much better, indicating that the dot is in the weakly coupled regime, where temperature determines the line width rather than tunnel coupling to the reservoirs.²⁸ Doing the same analysis for 50 peaks we find that they are consistently in the weakly coupled regime. We extract an electron temperature of 69 ± 14 mK.

Concluding, we developed a new bilayer graphene device platform for electrostatic confinement based on hBN top and bottom gate dielectrics. Transport through a single-barrier device shows clean pinch-off characteristics with signs of conductance quantization. In double-barrier devices clear Coulomb blockade is observed. These first results invite further development of this new platform. Then the question can be addressed how electron–electron interactions, electron–phonon interactions, and spin and valley lifetimes in graphene are modified by the confinement. Moreover, this double-gated device structure can be used to explore the nature of the electric field induced bandgap in clean bilayer graphene and the broken symmetry states at zero magnetic and electric field.²⁹ Further development of this technology by adding local bottom gates will open the way to create topological confinement in bilayer graphene.^{30,31}

■ ASSOCIATED CONTENT

§ Supporting Information

The Supporting Information contains an optical microscope picture of the sample with all devices, an AFM image of device B, and detailed information on the subtraction procedure for the background resistance. This material is available free of charge via the Internet at <http://pubs.acs.org>.

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Notes

The authors declare no competing financial interest.

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