

See discussions, stats, and author profiles for this publication at: <https://www.researchgate.net/publication/47297453>

# Controllable p-n Junction Formation in Monolayer Graphene Using Electrostatic Substrate Engineering

ARTICLE *in* NANO LETTERS · OCTOBER 2010

Impact Factor: 13.59 · DOI: 10.1021/nl102756r · Source: PubMed

---

CITATIONS

71

---

READS

65

## 4 AUTHORS, INCLUDING:



**Hsin-Ying Chiu**

University of Kansas

42 PUBLICATIONS 2,438 CITATIONS

SEE PROFILE



**Vasili Perebeinos**

Skolkovo Institute of Science and Technol...

106 PUBLICATIONS 6,680 CITATIONS

SEE PROFILE



**Phaeton Avouris**

IBM, T. J. Watson Research Center

520 PUBLICATIONS 45,949 CITATIONS

SEE PROFILE

# Controllable p-n Junction Formation in Monolayer Graphene Using Electrostatic Substrate Engineering

Hsin-Ying Chiu,\* Vasili Perebeinos, Yu-Ming Lin, and Phaeton Avouris\*

IBM Thomas J. Watson Research Center, Yorktown Heights, New York 10598, United States

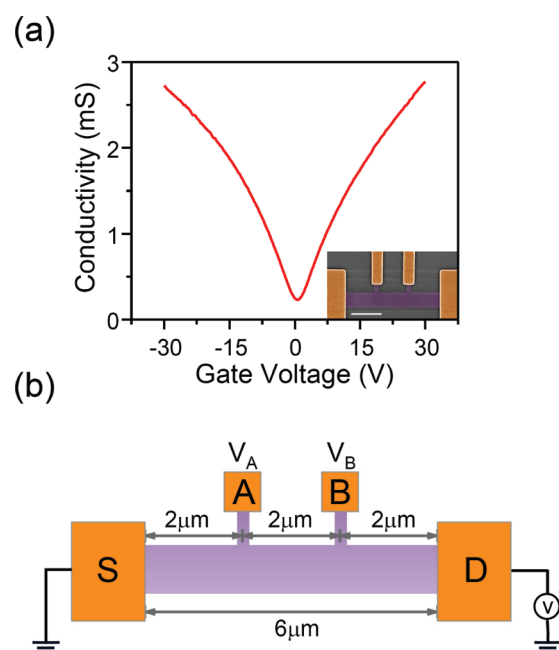
**ABSTRACT** We investigate electric transport in graphene on SiO<sub>2</sub> in the high field limit and report on the formation of p-n junctions. Previously, doping of graphene has been achieved by using multiple electrostatic gates, or charge transfer from adsorbants. Here we demonstrate a novel approach to create p-n junctions by changing the local electrostatic potential in the vicinity of one of the contacts without the use of extra gates. The approach is based on the electronic modification not of the graphene but of the substrate and produces a well-behaved, sharp junction whose position and height can be controlled.

**KEYWORDS** Graphene, transistor, p-n junction, high-field transport, trap charges, substrate

While the low field carrier transport in graphene has already been the focus of numerous studies,<sup>1–6</sup> the behavior of graphene devices in the high field limit has received much less attention.<sup>7–12</sup> Thus, while it was shown that graphene itself can withstand current densities approaching 10<sup>9</sup> A/cm<sup>2</sup>,<sup>13,14</sup> the behavior of graphene devices at high fields still remains largely unexplored. However, for nanoelectronic applications the interest is in the high field transport regime since devices are usually operated at or near the current saturation limit. Currently, little is known about graphene under those conditions. In this paper, we study the high field regime and show that while graphene itself is stable, there are crucial changes induced in the gate dielectrics that strongly affect the transport in graphene channel. This effect is enhanced in the atomic-layer thin body of the graphene channel. Thus, conclusions about the behavior of devices at high bias need to be carefully examined. Most importantly, we show that the electrostatic modifications of the substrate can be exploited to create an abrupt graphene p-n junction, which offers opportunities extending beyond CMOS technology, such as planar electron Veselago lenses.<sup>15</sup> The process is controllable and we create these junctions with desired lengths and barrier heights without resorting to the use of multiple gates,<sup>7,16–25</sup> or charge transfer from adsorbates,<sup>24–26</sup> as is currently the case.

To explore high bias regime, we fabricated four-terminal, back-gated transistors from exfoliated graphene on an undoped Si substrate covered with 90 nm thick SiO<sub>2</sub>. As shown in Figure 1b, the graphene channel is 1 μm wide and 6 μm long and contacted by titanium source (S) and drain (D)

electrodes.<sup>27</sup> Two voltage probes, A and B, were placed along the channel separating it into three segments (denoted as SA, AB, and BD) with equal lengths of 2 μm. We first consider the case of p-type (hole) transport in the channel by choosing negative drain ( $V_D < 0$ ) and gate voltages ( $V_G - V_{CNP} < 0$ , where  $V_{CNP}$  is the charge neutrality point, also referred to as the Dirac point). Overnight thermal annealing under vacuum minimizes the hysteretic behavior, the ob-

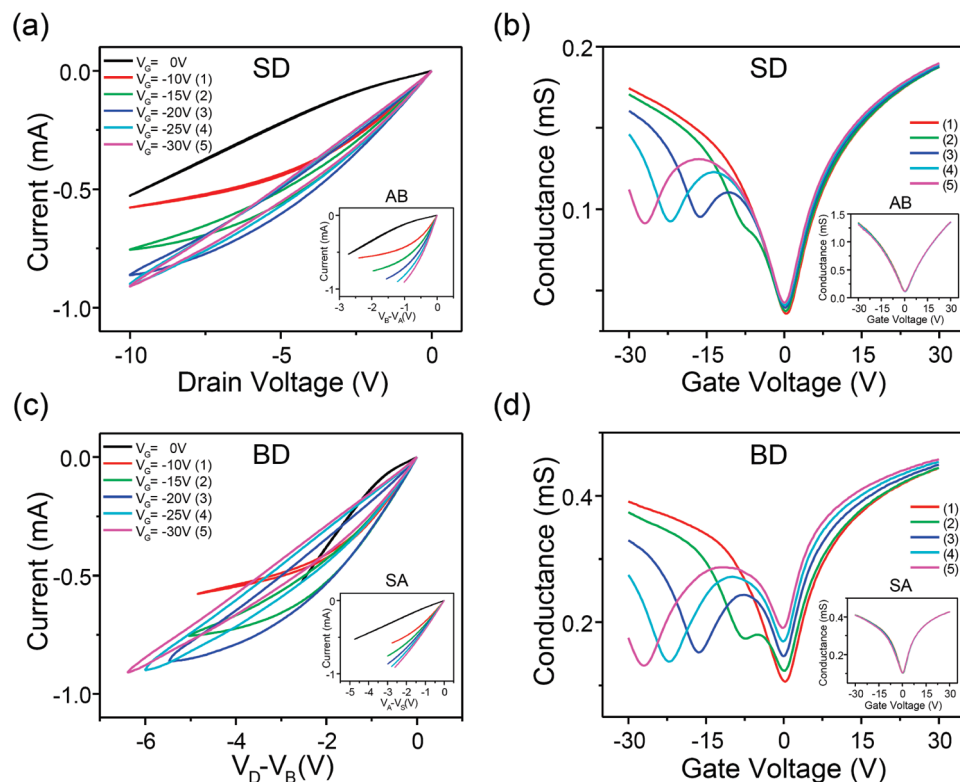


**FIGURE 1.** Device electrical characteristic and configuration. (a) The channel conductivity ( $\sigma$ ) versus gate voltage ( $V_G$ ) curve of a pristine graphene transistor at source-drain bias ( $V_D$ ) as 10 mV. The four-probe carrier mobility is about 3500 cm<sup>2</sup>/(V s) in both electron and hole branches. The false-colored SEM image with 2 μm scale bar is shown in the inset. (b) Schematic of device configuration. One 6 μm long and 1 μm wide graphene layer is connected with S (source) and D (drain) contacts, while A and B terminals are voltage probes.

\* To whom correspondence should be addressed. E-mail: (H.-Y.C) hchiu@us.ibm.com; (P.A) avouris@us.ibm.com.

Received for review: 08/5/2010

Published on Web: 10/01/2010



**FIGURE 2.** Output characteristics ( $I_D$ – $V_D$ ) and the conductance versus gate voltage ( $G$ – $V_G$ ) curves for different segments (Device 1). (a) The output characteristics ( $I_D$ – $V_D$ ) of total segment SD at fixed gate voltages. Stress condition  $V_G$  starts from 0 ( $\sim V_{\text{CNP}}$ ) to  $-30$  V in  $-5$  V step. Insets are the  $I$ – $V$  curves for segment AB. These hystereses represent the process of modifying the surface electrostatic potentials, also indicate that the slopes (conductance) of trace and retrace curves at origin are different. (b) The conductance versus gate voltage ( $G$ – $V_G$ ) curves of segment SD. Each curve is taken subsequently after each individual  $I$ – $V$  sweep, corresponding to (a). Under the same condition, data shown in the inset is  $G$ – $V_G$  curves for segment AB, which was unaffected under the high-field stress. (c,d) The output characteristics and  $G$ – $V_G$  curves, respectively, for segment BD, which is identified as the only segment accounting for entire developments. Insets show  $I$ – $V$  and  $G$ – $V_G$  curves of segment SA, which is also unaffected under the high-field stress.

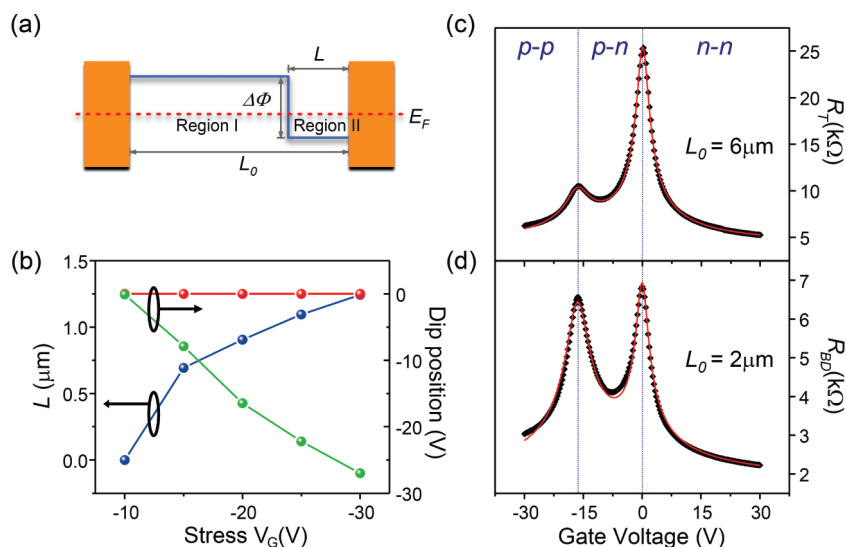
served clean “V” shape characteristic and a nearly zero  $V_{\text{CNP}}$  in Figure 1a signify negligible unintentional doping<sup>28</sup> including water molecules<sup>29</sup> and good channel uniformity in the initial device. A doping profile along the channel is then created by applying a large drain bias, up to  $-10$  V, to electrically stress the devices. We have systematically varied the extent of the electrical stress by applying different gate voltages. The amount of doping induced by the high-field stress can subsequently be inferred from the change of  $V_{\text{CNP}}$  in a  $I_D$ – $V_G$  gate sweep performed at low bias. Therefore, in this work, each high-bias measurement is followed by a low-bias gate sweep as a monitoring routine.

Our experimental procedure involves to first sweep  $V_D$  up to  $-10$  V, as  $V_G$  is varied from  $V_{\text{CNP}}$  ( $\sim 0$  V for this device) toward more negative gate voltages up to  $V_G = -30$  V in steps of  $-5$  V. Figure 2a shows a series of the  $I_D$ – $V_D$  output characteristics of the graphene device. A clear hysteresis in the  $V_D$  sweep is observed when  $|V_G - V_{\text{CNP}}|$  is increased above 15 V (green curve). Interestingly, this hysteresis is accompanied by a small plateau-like feature in the corresponding conductance,  $G = I_D/V_D$ , versus gate voltage curves in the subsequent low-bias measurement (see Figure 2b). The hysteresis in the output characteristics becomes more

pronounced as the device is stressed at larger  $|V_G - V_{\text{CNP}}|$  biases, and the plateau in the  $G$ – $V_G$  curves eventually becomes a second dip to the left of the original Dirac point.

Using the four-probe configuration, the development of these features is monitored for each segment simultaneously. From the output characteristics and  $G$ – $V_G$  curves shown in Figure 2c,d, we find that only segment BD exhibits similar dip features, while those of the other two segments SA and AB do not show any discernible variation as a result of the stress (insets of Figure 2a–d). This indicates that the observed new features result from changes in the graphene channel in the vicinity of the drain contact. The effect of a possible asymmetrical initial contact resistance is ruled out and verified by swapping the polarity of the bias at the source/drain contacts. We also note that the voltage drop in the AB segment decreases while the voltage drop in segment DB increases; the overall performance of the device is eventually limited by this feature as shown in the inset of Figure 2a,c.

The two dips observed in the  $G$ – $V_G$  curves in both Figure 2b,d indicate the creation of a doped region near the drain contact as a result of the stressing at high drain biases in contrast to the initial, nearly pristine, graphene channel.



**FIGURE 3.** A step-potential model of graphene p-n junction and its analysis. (a) Schematic band diagram of a p-n junction along the graphene channel. Region I indicates the main unaffected region while Region II represents the interfacial trap charges present near the interface.  $L_0$  and  $L$  are the full channel length and doped channel length, respectively, and  $\Delta\Phi$  is the potential step barrier between Region I and II. The red dashed line is a guide line for the chemical potential ( $E_F$ ) varying with the gate voltage. (b) The relationship between  $L$  and dip positions vs stress  $V_G$ . The constant main dip position is shown in red. Both the second developed dip (green curve) and the length  $L$  (blue curve) vary almost linearly with stress condition. (c) and (d) show transfer characteristics at the stress condition  $V_G = -20$  V. The experimental data are shown in black and the modeled results are shown in red for different lengths  $L_0 = 6 \mu\text{m}$  and  $L_0 = 2 \mu\text{m}$  in (c,d), respectively. As the gate varies, the graphene channel exhibit different junction (p-p, p-n and n-n) configurations.

Furthermore, the position of the second dip depends on the gate voltage  $V_G$  used during the stressing, while the original Dirac point stays unaffected. In Figure 3b, we plot the gate voltages corresponding to these two conductance minima as a function of the applied  $V_G$  during the stress. The unvarying position of the main dip corresponds to the original, unaffected graphene domain in the channel, while the progressive evolution of the second dip demonstrates the correlation between the stress condition and the doping of the channel and the control that the stress voltage provides. We tested twelve devices with the same device geometry and the same result was observed. We thus conclude that the two dips (Dirac points) are topologically well-defined and can be controlled by the applied stress voltage  $V_G$ . The position of the second Dirac point relative to the initial one indicates the generation of positive charges close to the drain contact. The observation of these two distinct and well-defined dips indicates that the graphene is unlikely to be structurally damaged during stressing. This conclusion is further supported by the fact that the double Dirac feature can be eliminated by overnight thermal annealing in vacuum at 475 K and the original characteristics recovered with  $V_{\text{CNP}} \approx 0$  V. The other possibility of field-induced accumulation associated with mobile charges (such as alkali atom contaminants) is also not likely, due to the absence of observable hysteresis in the original device and, most importantly, the fact that the application of stress voltages with the opposite polarity does not affect the double dip structure. Therefore, the above observations and the known properties of insulators under stress<sup>30</sup> strongly suggest that trapped charge in the silicon oxide substrate is the

source of the local doping under high bias conditions. The electron affinity energy and the band gap of silicon oxide are 0.95 and 8.9 eV, respectively,<sup>31</sup> while the graphene work function is  $\sim 4.5$  eV.<sup>32</sup> Therefore, the barriers for an electron or hole to be injected into bulk traps in  $\text{SiO}_2$  are  $\sim 3.6$  and  $\sim 4.3$  eV, respectively. These energies are too high to account for our observations. In addition, the leakage current into the back-gate remains constant and in the few picoamps range throughout the entire drain voltage sweep. Thus, we attribute the positive charges to trapped charge sites with energies within the  $\text{SiO}_2$  bandgap and in the vicinity of the graphene/oxide interface.

To investigate whether there is charge carrier type preference for trapping in these sites, we performed similar stressing studies under n-type (electron) transport conditions (i.e.,  $V_D > 0$ ,  $V_G - V_{\text{CNP}} > 0$ ) in other graphene devices with identical layouts. Contrary to the case of p-type transport, no new dip was observed even at higher current densities, except for a slight hysteresis in the output characteristics that is likely due to joule-heating and the modification of surface chemistry after current annealing.<sup>14,33–36</sup> Therefore, under similar stress conditions, hole carriers are much easier to be injected into the traps than electrons, which indicates that the processed silicon oxide surface tends to be donorlike (that is, positively charged when empty and neutral when filled with an electron).

The two Dirac points seen in the gate voltage sweep are a signature of the formation of a p-n junction in the graphene channel. To gain further insight, we use a step-potential model to investigate this process. A schematic of the p-n junction band diagram is shown in Figure 3a. The different

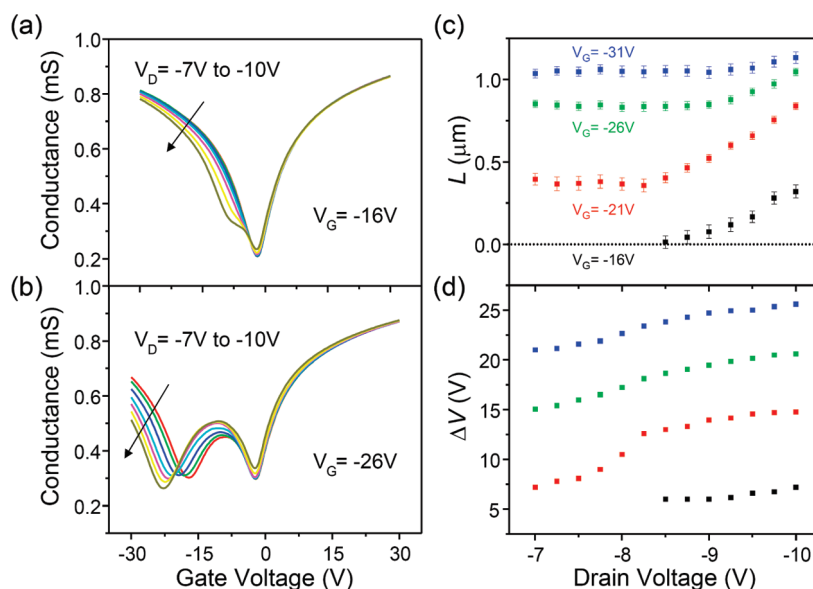


FIGURE 4. Study of the threshold conditions of Device 2. (a,b) The  $G$ - $V_G$  curves taken after different  $V_D$  stress at  $V_G = -16$  and  $-26$  V, respectively. Indiscernible changes in  $G$ - $V_G$  were observed for the stress conditions at  $V_G = -1$ ,  $-6$ , and  $-11$  V. In both panels,  $V_D$  ranges from  $-7$  to  $-10$  V in  $-0.5$  V steps (guided by arrow and shown in the same color code). (c) Length  $L$  as a function of different stress conditions in gate and drain voltages. (d) The voltage difference  $\Delta V$  between two dips as a function of the drain voltage. Data in each color represent a fixed gate voltage for  $V_G$  ranging from  $-16$  to  $-31$  V.

electrostatic potential in Region II is due to the interfacial charges induced by the high field stress described above, which gives rise to the electrostatic potential step relative to the unperturbed Region I. We note that this is the first time a controllable junction was generated in a graphene channel without resorting to multiple gates<sup>7,16–23</sup> or chemical doping.<sup>24–26</sup>

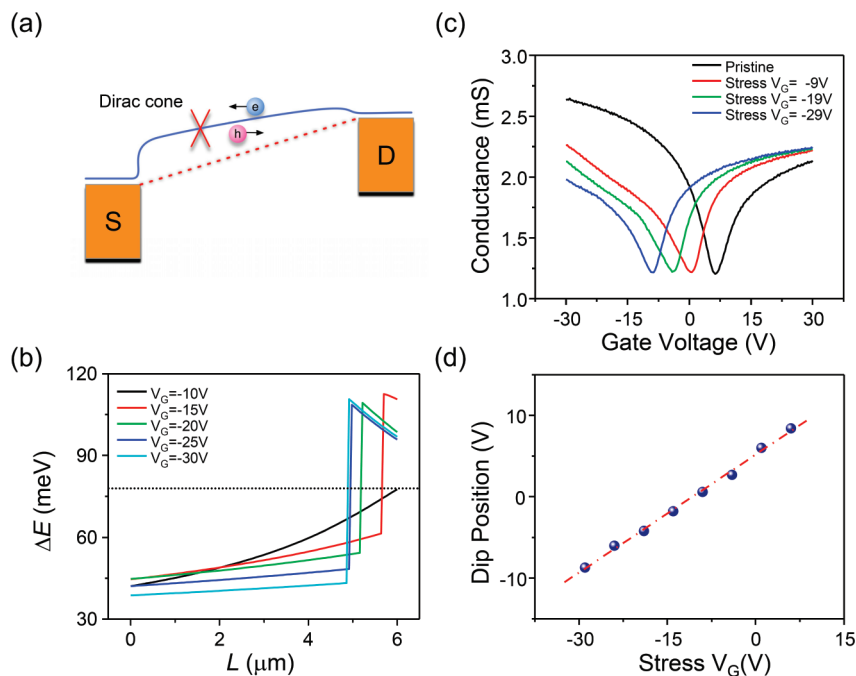
The total channel resistance ( $R_T$ ) can be written as (see Supporting Information)

$$R_T = R_C + \frac{A}{\sqrt{n_{01}^2 + n_1[V_G^*]^2}} + \frac{B}{\sqrt{n_{02}^2 + n_2[V_G^*]^2}} \quad (1)$$

where  $R_C$  is the contact resistance, assumed to be gate independent, with the gate affecting the carrier numbers in regions I and II as  $(n_0^2 + n[V_G^*]^2)^{1/2}$ .<sup>37</sup> The parameters  $A$  and  $B$  are related to the mobilities  $\mu_1$  and  $\mu_2$ , and residual electron-hole puddle densities  $n_{01}$  and  $n_{02}$  by  $A = (L_0 - L)/(e W \mu_1)$  and  $B = L/(e W \mu_2)$ . The carrier densities in these two regions are determined by the electrostatic potential as  $en_1 = V_G^* C_{ox}$  and  $en_2 = C_{ox} V_G^* + en_{it}$ , where  $V_G^* = V_G - V_{CNP}$  and  $n_{it}$  is the trap charge density. The latter can be inferred from the measured gate voltage difference  $\Delta V$  between the two resistance maxima as  $en_{it} = C_{ox} \Delta V$ . From the low-bias resistance measurements in segments SD and BD of length  $L_0 = 6$  and  $2 \mu\text{m}$  correspondingly, and the length  $L$  of Region II can be deduced from the following relation  $A_6/A_2 = (6 - L)/(2 - L)$ ,<sup>38</sup> which is insensitive to the mobility value  $\mu_1$ .

The relationship between length  $L$  and the stress condition  $V_G$  is shown in Figure 3b. Figure 3c,d shows the measured resistance of segments SD and BD after device stressing at  $V_G = -20$  V and the corresponding fit obtained from the step potential model described by eq 1. The excellent agreement between the measurements and the modeled curves confirms the abruptness of the p-n junction formed. These results demonstrate a novel, straightforward scheme to create a p-n junction in graphene controllable by the stress conditions, that is,  $V_G$ . The long-term stability of the junction as a function of the environmental conditions will be the subject of a future study. To determine the threshold conditions required for the formation of interfacial trap charges, a systematic stress study was performed on another graphene device (Device 2) with identical geometry. Different from the previous stress procedures, the stress was applied at a constant gate voltage  $V_G$  while varying the drain voltage successively from  $-7$  to  $-10$  V. The evolution of the device characteristics at two stress gate voltages,  $V_G = -16$  and  $-26$  V, is shown in Figure 4a,b, respectively. By performing an analysis of the data using the described method,  $L$  and  $\Delta V$  as a function of stress  $V_D$  at a sequence of different  $V_G$  are shown in Figure 4c,d, respectively. We note that both the hysteresis and the distinct features in output and  $G$ - $V_G$  curves occur at  $V_D = -8.5$  V and  $V_G = -16$  V. (When  $|V_D|$  is below  $8.5$  V, we cannot distinguish the voltage difference between the two peaks). From the four-terminal  $I$ - $V$  curve and the known contact resistance for this device  $\sim 1.9 \text{ k}\Omega \mu\text{m}$  in the p-branch,<sup>39</sup> the average onset field (not peak field) is estimated to be  $\sim 2 \text{ V}/\mu\text{m}$  across the BD segment.





**FIGURE 5.** Schematic band bending diagram and short channel graphene device. (a) Illustration of the band bending under high field stress. The blue line indicates the neutrality point along the channel while the chemical potential is shown in dashed line. In this case, holes are the majority carriers,  $V_D < 0$ ,  $V_G - V_{\text{CNP}} < V_D$ , moving from source to drain. (b) The excess energy ( $\Delta E$ ) vs position along the channel length ( $x$ ). This simulation is based on the experimental values of current density of Device 1 at different stress condition  $V_G$  with fixed  $V_D = -10$  V. (c) The transfer characteristics of a 200 nm long graphene device under the bias stress  $V_D = -2.5$  V at various  $V_G$  conditions. There is no sign of second dip, indicating that the channel is uniformly doped. (d) The main dip as a function of the stress voltage in the 200 nm long device, showing a slope of  $\sim 0.5$ .

To understand the dependence of the spatial position of the trapped charges as a function of the bias conditions, we consider a simple model based on the current continuity equation

$$j = n_{\text{tot}}(x)v(x) \quad (2)$$

where  $j$  is a measured current density,  $v(x)$  is drift velocity of the carriers, and  $n_{\text{tot}}(x) = [n_0^2 + n^2(x)]^{1/2}$  is the carrier density, where we use a typical electron-hole puddle density of  $n_0 = 5 \times 10^{11} \text{ cm}^{-2}$ . The carrier concentration  $n(x)$  in the channel is determined by the electrostatic gate and drain biases and the trap carrier density according to

$$n(x) = -C_{\text{ox}}(V_G - V(x))/e - n_{\text{it}} \quad (3)$$

$$n(x) = (eV(x) - E_F(x)) / (eV(x) - E_F(x)) / (\pi \hbar^2 v_F^2) \quad (3)$$

where the self-consistent potential  $V(x)$  is found by assuming a linear drop of the Fermi energy  $E_F(x)$  from source to drain reduced by the voltage drop at the contacts of about 30 %, as determined by our four-probe measurements. Since the carrier density  $n(x)$  decreases as the position moves toward the drain

electrode, it is expected that the velocity  $v(x)$  will become higher near the drain contact. A hotter carrier distribution at the drain side yields an enhanced population of the interfacial trap states in the silicon oxide. In particular, these high energy carriers are expected in the region where the traps have already been produced by the previous  $I-V_D$  stress sweep. To quantify the energy of the hot carrier distribution, we assume that at a finite bias the positively moving carriers have higher energy than the negatively moving carriers by an energy  $\Delta E$ . The drift velocity is related to  $\Delta E$  according to<sup>40</sup>

$$\Delta E = \frac{\pi}{2} \hbar v(x) \sqrt{\pi n(x)} \quad (4)$$

In Figure 5a, we estimate the energy  $\Delta E$  as a function of position along the channel using the experimentally extracted values of trap charge densities and doping length  $L$  for different  $I_D-V_D$  stress sweeps. The simulations qualitatively explain the onset of the p-n junction formation at the drain side and its evolution with the subsequent sweeps, such that, the source region stays intact due to the absence of the hot carriers. Once the trap charges form, the local carrier density will be low in Region II, which causes a larger potential drop under the aforementioned stress conditions. Therefore, the current density is limited by the interfacial trap charges and the device performance is restricted as shown in the inset of Figure 2a.

As shown in Figure 4c, the length of the doped Region II can be extended to be as long as 1  $\mu\text{m}$ . This indicates that for a shorter channel device, the entire graphene channel could be doped, causing a smooth shift of the Dirac point instead of the occurrence of two resistance maxima. To verify this uniform doping effect in a short channel device, a two-terminal graphene device with 200 nm channel length was fabricated. Following similar procedures for creating an n-doped junction, we find that the transfer characteristics remain dominated by only a single Dirac point, which shifts toward negative voltages, as shown in Figure 5c. The Dirac position depends linearly on the stress gate voltage, as shown in Figure 5d. This result indicates that we achieved uniform charging of the interfacial traps along the channel in a short-channel device.

In conclusion, we have shown that a sharp p-n junction can be produced in monolayer graphene device structures through the electrostatic modification of the gate insulator surface. Furthermore, we demonstrated the ability of controlling both the length and the potential difference of the doped region along the graphene transistor channel. This novel approach to produce a well-defined p-n junction without extra gates or adsorbates opens up new opportunities for studying quantum transport in graphene devices and the results provide new insight into the phenomena that can take place at the high field transport limit, also demonstrating the need to clearly distinguish between substrate-induced effects and the intrinsic high-field transport behavior of graphene.

**Acknowledgment.** We thank B. Ek, J. Bucchignano, and G. Wright for expert technical assistance. We also thank James Stathis, Marcus Freitag, Marc Bockrath, Shu-Jen Han, Damon Farmer, Ching-Tzu Chen, Wenjuan Zhu, and Yan-qing Wu for helpful discussions. This work was supported by DARPA under Contract FA8650-08-C-7838 through the CERA program. The views, opinions, and/or findings contained in this article are those of the authors and should not be interpreted as representing the official views or policies, either expressed or implied, of the Defense Advanced Research Projects Agency or the Department of Defense.

**Supporting Information Available.** Details of sample fabrication, electrical measurements, data analysis method, and additional fitting model with e-h puddles. This material is available free of charge via the Internet at <http://pubs.acs.org>.

## REFERENCES AND NOTES

- Geim, A. K. *Science* **2009**, *324* (5934), 1530.
- Castro Neto, A. H.; Guinea, F.; Peres, N. M. R.; Novoselov, K. S.; Geim, A. K. *Rev. Mod. Phys.* **2009**, *81* (1), 109.
- Chen, J.-H.; Jang, C.; Xiao, S.; Ishigami, M.; Fuhrer, M. S. *Nat. Nanotechnol.* **2008**, *3* (4), 206.
- Adam, S.; Hwang, E. H.; Galitski, V. M.; Das Sarma, S. *Proc. Nat. Acad. Sci. U.S.A.* **2007**, *104* (47), 18392.
- Geim, A. K.; MacDonald, A. H. *Phys. Today* **2007**, *60* (8), 35.
- Avouris, Ph.; Chen, Z.; Perebeinos, V. *Nat. Nanotechnol.* **2007**, *2* (10), 605.
- Meric, I.; Han, M. Y.; Young, A. F.; Ozyilmaz, B.; Kim, P.; Shepard, K. L. *Nat. Nanotechnol.* **2008**, *3* (11), 654.
- Luo, X.; Lee, Y.; Konar, A.; Fang, T.; Xing, G.; Snider, G.; Jena, D. Current-carrying Capacity of Long & Short Channel 2D Graphene Transistors. In *66th Device Research Conference*, Santa Barbara, CA, **2008**.
- Freitag, M.; Steiner, M.; Martin, Y.; Perebeinos, V.; Chen, Z.; Tsang, J. C.; Avouris, Ph. *Nano Lett.* **2009**, *9* (5), 1883.
- Barreiro, A.; Lazzeri, M.; Moser, J.; Mauri, F.; Bachtold, A. *Phys. Rev. Lett.* **2009**, *103* (7), No. 076601.
- DaSilva, A. M.; Zou, K.; Jain, J. K.; Zhu, J. *Phys. Rev. Lett.* **2010**, *104* (23), 236601.
- Dorgan, V. E.; Bae, M.-H.; Pop, E. *Appl. Phys. Lett.* **2010**, *97* (8), No. 082112.
- Murali, R.; Yang, Y.; Brenner, K.; Beck, T.; Meindl, J. D. *Appl. Phys. Lett.* **2009**, *94* (24), 243114.
- Moser, J.; Barreiro, A.; Bachtold, A. *Appl. Phys. Lett.* **2007**, *91* (16), 163513.
- Cheianov, V. V.; Fal'ko, V.; Altshuler, B. L. *Science* **2007**, *315* (5816), 1252.
- Williams, J. R.; DiCarlo, L.; Marcus, C. M. *Science* **2007**, *317* (5838), 638.
- Ozyilmaz, B.; Jarillo-Herrero, P.; Efetov, D.; Abanin, D. A.; Levitov, L. S.; Kim, P. *Phys. Rev. Lett.* **2007**, *99* (16), 166804.
- Huard, B.; Sulpizio, J. A.; Stander, N.; Todd, K.; Yang, B.; Goldhaber-Gordon, D. *Phys. Rev. Lett.* **2007**, *98* (23), 236803.
- Liu, G.; Velasco, J., Jr.; Bao, W.; Lau, C. N. *Appl. Phys. Lett.* **2008**, *92* (20), 203103.
- Stander, N.; Huard, B.; Goldhaber-Gordon, D. *Phys. Rev. Lett.* **2009**, *102* (2), No. 026807.
- Velasco, J.; Liu, G.; Jing, L.; Kratz, P.; Zhang, H.; Bao, W.; Bockrath, M.; Lau, C. N. *Phys. Rev. B* **2010**, *81* (12), 121407.
- Velasco, J., Jr.; Liu, G.; Bao, W.; Lau, C. N. *New J. Phys.* **2009**, *11* (9), No. 095008.
- Young, A. F.; Kim, P. *Nat. Phys.* **2009**, *5* (3), 222.
- Farmer, D. B.; Lin, Y.-M.; Afzal-Ardakani, A.; Avouris, Ph. *Appl. Phys. Lett.* **2009**, *94* (21), 213106.
- Lohmann, T.; von Klitzing, K.; Smet, J. H. *Nano Lett.* **2009**, *9* (5), 1973.
- Brenner, K.; Murali, R. *Appl. Phys. Lett.* **2010**, *96* (6), No. 063104.
- Two types of metal composition have been used in our study and show the similar transport behaviors. One is the stack of Ti/Au (20 nm/30 nm) and the other is Ti/Pd/Au (0.5 nm/20 nm/30 nm). In the second case, Ti is used for the adhesion layer.
- The estimated residual concentration for this device  $n_0$  is  $\sim 3.9 \times 10^{11} \text{ cm}^{-2}$ .
- Kim, W.; Javey, A.; Vermesh, O.; Wang, Q.; Li, Y.; Dai, H. *Nano Lett.* **2003**, *3* (2), 193.
- Nicollian, E. H.; Brews, J. R. *MOS (Metal Oxide Semiconductor) Physics and Technology*; Wiley: New York, 1982.
- Muller, R. S.; Kamins, T. I.; Chan, M., *Device Electronics for Integrated Circuits*; Wiley: New York, 2003.
- Giovannetti, G.; Khomyakov, P. A.; Brocks, G.; Karpan, V. M.; van den Brink, J.; Kelly, P. J. *Phys. Rev. Lett.* **2008**, *101* (2), No. 026803.
- Romero, H. E.; Shen, N.; Joshi, P.; Gutierrez, H. R.; Tadigadapa, S. A.; Sofo, J. O.; Eklund, P. C. *ACS Nano* **2008**, *2* (10), 2037.
- Carla, M. A.; Pierre, L. L.; Matthieu, P.; François, L.; Benoit, C. S.-A.; Patrick, D.; Richard, M. *Adv. Mater.* **2009**, *21* (30), 3087.
- Connolly, M. R.; Chiou, K. L.; Smith, C. G.; Anderson, D.; Jones, G. A. C.; Lombardo, A.; Fasoli, A.; Ferrari, A. C. *Appl. Phys. Lett.* **2010**, *96* (11), 113501.
- Nourbakhsh, A.; Cantoro, M.; Klekachev, A.; Clemente, F.; Soree, B.; van der Veen, M. H.; Vosch, T.; Stesmans, A.; Sels, B.; De Gendt, S. J. *Phys. Chem. C* **2010**, *114* (15), 6894.
- Seyoung, K.; Jung, N.; Insun, J.; Davood, S.; Luigi, C.; Zhen, Y.; Emanuel, T.; Sanjay, K. B. *Appl. Phys. Lett.* **2009**, *94* (6), No. 062107.
- For voltage probing, terminal A and B are set at  $I_{A,B} = 0$  A and the voltage reading during the measurement is monitored. Thus, we can extract data between each terminal and compile two different data sets from the same run: one for whole channel, segment SD, and second for segment BD.
- We calculate the contact resistance in the following way:  $R_{c,x} = 1/2(R_{2p} - 3R_{4p})_x$  where x is for either the p-branch or e-branch.
- Perebeinos, V.; Avouris, Ph. *Phys. Rev. B* **2010**, *81* (19), 195442.