Multilevel Resistive Switching in Planar Graphene/SiO_2 Nanogap Structures

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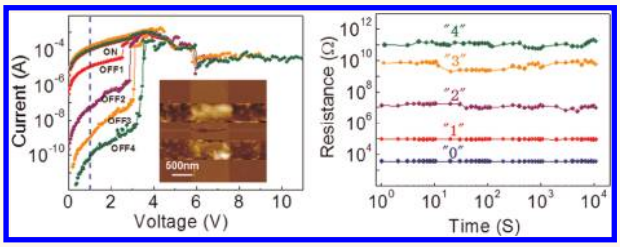
ABSTRACT



We report a planar graphene/SiO_2 nanogap structure for multilevel resistive switching. Nanosized gaps created on a SiO_2 substrate by electrical breakdown of nanographene electrodes were used as channels for resistive switching. Two-terminal devices exhibited excellent memory characteristics with good endurance up to 10^4 cycles, long retention time more than 10^5 s, and fast switching speed down to 500 ns. At least five conduction states with reliability and reproducibility were demonstrated in these memory devices. The mechanism of the resistance switching effect was attributed to a reversible thermal-assisted reduction and oxidation process that occurred at the breakdown region of the SiO_2 substrate. In addition, the uniform and wafer-size nanographene films with controlled layer thickness and electrical resistivity were grown directly on SiO_2 substrates for scalable device fabrications, making it attractive for developing high-density and low-cost nonvolatile memories.

KEYWORDS: nanographene · electronic devices · resistive switching · multilevel memory

Resistance switching random access memory (RRAM)[1−5] is one category of next-generation nonvolatile memory and has attracted broad interests recently due to its simple structure, high operation speed, long retention time, low power consumption, and capability of multilevel switching which enables multibit storage.[6−11] A typical RRAM device is known as a two-terminal metal−insulator−metal (MIM) structure.[12−14] Instead of metals, various carbon materials, such as amorphous carbon, carbon nanotubes, and graphene, were recently explored as alternatives for metals due to their superior properties.[15−19] However, multilevel switching characteristics were rarely investigated in these carbon-electrode devices. Here, we studied the multilevel switching effects in planar graphene/SiO_2 nanogap structures. These RRAM devices show excellent performance with long endurances (>10^4 cycles), long retention time (>10^5 s), and fast switching speed (<500 ns). At least five stable and controllable resistance states were successfully created in these graphene/SiO_2 nanogap devices.

In this study, wafer-scale and uniform nanographene (NG) film was directly deposited on SiO_2 substrates for scalable device fabrication. A typical growth was carried out at 525 °C on SiO_2 substrates in a remote plasma-enhanced chemical vapor deposition (RPECVD) system.[20] Typical NG film consists of interconnected NG domains of tens of nanometers in size. Use of NG film as electrode materials for low-cost RRAM obviously offers several advantages. (1) Facile device fabrication: Unlike previous scaled-up growth of graphene on SiC or catalytic metal surfaces, NG was directly grown on SiO_2, thus a postgrowth transfer process of graphene was avoided. (2) Tunable conductivity: NG film has controllable conductivity by tuning the packing density of NG domains and their layer thickness from one to few layers or more. For a typical 1 nm thick NG film, its sheet resistance can be as low as ~40 kΩ/□, which is somewhere between perfect monolayer graphene and amorphous carbon. (3) Fabrication compatible with modern CMOS technology: Both the low-temperature growth and device fabrications are compatible to existing semiconductor processing. Standard lithographic and etching techniques can be used to define the NG electrodes with desired shapes and sizes. (4) Scaled-up capability of integration: NG film can be grown into at least 4 in. wafer-scale with good uniformity, indicating an enormous potential for applications in multilevel, scalable, and low-cost nonvolatile memory.

RESULTS AND DISCUSSION

Figure 1a illustrates the fabrication process and structure of the two-terminal

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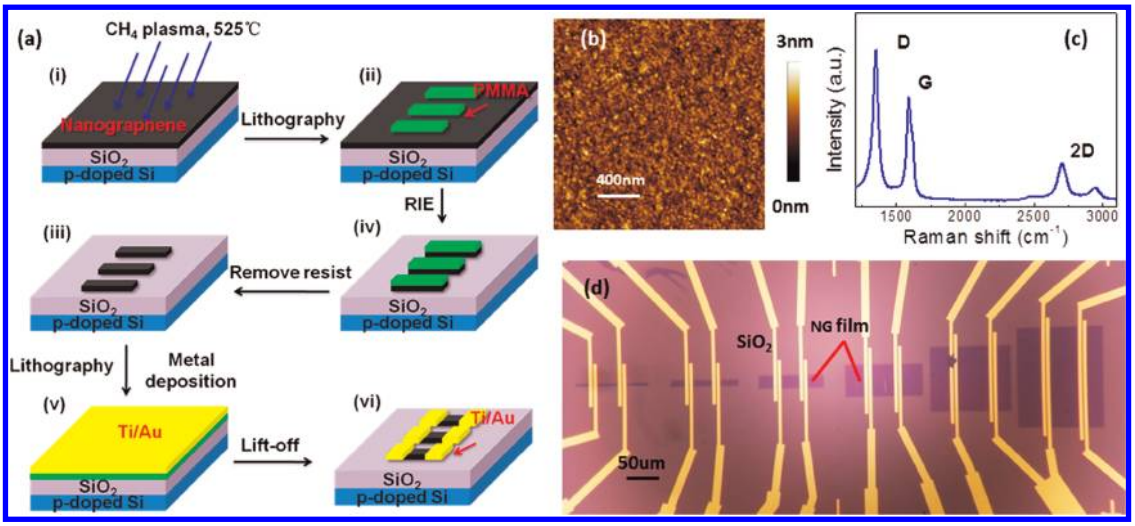

Figure 1. (a) Schematic diagram of the fabrication process for the two-terminal devices. (i) Uniform and large-area nanographene film on SiO_2 (300 nm)/Si substrates was used as starting materials; (ii) PMMA resist mask was patterned by e-beam lithography; (iii) removal of the exposed nanographene by reactive ion etching; (iv) removal of the PMMA overlay in hot acetone; (v) contact electrodes formation by a second-step e-beam lithography and Ti/Au (2 nm/30 nm) deposition by e-beam evaporation; (vi) lifting-off of the metals for the two-terminal resistive switching devices. (b) AFM image of nanographene film grown on SiO_2 with the sheet resistance of 20 kΩ/□. (c) Typical Raman spectra of the nanographene film. (d) Optical image of the two-terminal devices.

resistive switching devices. NG film grown on commercial SiO_2 (300 nm)/p^{++}Si substrates was first patterned into ribbons by electron beam lithography and reactive ion etching techniques. Electrodes were then defined by a second-step EBL, deposition of Ti/Au (2 nm/30 nm) by electron beam evaporation, and metal lifting-off techniques. As-made devices were annealed at 400 °C for 0.5 h in hydrogen atmosphere to improve contacts before any electrical measurements. All electrical operation and measurements were carried out in a vacuum of $<2 \times 10^{-4}$ Torr.

The atomic force microscope (AFM) image of the NG film grown on the surface of SiO_2 is shown in Figure 1b, whose sheet resistance is about 20 kΩ/□. We can see that the substrate surface is uniformly and fully covered by nanographene film with nanoislands packed densely. To identify sp^2 structure of the nanographene, Raman scattering of the NG film was carried out in a micro-Raman microscope. The typical Raman spectra of the NG film are shown in Figure 1c. The G peak, D peak, and 2D peak were observed at around 1591, 1354, and 2707 cm^{-1}, respectively, indicating that nanographene mainly consists of sp^2 graphitic bonded carbon. The strong D peak intensity originates from scattering of abundant edges of the nanographene. The full width at half-maximum (fwhm) values of the D, G, and 2D peaks are 41.9, 36.0, and 58.8 cm^{-1}, respectively, indicating a relatively high-quality nanographene.[21] Figure 1d indicates the optical image of the two-terminal devices.

A forming process by applying a certain forming voltage to the two electrodes was necessary for a fresh device to activate its resistive switching behavior. After the forming process, electrical breakdown occurred for the NG film between two electrodes due to Joule heating generated by the applied bias voltage.[22,23] Figure 2a shows an electrical breakdown $I-V$ curve for a typical device with a channel width of 1 μm and a length of 450 nm, with breakdown voltage V_{break} = 5.5 V. The inset shows the electrical measurement of the two-terminal devices. Figure 2b,c show the AFM images of this device before and after the forming process, respectively. The thickness of NG film is about 2.3 nm, which is equivalent to approximately 4 layers of nanographene. After breakdown, a broken gap was clearly seen at the central area of NG. The SEM images of devices before and after the forming process (refer to Figure S1a,b in Supporting Information, respectively) also clearly demonstrate a crack formation across the NG stripe, and the gap width usually varies from 30 to 100 nm. It was noted that the breakdown location always appeared near the middle of the NG strip, which was attributed to the uniform heat generation[23] in the two-terminal devices.[24,25] According to the previous theoretical calculations,[23] the hottest point is near the middle of the NG strip, where the breakdown takes place. In order to further understand the breakdown process, we investigated the two-terminal resistive switching devices with different length (L) and width (W) nanographene ribbons. The breakdown $I-V$ characteristics of various switching devices are shown in Figure S2a–c. For the NG channels with the same W but different L, V_{break} increases with L, while I_{break} (the current at V_{break} defined as I_{break}) does not depend on L. In contrast, for the channels with the same L, I_{break} increases with W, whereas V_{break} remains the same. These observations further support the Joule heating model (please also see Supporting

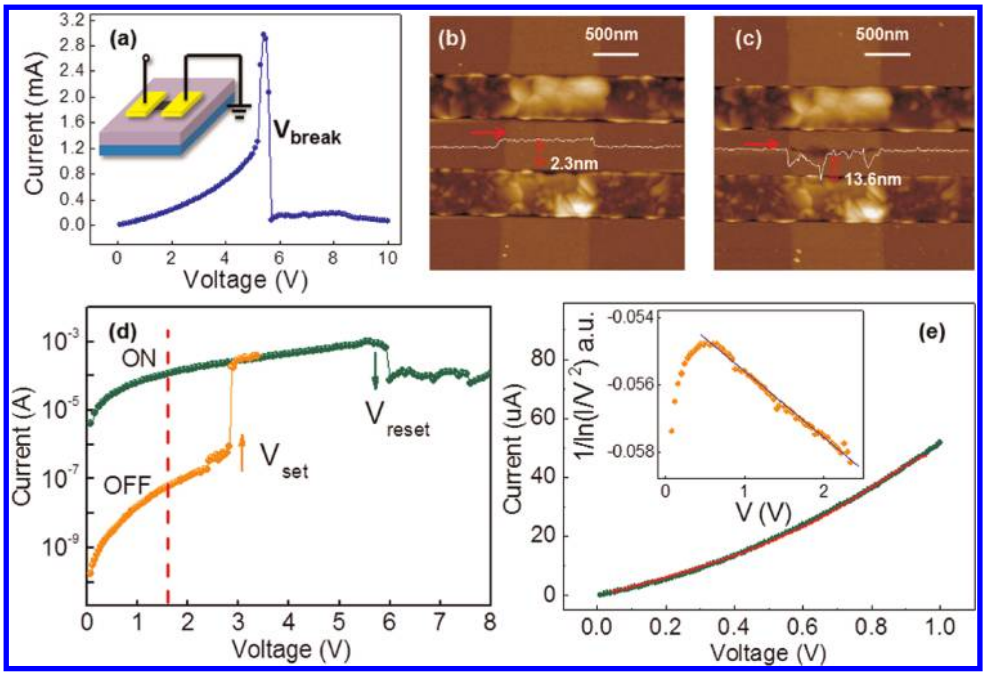

Figure 2. Forming process and *I*−*V* switching characteristics of the two-terminal resistance switching devices. (a) *I*−*V* characteristic of the electrical breakdown of a device with NG width of 1 μm and length of 450 nm. The electrical measurements are illustrated in the inset. (b) AFM image of the as-made device. Height profiles marked by the arrow show the NG thickness of 2.3 nm. (c) AFM image of the same device after the forming process, revealing a broken gap region marked by an arrow with a depth of 13.6 nm. (d) Typical *I*−*V* switching characteristics of a device with NG width of 1 μm, length of 1 μm, and thickness of 2.3 nm. Linear scale data are shown in the inset. ON/OFF ratio of $\sim 10^4$ is marked by the dashed line at 1 V. (e) Experimental (points) and calculated (line) *I*−*V* curves of the ON state before the conduction change. The inset is the plot of $1/\ln(I/V^2)$ *versus* *V* generated from the *I*−*V* data of the OFF state before the conduction change.

Information for more discussions). From the AFM image, the depth of the broken gap is more than 13.6 nm and the NG film has a thickness of only 2.3 nm. Thus, we can infer that the SiO_2 substrate, at least part of it, was also cracked due to the Joule heating. In order to investigate the morphology of the gap region, we carried out H_2 plasma etching,[26] which could etch the NG film away but leave the SiO_2 substrate. The AFM and SEM images, seen in Figure S1c,d, show clearly substantial damage to the SiO_2 substrate in the gap region. It is reasonable to infer that the temperature of the gap region during breakdown should be near 1700 °C,[23] the melting temperature of SiO_2. At this temperature, the separation of the Si and SiO_2 phases could appear, resulting in the formation of Si nanocrystals embedded in the insulating matrix,[27,28] which is believed to play an important role for the resistive switching effect working as localized conduction paths.[29]

After the forming process, the device can switch between high resistance state (HRS) and low resistance state (LRS) steadily, and both the HRS and LRS are nonvolatile. The device yields are up to 98% out of over 50 devices studied. LRS is commonly used as the ON state and HRS as the OFF state. Binary digital data can be recorded in these resistance states, for example, LRS for logic "0" and HRS for logic "1". Figure 2c shows the *I*−*V* characteristics of the memory cell measured by dc voltage sweep. During the measurements, the voltage was swept from 0 to 3.5 V. While increasing the voltage steadily, the current jumps abruptly at a voltage value of ~2.8 V, where we can see an expected change of resistance from the HRS to LRS. The HRS-to-LRS switching is called the "set" process, and the corresponding switch voltage was defined as V_{set}. Subsequently, the LRS-to-HRS switching is called the "reset" process, and the corresponding switch voltage was defined as V_{reset}. By sweeping the voltage from 0 to 8 V, the device holds on the LRS and recovers to the HRS at the voltage of 5.5 V. The vertical dashed line marked in Figure 2c indicates an ON/OFF ratio more than 10^3 at 1 V. Both the *I*−*V* curves of the ON state and OFF state before the conduction change are nonlinear and increase exponentially, which could be explained by a model based on tunneling mechanisms.[30−35] We estimated the radius of the Si nanocrystalline filament of ~13.4 nm and the tunneling distance of ~0.77 nm by fitting the *I*−*V* curve of the ON state under intermediate voltage bias at 200 K by Simmons' equation,[36−38] as shown in Figure 2d. The tunneling distance, *d*, indicated that the silicon nanocrystallites formed in the forming process were arranged in a nearly continuous conductive pathway embedded in the SiO_2 matrix on the ON state (please also see the Supporting Information for more details). The inset of Figure 2d shows the plot of $1/\ln(I/V^2)$ *versus* *V* generated from the *I*−*V* data of the OFF state

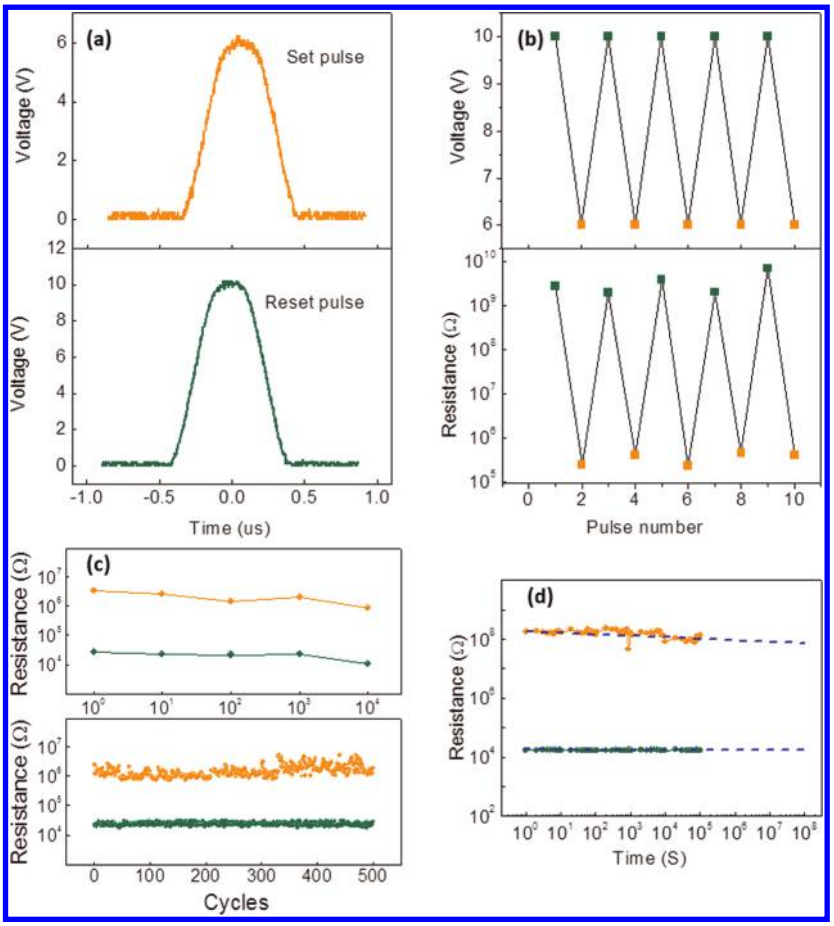

Figure 3. Memory characteristics of graphene/SiO_2 nanogap structures. (a) Device switching speed measurements. A set pulse of 6 V (top panel) and a reset pulse of 10 V (bottom panel) with 500 ns pulse width were applied to the cell for writing and erasing. (b) Device switching behavior by using a series of pulses. (c) Endurance date of a device. V_{set} = 4 V and V_{reset} = 8 V. Top: Wwitching cycles are more than 10^4. Bottom: Switching cycles shows both HRS and LRS after every programming pulse. Resistances of both HRS and LRS were read at 1 V. (d) Retention of the conduction state tested by continuous 1 V read voltage for both ON and OFF states. The dashed lines indicate the extrapolated tendency.

before the conduction change. An obvious linear relationship at high bias voltages was observed, indicating a typical FN tunneling behavior in this voltage range. FN tunneling is an electric-field-assisted tunneling mechanism, and it has been widely studied in MIM structures with longer tunneling distance (~5 nm).[39] The tunneling current density is characterized by $J \sim V^2\exp(-1/V)$.[33] In the present case, the FN tunneling conduction was attributed to a longer tunneling distance of the silicon nanocrystallite pathway, part of which was reoxidated to SiO_x in the reset process. This is consistent with the result reported by Tour *et al.*,[29] in which the silicon nanocrystallite pathways were observed by a transmission electron microscope (TEM), and the ruptured region (corresponding the tunneling distance *d*) in the Si pathway was considered as ~5 nm. The reversible reduction and oxidation of these silicon nanocrystallites are the keys for the resistance switching effect. This redox model is further supported by Figure S3, which shows that the set process only occurs in vacuum or in nitrogen but cannot be achieved in air, while the reset process was not affected by environments.

Figure 3 shows the memory properties of the switching device. The programming speed of the graphene/SiO_2 nanogap structure was tested by applying pulse stimuli. Figure 3a shows the set pulse of 6 V/500 ns and a reset pulse of 10 V/500 ns applied to a cell for writing and erasing, respectively. Figure 3b depicts a sequence of write/erase cycles stimulated by these short pulses. When a set pulse was applied on the device, a switching from OFF state to ON state was triggered with a low resistance recorded in the following read period. On the contrary, a reset pulse switches the device back to OFF state. Note here that the programming speed of the graphene/SiO_2 nanogap structure was down to 500 ns in the present measurement, and the programming speed should be much faster.[29] The device endurance is also one critical parameter for evaluating memory performance. The top panel in Figure 3c demonstrates the evolution of resistance of the two well-resolved states for 10^4 cycles, and the bottom panel shows the two states after every programming pulse. The set voltage and reset voltage applied on this device were 4 and 8 V, respectively, and resistances of

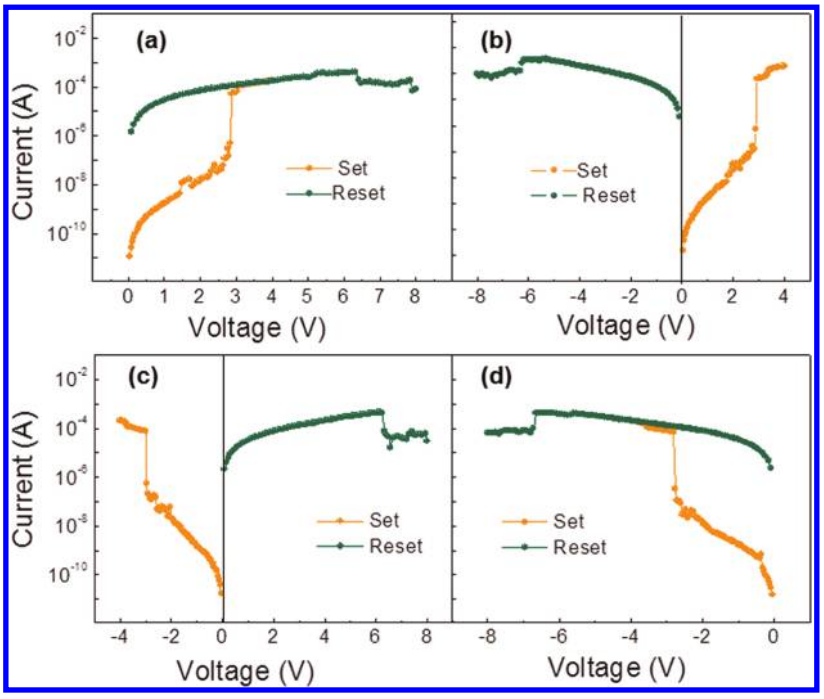

Figure 4. Nonpolar RS behaviors of the two-terminal device. The set−reset processes can be achieved by (a) positive−positive, (b) positive−negative, (c) negative−positive, and (d) negative−negative voltage polarities.

both HRS and LRS were read at 1 V. Although HRS shows some fluctuations, the on/off ratios are about 10^2 without any obvious degradation within 10^4 cycles. As for the retention test, the device was switched ON or OFF state by dc voltage sweeping. Both HRS and LRS were tested by a continuous 1 V reading pulse. The readout was found to be nondestructive, and both LRS and HRS can be retained stably for more than 10^5 s in vacuum at room temperature after removing the external electrical power. The dashed lines in Figure 3d indicate the extrapolated retention time beyond 10 years, which demonstrates that the memory device is nonvolatile and has a long retention time.

The switching behaviors can be classified into three types: unipolar, bipolar, and nonpolar.[40,41] Unipolar or bipolar switching are defined if a device was realized in the set and reset processes by applying the same or alternating polarity of *V*, respectively. If the unipolar and bipolar actions are coexisting in a quite unique fashion, it was called nonpolar switching, which was independent of the polarity of the applied voltage. The present two-terminal memory devices exhibit voltage-polarity-independent nonpolar characteristics, as shown in Figure 4. The set−reset processes can be achieved by positive−positive (Figure 4a), positive−negative (Figure 4b), negative−positive (Figure 4c), and negative−negative (Figure 4d) voltage polarities. This nonpolar switching behavior indicated that the switching effect has a close relationship with the heat generated by local current[1,41] rather than the driven electrical field.

To further understand the role of heat in the RS process, we investigated the temperature-dependent *I*−*V* switching characteristics of our devices after the forming process established at room temperature, as shown in Figure 5. When the devices were gradually cooled to 200 K, the current of HRS decreased much while the LRS current decreased slightly (left panel of Figure 5a). With temperature decreasing, the reset process becomes easier to trigger while it is more difficult for the set process. When the temperature was decreased below 200 K, the ON state resistance increased much and the ON/OFF ratio decreased greatly, as shown in the right panel of Figure 5a. Finally, the device could not be set to the ON state when the temperature is down to about 150 K. Figure 5b shows that only the reset process can be triggered at 10 K. The switching effect can be recovered as temperature increases back to room temperature. The temperature dependence of *I*−*V* switching characteristics indicates that heat is very important for the switching effect, especially for the set process. Below 150 K, the heat generated by local current, which is necessary for the switching effect, is not enough to reduce SiO_x to Si (endothermic process) due to the faster heat dissipation to the environment. The reset process, corresponding to the process of Si→SiO_x, can still be realized due to a much higher current of ON state.

From the *I*−*V* switching characteristic shown in Figure 2c, we can see that, in the reset process, the current fluctuates near a constant value with voltage increasing steadily. Different high resistance states can thus be achieved by applying different V_{reset}, and typical *I*−*V* characteristics of the graphene/SiO_2 nanogap structure resistive switching device at different

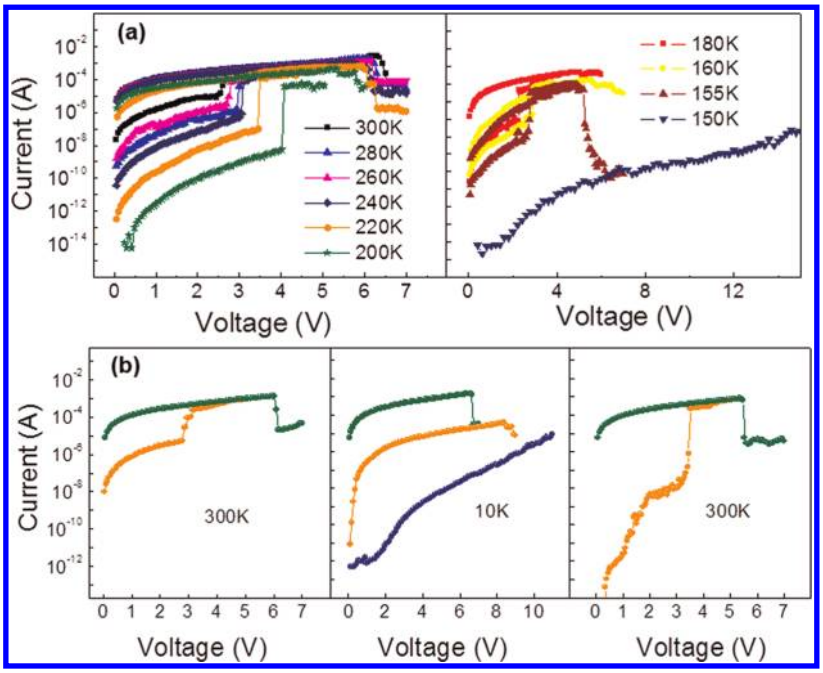

Figure 5. (a) Temperature dependence of the *I*–*V* switching characteristics of the gaphene/SiO_2 nanogap sructures for deceaseing temperature from 300 to 150 K. (b) *I*–*V* switching curves of the device with temperature at 300 K, decreasing to 10 K, and increasing back to 300 K.

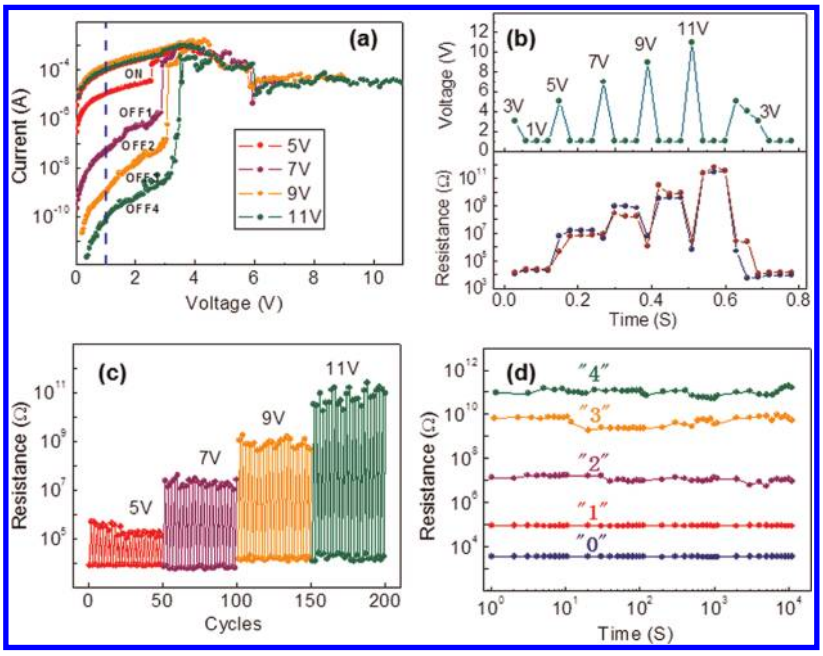

Figure 6. Multilevel resistive switching properties of graphene/SiO_2 nanogap structures. (a) Typical *I*–*V* characteristics of a device with a width of 1 μm, length of 0.4 μm, and thickness of 2.3 nm. The vertical line cut at 1 V indicates five resistance states. By sweeping the reset voltage from 0 to 5 V, the OFF1 state (red) was established. The subsequent reset voltages sweep up to higher voltage of 7 V (purple), 9 V (orange), and even higher to 11 V (olive) from 0 V, and lower conduction states of OFF2, OFF3, and OFF4 were achieved subsequently. (b) Top: series of bias pulses with different magnitudes of 3, 5, 7, 9, and 11 V, corresponding to the sweep voltages in (a) with three reading pulses of 1 V after each programming pulse was applied. Bottom: resistance changes corresponding to the each voltage pulse in the top panel. (c) Cycled switching of the device under various reset voltages. (d) Retention time of more than 10^4 s for each conduction state tested by a continuous 1 V pulse.

V_{reset} are shown in Figure 6a. These tunable conduction states were observed for all devices, indicating a potential use for multilevel switching. For example, the vertical dashed line at 1 V marked in the Figure 6a indicates five resistance states (one ON state and four different OFF states). By sweeping the reset voltage from 0 to 5 V, the resistance state switches to the OFF1 state from the ON state (the red curve). In the

subsequent sweep, the reset voltages were applied up to higher voltages of 7 V (the purple curve), 9 V (the orange curve), and even higher to 11 V (the olive curve) from 0 V, and lower conduction OFF2, OFF3, and OFF4 states were subsequently established. In principle, more OFF states could be generated this way by employing more V_{reset}. Different reset voltages could induce oxidation of the silicon nanocrystal conduction paths to a different degree, resulting in various conduction states. Moreover, it is possible to use the continuously changing conductance states modulated by bias pulses of quasi-continuous amplitudes for a potential artificial neuromorphic network and supercomputing simulations.[42,43]

These different high resistance states can also be achieved by applying a series of bias pulses with different amplitudes. The top panel in Figure 6b shows a series of bias pulses of 3, 5, 7, 9, and 11 V, which are corresponding to the sweep voltages marked in Figure 6a. Three reading pulses of 1 V after each programming pulse were applied to the memory cell. Resistances at every voltage pulse are shown in the bottom panel of Figure 6b. Figure 6c shows the cycled switching at various V_{reset}, indicating that the multilevel switching behavior was reproducible and reliable. The stability of the multilevel resistance states was also investigated. The retention time of each conduction state tested by a continuous 1 V pulse is more than 10^4 s. Figure S4 shows the multilevel switching behaviors obtained in five memory cells, and it is reliable and controllable for all cells (please see Supporting Information).

CONCLUSIONS

In conclusion, reliable and controllable multilevel resistive switching behaviors were investigated in the two-terminal graphene/SiO_2 nanogap structures. At least five stable and repeatable conduction states were demonstrated for these devices. These two-terminal devices in our study also exhibited excellent endurance, good retention characteristics, and fast switching speed. The resistance switching effect was attributed to a reversible thermal-assisted reduction and oxidation process that occurred at the breakdown region of the SiO_2 substrate. The multilevel resistive switching characteristics show a promising prospect for an artificial neuromorphic network and supercomputing simulations. In addition, the uniform nanographene films on the SiO_2 substrate grown by catalyst-free RPECVD with scalable and low-cost characters can be easily fabricated into two-terminal memory devices by conventional standard techniques, making it attractive for application in scalable, high-density, and low-cost nonvolatile memory.

METHODS

Growth of Nanographene Film. The NG film was grown on a premarked SiO_2 (300 nm)/p^{++}Si substrate by a catalyst-free growth process in a remote plasma-enhanced chemical vapor deposition (RPECVD) system using pure methane as the precursor. The substrate temperature, RF power, CH_4 pressure, flow rate, and growth duration are 525 °C, 100 W, 0.20 Torr, 30 sccm, 3 h, respectively.

Fabrication of the Two-Terminal Resistive Switching Devices. Five percent 495 PMMA in anisole (or photoresist) was spin-coated at 4000 rpm on the as-prepared samples and then was patterned into ribbons by a Raith e-line e-beam lithography system (or optical lithography). O_2 plasma etching was performed in a reactive ion etching system (PlasmaLab 80 Plus, Oxford Instruments Company) by using pure O_2 as reactive gas. The plasma power, O_2 pressure, and etching time are 100 W, 0.1 Torr, and 14 s, respectively. Metal electrodes were then made for the patterned nanographene by electron beam lithography (or optical lithography), metal film deposition, and lifting-off techniques. As-made devices were annealed at 400 °C for 0.5 h in hydrogen atmosphere to improve contacts before any electrical measurements.

Raman Characterizations. Raman spectroscopy was carried out using a Horiba Jobin Yvon LabRAM HR-800 Raman microscope. The excitation light is a 532 nm laser, with an estimated laser spot size of 1 μm and laser power of 1 mW.

Forming Process. A certain voltage (usually ~10 V) was applied to the two electrodes of a fresh device. The current increased steadily with the voltage increasing, then dropped abruptly when the current reach ~mA. The corresponding voltage was defined as forming voltage, and the electrical breakdown process was defined as forming process. A forming process was necessary for a fresh device to activate its resistive switching behavior.

Imaging and Characterization of NG Film and Devices. An atomic force microscope (MultiMode IIId, Veeco Instruments Inc.) was used for imaging and measuring the thickness of NG film, the width and the length of the resistance switching devices, and the crack formation during the electrical breakdown process. The SEM images were obtained by the SEM mode of a Raith e-line e-beam lithography system.

Measurements of the Switching Devices. The dc sweep $I-V$ properties were characterized by an Agilent 4156C semiconductor parameter analyzer in a vacuum of $<2 \times 10^{-4}$ Torr at room temperature. The programming speed of the switching devices was measured by an Agilent 81110A pulse generator and a Keithley 4200 semiconductor characterization system (SCS). The pulse generator was connected to the probe station by using triax cables. DUT was loaded onto a sample holder inside the measurement vacuum chamber with the Ti/Au electrode pads attached to gilded probes, which were connected to the atmosphere *via* a feed-through.

Conflict of Interest: The authors declare no competing financial interest.

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Supporting Information Available: Additional figures and details. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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