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MATRIX-BASED SEARCH OF A PAIR OF COMPATIBLE i - v ORIENTATIONS FOR THE UNIQUENESS ANALYSIS OF NONLINEAR RESISTIVE CIRCUITS.

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ABSTRACT: A method based on matrix techniques for finding a pair of compatible i - v orientations is presented. The existence of such a pair of orientations is used to assess the uniqueness of the DC solution.

The method deals with circuits containing V -resistors, I -resistors, independent current and vol-tage sources, nullators and norators.

1. INTRODUCTION

THE complete solution to the DC general problem of nonlinear circuits must include three aspects [1]: assessing the uniqueness of the solutions, establishing an upper bound on its number, and calculating all DC solutions.

A line of research developed in recent years has attempted to determine the link between the circuit topology and the DC problem, which has derived in a deeper knowledge in nonlinear resistive circuits [2], [3].

In [4] and [5], a topological criterion for the existence and uniqueness of the solution of nonlinear circuits has been proposed. This criterion is based on two definitions of Graph Theory: the pair of conjugate trees and the uniform partial orientation of the resistors.

For small circuits, this question can be solved by inspection, but if the circuit is large then the search for both conditions becomes difficult.

This paper introduces a matrix-based method focussed on finding a pair of compatible i - v orientations necessary for establishing the uniqueness of the solutions of nonlinear resistive circuits.

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L. Hernández M. is holder of a scholarship from CONACyT under contract 71941.

2. EXISTENCE AND UNIQUENESS CRITERIA

The scope of our analysis is restricted to nonlinear resistive circuits containing nullators and norators, with the additional condition that nullators and norators appear in equal number [6]. Other circuit devices can be modeled by connections of basic elements, e.g. operational amplifiers and transistors.

Herein, we retake two definitions from [7] in order to set up the further development of our method:

DEFINITION 1

A nonlinear resistive circuit is assumed to contain:

- independent voltage sources
- independent current sources
- V -resistors (voltage controlled)
- I -resistors (current controlled)
- nullators
- norators

DEFINITION 2

A partial orientation of the resistors is uniform, if

- every oriented resistor is part of a uniform loop composed only by oriented resistors, norators and voltage sources, and
- every oriented resistor is part of a uniform cutset composed only by oriented resistors, norators and voltage sources.

A loop (resp. cutset) is uniform if all oriented branches in the loop (resp. cutset) are oriented in the same sense. If none resistor is oriented, then the uniform partial orientation of the resistors is considered trivial.

The definition of a pair of compatible i - v orientation is schematically shown in the Figure

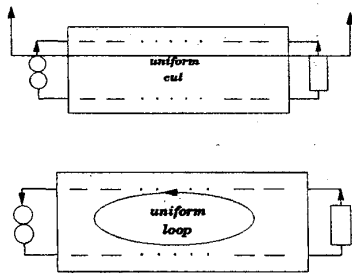


Fig. 1. The simplest pair of compatible i - v orientations.

3. OUTLINE OF THE ALGORITHM

The method is based on a modified version of the reduction-to-echelon RE algorithm [8]. The aim of the method is to generate the pair of conjugate trees (t' and t'') and a tree having nullators and norators (t_{nN}).

All trees are used in a further step to generate the loops and cutsets incidence matrices, although the loops and cutsets may not be uniform. By resorting to the colored-branch algorithm [9], the uniform orientation can be obtained. The Figure 2 shows this procedure.

3.1 Algorithm

The algorithm can be recast in the next steps:

1. Search t' and t'' with the modified RE algorithm.
2. if t' and t'' does not exist **then** the algorithm terminates **else** form t_{nN} .
3. if t_{nN} do not exist **then** the algorithm terminates **else** goto 4.
4. Form the loops and cutset matrices (C and D) for t' , t'' and t_{nN} .
5. Separate the loops and cutsets into four subsets:
 - (a) loops containing nullators λ_n .
 - (b) loops no containing nullators $\lambda_{\bar{n}}$.
 - (c) cutset containing nullators κ_n .
 - (d) cutset no containing nullators $\kappa_{\bar{n}}$.
6. Apply the colored-branch algorithm to the $\lambda_{\bar{n}}$ and $\kappa_{\bar{n}}$ sets. By taking as initial guess for coloring the no-nullator branches from λ_n and κ_n , the following:
 - Green set (G): The oriented resistors.
 - Red set (R): The branches belonging to cutsets.

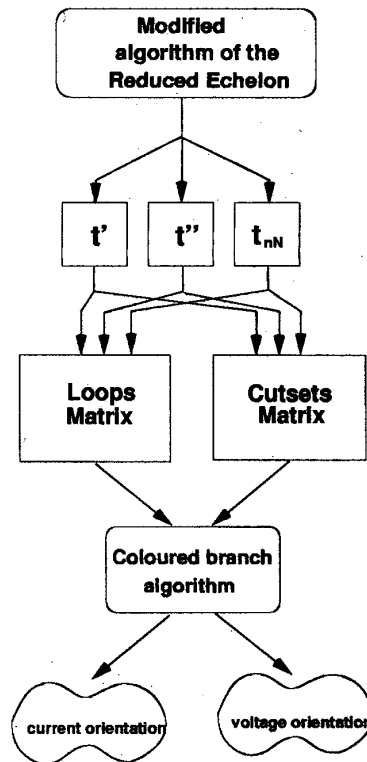


Fig. 2. General Procedure

loops.

7. if $G \cup R$ forms a loop and $G \cup B$ forms a cutset, then there exists a nontrivial of orientation **else** the algorithm terminates.

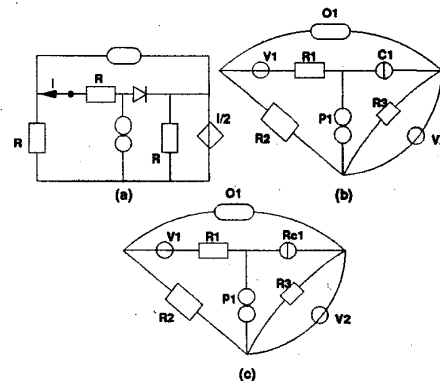


Fig. 3. Circuit for Example

4. EXAMPLE

The circuit shown in the Figure 3(a) will be used to illustrate the algorithm. The linear structure is obtained by replacing the diode

3(b). Besides, the associated linear structure is obtained by replacing the diode by the linear resistor R_{C1} , as shown in the Figure 3(c).

Firstly, the trees t' , t'' and t_{nN} , as well as their corresponding C and D matrices are obtained, which are shown in the Figures 4, 5 and 6, respectively.

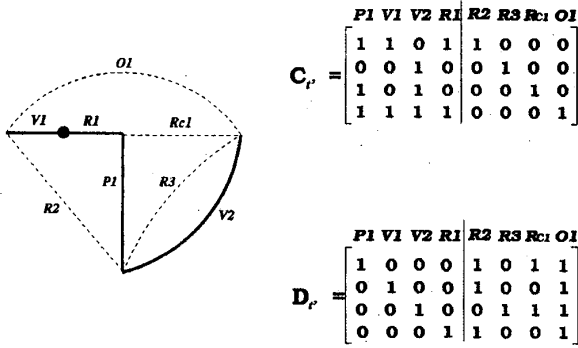


Fig. 4. The tree t' and its C and D matrices.

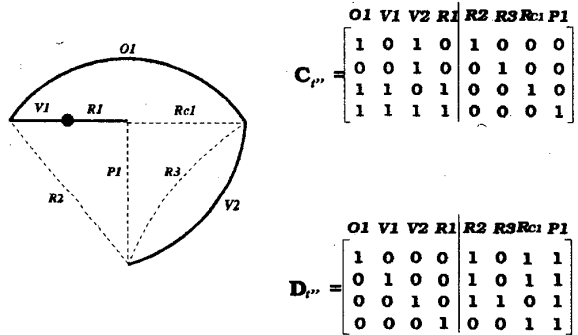


Fig. 5. The tree t'' and its C and D matrices.

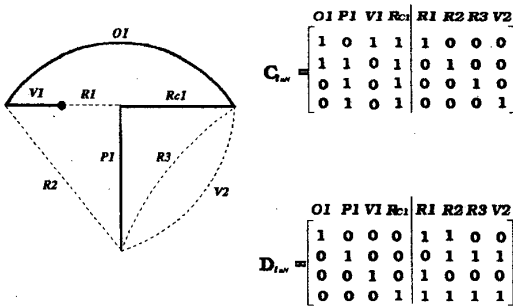


Fig. 6. The tree t_{nN} and its C and D matrices.

The four involved subset, λ_n , $\lambda_{\bar{n}}$, κ_n and $\kappa_{\bar{n}}$ are given in the Table I and II.

	loops
l_0	$\{R1, R2, V1, P1\}$
l_1	$\{R3, V2\}$
l_2	$\{R_{C1}, V2, P1\}$
l_3	$\{R3, R_{C1}, P1\}$
l_4	$\{R_{C1}, V2, P1\}$
l_5	$\{R1, V1, V2, P1, O1\}$
l_6	$\{R2, V2, O1\}$
l_7	$\{R1, R_{C1}, V1, O1\}$
l_8	$\{R2, R_{C1}, P1, O1\}$

TABLE I
LOOPS.

	cutsets
c_0	$\{R2, R_{C1}, P1, O1\}$
c_1	$\{R2, V1, O1\}$
c_2	$\{R3, R_{C1}, V2, O1\}$
c_3	$\{R1, R2, O1\}$
c_4	$\{R2, R_{C1}, V1, P1\}$
c_5	$\{R2, R3, V2, P1\}$
c_6	$\{R1, R_{C1}, P1\}$
c_7	$\{R1, V1\}$
c_8	$\{R1, R2, R3, R_{C1}, V2\}$

TABLE II
CUTSETS.

as:

$$\begin{aligned} R &= \{R_{C1}, V1, V2, P1\} \\ B &= \{R_{C1}, V1, V2, P1\} \\ G &= \{R1, R2, R3\} \end{aligned}$$

By applying the colored-branch algorithm, it yields:

$$\begin{aligned} R &= \{R_{C1}, V1, V2, P1\} \\ B &= \{R_{C1}, P1, V2\} \\ G &= \{R1, R2, R3\} \end{aligned}$$

Therefore

$$\begin{aligned} G \cup R &= \{R_{C1}, V1, V2, P1, R1, R2, R3\} \\ G \cup B &= \{R1, R2, R3, R1, R2, R3\} \end{aligned}$$

which yields the next uniform loops and cut-

$$\begin{aligned}
l_0 &= \{R1, R2, V1, P1\} \\
l_3 &= \{R3, R_{C1}, P1\} \\
l_4 &= \{R_{C1}, V2, P1\} \\
c_5 &= \{R2, R3, V2, P1\} \\
c_6 &= \{R1, R_{C1}, P1\}
\end{aligned}$$

as shown in the Figure 7.

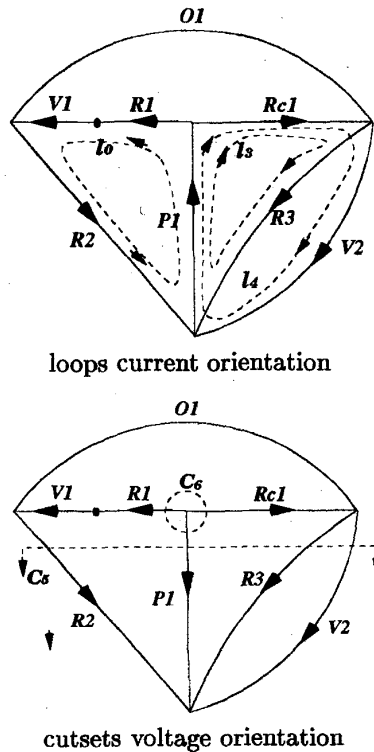


Fig. 7. The non-trivial pair of compatible $i-v$ orientations.

5. CONCLUSIONS

An algorithm for determining the nontrivial uniform partial orientations of within the graphs emanating from nonlinear resistive circuits has been presented. Although, this approach is used for circuits containing independent voltage and current sources, resistors, nullators and norators, other elements can be easily incorporated if they are substituted by an equivalent composed by basic components.

6. ACKNOWLEDGMENT

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