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In-Plane Epitaxial Growth of Silicon Nanowires and Junction Formation on Si(100) Substrates

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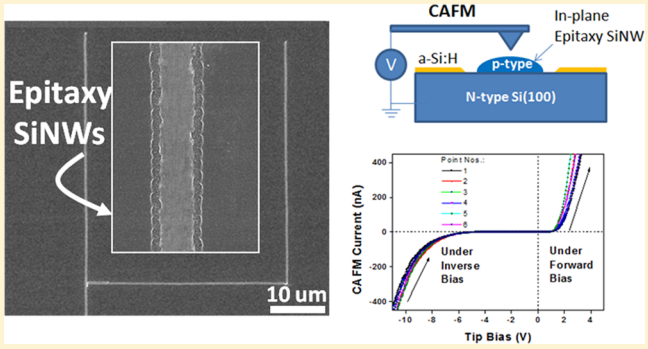
Supporting Information

ABSTRACT: Growing self-assembled silicon nanowires (SiNWs) into precise locations represents a critical capability to scale up SiNW-based functionalities. We here report a novel epitaxy growth phenomenon and strategy to fabricate orderly arrays of self-aligned in-plane SiNWs on Si(100) substrates following exactly the underlying crystallographic orientations. We observe also a rich set of distinctive growth dynamics/modes that lead to remarkably different morphologies of epitaxially grown SiNWs/or grains under variant growth balance conditions. High-resolution transmission electron microscopy cross-section analysis confirms a coherent epitaxy (or partial epitaxy) interface between the in-plane SiNWs and the Si(100) substrate, while conductive atomic force microscopy characterization reveals that electrically rectifying p−n junctions are formed between the p-type doped in-plane SiNWs and the n-type c-Si(100) substrate. This in-plane epitaxy growth could provide an effective means to define nanoscale junction and doping profiles, providing a basis for exploring novel nanoelectronics.



KEYWORDS: *In-plane nanowire, epitaxy growth, junction formation, self-assembly*

Silicon nanowires (SiNWs) are popular building blocks for developing a new generation of electronics and optoelectronics,[1,2] where precise position or orientation control of the self-assembled SiNWs, ideally in a convenient planar architecture, is a prerequisite. In the past decade, research efforts have been devoted to transferring vertically grown SiNWs via a vapor−liquid−solid (VLS) process[3] onto planar substrates with the aid of postgrowth manipulation[4,5] or by forcing them into growing in-plane by using elaborated nano holes or channels defined on substrate surface.[6,7] This is because planar electric connection or circuitry still remains the most convenient architecture for prototyping various SiNW-based functionalities. A controlled in-plane growth of SiNWs is thus considered as an important opportunity to deploy and even integrate large scale self-assembled SiNW functionalities. Recently, Tsivion and Schvartzman have demonstrated lateral epitaxial growth of ZnO or GaN nanowires via VLS mode along facet-grooves structured on miscut sapphire substrates,[8,9] which open up exciting opportunities for self-integration of nanowires into circuits. However, this in-plane epitaxial growth control strategy has not yet been explored so far in SiNWs, which are intrinsically more relevant to the established Si electronics and device integration.

Recently, we have proposed a new in-plane growth mode of SiNWs,[10−12] wherein a thin layer of hydrogenated amorphous Si (a-Si:H) deposited on a substrate, instead of gaseous silane as used in VLS process, is consumed by a surface-moving indium catalyst droplet to produce well-defined in-plane SiNWs. This in-plane solid−liquid−solid (IPSLS) growth mode has enabled a new control dimension to engineer the morphology[12,13] and growth routine of in-plane SiNWs with the aid of simple surface feature like a step-edge.[14,15]

In this work, we report on a new and interesting epitaxial growth phenomenon of in-plane SiNWs on Si(100) wafers, emphasizing the capability to achieve ultralong self-aligned SiNWs following the crystallographic orientations of the Si(100) substrate without the need for any presurface patterning. We show that a rich set of growth dynamics for epitaxial growth of in-plane SiNWs with different morphologies and growth modes can be triggered by the growth balance conditions. Conductive atomic force microscopy (CAFM) was used to reveal a rectifying transport behavior between the p-

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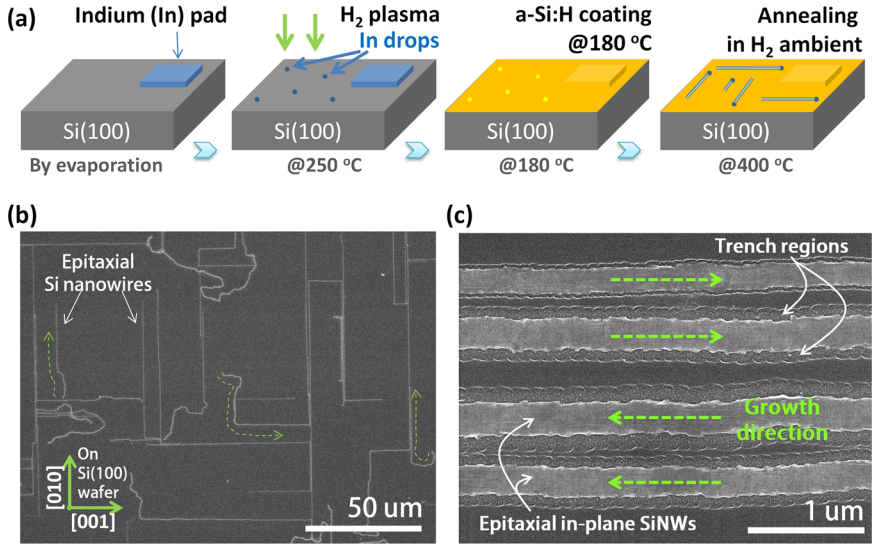

Figure 1. (a) Schematic illustration of the fabrication procedure for in-plane Si nanowires (SiNWs) growth on Si(100) wafers; (b) a typical SEM image of the as-grown epitaxial SiNWs, while (c) provides a close view of an array of parallel in-plane SiNWs but with different orientations as marked by the dashed arrows.

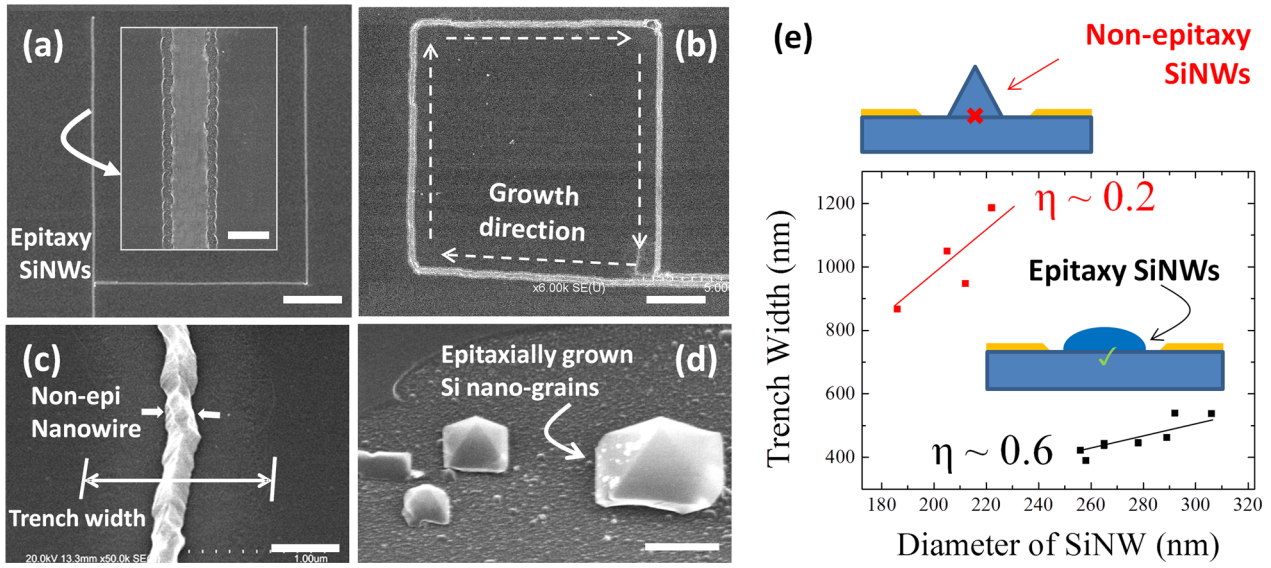

Figure 2. (a,b) The enlarged SEM images of epitaxially grown in-plane SiNWs, showing always regular orientations and 90° turnings. Scaling bars in (a) and the insets of (a) and (b) correspond to 10 μm, 300 nm, and 3 μm, respectively; (c,d) the typical SEM images of free-roaming in-plane SiNWs and discontinuous c-Si grains. Scaling bars are 500 and 250 nm. (e) The ratio of trend-width over diameter for the in-plane SiNWs grown in an epitaxial (black) mode or a nonepitaxial (red) mode.

type epitaxial SiNWs and the n-type c-Si substrate, indicating the formation of a p−n diode/junction. This epitaxial growth of in-plane SiNWs provides an interesting testing-bed to study and engineer nanoscale epitaxial growth dynamics, junction formation, and doping profiles for developing novel nanoelectronics.

Experiments. The in-plane SiNWs were grown on top of n-type Si(100) substrates in a conventional plasma enhanced chemical deposition system (PECVD). The fabrication procedure is briefly illustrated step-by-step in Figure 1a, which involves (i) first, the deposition of indium pads by thermal evaporation through the holes of a shadow mask, upon n-type Si(100) wafers (resistivity of 1−5 Ω. cm) after dipping in 5% diluted HF solution for 2 min to remove the native oxide and form a hydrogen terminated surface; (ii) then, catalyst droplet formation by H_2 plasma treatment for 2 min at substrate temperature of 350 °C in PECVD with H_2 flow rate, chamber pressure, and rf power density of 100 SCCM, 600 mTorr and 14 mW/cm^2, respectively. During this step, surface oxide layer on indium pads is removed and the indium starts to spread over the bare Si wafer surface. (iii) In the next step, an a-Si:H layer of ∼25 nm is deposited at 180 °C to cover both the Si substrate surface and the indium droplets, and (iv) finally, SiNWs growth was activated by raising the substrate temperature to 550 °C (nominal) and kept in 1Torr H_2 atmosphere for 1 h. During the final annealing step, the indium catalyst becomes molten again and starts to move around and absorb a-Si:H in the front interface and produces c-SiNW behind.

Results and Discussion. In Figure 1b, we show a typical SEM image of the in-plane SiNWs grown on a Si(100)

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substrate, where the in-plane SiNWs can be identified as ultralong straight white lines measuring hundreds of micrometers, mostly aligned with the Si[010] and Si[001] orientations in the underlying c-Si(100) substrate. A close SEM view of these epitaxially grown in-plane SiNWs is provided in Figure 1c, where four parallel in-plane SiNWs grow along the Si[001] direction with clear trench regions on both sides of each wire. Regular corrugation features were found along the trench edges and the SiNWs, which are caused by the regular vibration of liquid catalyst droplets during their in-plane growth.[10,12] Interestingly, as seen in Figure 2a,b, the turnings of the long and straight SiNWs always happen at 90°, that is, switching between mutual normal crystallographic orientations in the Si(100) substrate. Among the straight SiNWs, some random SiNWs are composed of free-roaming wires (Figure 2c) or discontinuous chains of broken islands (Figure 2d), particularly at the initial segments as indicated by the dashed green lines in Figure 1b. Details of these distinctive morphologies are shown in an enlarged SEM image in Supporting Information Figure S.1, which happens to capture all kinds of these typical in-plane growth morphologies in a close neighborhood.

We found that the epitaxially grown straight SiNWs, following exactly the substrate Si(100) orientations and regular turning, are thinner compared to the other two kinds of free-roaming SiNWs/or c-Si chains (see for example in Supporting Information Figure S.1). Closer scrutiny of Figure 2a–d reveals that shallow trench regions are formed on both sides of the SiNWs, which are actually empty regions where the a-Si:H layer has been consumed by the indium catalyst droplets. So, the width of these trenches provides a rough estimate of the width of the absorption swath of the passing indium catalyst droplet. Examining the major differences between the epitaxial SiNWs and the free-roaming nonepitaxial ones, as seen in Figure 2a–c, we found that the epitaxial wires have a relative flat top and a larger SiNW-to-trench width ratio $\eta = (d_{\mathrm{SiNW}}/d_{\mathrm{trench}}) \sim 0.6$ (according to the statistic plots in Figure 2e), while the nonepitaxy ones demonstrate roughly a triangular cross-section (corresponding to Si(111) sidewall facets, see Figure 2c) with a much lower $\eta \sim 0.2$ (see the corresponding red plots in Figure 2e). For even large catalyst droplets (inferred from their trench widths), their lateral growth produces only broken chain of c-Si grains (see Supporting Information Figure S.1) of different sizes ranging from 10 to 400 nm but still distributed with coordinated orientations and pyramidal shape (Figure 2d). This implies that an epitaxial interface/connection has been formed between them and the underlying Si(100) substrate.

These distinctive growth morphologies can be understood by analyzing the different growth balance conditions experienced by the catalyst droplets of different sizes during the in-plane growth. To formulate this growth balance condition, we assume that the influx of Si atoms absorbed at the front catalyst/a-Si:H interface is

$$J_{\mathrm{abs}} \approx \nu_{\mathrm{abs}} \frac{h_a w_c}{\Omega_{\mathrm{si}}} \sim \nu_{\mathrm{abs}} \frac{h_a w_c^{1/3}}{\Omega_{\mathrm{si}}} \tag{1}$$

where ν_{abs} is the instantaneous moving rate of the front absorption interface, h_a is the thickness of a-Si:H coating layer, w_c is the width of the catalyst droplet (equals to the trench wide), and Ω_{Si} is the atomic volume of Si atom. Considering that the dimension of catalyst droplet (in width or height) is basically proportional to the cube root of the constant catalyst volume (V_c), thus $w_c \sim h_c \sim V_c^{1/3}$. Equation 1 tells J_{abs} scales linearly with the size of catalyst droplet $V^{1/3}$. In the meantime, the flux of Si atoms deposited at the rear SiNW/catalyst interface can be approximated as

$$J_{\mathrm{dep}} \approx \nu_{\mathrm{dep}} \frac{h_{\mathrm{NW}} w_{\mathrm{NW}}}{\Omega_{\mathrm{si}}} \sim \nu_{\mathrm{dep}} \frac{h_C w_C}{\Omega_{\mathrm{si}}} \sim \nu_{\mathrm{dep}} \frac{V_C^{2/3}}{\Omega_{\mathrm{si}}} \tag{2}$$

where h_{NW} and w_{NW} stand for the height and width of the in-plane SiNW, respectively. Here, we assume the cross-section dimension of SiNW being proportional to that of the catalyst droplet. Note that for the sake of simplicity, the volume contraction effect of a-Si:H matrix when being converted into c-Si (by ratio close to unity) is not taken into account in the formulation. According to mass conservation criterion, we have

$$J_{\mathrm{abs}} = J_{\mathrm{dep}} \rightarrow \frac{\nu_{\mathrm{abs}}}{\nu_{\mathrm{dep}}} \sim V_C^{1/3} \tag{3}$$

Equation 3 gives a phenomenological trend, that is, during the in-plane growth of SiNWs, for a catalyst droplet with a larger and larger size ($V^{1/3}$), the front absorption interface will tend to develop faster than the rear deposition interface and thus stretch the produced SiNWs behind. To some extent, this force could become significant enough to break up the continuous growth of in-plane SiNWs, or causing regular deposition and detachment of the rear deposition interface from the segment of SiNWs or c-Si gains. When this happens, discrete c-Si nuclei are separately formed and developed within the large catalyst droplet volume, producing thus a chain of broken Si grains along the moving course passed by the large catalyst droplets (as seen in Figure 2d and Supporting Information S.1).

Furthermore, in the side-view SEM image in Figure 3a, we notice that the edge of the epitaxy SiNWs or the interface with the Si(100) substrate is not always continuous. Instead, it shows gaps or voids from place to place. Transmission electron microscopy (TEM, FEI Tecnai G2 F20 S-Twin) cross-section analysis of the epitaxy in-plane SiNW was then used to assess the epitaxial SiNW/Si(100) interface. In order to protect

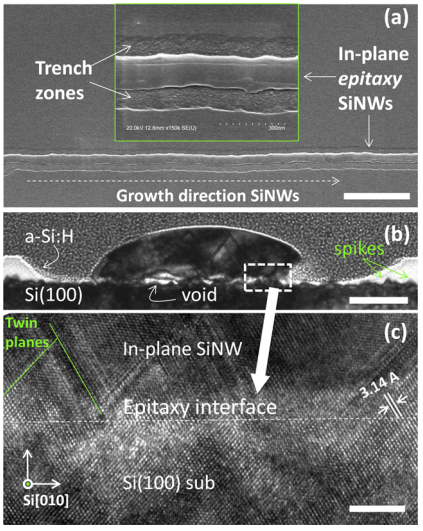

Figure 3. (a) A close SEM tilted-view of an in-plane epitaxy SiNW; (b) a cross-section TEM characterization of an epitaxy SiNW with a high resolution TEM image at the epitaxy-SiNW/Si(100) interface shown in (c). Scaling bars in (a–c) represent 1 μm, 50 nm, and 5 nm, respectively.

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crystalline SiNW from direct ion bombardment during focused gallium ion beam (FIB, FEI Helios Nanolab 600) operations, the in-plane SiNWs structure were clad with a 200 nm thick platinum on top and then milled by FIB to prepare a thin slice of cross-section of ~1 μm thick. After FIB preparation, the specimen was taken and mounted by using in situ nanomanipulator for TEM characterization.

In a low-magnification bright-field TEM image in Figure 3b, we see that the epitaxial in-plane SiNW has an ellipsoidal-like cross-section with a width of ~180 nm and a height of ~45 nm, surrounded on both sides by empty trench zones and separated from the a-Si:H matrix. The a-Si:H layer measures around 25 nm in thickness and appears brighter in the TEM imaging due to its lower density compared to that of the c-Si matrix. At the SiNW/Si(100) substrate interface, high-resolution TEM imaging (Figure 3c) reveals several coherent epitaxial connection zones between the in-plane SiNWs and the underlying c-Si(100) substrate, while voids are also found at the SiNW/Si(100) interface as indicated in Figure 3b. We notice that there are plenty of twin planes found among the lattice of epitaxially grown in-plane SiNWs, as seen for example in the TEM cross-section overview in Figure 3b and the HR-TEM image in Figure 3c. Actually, most of the twin planes originate and extend from the SiNW/Si(100) interface, indicating that they could arise from the structure defects at the Si(100) substrate surface. On the other hand, such twin planes or stacking faults are also commonly found among self-assembly growth of SiNWs, particularly at a relatively low-temperature process as a result of local growth kinetic variations.[2,14,15]

These observations confirm that the epitaxial interface has been formed during the in-plane growth of SiNWs, which helps to direct them into exact crystallographic Si[010] or Si[001] orientations. In addition, we also carried out similar experiments on Si(111) substrates but most of the in-plane SiNWs grown there are found as free-roaming ones (not shown here). This is reasonable if one recalls that epitaxy growth of Si on Si(100) is easier than that upon Si(111) interface.[16−19] Though epitaxy layer-by-layer growth of Si atoms on a Si(111) facet has been commonly observed in relatively thick VLS-grown SiNWs catalyzed by noble metal particles,[20,21] epitaxy growth on Si(111) surface involves essentially a bilayer ledge-flow dynamics, which is energetically less efficient compared to the situation on Si(100) surfaces, where new adatoms can be easily stabilized by bonding two neighboring Si atoms on the lower surface atomic layer leading to an effective epitaxy growth.

A closer view of the a-Si:H−Si(100) interface in Figure 3b reveals still some remarkable features; for example, there are many tiny faceted spikes of only several nanometers height, extending from the a-Si:H−Si(100) interface into the a-Si:H coating layer. This interface roughness does not exist before annealing growth (as confirmed by separate SEM and TEM examinations). It is possible that these tiny spikes result from a solid phase epitaxy (SPE) process[22,23] taking place at the a-Si:H−Si(100) interface during the high temperature annealing step without the involvement of metal catalyst.[24] Actually, the existence of such SPE-grown spikes may have important impact upon the epitaxial growth of in-plane SiNWs. The formation of these tiny c-Si spikes convert a portion of the flat Si(100) interface into incline Si(111) facets, as illustrated in Figure 4a,b, which are known to be energetically stable facets[25] but less efficient or favorable for an epitaxy growth.[24] As a consequence, the in-plane epitaxial SiNWs grown over the spike-populated

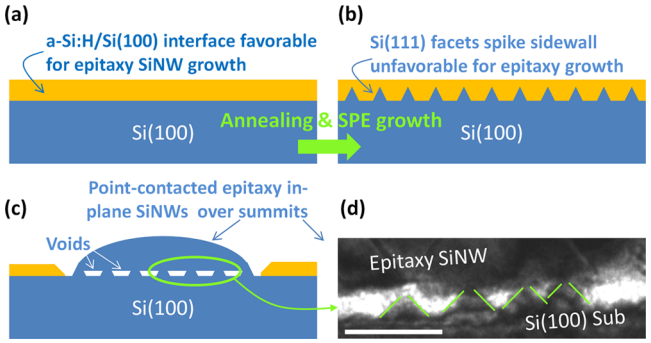

Figure 4. (a,b) Schematic depiction of the formation of tiny c-Si spikes at the a-Si:H−Si(100) interface during annealing via a solid-phase-epitaxy (SPE) mechanism; (c) the situation where the in-plane SiNWs form epitaxial contacts with the SPE-grown spikes summits with a corresponding cross-section TEM image at the interface shown in (d). Scaling bar in (d) is 50 nm.

Si(100) surface could eventually develop coherent epitaxial point-contacts through the spike summits to the underlying Si(100) substrate, as schematically depicted in Figure 4c and witnessed indeed in the TEM image in Figure 4d. This behavior may explain why the SiNW/Si(100) epitaxy interface (though energetically favorable) is not always continuous all the way during the in-plane growth of SiNWs. Nevertheless, it is very important to note that these regional epitaxial point-contacts can still guarantee an effective guided growth of the ultralong parallel and straight in-plane SiNWs. We suggest that these unique spiky epitaxial point-contacts could find advantages for the subsequent detachment and transferring of the in-plane SiNWs onto foreign flexible substrates.

To evaluate the electrical connection between the in-plane epitaxy SiNW and the Si(100) substrate, we use conductive atomic force microscopy (CAFM Bruker, Nanoscope 3D Multimode AFM) to probe the local voltage−current characteristics, where a n-type Si(100) wafer was used as a grounded substrate, while the conductive AFM tip (Si cantilever coated with Pt−Ir) was biased under different voltages. It is important to note that because the indium catalyst atoms get incorporated into the SiNWs during the growth, the as-produced in-plane SiNWs become effectively p-type doped, which has been confirmed by atomic probe tomography (APT) characterizations[26] or inferred from the SiNW FET transfer properties reported in our previous studies.[27] If the p-type SiNW is indeed epitaxially grown upon an n-type Si substrate, there should be a well-defined p−n junction with rectifying diode behavior in a vertical transport characteristic as configured in a way depicted in Figure 5c. To check out, we first carry out a CAFM current mapping scan under different bias voltages V_{tip} = 0, −1, and 1 V. The corresponding AFM morphology and CAFM current mapping of a segment of in-plane epitaxy SiNWs are shown together in Figure 5a,d, respectively. Note that the norm of I_{tip} current in Figure 5d has been displayed in log-scale. It shows that only the epitaxially grown SiNWs give the highest current responses under positive tip voltage of V_{tip} = 1 V, while the regions covered with a-Si:H layer (which are basically intrinsic and highly resistive) give on average much lower current.

Furthermore, we manage to position the CAFM tip directly upon one straight in-plane epitaxy SiNW (as seen for example in the AFM morphology image in Figure 5a and its corresponding line-section profile in Figure 5b). Then, we sample six different locations, record their local current−voltage

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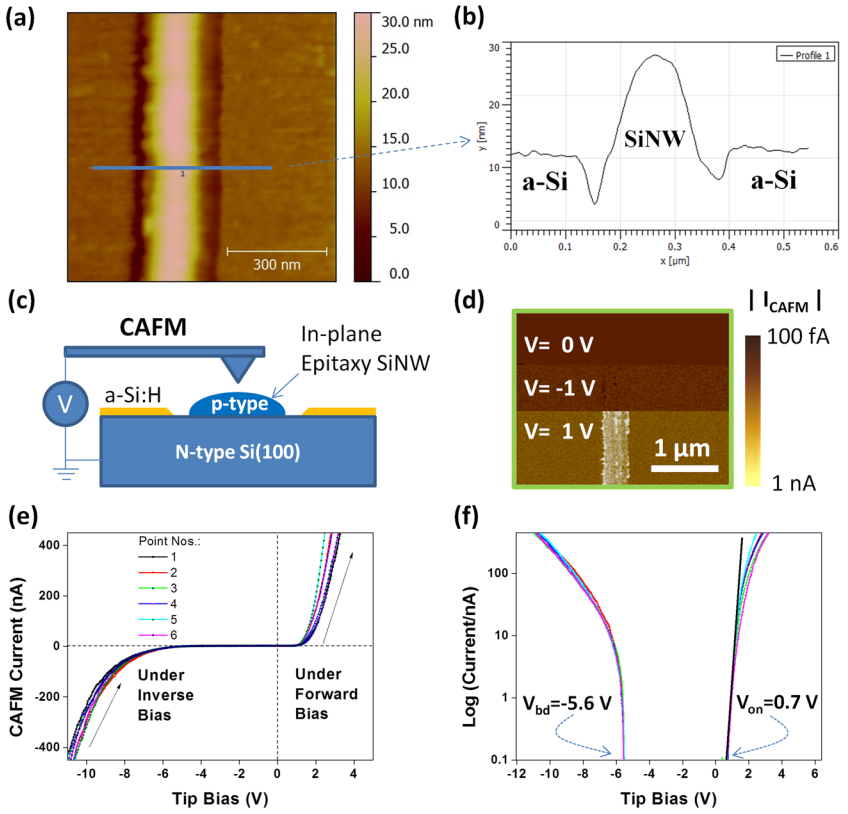

Figure 5. (a) AFM image of an in-plane epitaxial SiNW with a line-profile analysis presented in (b); (c) the conductive AFM setup and junction for the electric characterization; (d) the CAFM current mapping of an in-plane epitaxy SiNW under different bias voltages; (e,f) the $I-V$ characteristics through the junction between the p-type epitaxial SiNW and the n-type Si(100) substrate in linear or log-normal plots, respectively.

($I-V$) curves and present them in Figure 5e. As we can see, under positive bias ($V_{tip} > 0$ V) the current increases exponentially when surpassing a turn-on Knee voltage of V_{on} = 0.7 V (defined here at the voltage when I_{on} = 0.1 nA as indicated in the log-plot inset of Figure 5f). Under negative bias, the current shows a low off-value until a repeatable nondestructive breakdown happens at voltages around V_{bd} = −5.6 V, which is a typical onset voltage for a mixed Zener-avalanche breakdown of a lightly doped Si p−n junction diode.[28,29] The apparent ideality factors for the epitaxy p−n junction diode (under positive bias) are extracted to be around $n^* \sim 3.7$, according to the formulation of $I_{on} \sim \exp(V/n^*kT)$. However, considering the fact that there is always an electric contact resistance R_{ct} between the CAFM tip and the in-plane SiNW (see Figure 5c), when the diode turns into an "on" state, this resistance could leverage a significant portion of applied voltage V, leading to the situation that the actual bias over the SiNW/Si(100) junction becomes $V_{diode} = \eta V$ (with $\eta < 1$), and thus the apparent ideality factor being overestimated by $n^* = n/\eta$. Of course, a more stable and reliable connection to the in-plane SiNWs has to be established to eliminate completely this side-effect, which will be addressed in our future works. Nevertheless, we emphasize that these vertical CAFM transport characterizations provide a straightforward and convincing evidence that a reasonably good p−n diode/junction has been established between the epitaxial in-plane SiNWs and the Si(100) substrate, which could provide an important basis and indicate a new strategy to define self-assembly nanoscale p−n junction profile for nano electro- or optoelectronic applications.

In summary, we report a novel approach to grow self-assembled and oriented in-plane SiNWs on c-Si(100) wafers, thanks to a coherent epitaxy (or partial epitaxy) interface formed between the in-plane SiNWs and the underlying c-Si substrate, as confirmed by cross-section TEM characterization. A rich set of growth morphologies has been observed under different growth balance conditions. Furthermore, conductive AFM characterizations have confirmed that a rectifying p−n junction has been formed between the intrinsically p-type epitaxy in-plane SiNWs and the n-type Si substrate, implicating potential application in defining nanoscale functional devices based on the self-aligned in-plane SiNWs.

■ ASSOCIATED CONTENT

Supporting Information

Extra experimental characterizations that show three kinds of typical morphologies of the in-plane growth of SiNWs. This material is available free of charge via the Internet at http://pubs.acs.org.

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Notes

The authors declare no competing financial interest.

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