Memory homework

1 Suppose we have 4 blocks cache with tag and valid bits. The processor will execute the data from memory address 2, 1, 3, 3, 5, 1, 6, 7 respectively. How many hit and miss if the cache are

1.1 directed mapped,

memory address

1 mod 4 = 1_{10} = 01

2 mod 4 = 2_{10} = 10

3 mod 4 = 3_{10} = 11

5 mod 4 = 1_{10} = 01

6 mod 4 = 2_{10} = 10

7 mod 4 = 3_{10} = 11

Order set of address 2 1 3 3 5 1 6 7

00	
01	~~1~~ ~~5~~ ~~1~~
10	~~2~~ 6
11	~~3~~ 7

Miss	IIIIIII
Hit	I

Answer : miss 7 times , hit 1 time

1.2 2-ways set associative,

2-ways set mean it only has 2 cache block but 2 tag bit so it will modulus by 2

memory address

1 mod 2 = 1

2 mod 2 = 0

3 mod 2 = 1

5 mod 2 = 1

6 mod 2 = 0

Order set of address 2 1 3 3 5 1 6 7

0	2	6
1	~~1~~ ~~5~~ 7	~~3~~ 1

Miss	IIIIIII
Hit	I

Answer : miss 7 times , hit 1 time

1.3 fully-set associative cache.

It is fully-set cache so it do not care about the tag bit

Order set of address 2 1 3 3 5 1 6 7

~~2~~ 6	~~1~~ 7	3	5

Miss	IIIIII
Hit	II

Answer : miss 6 times , hit 2 time

---

2. Suppose we have 8 blocks cache with tag and valid bits. The processor will execute the data from memory address 4, 2, 6, 6, 10, 2, 12, 14, 11 respectively. How many hit and miss if the cache are

2.1 directed mapped,

Memory address

$2 \bmod 8 = 2_{10} = 010_2$

$4 \bmod 8 = 4_{10} = 100_2$

$6 \bmod 8 = 6_{10} = 110_2$

$10 \bmod 8 = 2_{10} = 010_2$

$11 \bmod 8 = 3_{10} = 011_2$

$12 \bmod 8 = 4_{10} = 100_2$

$14 \bmod 8 = 6_{10} = 110_2$

Order set of memory address

4 2 6 6 10 2 12 14 11

000	
001	
010	~~2~~ ~~10~~ 2
011	11
100	~~4~~ 12
101	
110	~~6~~ 14
111	
Miss	IIIIIIII
Hit	I

Answer : miss 8 times , hit 1 time

2.2 2-ways set associative,

Memory address

2 mod 4 = 2_{10} = 10_2

4 mod 4 = 0_{10} = 00_2

6 mod 4 = 2_{10} = 10_2

10 mod 4 = 2_{10} = 10_2

11 mod 4 = 3_{10} = 11_2

12 mod 4 = 0_{10} = 00_2

14 mod 4 = 2_{10} = 10_2

Order set of memory address

4 2 6 6 10 2 12 14 11

00	4	12
01		
10	~~2~~ ~~10~~ 14	~~6~~ 2
11	11	

Miss	IIIIIIII
Hit	I

Answer : miss 8 times , hit 1 time

2.3 4-ways set associative,

Memory address

2 mod 2 = 0_{10} = 0_2

4 mod 2 = 0_{10} = 0_2

6 mod 2 = 0_{10} = 0_2

10 mod 2 = 0_{10} = 0_2

11 mod 2 = 1_{10} = 1_2

12 mod 2 = 0_{10} = 0_2

14 mod 2 = 0_{10} = 0_2

Order set of memory address

4 2 6 6 10 2 12 14 11

0	~~4~~ 12	~~2~~ 14	6	10
1	11			

Miss	IIIIIII
Hit	II

Answer : miss 7 times , hit 2 time

2.4 fully-set associative cache.

Order set of memory address

4 2 6 6 10 2 12 14 11

4	2	6	10	12	14	11	

Miss	IIIIIII
Hit	II

Answer : miss 7 times , hit 2 time

---

3. From Question 1 and 2, Suppose memory address is 4 bits. How many tag bits and valid bits of

3.1 directed mapped cache,

Question 1 has 2 tag bit 3 valid bit
Qusetion 2 has 3 tag bit 4 valid bit

3.2 2-ways set associative cache,

Question 1 has 1 tag bit 2 valid bit
Qusetion 2 has 2 tag bit 3 valid bit

3.3 4-ways set associative cache

Question 1 has 0 tag bit 0 valid bit
Qusetion 2 has 1 tag bit 2 valid bit

3.4 fully-set associative cache

Question 1 has 0 tag bit 1 valid bit
Qusetion 2 has 0 tag bit 1 valid bit

4. Suppose we have a processor with a base CPI of 2.0, assuming all references hit in the primary cache, and a clock rate of 2 GHz. Assume a main memory access time of 100 ns, including all the miss handling. Suppose the miss rate per instruction at the primary cache is 5%. How much faster will the processor be if we add a secondary cache that has a 5 ns access time for either a hit or a miss and is large enough to reduce the miss rate to main memory to 0.5%?

We know

CPI = 2

Clock rate = 2 GHz

Primary cache = 5%

Main memory access time = 100 ns

Secondary cache = 5 ns

Miss rate = 0.5%

solution

Miss penalty = main memory access time / clockrate

= 200 clock cycle

TotalCPI = baseCPI + cycle per instruction

= 2 + (5% x 200) = 12

Two level of cahing = secondary cache / clock rate

= 5/0.5 = 10

TotalCPI = baseCPI + primarystall + secondarystall

= 2 + (5%x10) + (0.5% x 200) = 3.5

Answer: the secondary cache is faster by 12 / 3.5 = 3.43