MEMORY HOMEWORK

1. Suppose we have 4 blocks cache with tag and valid bits. The processor will execute the data from memory address 2, 1, 3, 3, 5, 1, 6, 7 respectively. How many hit and miss if the cache are directed mapped, 2-ways set associative, fully-set associative cache.

- 2. Suppose we have 8 blocks cache with tag and valid bits. The processor will execute the data from memory address 4, 2, 6, 6, 10, 2, 12, 14, 11 respectively. How many hit and miss if the cache are directed mapped, 2-ways set associative, 4-ways set associative, fully-set associative cache.

3. From Question 1 and 2, Suppose memory address is 4 bits. How many tag bits and valid bits of directed mapped cache, 2-ways set associative cache, 4-ways set associative cache and fully-set associative cache

MEMORY HOMEWORK 3

Suppose we have a processor with a base CPI of 2.0, assuming all references hit in the primary cache, and a clock rate of 2 GHz. Assume a main memory access time of 100 ns, including all the miss handling. Suppose the miss rate per instruction at the primary cache is 5%. How much faster will the processor be if we add a secondary cache that has a 5 ns access time for either a hit or a miss and is large enough to reduce the miss rate to main memory to 0.5%?