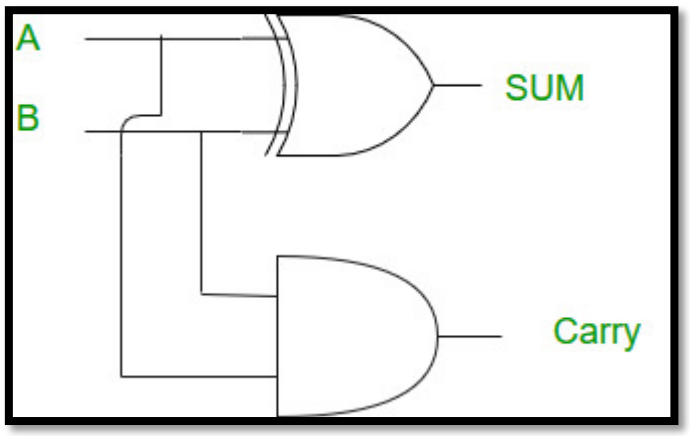
Half adder:

A half adder is a digital logic circuit that performs binary addition of two single-bit binary numbers. It has two inputs, A and B, and two outputs, SUM and CARRY. The SUM output is the least significant bit (LSB) of the result, while the CARRY output is the most significant bit (MSB) of the result, indicating whether there was a carry-over from the addition of the two inputs. The half adder can be implemented using basic gates such as XOR and AND gates

Logic Circuit:



Truth Table:

A	B	Sum	Carry
0	**0**	**0**	**0**
0	**1**	**1**	**0**
1	**0**	**1**	**0**
1	**1**	**0**	**1**

Verilog Code:

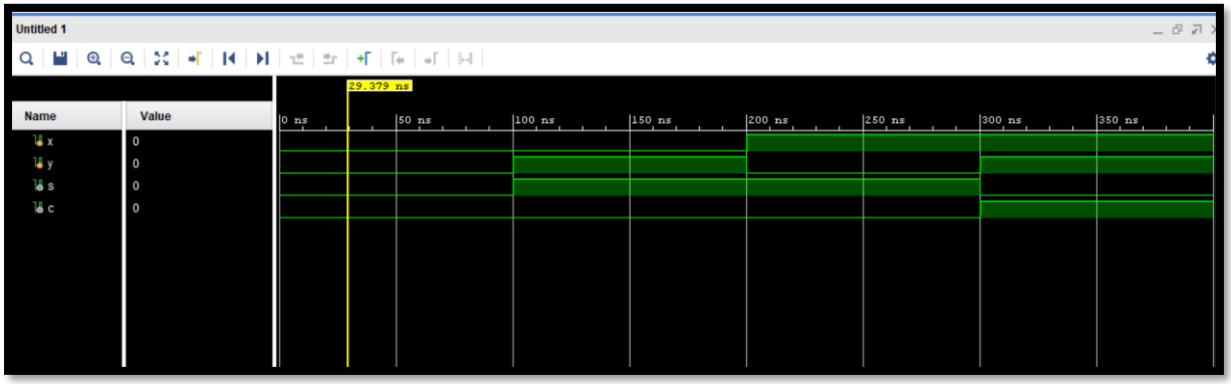
```
module half_adder(a,b,s,c);
input a,b;
output s,c;
assign s=a^b;
assign c=a&b;
endmodule
```

Testbench:

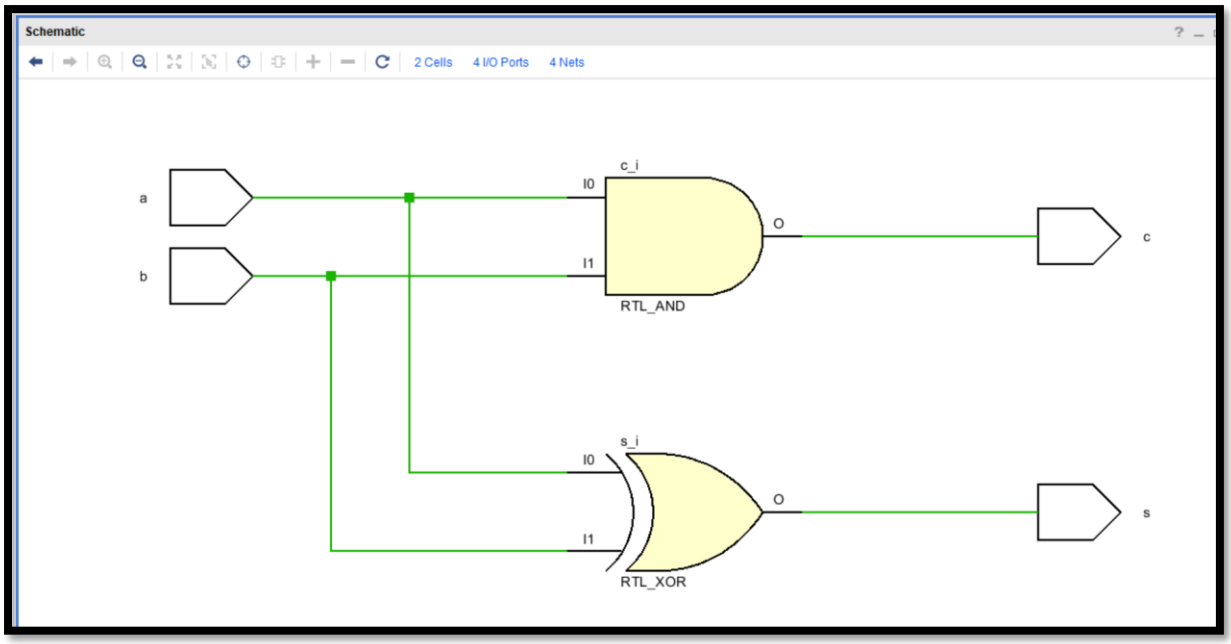
```
module half_adder_tb();
reg x,y;
wire s,c;
half_adder h1(x,y,s,c);
initial
begin
x=0;y=0;
#100
x=0;y=1;
#100
x=1;y=0;
```

	#100
	x=1;y=1;
	#100 $finish;
	end
	initial
	begin
	$display("\t\t\t\tTime\tx\ty\ts\tc");
	$monitor($time,"\t",x,"\t",y,"\t",s,"\t",c);
	end
	endmodule

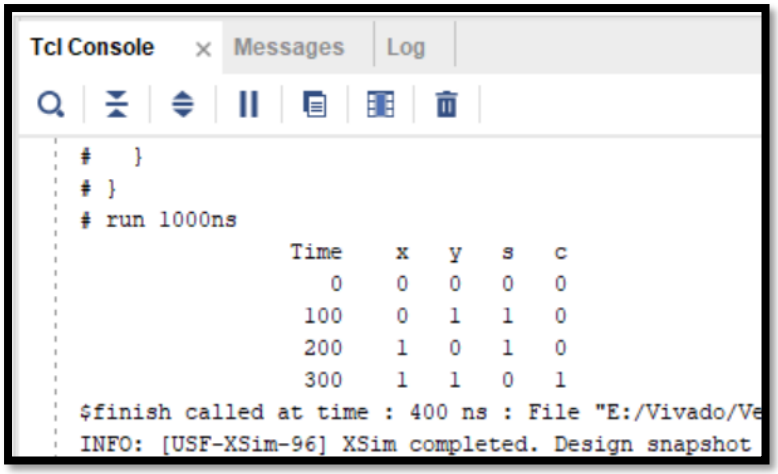
Simulation:



RTL Design:



Tcl Console:



Application:

1.Arithmetic circuits: Half adders are utilized in number-crunching circuits to add double numbers. At the point when different half adders are associated in a chain, they can add multi-bit double numbers.

2.Data handling: Half adders are utilized in information handling applications like computerized signal handling, information encryption, and blunder adjustment.

3.Address unravelling: In memory tending to, half adders are utilized in address deciphering circuits to produce the location of a particular memory area.

4.Encoder and decoder circuits: Half adders are utilized in encoder and decoder circuits for computerized correspondence frameworks.

5.Multiplexers and demultiplexers: Half adders are utilized in multiplexers and demultiplexers to choose and course information.

6.Counters: Half adders are utilized in counters to augment the count by one.