

```

1  GPIO_PORTB_DATA EQU 0x400053FC
2
3  AREA init_isr , CODE, READONLY, ALIGN=2
4  THUMB
5  EXTERN stepper
6  EXTERN delay
7  EXTERN init_port_b
8  EXTERN InitSysTick
9  EXPORT __main
10
11 __main PROC
12 BL init_port_b
13 BL InitSysTick
14 CPSIE I
15 LDR R10,=0x20000400
16 MOV R1,#0
17 STRB R1,[R10]
18
19
20 debnc_inp LDR R1,=GPIO_PORTB_DATA ;Debounce algorithm for pressing
21 LDR R10,[R1] ;wait a delay between two data
22 BL delay ;samples and if they are the same
23 LDR R1,=GPIO_PORTB_DATA ;it continues to check columns
24 LDR R9,[R1]
25 CMP R9,R10 ;it loads the data onto R9 reg.
26 BEQ devam
27 B debnc_inp
28
29 devam AND R8,R9,#0x0F
30 CMP R8,#0xF
31 BEQ debnc_inp
32
33 debnc_out LDR R1,=GPIO_PORTB_DATA ;This debounce part looks for the
34 LDR R7,[R1] ;relase of the key
35 AND R6,R7,#0xF ;if it sees an input it loops until
36 CMP R6,#0xF ;it does not see one.
37 BNE debnc_out ;It also double checks with a
38
39 delayed time BL delay
40 LDR R1,=GPIO_PORTB_DATA
41 LDR R9,[R1]
42 AND R6,R9,#0xF
43 CMP R6,#0xF
44 BNE debnc_out
45
46 LDR R10,=0x20000400
47 MOV R0,#1
48 CMP R8,#0x7
49 STREQ R0,[R10]
50 BEQ cont
51 MOV R0,#2
52 CMP R8,#0xB
53 STREQ R0,[R10]
54 BEQ cont
55
56 LDR R10,=0x20000401
57 MOV R0,#3
58 CMP R8,#0xD
59 STREQ R0,[R10]
60 BEQ cont
61 MOV R0,#4
62 CMP R8,#0xE
63 STREQ R0,[R10]
64 BEQ cont
65
66 cont B debnc_inp
67 ENDP
68 ALIGN
69 END

```