

# Obed K. Allotey Babington

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## SUMMARY

Dedicated to advancing AI for edge systems, with a focus on leveraging reconfigurable computing to accelerate machine learning inference. Actively seeking PhD opportunities for Fall 2026 and beyond to contribute to cutting-edge research in these areas.

## EDUCATION

**B.Sc. (Hons) Computer Engineering, Ashesi University** 2021 – 2025  
Cumulative GPA: 3.84/4.0

**Relevant Courses:** Embedded Systems, Digital System Design, Internet of Things (IoT), Deep Learning, Circuits and Electronics, Data Structures and Algorithms, Object-Oriented Programming.

## HONORS & AWARDS

<b>IEEE Memberships:</b> Student Member, Young Professionals, Computer Society	2024 – Present
<b>Magna Cum Laude</b> , Ashesi University	Jun 2025
<b>Technical Excellence Award in Computer Engineering</b> , Ashesi University	May 2025
<b>Dean's List</b> (All semesters), Ashesi University	Sep 2021 – Jun 2025
<b>Selected for Study Abroad</b> , University of Toronto Exchange Program	May 2024
<b>1st Place</b> , Ashesi D:Lab Hackathon	Nov 2022
<b>TEDx Speaker</b> , TEDxAshesiUniversity	Apr 2022

## WORK EXPERIENCE

**Research Assistant** Smart Technologies Lab, Ashesi University  
*Aug 2025 – Present*

- Conducting research on **embedded machine learning (TinyML)** solutions for deploying AI models on resource-constrained microcontrollers and SoC for local applications.
- Designing and implementing **hardware acceleration strategies** for neural network inference using **FPGAs (Xilinx Artix-7, ZYNQ-7000)** with custom accelerators and **co-design methodologies** involving softcore processors (**MicroBlaze**).
- Benchmarking performance across microcontrollers and FPGA-based accelerators, analyzing **latency and energy efficiency trade-offs**.

**Research Consultant (Intern)** Schneider Electric Sustainability Business  
*May 2025 – Jul 2025* Wooster, Ohio

- Through the AMRE Program at the College of Wooster, collaborated with a research team to design and prototype an **Energy Management Co-Pilot** using large language models (LLMs) and autonomous agent architectures.
- Developed an **evaluation pipeline** leveraging LlamaIndex's **CorrectnessEvaluator** to assess agent responses against ground-truth datasets across multiple query categories.
- Delivered a **35-minute final presentation** to Schneider Electric's Sustainability Business team and co-authored a **66-page technical report** documenting research findings, methodologies, and recommendations.

**Undergraduate Research Assistant**  
*May 2024 – Sep 2024*

Smart Technologies Lab, Ashesi University

- Investigated hardware acceleration of **neural network inference** using a Xilinx Basys 3 Artix-7 FPGA in parallel communication with microcontroller units (MCUs).
- Interfaced the FPGA with both an 8-bit Arduino Uno and a 32-bit Freedom KL25Z MCU, analyzing the effect of MCU **bit-width architecture** on inference latency.
- Demonstrated up to **86% performance improvement** in inference execution time across both MCU platforms through FPGA-based acceleration.

**Telematics Engineer (Intern)**  
*Jun 2023 – Dec 2023*

Swoove360, Accra, Ghana

- Contributed to the launch of **Fleet360**, a fleet management platform designed to optimize vehicle operations in Ghana.
- Configured and synchronized telematics devices with company servers and APIs, ensuring reliable **real-time data streaming**.
- Maintained and managed a ledger of SIM cards for device connectivity, supporting data integration with Swoove360's API endpoints.
- Authored and updated comprehensive telematics documentation, enhancing troubleshooting workflows and system optimization across engineering operations.

## SELECTED PROJECTS

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**Hardware-Accelerated Embedded ML on a Softcore Processor** Sep 2024 – May 2025

Designed and deployed a hardware–software co-designed embedded ML system by integrating a **MicroBlaze softcore processor** with a custom neural network accelerator on an FPGA. Achieved a **420× inference speedup** over the softcore baseline, eliminating off-chip latency and enabling real-time inference for edge AI and IoT applications.

**On-Chip vs. Off-Chip FPGA Acceleration for Embedded ML** Sep 2024 – May 2025

Conducted a comparative study evaluating communication latency in hardware-accelerated embedded ML systems by benchmarking **4 distinct hardware configurations** across softcore and silicon microcontrollers in on- and off-chip acceleration scenarios. Demonstrated a **9369% improvement** in the on-chip accelerated configuration, validating and quantifying communication overhead impact on inference latency.

**Real-Time Morse Code Decoder as Embedded Neural Network** Sep 2024 – Dec 2024

Developed a **multilayer perceptron (MLP) decoder** for Morse code sequences, trained on STM32-collected button-press timing data with preprocessing and early stopping. Deployed inference on both STM32 (**bare-metal C**) and MicroBlaze/FPGA (**C/C++ in Vitis**). Achieved **85.58% accuracy** on evaluation data, and the project served as a benchmarking workload for subsequent embedded ML acceleration research.

**Automation of a Robotic Vehicle** Nov – Dec 2024

Designed a remotely operated vehicle in register-level, bare-metal C using **dual microcontrollers** (M0 and M7) with **UART-based communication**. Integrated advanced embedded systems capabilities on the **STM32 M7**, including **RTOS-based task scheduling**, variable speed control, keypad-driven motion, and built-in self-test features.

**Automatic Speech Recognition System for Asante Twi Language** Nov – Dec 2024

Developed an **Encoder–Decoder LSTM model** for automatic speech recognition of Asante Twi. Despite limited linguistic resources, achieved an average **Word Error Rate (WER) of 20%** on test data, demonstrating the feasibility of deep learning for low-resource African languages.

## Tennis Scoreboard Digital System Design

Jun – Jul 2024

Engineered a digital tennis scoring system on a Xilinx Basys 3 Artix-7 FPGA using dual **VHDL architectures** (structural with JK flip-flops and behavioral with FSM). Verified functionality through testbenches and validated outputs on 7-segment displays.

## 32-bit Single-Cycle MIPS Processor Components in VHDL

Mar – Apr 2024

Designed and simulated components of a 32-bit single-cycle **MIPS processor**, implementing arithmetic, logical, control-flow, and memory instructions. Verified correctness with comprehensive **ModelSim testbenches**.

## Low-Cost Optical Heartbeat Monitoring System

Mar – Apr 2024

Constructed an optical heartbeat monitoring device using an **infrared LED and phototransistor**. Designed a multi-stage **active filter and amplifier chain** for signal conditioning, validated outputs via oscilloscopes, and converted frequency measurements to beats per minute for real-time monitoring.

## Estimating the Impact of Soiling on Solar Panels

Jan – May 2023

Collaborated on developing **IoT-based embedded models** to quantify the soiling effect on solar panels. Engaged with industry partners to evaluate products and align system specifications with project requirements.

# RESEARCH LEADERSHIP & ENGAGEMENT

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## President, Ashesi Research Club

Ashesi University

*June 2023 – June 2024*

- Served as the first active president of the Ashesi Research Club, expanding students' understanding of the research landscape and fostering a culture of scholarship and innovation.
- Co-organized the **first-ever campus-wide research festival**, themed “*Exploring New Horizons*”, under the auspices of the Provost's Office, to celebrate student research and inspire future inquiry.
- Directed the development of research workshops, championed student-led research projects, and supported proposal writing, leading to increased engagement and measurable growth in undergraduate research output.

## Research and Innovation Lead, Arm(E<sup>3</sup>)NGAGE Student Club

Ashesi University

*May 2023 – May 2024*

- Led engineering projects within a collaboration between ARM and Ashesi University to advance student knowledge in **IoT and embedded systems** using ARM technologies.
- Directed development of an **automated parking system**, conducting Arduino C workshops, introducing GitHub for collaborative development, and mentoring peers in algorithmic problem-solving.
- Authored project documentation and design outlines to ensure clarity, reproducibility, and knowledge transfer.
- Built a network of student researchers in engineering and computer science, resulting in the production of **five research articles** and pioneering a research-driven culture within the club.

# SKILLS & LANGUAGES

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**Hardware:** ARM Cortex-M (STM32), FPGA (Xilinx Artix-7, ZYNQ-7000), Arduino, ESP32, Raspberry Pi, Oscilloscopes, Signal Generators

**Programming:** Embedded C, VHDL, Python, Java, MATLAB, C++, Assembly

**Tools:** Vivado, Vitis IDE, ModelSim, Logisim Evolution, Git/GitHub, Linux/UNIX, VS Code, Microsoft Office Suite, Notion

# LICENSES & CERTIFICATIONS

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- **Embedded Systems Essentials with Arm: Getting Started**, edX Issued Jan 2025
- **Operating Systems Basics**, Cisco Issued Dec 2024
- **Python & Data Science Foundations**, DataCamp Issued Jun 2023  
(Courses: Introduction to Python, Intermediate Python, Data Manipulation with Pandas, Joining Data with Pandas, Introduction to Statistics in Python)