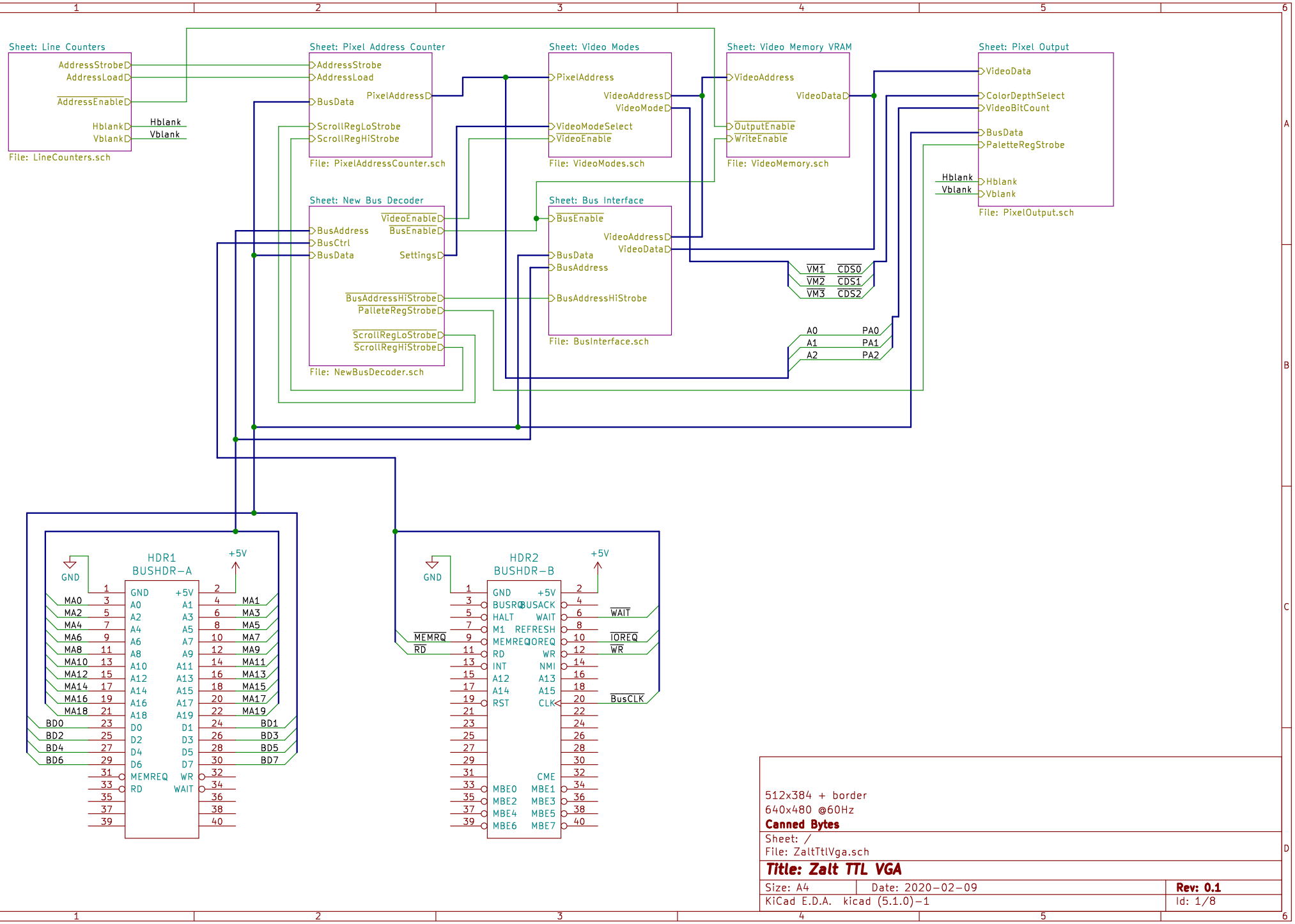
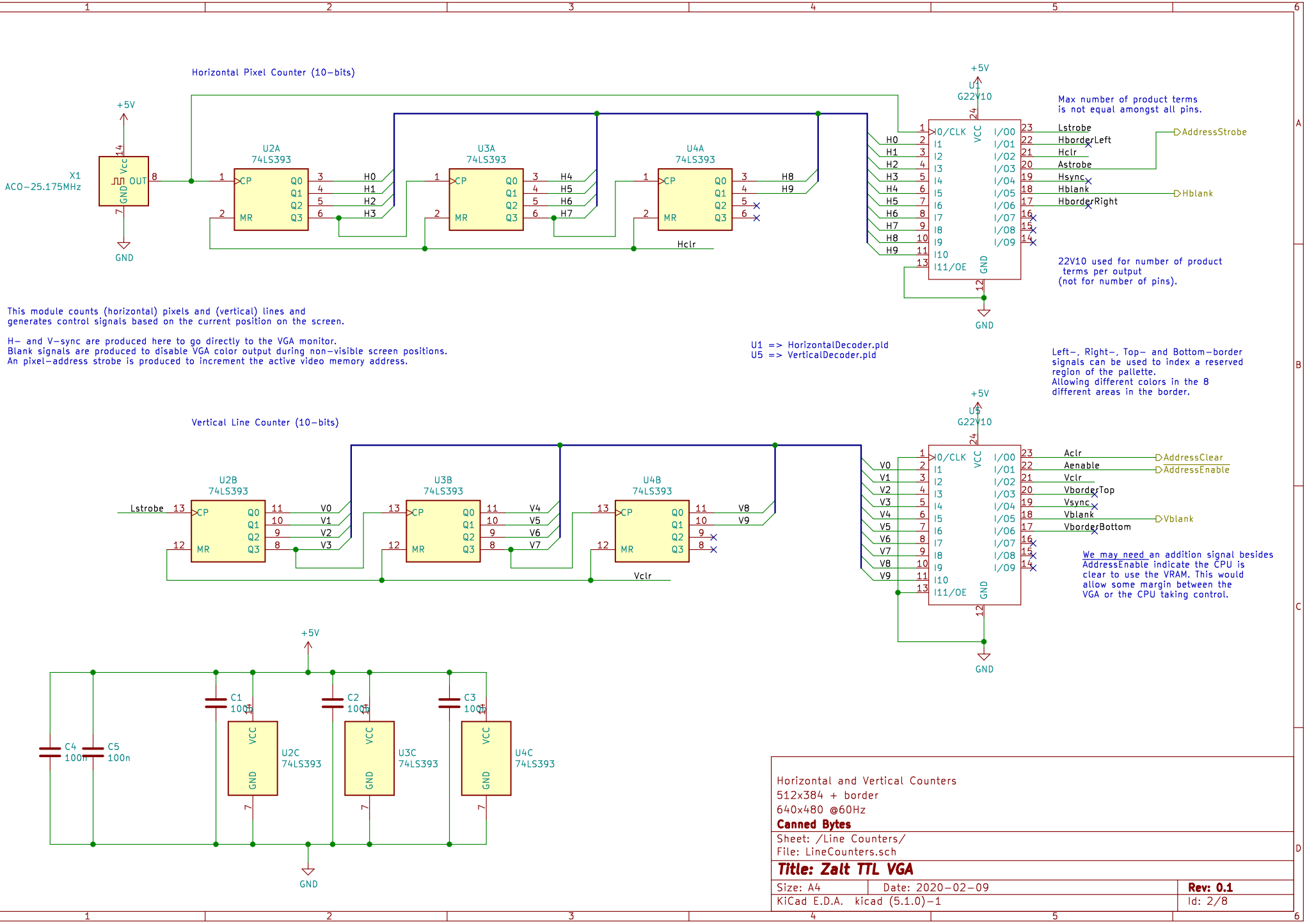

Sheet: Line Counters
AddressStrobe
AddressLoad
AddressEnable
Hblank
Vblank
Hblank
Vblank
File: LineCounters.sch
Sheet: Pixel Address Counter
AddressStrobe
AddressLoad
BusData
PixelAddress
ScrollRegLoStrobe
ScrollRegHiStrobe
File: PixelAddressCounter.sch
Sheet: Video Modes
PixelAddress
VideoAddress
VideoMode
VideoModeSelect
VideoEnable
File: VideoModes.sch
Sheet: Video Memory VRAM
VideoAddress
VideoData
OutputEnable
WriteEnable
File: VideoMemory.sch
Sheet: Pixel Output
VideoData
ColorDepthSelect
VideoBitCount
BusData
PaletteRegStrobe
Hblank
Vblank
Hblank
Vblank
File: PixelOutput.sch
Sheet: New Bus Decoder
VideoEnable
BusEnable
BusAddress
BusCtrl
BusData
Settings
BusAddressHiStrobe
PalleteRegStrobe
ScrollRegLoStrobe
ScrollRegHiStrobe
File: NewBusDecoder.sch
Sheet: Bus Interface
BusEnable
VideoAddress
VideoData
BusData
BusAddress
BusAddressHiStrobe
File: BusInterface.sch
VM1
VM2
VM3
CDS0
CDS1
CDS2
A0
A1
A2
PA0
PA1
PA2
HDR1
BUSHDR-A
GND
+5V
MA0
MA1
MA2
MA3
MA4
MA5
MA6
MA7
MA8
MA9
MA10
MA11
MA12
MA13
MA14
MA15
MA16
MA17
MA18
MA19
BD0
BD1
BD2
BD3
BD4
BD5
BD6
BD7
MEMREQ
WR
RD
WAIT
HDR2
BUSHDR-B
GND
+5V
BUSRQ
BUSACK
HALT
WAIT
M1
REFRESH
MEMREQ
IOREQ
RD
WR
INT
NMI
A12
A13
A14
A15
RST
CLK
CME
MBE0
MBE1
MBE2
MBE3
MBE4
MBE5
MBE6
MBE7
MEMRQ
RD
WAIT
IOREQ
WR
BusCLK
512x384 + border
640x480 @60Hz
Canned Bytes
Sheet: /
File: ZaltTtlVga.sch
Title: Zalt TTL VGA
Size: A4
Date: 2020-02-09
Rev: 0.1
KiCad E.D.A. kicad (5.1.0)-1
Id: 1/8


Horizontal Pixel Counter (10-bits)
+5V
X1
ACO-25.175MHz
Vcc
GND
OUT
U2A
74LS393
U3A
74LS393
U4A
74LS393
CP
MR
Q0
Q1
Q2
Q3
H0
H1
H2
H3
H4
H5
H6
H7
H8
H9
Hclr
U1
G22V10
I0/CLK
I1
I2
I3
I4
I5
I6
I7
I8
I9
I10
I11/OE
VCC
I/O0
I/O1
I/O2
I/O3
I/O4
I/O5
I/O6
I/O7
I/O8
I/O9
Lstrobe
HborderLeft
Hclr
Astrobe
Hsync
Hblank
HborderRight
AddressStrobe
Hblank
Max number of product terms
is not equal amongst all pins.
22V10 used for number of product
terms per output
(not for number of pins).
This module counts (horizontal) pixels and (vertical) lines and
generates control signals based on the current position on the screen.
H- and V-sync are produced here to go directly to the VGA monitor.
Blank signals are produced to disable VGA color output during non-visible screen positions.
An pixel-address strobe is produced to increment the active video memory address.
U1 => HorizontalDecoder.pld
U5 => VerticalDecoder.pld
Left-, Right-, Top- and Bottom-border
signals can be used to index a reserved
region of the pallette.
Allowing different colors in the 8
different areas in the border.
Vertical Line Counter (10-bits)
U2B
74LS393
U3B
74LS393
U4B
74LS393
Lstrobe
V0
V1
V2
V3
V4
V5
V6
V7
V8
V9
Vclr
U5
G22V10
Aclr
Aenable
Vclr
VborderTop
Vsync
Vblank
VborderBottom
AddressClear
AddressEnable
Vblank
We may need an addition signal besides
AddressEnable indicate the CPU is
clear to use the VRAM. This would
allow some margin between the
VGA or the CPU taking control.
C1
100n
C2
100n
C3
100n
C4
100n
C5
100n
U2C
74LS393
U3C
74LS393
U4C
74LS393
GND
Horizontal and Vertical Counters
512x384 + border
640x480 @60Hz
Canned Bytes
Sheet: /Line Counters/
File: LineCounters.sch
Title: Zalt TTL VGA
Size: A4
Date: 2020-02-09
Rev: 0.1
KiCad E.D.A. kicad (5.1.0)-1
Id: 2/8

This module contains the color palette and color depth selection logic for the various video modes.

ColorDepthSelect

bits per pixel

CDS0	1bit
CDS1	2bit
CDS2	4bit
	8bit

TODO: 8-bit mode

Data from VRAM

VideoData

U?
74LS245

VD0	2	A0	B0	18	PD0
VD1	3	A1	B1	17	PD1
VD2	4	A2	B2	16	PD2
VD3	5	A3	B3	15	PD3
VD4	6	A4	B4	14	PD4
VD5	7	A5	B5	13	PD5
VD6	8	A6	B6	12	PD6
VD7	9	A7	B7	11	PD7
		VCC		20	
1		A->B			
8bit	19	CE	GND	10	

VideoBitCount

Pixel-Address lines that select what data bits to select for the output of each pixel. (multiple pixels per VRAM-Address)

PA0
PA1
PA2
PA3

U?
74LS257

VD0	2	I0a	Za	4	PalA0
VD4	3	I1a		
VD1	5	I0b	Zb	7	PalA1
VD5	6	I1b		
VD2	14	I0c	Zc	12	PalA2
VD6	13	I1c		
VD3	11	I0d	Zd	9	PalA3
VD6	10	I1d		
PA0	1	S		
4bit	15	OE	GND	8	
		VCC		16	

22V10 GAL will fit:
quad 2:1
dual 4:1
single 8:1

OE (used a spare output)

U?
74LS253

VD0	6	I0a	Za	7	PalA0
VD2	5	I1a		
VD4	4	I2a		
VD6	3	I3a		
2bit	1	OEa		
VD1	10	I0b	Zb	9	PalA1
VD3	11	I1b		
VD5	12	I2b		
VD7	13	I3b		
2bit	15	OEb		
PA0	14	A0		
PA1	2	A1	GND	8	
		VCC		16	

U?
UM61512A

PalA0	12	A0	D0	13	PD0
PalA1	11	A1	D1	14	PD1
PalA2	10	A2	D2	15	PD2
PalA3	9	A3	D3	17	PD3
PalA4	8	A4	D4	18	PD4
PalA5	7	A5	D5	19	PD5
PalA6	6	A6	D6	20	PD6
PalA7	5	A7	D7	21	PD7
PalA8	27	A8		
PalA9	26	A9	CE1	22
PalA10	23	A10	CE2	30
PalA11	25	A11	OE	24
	4	A12	WE	29
	28	A13		
	3	A14	VCC	32
	31	A15	GND	16

Palette RAM

8-bit color depth will bypass the Palette.
If we have 8-bit colors.
If we choose 15/16-bit colors we need to map.

U?
74HCT574

BD0	2	D0	Q0	19	PalA4
BD1	3	D1	Q1	18	PalA5
BD2	4	D2	Q2	17	PalA6
BD3	5	D3	Q3	16	PalA7
BD4	6	D4	Q4	15	PalA8
BD5	7	D5	Q5	14	PalA9
BD6	8	D6	Q6	13	PalA10
BD7	9	D7	Q7	12	PalA11
		VCC		20	
PaletteRegStrobe	11	Cp		
	1	OE	GND	10	

BusData

A Register that selects the active Palette.
Allows the CPU to switch quickly between presets.
Only if not 8-bit color depth.
Stobe allowed mid-frame.

The output will be 'black' when either blank signal is active.

U19 => BlankMux.pld

Hblank
Vblank

U19
GAL16V8

+5V

TODO: RGB (9-bit) DAC

	1	I1/CLK	IO1	19	R0
PD0	2	I2	IO2	18	R1
PD1	3	I3	IO3	17	R2
PD2	4	I4	IO4	16	G0
PD3	5	I5	IO5	15	G1
PD4	6	I6	IO6	14	G2
PD5	7	I7	IO7	13	B0
PD6	8	I8	IO8	12	B1
PD7	9	I9			B2
	11	I10/OE	GND	10	
		VCC		20	

GND

8-bit RGB

R (3-bits)
G (3-bits)
B (2-bits)

U?
74LS251

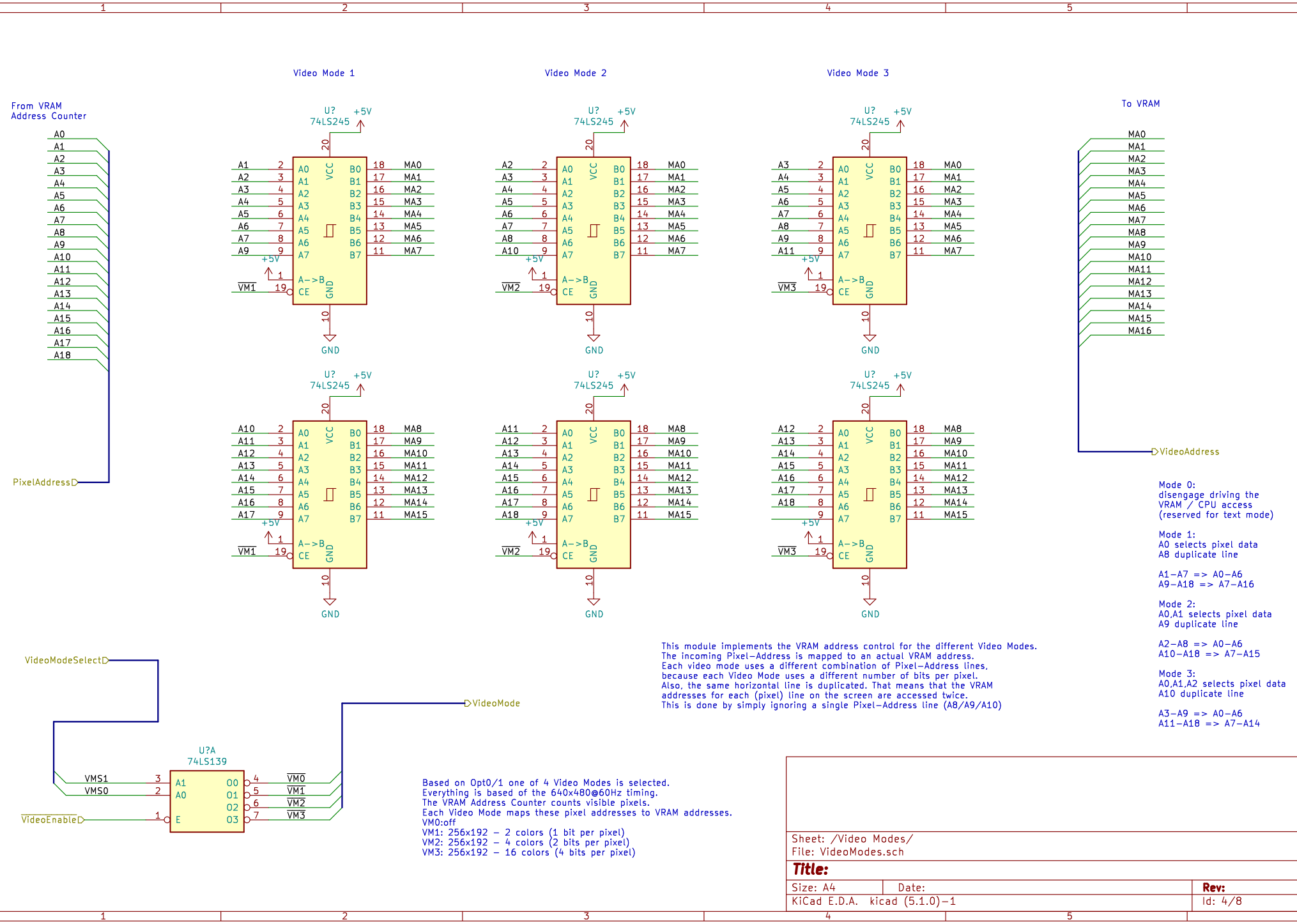
VD0	4	I0	Y	5	PalA0
VD1	3	I1	Y	6	
VD2	2	I2		
VD3	1	I3		
VD4	15	I4		
VD5	14	I5		
VD6	13	I6		
VD7	12	I7		
PA0	11	S0		
PA1	10	S1		
PA2	9	S2		
1bit	7	OE	GND	8
		VCC		16

Pixel Output
512x384 + border
640x480 @60Hz
Canned Bytes

Sheet: /Pixel Output/
File: PixelOutput.sch

Title: Zalt TTL VGA

Size: A4	Date: 2020-02-09	**Rev: 0.1**
KiCad E.D.A. kicad (5.1.0)-1		Id: 3/8


Video Mode 1
Video Mode 2
Video Mode 3
From VRAM
Address Counter
To VRAM
PixelAddress
VideoAddress
U?
74LS245
+5V
GND
VM1
VM2
VM3
A->B
CE
VCC
Mode 0:
disengage driving the
VRAM / CPU access
(reserved for text mode)
Mode 1:
A0 selects pixel data
A8 duplicate line
A1–A7 => A0–A6
A9–A18 => A7–A16
Mode 2:
A0,A1 selects pixel data
A9 duplicate line
A2–A8 => A0–A6
A10–A18 => A7–A15
Mode 3:
A0,A1,A2 selects pixel data
A10 duplicate line
A3–A9 => A0–A6
A11–A18 => A7–A14
This module implements the VRAM address control for the different Video Modes.
The incoming Pixel–Address is mapped to an actual VRAM address.
Each video mode uses a different combination of Pixel–Address lines,
because each Video Mode uses a different number of bits per pixel.
Also, the same horizontal line is duplicated. That means that the VRAM
addresses for each (pixel) line on the screen are accessed twice.
This is done by simply ignoring a single Pixel–Address line (A8/A9/A10)
VideoModeSelect
VideoMode
VideoEnable
U?A
74LS139
VMS1
VMS0
Based on Opt0/1 one of 4 Video Modes is selected.
Everything is based of the 640x480@60Hz timing.
The VRAM Address Counter counts visible pixels.
Each Video Mode maps these pixel addresses to VRAM addresses.
VM0:off
VM1: 256x192 – 2 colors (1 bit per pixel)
VM2: 256x192 – 4 colors (2 bits per pixel)
VM3: 256x192 – 16 colors (4 bits per pixel)
Sheet: /Video Modes/
File: VideoModes.sch
Title:
Size: A4
Date:
Rev:
KiCad E.D.A. kicad (5.1.0)-1
Id: 4/8

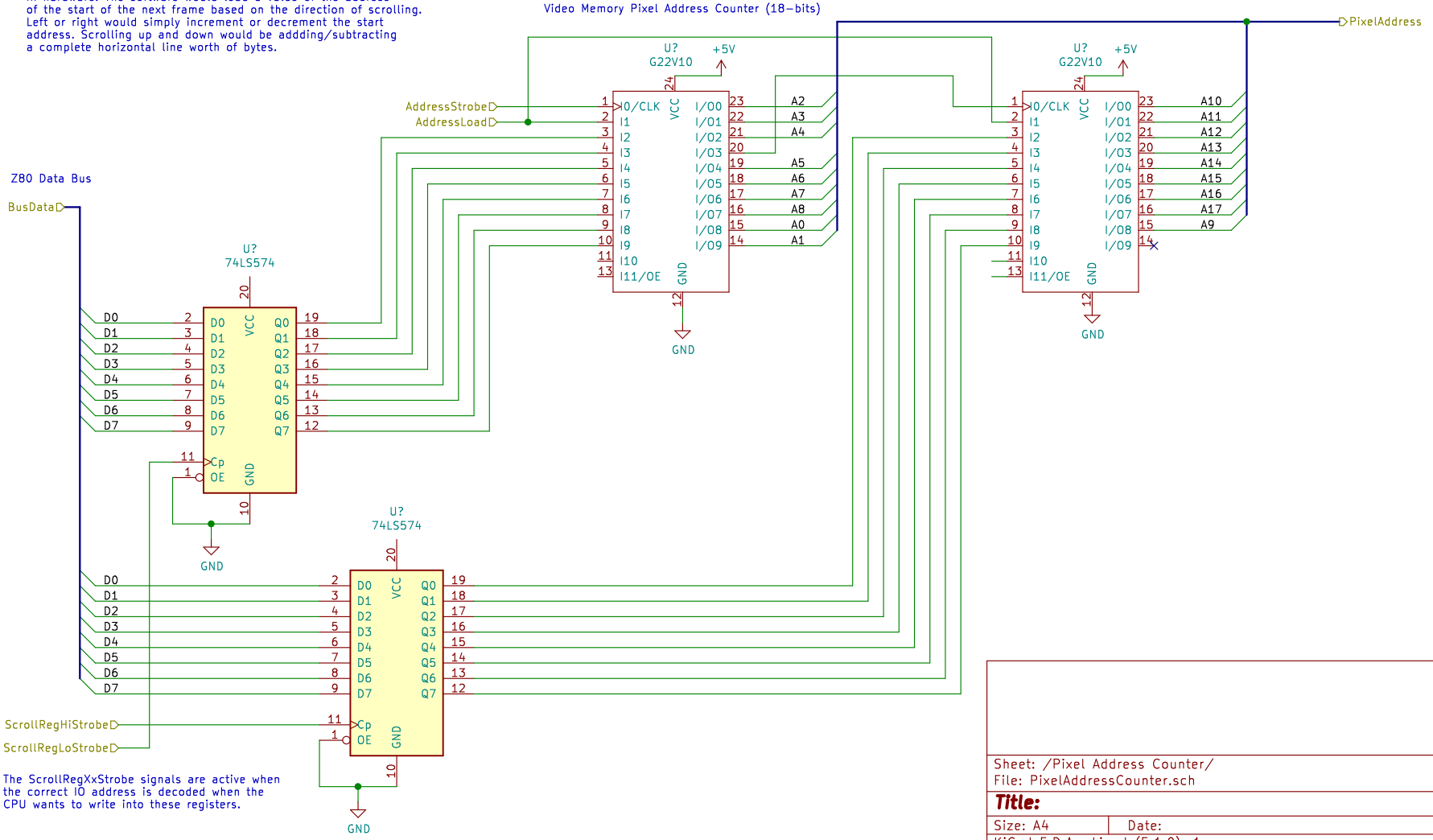
This module counts the pixel-address strobes and generates 18-bit address lines.
Both counters count 9-bits. The first (lo) counter generates the 'clock' for the 2nd (hi) counter.

Later this 18-bit pixel address is used as a basis for addressing VRAM.

We have registers here that load in a start address for each frame. That way a scrolling function can be supported in hardware. The software would load a value of the address of the start of the next frame based on the direction of scrolling. Left or right would simply increment or decrement the start address. Scrolling up and down would be addding/subtracting a complete horizontal line worth of bytes.

U6 => BinaryCounterLo.pld
U7 => BinaryCounterHi.pld

Video Memory Pixel Address Counter (18-bits)



The ScrollRegXxStrobe signals are active when the correct IO address is decoded when the CPU wants to write into these registers.

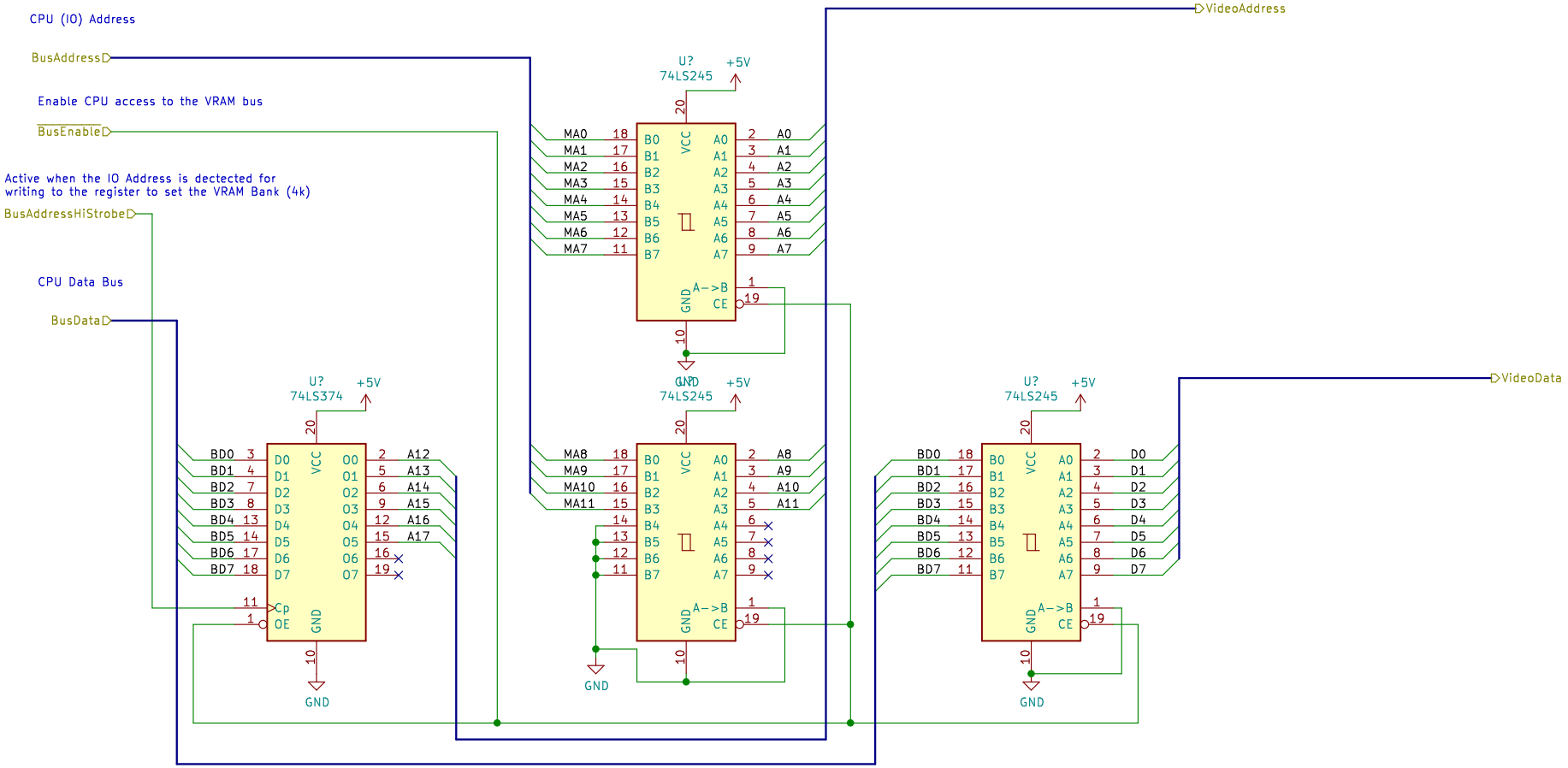
Sheet: /Pixel Address Counter/
File: PixelAddressCounter.sch

Title:

Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.0)-1		Id: 5/8

This module connects the CPU bus to the VRAM bus
when the BusEnable signal is active.

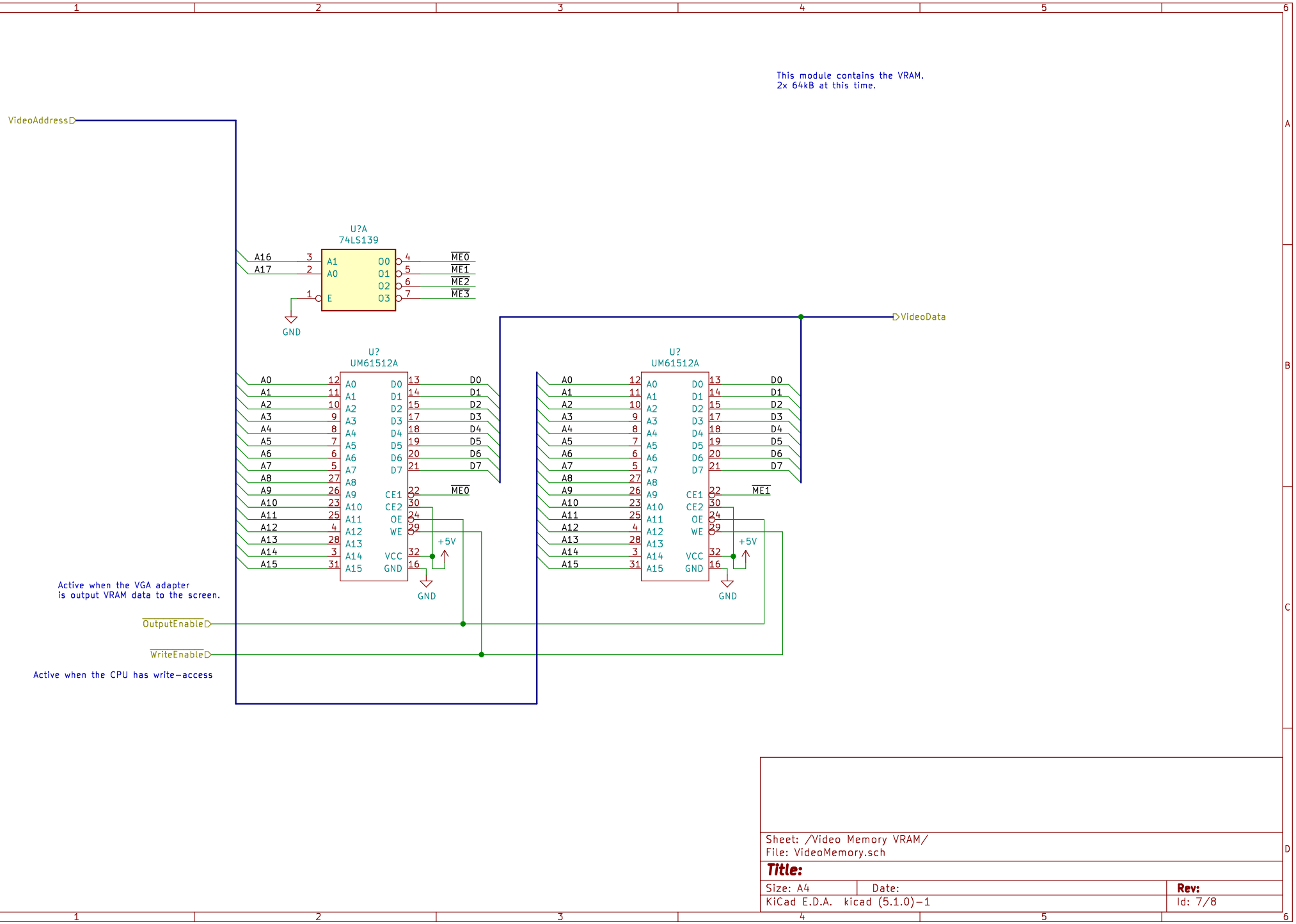
Will probably add the ability for the VGA adapter to issue
an IM2 (vector) interrupt to CPU when it is allowed access.



Z80 interfaces through a 4k Memory Page.
The location (bit address) of this memory page is determined by the Bus Decoder.

The Control Register provides the upper 6 bits A12..A17 of the
VRAM address and can only be changed through an IO write.
The IO address (A0-A7) is also determined by the Bus Decoder.

Sheet: /Bus Interface/		
File: BusInterface.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.0)-1		Id: 6/8


This module contains the VRAM.
2x 64kB at this time.
VideoAddress
U?A
74LS139
A16
A17
A1
A0
E
O0
O1
O2
O3
ME0
ME1
ME2
ME3
GND
VideoData
U?
UM61512A
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
D0
D1
D2
D3
D4
D5
D6
D7
CE1
CE2
OE
WE
VCC
GND
+5V
Active when the VGA adapter
is output VRAM data to the screen.
OutputEnable
WriteEnable
Active when the CPU has write-access
Sheet: /Video Memory VRAM/
File: VideoMemory.sch
Title:
Size: A4
Date:
Rev:
KiCad E.D.A. kicad (5.1.0)-1
Id: 7/8

This module decodes IO addresses for the Z80 CPU to access various parts of the VGA adapter.

- VRAM banks (4k)
- Video Modes
- Color Palette

VRAM bank register strobe

BusAddressHiStrobe

CPU interface

BusAddress

BusCtrl

TODO

VGA video is active

VideoEnable

CPU access to the Video Memort Bus

BusEnable

TODO: CPU access to the content of the Pallete

BusData

Pallette Register for selecting an active color pallete.

PalleteRegStrobe

Low and High address of the scroll register strobe.
Value loaded when the line counters reset.

ScrollRegLoStrobe

ScrollRegHiStrobe

Settings

Signals that control VGA behavior
-Video Mode

Sheet: /New Bus Decoder/ File: NewBusDecoder.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.0)-1		Id: 8/8