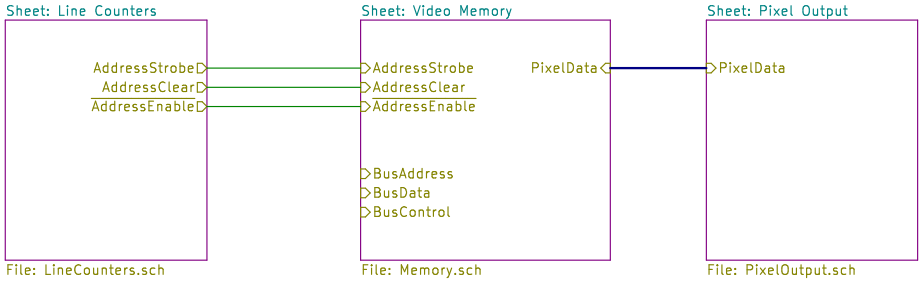
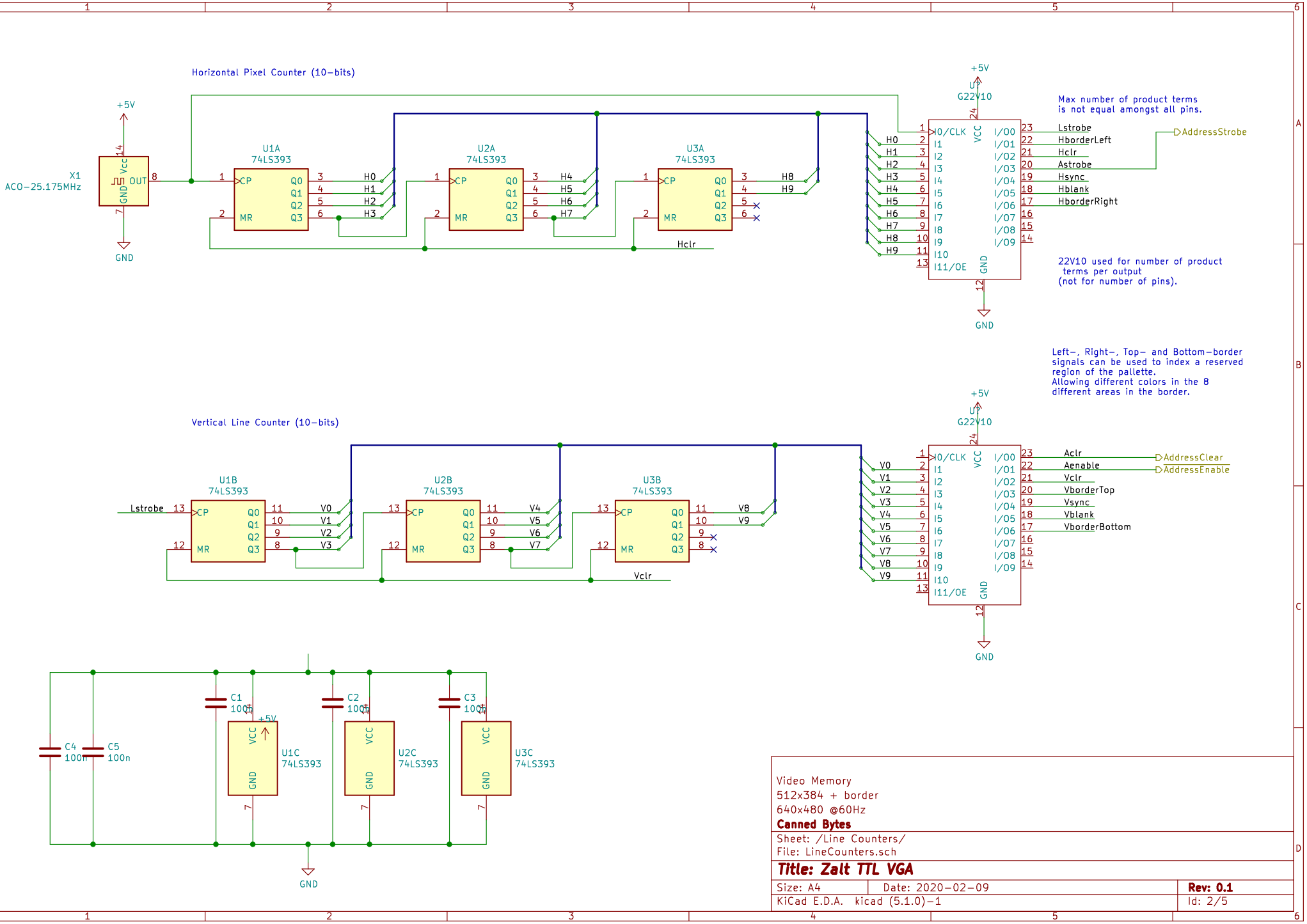



Video Memory
512x384 + border
640x480 @60Hz
**Canned Bytes**

Sheet: /
File: ZaltTtlVga.sch

***Title: Zalt TTL VGA***

| Size: A4 | Date: 2020-02-09 | **Rev: 0.1** |
|---|---|---|
| KiCad E.D.A. kicad (5.1.0)-1 | | Id: 1/5 |

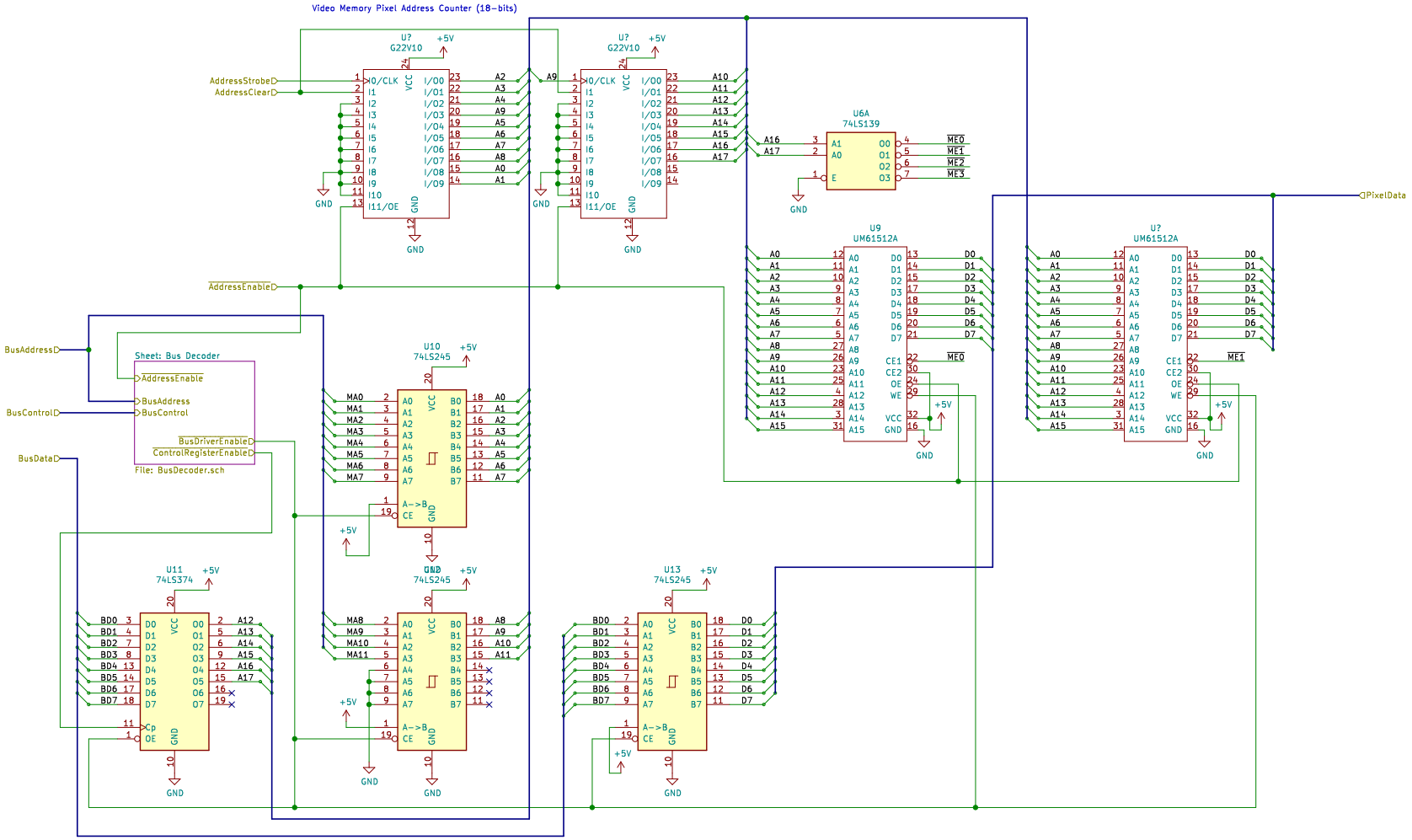



Video Memory
512x384 + border
640x480 @60Hz
**Canned Bytes**

Sheet: /Line Counters/
File: LineCounters.sch

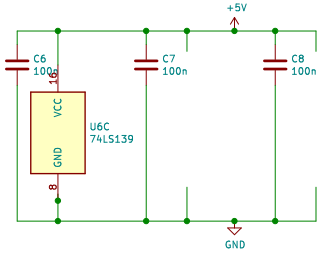
**Title: Zalt TTL VGA**

| Size: A4 | Date: 2020-02-09 | **Rev: 0.1** |
|---|---|---|
| KiCad E.D.A. kicad (5.1.0)-1 | | Id: 2/5 |




Z80 interfaces through a 4k Memory Page.
The location (bit address) of this memory page is determined by the Bus Decoder.

The Control Register provides the upper 6 bits A12..A17 of the
VRAM address and can only be changed through an IO write.
The IO address (A0-A7) is also determined by the Bus Decoder.

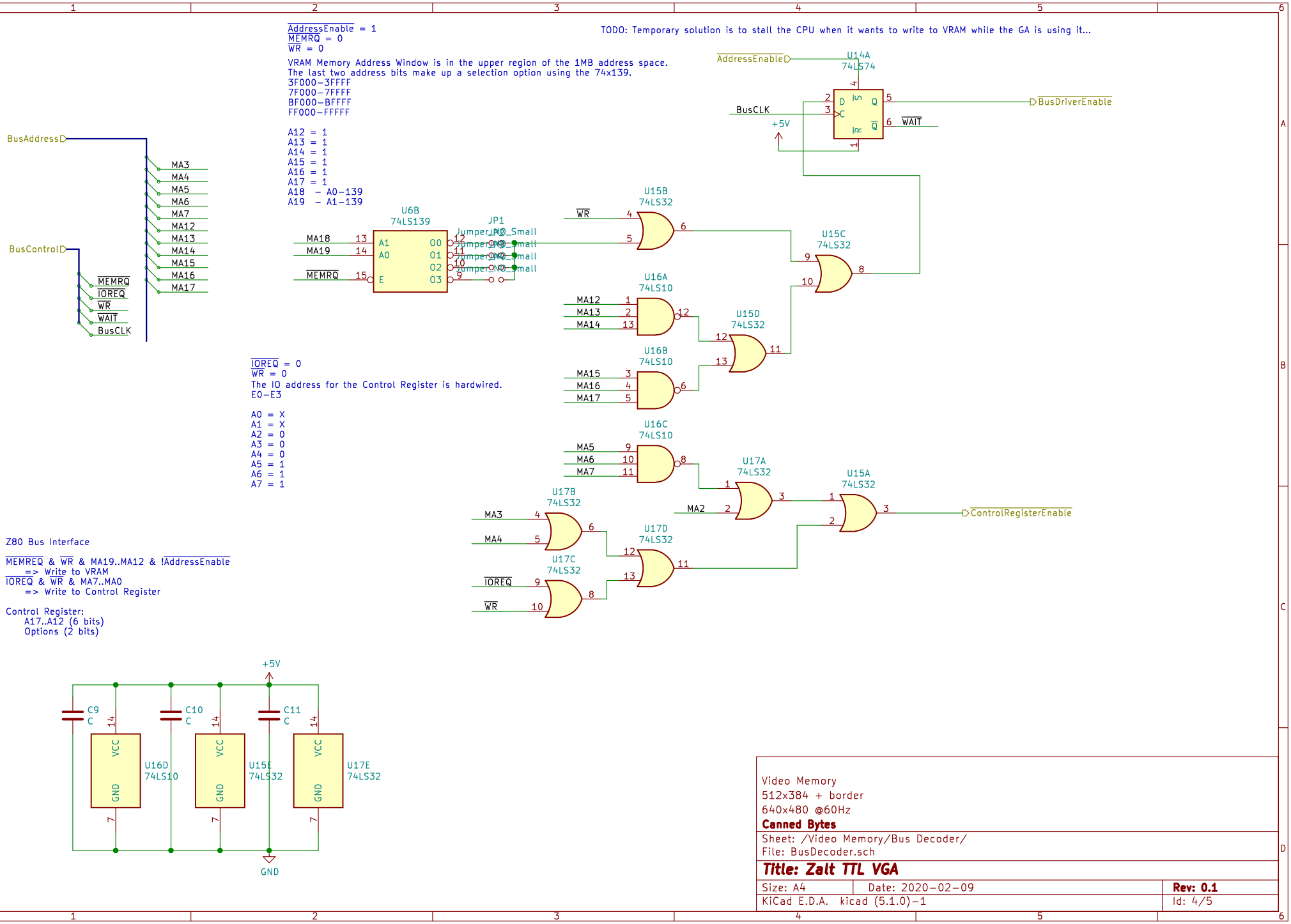



Video Memory
512x384 + border
640x480 @60Hz
**Canned Bytes**

Sheet: /Video Memory/
File: Memory.sch

**Title: Zalt TTL VGA**

| Size: A3 | Date: 2020-02-09 | **Rev: 0.1** |
|---|---|---|
| KiCad E.D.A. kicad (5.1.0)-1 | | Id: 3/5 |


AddressEnable = 1
MEMRQ = 0
WR = 0
VRAM Memory Address Window is in the upper region of the 1MB address space.
The last two address bits make up a selection option using the 74x139.
3F000-3FFFF
7F000-7FFFF
BF000-BFFFF
FF000-FFFFF
A12 = 1
A13 = 1
A14 = 1
A15 = 1
A16 = 1
A17 = 1
A18 - A0-139
A19 - A1-139
TODO: Temporary solution is to stall the CPU when it wants to write to VRAM while the GA is using it...
AddressEnable
U14A
74LS74
BusCLK
+5V
BusDriverEnable
WAIT
BusAddress
BusControl
MA3
MA4
MA5
MA6
MA7
MA12
MA13
MA14
MA15
MA16
MA17
MEMRQ
IOREQ
WR
WAIT
BusCLK
U6B
74LS139
JP1
Jumper_NO_Small
MA18
MA19
MEMRQ
U15B
74LS32
U15C
74LS32
U16A
74LS10
U15D
74LS32
U16B
74LS10
IOREQ = 0
WR = 0
The IO address for the Control Register is hardwired.
E0-E3
A0 = X
A1 = X
A2 = 0
A3 = 0
A4 = 0
A5 = 1
A6 = 1
A7 = 1
U16C
74LS10
U17A
74LS32
U15A
74LS32
MA2
ControlRegisterEnable
U17B
74LS32
U17D
74LS32
U17C
74LS32
Z80 Bus Interface
MEMREQ & WR & MA19..MA12 & !AddressEnable
=> Write to VRAM
IOREQ & WR & MA7..MA0
=> Write to Control Register
Control Register:
A17..A12 (6 bits)
Options (2 bits)
+5V
C9
C
C10
C
C11
C
U16D
74LS10
U15E
74LS32
U17E
74LS32
VCC
GND
GND
Video Memory
512x384 + border
640x480 @60Hz
Canned Bytes
Sheet: /Video Memory/Bus Decoder/
File: BusDecoder.sch
Title: Zalt TTL VGA
Size: A4
Date: 2020-02-09
Rev: 0.1
KiCad E.D.A. kicad (5.1.0)-1
Id: 4/5

PixelData

Pixel Output
512x384 + border
640x480 @60Hz
**Canned Bytes**

Sheet: /Pixel Output/
File: PixelOutput.sch

**Title: Zalt TTL VGA**

| | | |
|---|---|---|
| Size: A4 | Date: 2020-02-09 | **Rev: 0.1** |
| KiCad E.D.A. kicad (5.1.0)-1 | | Id: 5/5 |