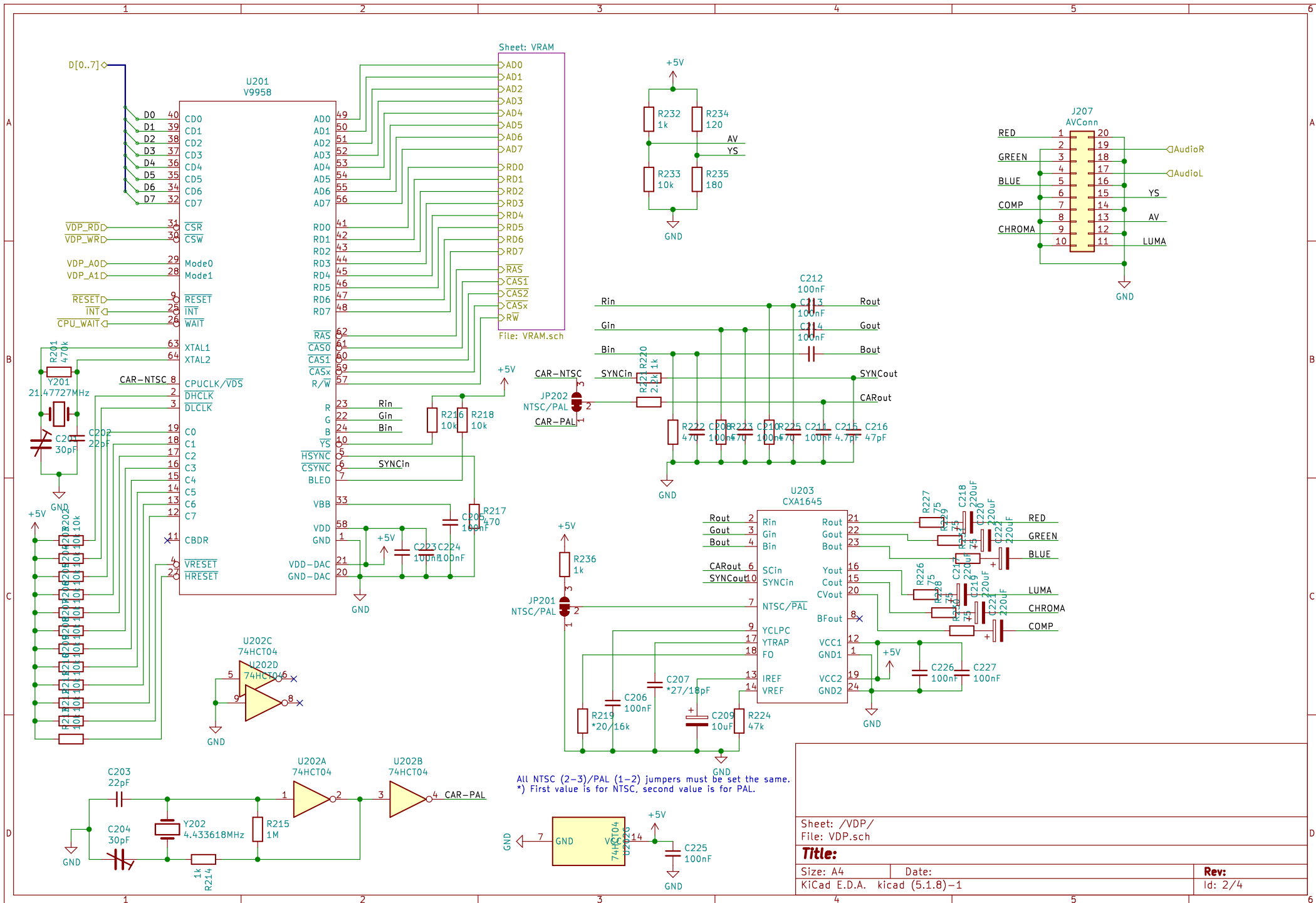


Interrupt Vector Load (IVL)
Activates when the correct IO Address is written to.

Interrupt Vector Output Enable (IVOR) Activates when a Z80 CPU Interrupt Acknowledge Cycle is detected: M1 and IOREQ both active.

IM0: Disable Vector-Enable Jumper (GND)
IM1: Load Vector Register with a RST instruction
IM2: Load Vector Register with an Interrupt Vector (D0 = 0)

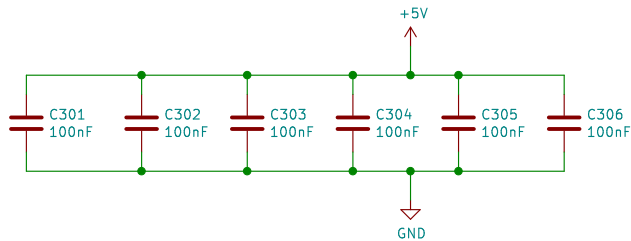
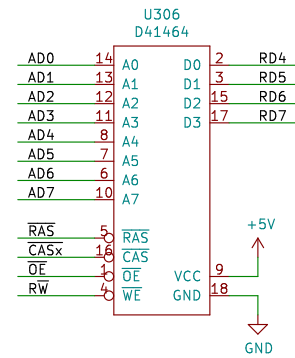
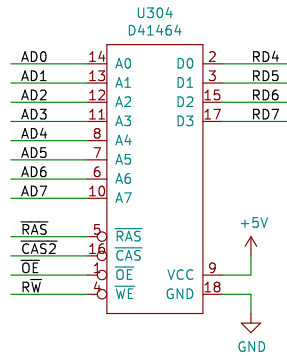
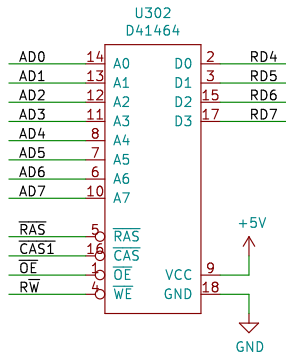
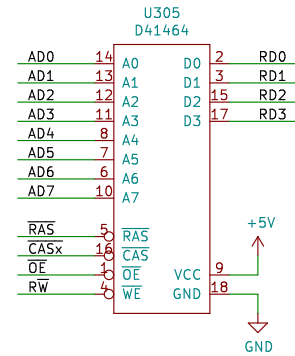
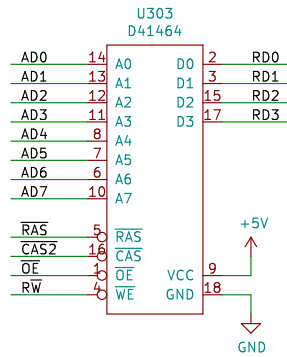
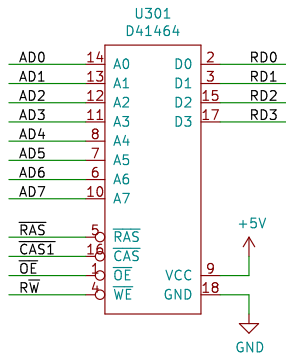
Sheet: /		D
File: VDP-Composite.sch		
Title:		
Size: A4	Date:	Rev:
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AD0▷ AD0
AD1▷ AD1
AD2▷ AD2
AD3▷ AD3
AD4▷ AD4
AD5▷ AD5
AD6▷ AD6
AD7▷ AD7

RD0▷ RD0
RD1▷ RD1
RD2▷ RD2
RD3▷ RD3
RD4▷ RD4
RD5▷ RD5
RD6▷ RD6
RD7▷ RD7

RAS▷ RAS
CAS1▷ CAS1
CAS2▷ CAS2
CASx▷ CASx
RW▷ RW
OE▷ OE
GND



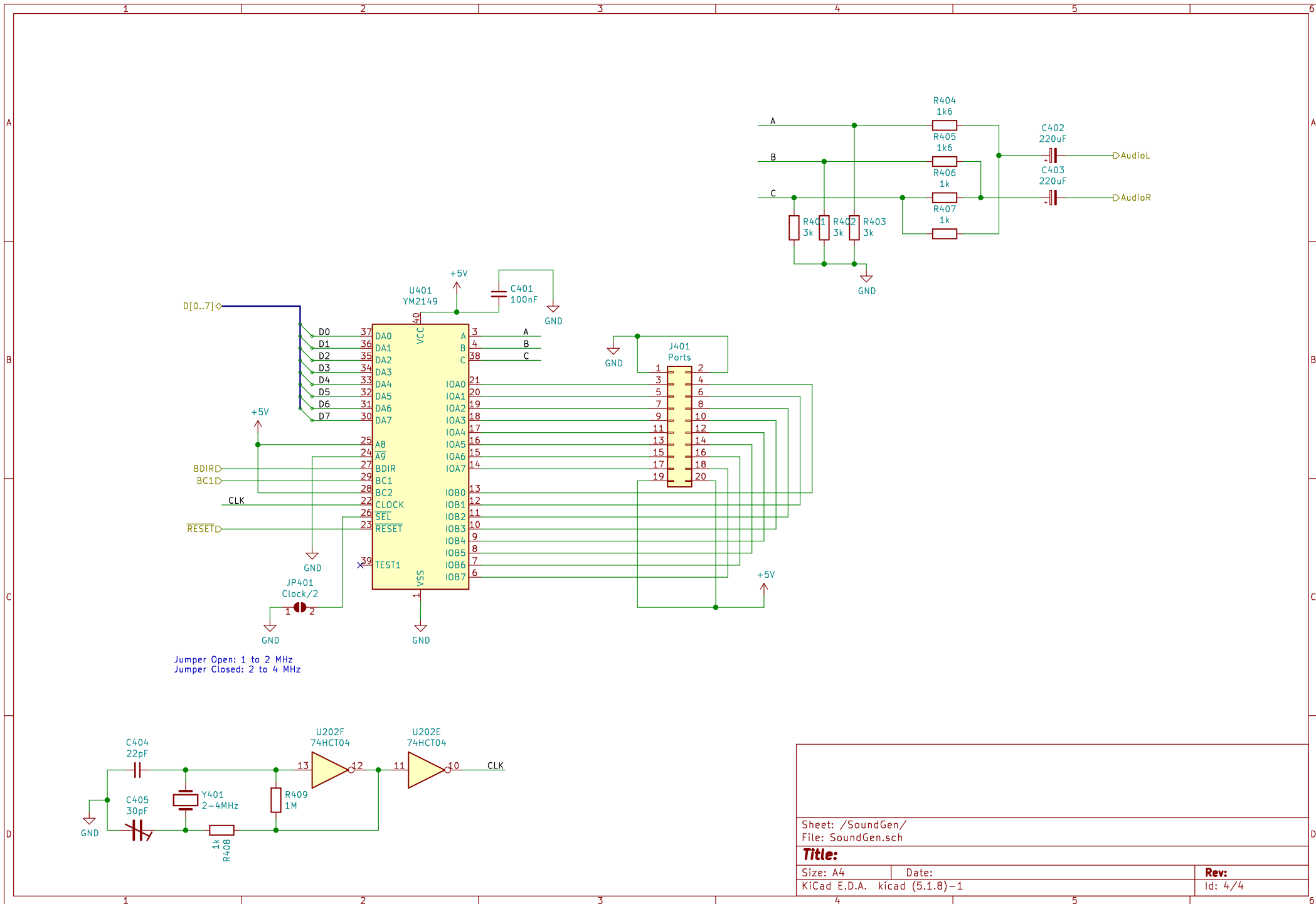
Sheet: /VDP/VRAM/
File: VRAM.sch

Title:

Size: A4
KiCad E.D.A. kicad (5.1.8)-1

Date:

Rev:
Id: 3/4



Sheet: /SoundGen/		
File: SoundGen.sch		
Title:		
Size: A4	Date:	Rev:
KiCad E.D.A. kicad (5.1.8)-1		Id: 4/4