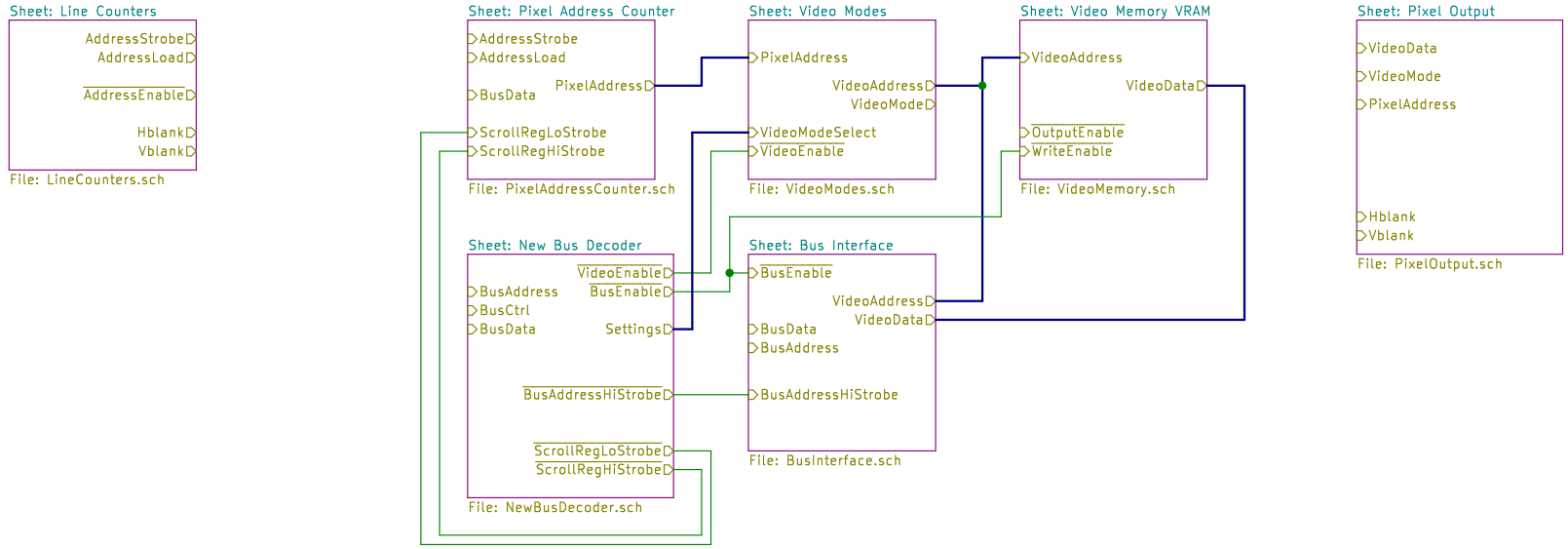
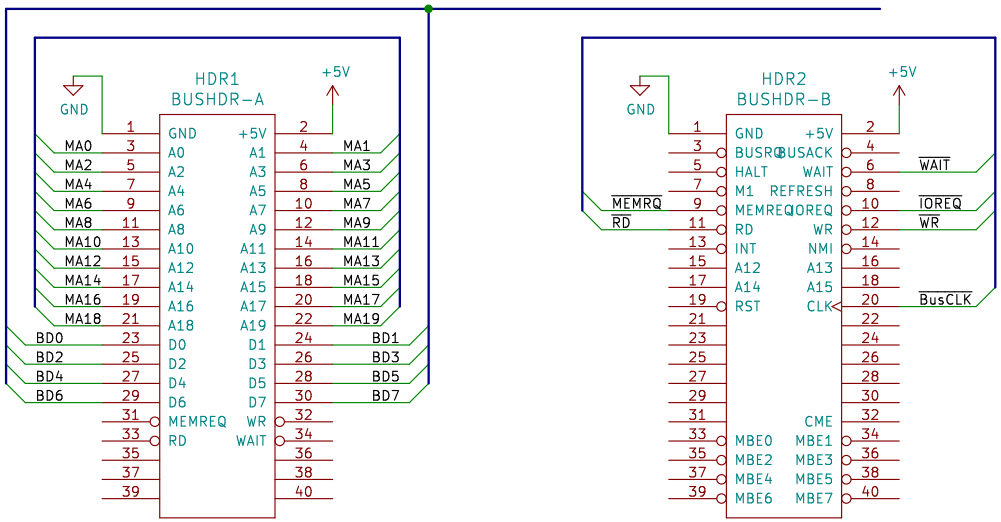


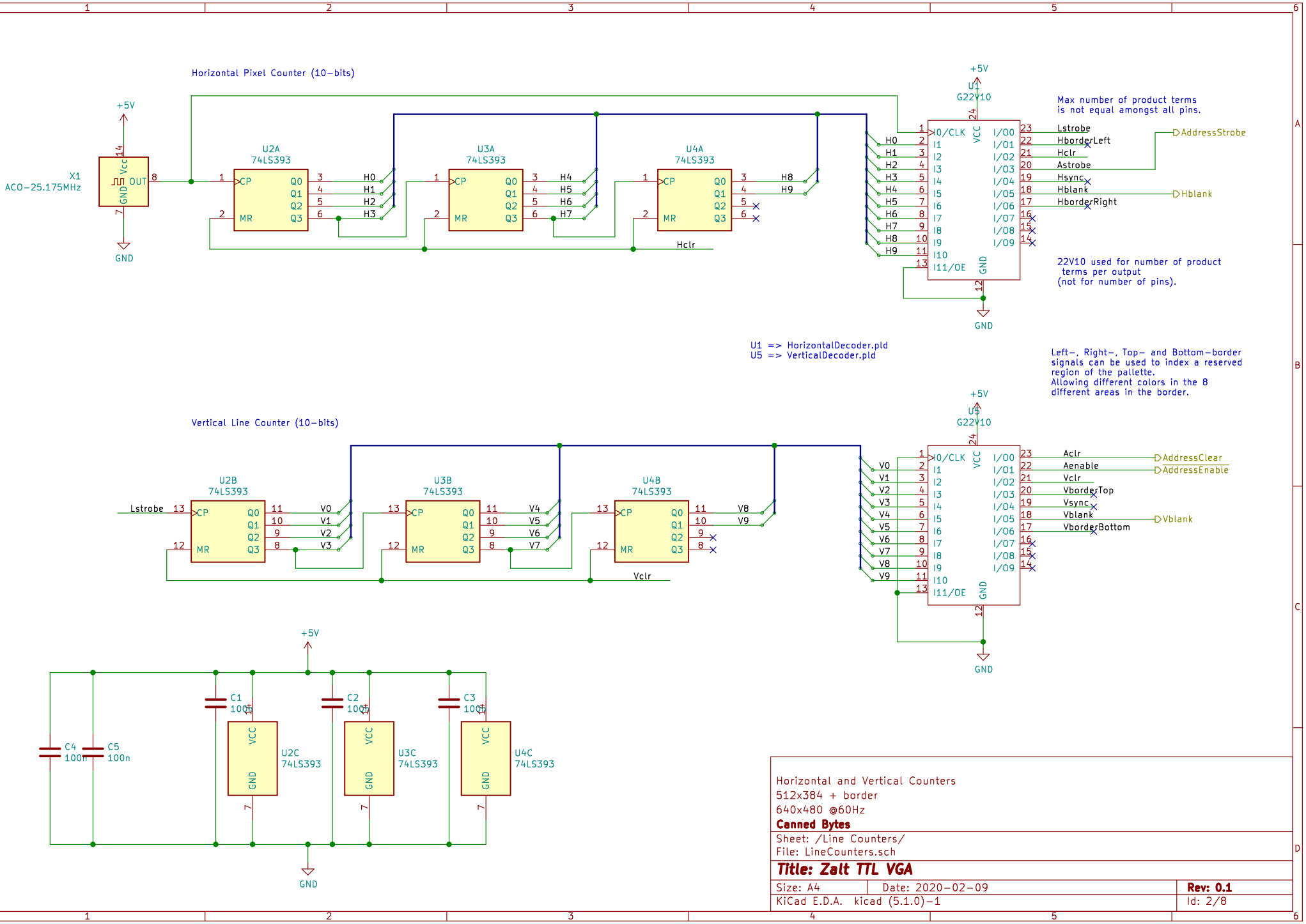


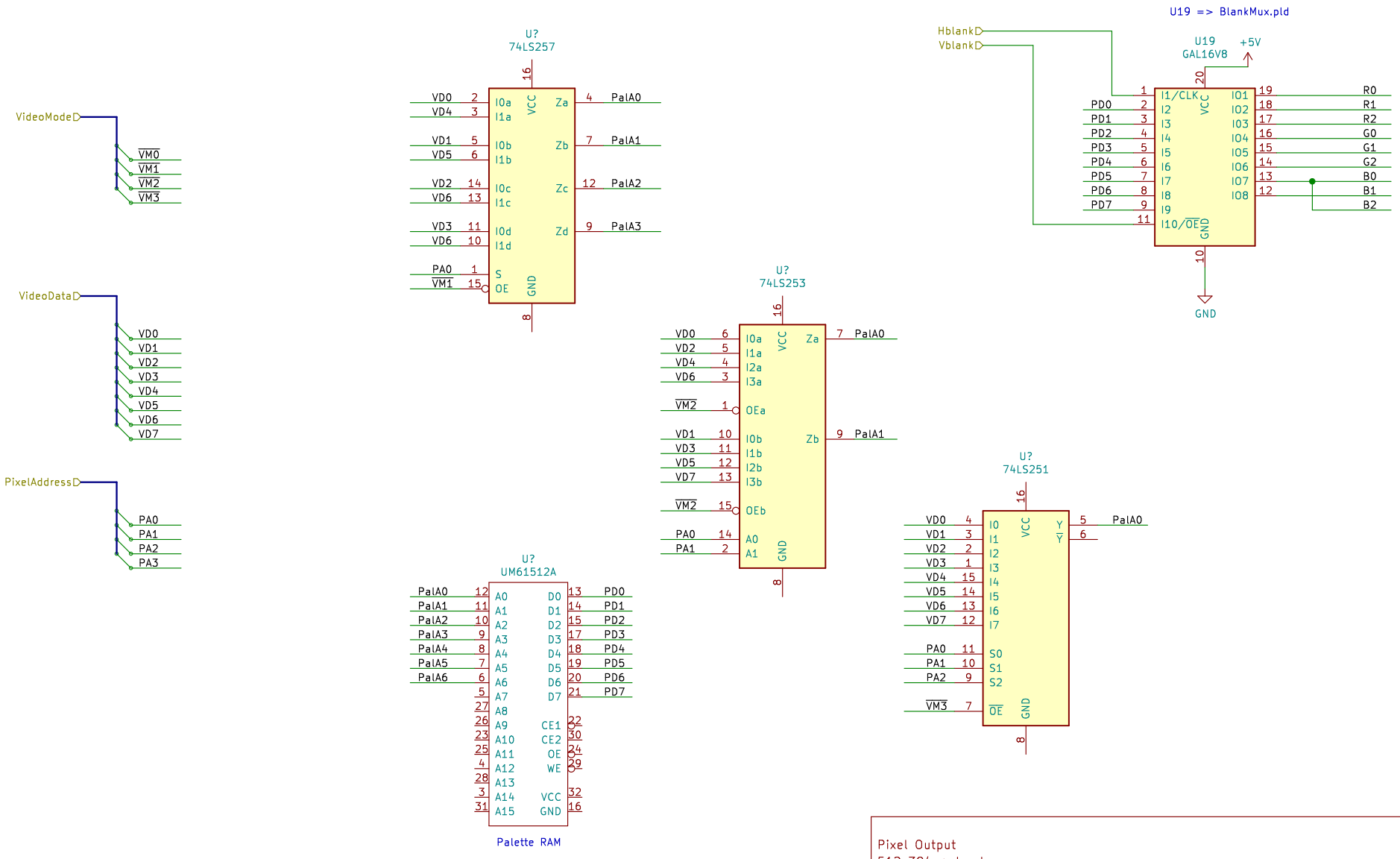
512x384 + border
640x480 @60Hz
Canned Bytes

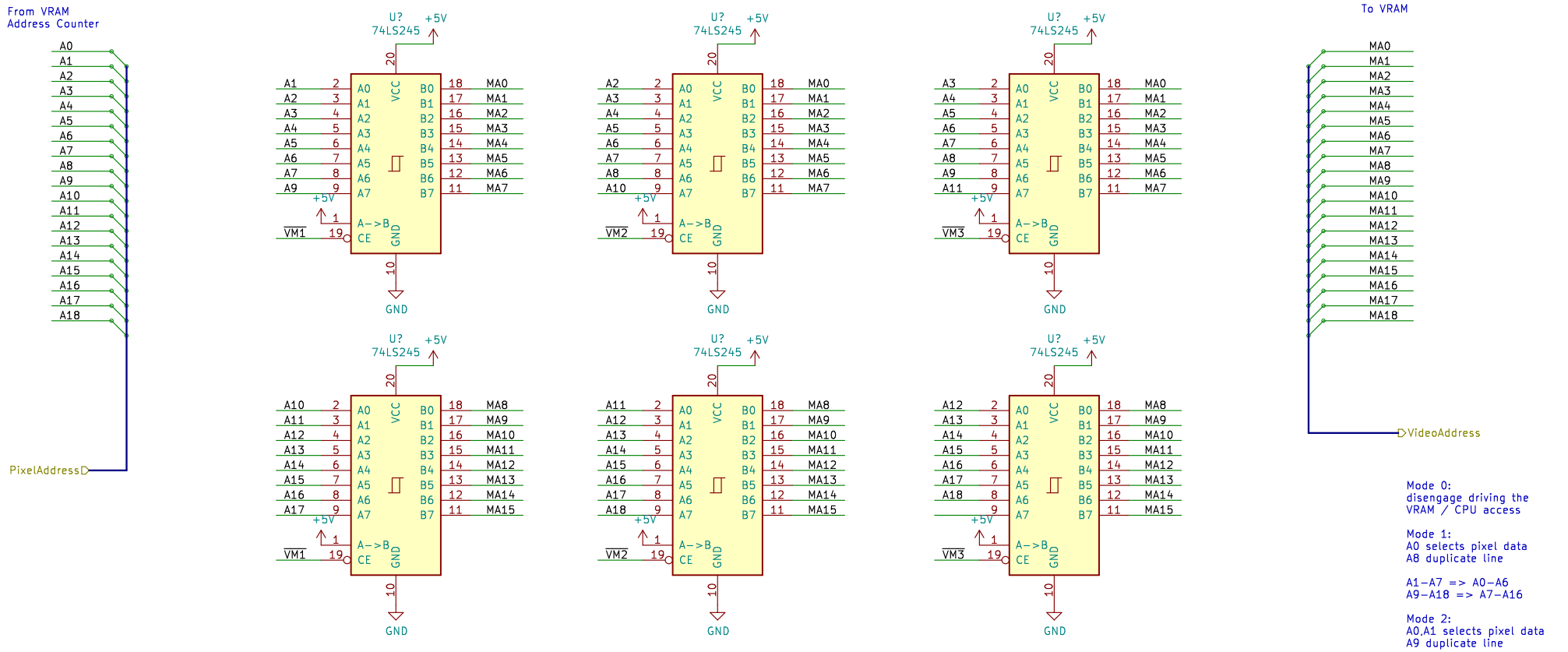
Sheet: /
File: ZaltTtlVga.sch

Title: Zalt TTL VGA

Size: A4	Date: 2020-02-09	**Rev: 0.1**
KiCad E.D.A. kicad (5.1.0)-1		Id: 1/8


Horizontal Pixel Counter (10-bits)
+5V
X1
ACO-25.175MHz
Vcc
OUT
GND
U2A
74LS393
U3A
74LS393
U4A
74LS393
CP
MR
Q0
Q1
Q2
Q3
H0
H1
H2
H3
H4
H5
H6
H7
H8
H9
Hclr
U1
G22V10
I0/CLK
I1
I2
I3
I4
I5
I6
I7
I8
I9
I10
I11/OE
VCC
I/O0
I/O1
I/O2
I/O3
I/O4
I/O5
I/O6
I/O7
I/O8
I/O9
Lstrobe
HborderLeft
Hclr
Astrobe
Hsync
Hblank
HborderRight
AddressStrobe
Hblank
Max number of product terms
is not equal amongst all pins.
22V10 used for number of product
terms per output
(not for number of pins).
U1 => HorizontalDecoder.pld
U5 => VerticalDecoder.pld
Left-, Right-, Top- and Bottom-border
signals can be used to index a reserved
region of the pallette.
Allowing different colors in the 8
different areas in the border.
Vertical Line Counter (10-bits)
U2B
74LS393
U3B
74LS393
U4B
74LS393
Lstrobe
V0
V1
V2
V3
V4
V5
V6
V7
V8
V9
Vclr
U5
G22V10
Aclr
Aenable
Vclr
VborderTop
Vsync
Vblank
VborderBottom
AddressClear
AddressEnable
Vblank
C1
100n
C2
100n
C3
100n
C4
100n
C5
100n
U2C
74LS393
U3C
74LS393
U4C
74LS393
Horizontal and Vertical Counters
512x384 + border
640x480 @60Hz
Canned Bytes
Sheet: /Line Counters/
File: LineCounters.sch
Title: Zalt TTL VGA
Size: A4
Date: 2020-02-09
Rev: 0.1
KiCad E.D.A. kicad (5.1.0)-1
Id: 2/8

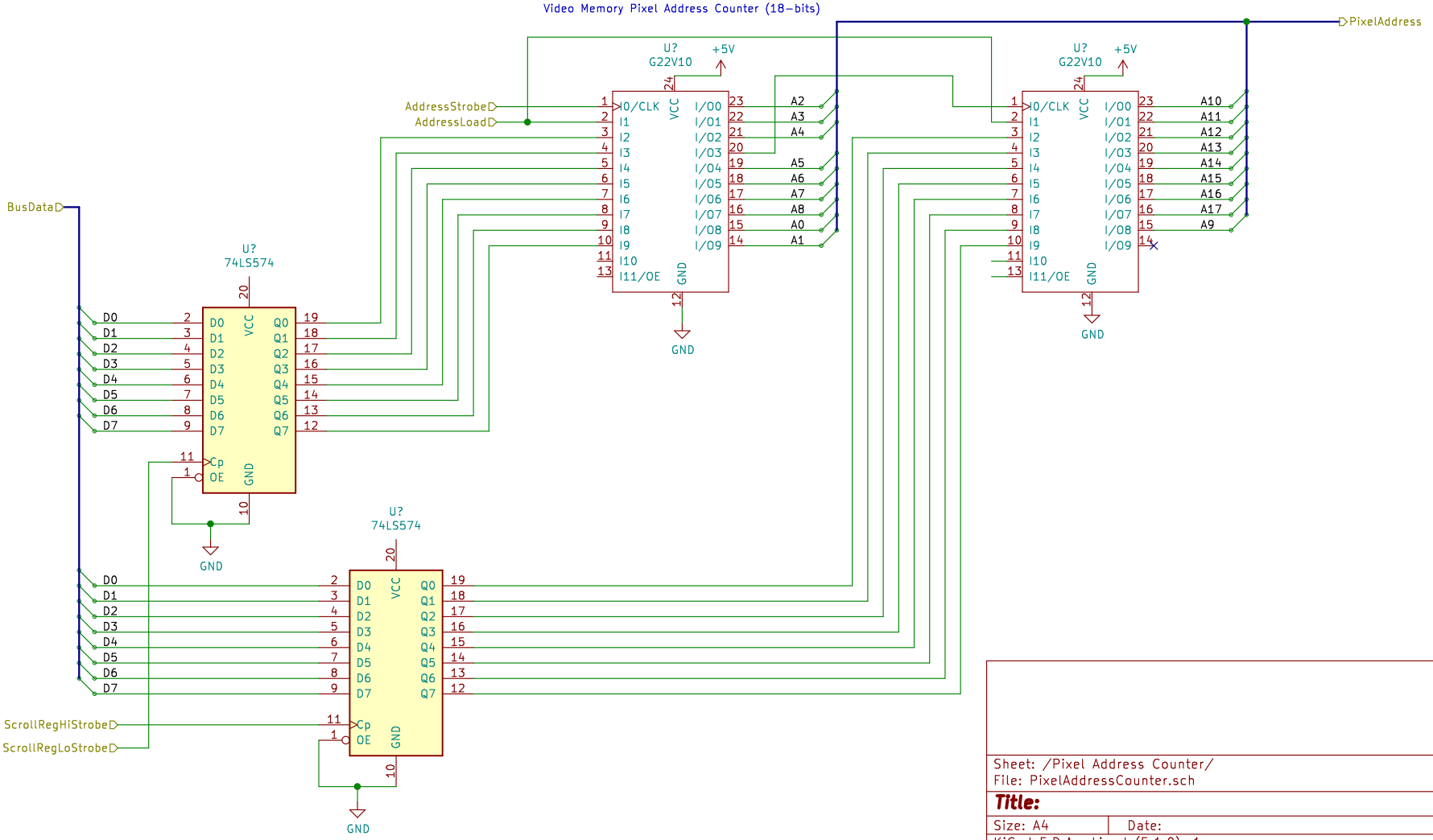

VideoMode
VM0
VM1
VM2
VM3
VideoData
VD0
VD1
VD2
VD3
VD4
VD5
VD6
VD7
PixelAddress
PA0
PA1
PA2
PA3
U?
74LS257
VD0 2
VD4 3
VD1 5
VD5 6
VD2 14
VD6 13
VD3 11
VD6 10
PA0 1
VM1 15
16
8
I0a
I1a
I0b
I1b
I0c
I1c
I0d
I1d
S
OE
VCC
GND
Za
Zb
Zc
Zd
4 PalA0
7 PalA1
12 PalA2
9 PalA3
U?
74LS253
VD0 6
VD2 5
VD4 4
VD6 3
VM2 1
VD1 10
VD3 11
VD5 12
VD7 13
VM2 15
PA0 14
PA1 2
16
8
I0a
I1a
I2a
I3a
OEa
I0b
I1b
I2b
I3b
OEb
A0
A1
VCC
GND
Za
Zb
7 PalA0
9 PalA1
U?
UM61512A
PalA0 12
PalA1 11
PalA2 10
PalA3 9
PalA4 8
PalA5 7
PalA6 6
5
27
26
23
25
4
28
3
31
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
D0
D1
D2
D3
D4
D5
D6
D7
CE1
CE2
OE
WE
VCC
GND
13 PD0
14 PD1
15 PD2
17 PD3
18 PD4
19 PD5
20 PD6
21 PD7
22
30
24
29
32
16
Palette RAM
U19 => BlankMux.pld
Hblank
Vblank
U19
GAL16V8
+5V
20
10
GND
1 I1/CLK
PD0 2
PD1 3
PD2 4
PD3 5
PD4 6
PD5 7
PD6 8
PD7 9
11 I10/OE
I1/CLK
I2
I3
I4
I5
I6
I7
I8
I9
I10/OE
VCC
GND
IO1 19
IO2 18
IO3 17
IO4 16
IO5 15
IO6 14
IO7 13
IO8 12
R0
R1
R2
G0
G1
G2
B0
B1
B2
U?
74LS251
VD0 4
VD1 3
VD2 2
VD3 1
VD4 15
VD5 14
VD6 13
VD7 12
PA0 11
PA1 10
PA2 9
VM3 7
16
8
I0
I1
I2
I3
I4
I5
I6
I7
S0
S1
S2
OE
VCC
GND
Y
Y
5 PalA0
6
VD0 VD1 VD2 VD3 VD4 VD5 VD6 VD7
VM1: | PA = 0 | PA = 1
VM2: | PA = 0 | PA =1 | PA = 2 | PA = 3
VM3: | PA0 | PA1 | PA2 | PA3 | PA4 | PA5 | PA6 | PA7
Pixel Output
512x384 + border
640x480 @60Hz
Canned Bytes
Sheet: /Pixel Output/
File: PixelOutput.sch
Title: Zalt TTL VGA
Size: A4
Date: 2020-02-09
Rev: 0.1
KiCad E.D.A. kicad (5.1.0)-1
Id: 3/8


From VRAM
Address Counter
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
A16
A17
A18
PixelAddress
U?
74LS245
+5V
A1 2
A2 3
A3 4
A4 5
A5 6
A6 7
A7 8
A9 9
A0
A1
A2
A3
A4
A5
A6
A7
VCC
20
B0 18
B1 17
B2 16
B3 15
B4 14
B5 13
B6 12
B7 11
MA0
MA1
MA2
MA3
MA4
MA5
MA6
MA7
+5V
1
A->B
CE
VM1 19
GND
10
GND
U?
74LS245
+5V
A2 2
A3 4
A4 5
A5 6
A6 7
A7 8
A8 9
A10 9
A0
A1
A2
A3
A4
A5
A6
A7
VCC
20
B0 18
B1 17
B2 16
B3 15
B4 14
B5 13
B6 12
B7 11
MA0
MA1
MA2
MA3
MA4
MA5
MA6
MA7
+5V
1
A->B
CE
VM2 19
GND
10
GND
U?
74LS245
+5V
A3 2
A4 3
A5 4
A6 5
A7 6
A8 7
A9 8
A11 9
A0
A1
A2
A3
A4
A5
A6
A7
VCC
20
B0 18
B1 17
B2 16
B3 15
B4 14
B5 13
B6 12
B7 11
MA0
MA1
MA2
MA3
MA4
MA5
MA6
MA7
+5V
1
A->B
CE
VM3 19
GND
10
GND
To VRAM
MA0
MA1
MA2
MA3
MA4
MA5
MA6
MA7
MA8
MA9
MA10
MA11
MA12
MA13
MA14
MA15
MA16
MA17
MA18
VideoAddress
U?
74LS245
+5V
A10 2
A11 3
A12 4
A13 5
A14 6
A15 7
A16 8
A17 9
A0
A1
A2
A3
A4
A5
A6
A7
VCC
20
B0 18
B1 17
B2 16
B3 15
B4 14
B5 13
B6 12
B7 11
MA8
MA9
MA10
MA11
MA12
MA13
MA14
MA15
+5V
1
A->B
CE
VM1 19
GND
10
GND
U?
74LS245
+5V
A11 2
A12 3
A13 4
A14 5
A15 6
A16 7
A17 8
A18 9
A0
A1
A2
A3
A4
A5
A6
A7
VCC
20
B0 18
B1 17
B2 16
B3 15
B4 14
B5 13
B6 12
B7 11
MA8
MA9
MA10
MA11
MA12
MA13
MA14
MA15
+5V
1
A->B
CE
VM2 19
GND
10
GND
U?
74LS245
+5V
A12 2
A13 3
A14 4
A15 5
A16 6
A17 7
A18 8
9
A0
A1
A2
A3
A4
A5
A6
A7
VCC
20
B0 18
B1 17
B2 16
B3 15
B4 14
B5 13
B6 12
B7 11
MA8
MA9
MA10
MA11
MA12
MA13
MA14
MA15
+5V
1
A->B
CE
VM3 19
GND
10
GND
Mode 0:
disengage driving the
VRAM / CPU access
Mode 1:
A0 selects pixel data
A8 duplicate line
A1–A7 => A0–A6
A9–A18 => A7–A16
Mode 2:
A0,A1 selects pixel data
A9 duplicate line
A2–A8 => A0–A6
A10–A18 => A7–A15
Mode 3:
A0,A1,A2 selects pixel data
A10 duplicate line
A3–A9 => A0–A6
A11–A18 => A7–A14
VideoModeSelect
VideoMode
U?A
74LS139
VMS1 3
VMS0 2
VideoEnable 1
A1
A0
E
O0 4
O1 5
O2 6
O3 7
VM0
VM1
VM2
VM3
Based on Opt0/1 one of 4 Video Modes is selected.
Everything is based of the 640x480@60Hz timing.
The VRAM Address Counter counts visible pixels.
Each Video Mode maps these pixel addresses to VRAM addresses.
VM0:off
VM1: 256x192 – 16 colors (4 bits per pixel)
VM2: 256x192 – 4 colors (2 bits per pixel)
VM3: 256x192 – 2 colors (1 bit per pixel)
Sheet: /Video Modes/
File: VideoModes.sch
Title:
Size: A4
Date:
Rev:
KiCad E.D.A. kicad (5.1.0)-1
Id: 4/8

We have registers here that load in a start address for
each frame. That way a scrolling function can be supported
in hardware. The software would load a value of the address
of the start of the next frame based on the direction of scrolling.
Left or right would simply increment or decrement the start
address. Scrolling up and down would be addding/subtracting
a complete horizontal line worth of bytes.

U6 => BinaryCounterLo.pld
U7 => BinaryCounterHi.pld

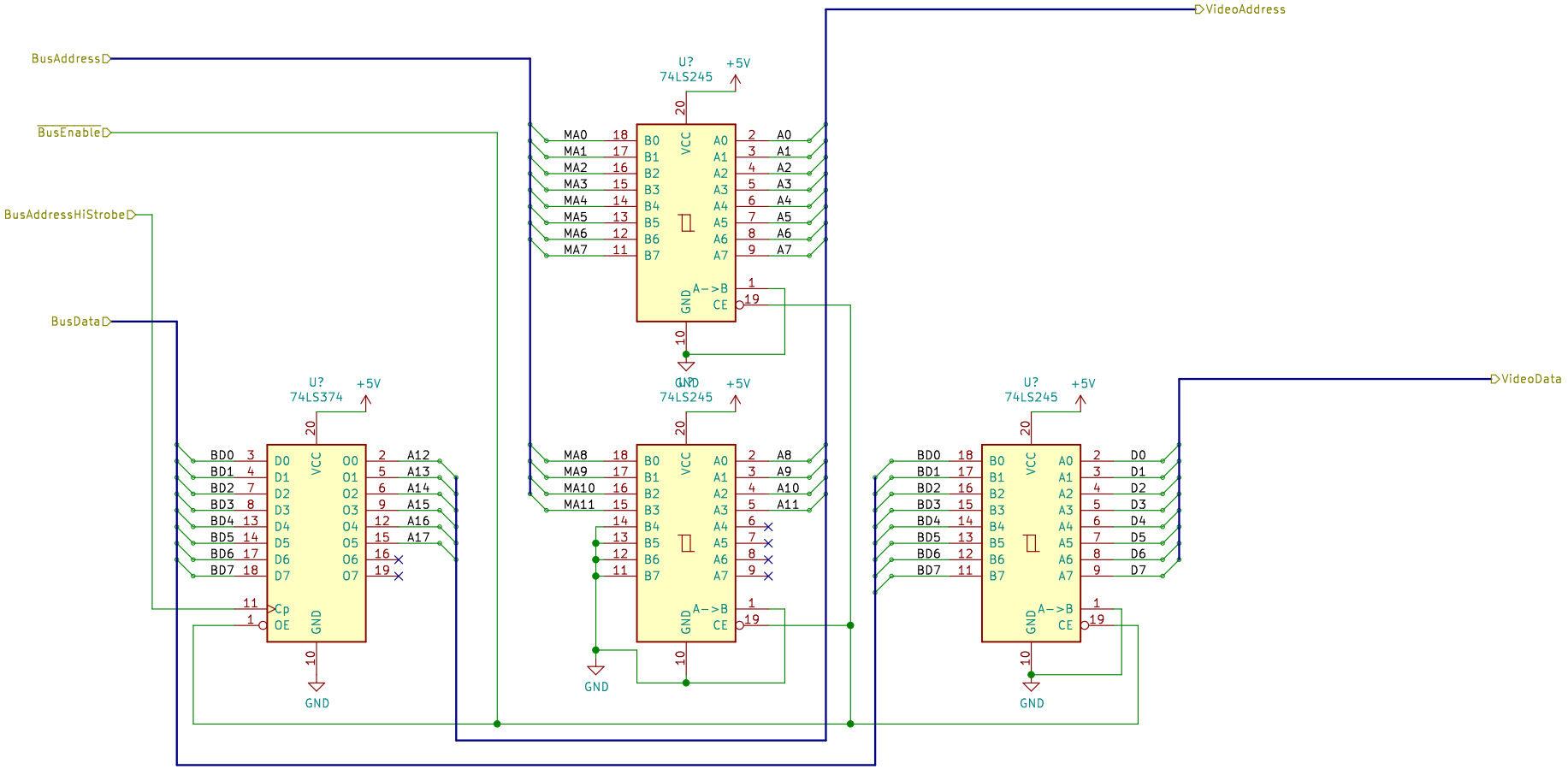
Video Memory Pixel Address Counter (18-bits)



Sheet: /Pixel Address Counter/
File: PixelAddressCounter.sch

Title:

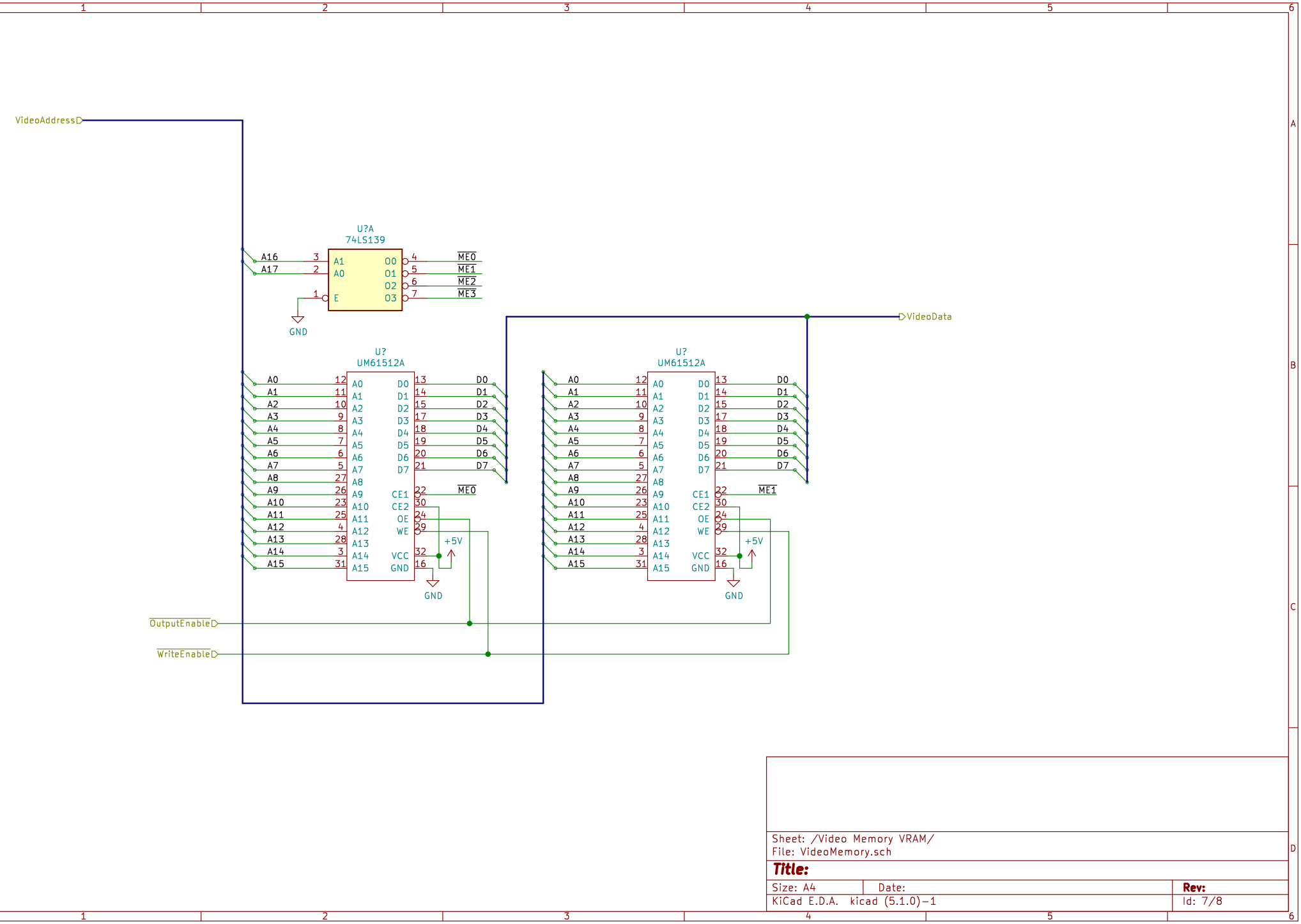
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.0)-1		Id: 5/8



Z80 interfaces through a 4k Memory Page.
The location (bit address) of this memory page is determined by the Bus Decoder.

The Control Register provides the upper 6 bits A12..A17 of the
VRAM address and can only be changed through an IO write.
The IO address (A0-A7) is also determined by the Bus Decoder.

Sheet: /Bus Interface/		
File: BusInterface.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.0)-1		Id: 6/8



Sheet: /Video Memory VRAM/		
File: VideoMemory.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.0)-1		Id: 7/8

BusAddressHiStrobe

BusAddress

VideoEnable

BusCtrl

BusEnable

BusData

ScrollRegLoStrobe

ScrollRegHiStrobe

Settings

Sheet: /New Bus Decoder/
File: NewBusDecoder.sch

Title:

Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.0)-1		Id: 8/8