# PSoC® Creator™
# Project Datasheet for SystemController

# Table of Contents

# 1 Overview

The Cypress PSoC 5 is a family of 32-bit devices with the following characteristics:

- High-performance 32-bit ARM Cortex-M3 core with a nested vectored interrupt controller (NVIC) and a high-performance DMA controller
- Digital system that includes configurable Universal Digital Blocks (UDBs) and specific function peripherals, such as USB, I2C and SPI
- Analog subsystem that includes 20-bit Delta Sigma converters (ADC), SAR ADCs, 8-bit DACs that can be configured for 12-bit operation, comparators, op amps and configurable switched capacitor (SC) and continuous time (CT) blocks to create PGAs, TIAs, mixers, and more
- Several types of memory elements, including SRAM, flash, and EEPROM
- Programming and debug system through JTAG, serial wire debug (SWD), and single wire viewer (SWV)
- Flexible routing to all pins

Figure 1 shows the major components of a typical CY8C58LP family member PSoC 5 device. For details on all the systems listed above, please refer to the PSoC 5 Technical Reference Manual .

Figure 1. CY8C58LP Device Family Block Diagram

Table 1 lists the key characteristics of this device.

Table 1. Device Characteristics

| Name | Value |
|---|---|
| Part Number | CY8C5888LTI-LP097 |
| Package Name | 68-QFN |
| Architecture | PSoC 5 |
| Family | CY8C58LP |
| CPU speed (MHz) | 80 |
| Flash size (kBytes) | 256 |
| SRAM size (kBytes) | 64 |
| EEPROM size (Bytes) | 2048 |
| Vdd range (V) | 1.71 to 5.5 |
| Automotive qualified | No (Industrial Grade Only) |
| Temp range (Celcius) | -40 to 85 |
| JTAG ID | 0x2E161069 |

NOTE: The CPU speed noted above is the maximum available speed. The CPU is clocked by Bus Clock, listed in the System Clocks section below.

Table 2 lists the device resources that this design uses:

Table 2. Device Resources

| Resource Type | Used | Free | Max | % Used |
|---|---|---|---|---|
| Digital Clocks | 3 | 5 | 8 | 37.50 % |
| Analog Clocks | 0 | 4 | 4 | 0.00 % |
| CapSense Buffers | 0 | 2 | 2 | 0.00 % |
| Digital Filter Block | 0 | 1 | 1 | 0.00 % |
| Interrupts | 3 | 29 | 32 | 9.38 % |
| IO | 38 | 10 | 48 | 79.17 % |
| Segment LCD | 0 | 1 | 1 | 0.00 % |
| CAN 2.0b | 0 | 1 | 1 | 0.00 % |
| I2C | 0 | 1 | 1 | 0.00 % |
| USB | 0 | 1 | 1 | 0.00 % |
| DMA Channels | 0 | 24 | 24 | 0.00 % |
| Timer | 0 | 4 | 4 | 0.00 % |
| UDB | | | | |
|    Macrocells | 28 | 164 | 192 | 14.58 % |
|    Unique P-terms | 46 | 338 | 384 | 11.98 % |
|    Total P-terms | 55 | | | |
|    Datapath Cells | 3 | 21 | 24 | 12.50 % |
|    Status Cells | 4 | 20 | 24 | 16.67 % |
|      Status Registers | 1 | | | |
|      StatusI Registers | 2 | | | |
|      Routed Count7 Load/Enable | 1 | | | |
|    Control Cells | 2 | 22 | 24 | 8.33 % |
|      Control Registers | 1 | | | |
|      Count7 Cells | 1 | | | |
| Opamp | 0 | 4 | 4 | 0.00 % |
| Comparator | 0 | 4 | 4 | 0.00 % |
| Delta-Sigma ADC | 0 | 1 | 1 | 0.00 % |
| LPF | 0 | 2 | 2 | 0.00 % |
| SAR ADC | 0 | 2 | 2 | 0.00 % |
| Analog (SC/CT) Blocks | 0 | 4 | 4 | 0.00 % |

| Resource Type | Used | Free | Max | % Used |
|---|---|---|---|---|
| DAC | | | | |
| VIDAC | 0 | 4 | 4 | 0.00 % |

# 2 Pins

Figure 2 shows the pin layout of this device.

Figure 2. Device Pin Layout
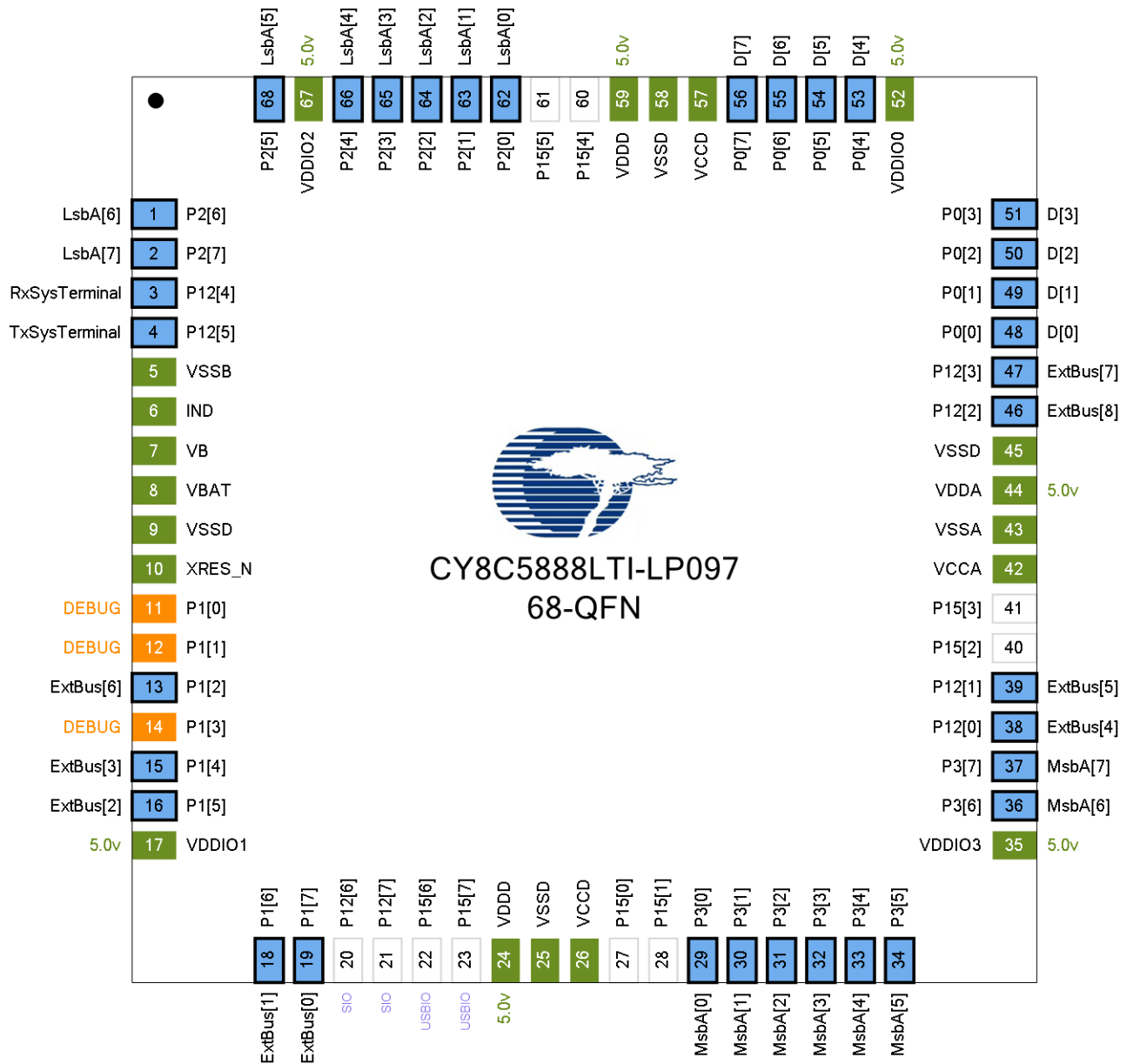
## 2.1 Hardware Pins

Table 3 contains information about the pins on this device in device pin order. (No connection ["n/c"] pins have been omitted.)

Table 3. Device Pins

| Pin | Port | Name | Type | Drive Mode | Reset State |
|---|---|---|---|---|---|
| 1 | P2[6] | LsbA[6] | Software In/Out | Strong drive | HiZ Analog Unb |
| 2 | P2[7] | LsbA[7] | Software In/Out | Strong drive | HiZ Analog Unb |
| 3 | P12[4] | RxSysTerminal | Dgtl In | HiZ digital | HiZ Analog Unb |
| 4 | P12[5] | TxSysTerminal | Dgtl Out | Strong drive | HiZ Analog Unb |
| 5 | VSSB | VSSB | Dedicated | | |
| 6 | IND | IND | Dedicated | | |
| 7 | VB | VB | Dedicated | | |
| 8 | VBAT | VBAT | Dedicated | | |
| 9 | VSSD | VSSD | Power | | |
| 10 | XRES_N | XRES_N | Dedicated | | |
| 11 | P1[0] | Debug:SWD_IO | Reserved | | |
| 12 | P1[1] | Debug:SWD_CK | Reserved | | |
| 13 | P1[2] | ExtBus[6] | Software Input | HiZ digital | HiZ Analog Unb |
| 14 | P1[3] | Debug:SWV | Reserved | | |
| 15 | P1[4] | ExtBus[3] | Dgtl In | Strong drive | HiZ Analog Unb |
| 16 | P1[5] | ExtBus[2] | Software In/Out | Strong drive | HiZ Analog Unb |
| 17 | VDDIO1 | VDDIO1 | Power | | |
| 18 | P1[6] | ExtBus[1] | Dgtl In | Strong drive | HiZ Analog Unb |
| 19 | P1[7] | ExtBus[0] | Software In/Out | Strong drive | HiZ Analog Unb |
| 20 | P12[6] | SIO [unused] | | | HiZ Analog Unb |
| 21 | P12[7] | SIO [unused] | | | HiZ Analog Unb |
| 22 | P15[6] | USB IO [unused] | | | HiZ Analog Unb |
| 23 | P15[7] | USB IO [unused] | | | HiZ Analog Unb |
| 24 | VDDD | VDDD | Power | | |
| 25 | VSSD | VSSD | Power | | |
| 26 | VCCD | VCCD | Power | | |
| 27 | P15[0] | GPIO [unused] | | | HiZ Analog Unb |
| 28 | P15[1] | GPIO [unused] | | | HiZ Analog Unb |
| 29 | P3[0] | MsbA[0] | Dgtl In | Strong drive | HiZ Analog Unb |
| 30 | P3[1] | MsbA[1] | Dgtl In | Strong drive | HiZ Analog Unb |
| 31 | P3[2] | MsbA[2] | Dgtl In | Strong drive | HiZ Analog Unb |
| 32 | P3[3] | MsbA[3] | Dgtl In | Strong drive | HiZ Analog Unb |
| 33 | P3[4] | MsbA[4] | Dgtl In | Strong drive | HiZ Analog Unb |
| 34 | P3[5] | MsbA[5] | Dgtl In | Strong drive | HiZ Analog Unb |
| 35 | VDDIO3 | VDDIO3 | Power | | |
| 36 | P3[6] | MsbA[6] | Dgtl In | Strong drive | HiZ Analog Unb |
| 37 | P3[7] | MsbA[7] | Dgtl In | Strong drive | HiZ Analog Unb |
| 38 | P12[0] | ExtBus[4] | Software Output | OD, DL | HiZ Analog Unb |
| 39 | P12[1] | ExtBus[5] | Software Input | HiZ digital | HiZ Analog Unb |

2 Pins

| Pin | Port | Name | Type | Drive Mode | Reset State |
|-----|------|------|------|------------|-------------|
| 40 | P15[2] | GPIO [unused] | | | HiZ Analog Unb |
| 41 | P15[3] | GPIO [unused] | | | HiZ Analog Unb |
| 42 | VCCA | VCCA | Power | | |
| 43 | VSSA | VSSA | Power | | |
| 44 | VDDA | VDDA | Power | | |
| 45 | VSSD | VSSD | Power | | |
| 46 | P12[2] | ExtBus[8] | Software Output | OD, DL | HiZ Analog Unb |
| 47 | P12[3] | ExtBus[7] | Dgtl Out | Strong drive | HiZ Analog Unb |
| 48 | P0[0] | D[0] | Dgtl In | Strong drive | HiZ Analog Unb |
| 49 | P0[1] | D[1] | Dgtl In | Strong drive | HiZ Analog Unb |
| 50 | P0[2] | D[2] | Dgtl In | Strong drive | HiZ Analog Unb |
| 51 | P0[3] | D[3] | Dgtl In | Strong drive | HiZ Analog Unb |
| 52 | VDDIO0 | VDDIO0 | Power | | |
| 53 | P0[4] | D[4] | Dgtl In | Strong drive | HiZ Analog Unb |
| 54 | P0[5] | D[5] | Dgtl In | Strong drive | HiZ Analog Unb |
| 55 | P0[6] | D[6] | Dgtl In | Strong drive | HiZ Analog Unb |
| 56 | P0[7] | D[7] | Dgtl In | Strong drive | HiZ Analog Unb |
| 57 | VCCD | VCCD | Power | | |
| 58 | VSSD | VSSD | Power | | |
| 59 | VDDD | VDDD | Power | | |
| 60 | P15[4] | GPIO [unused] | | | HiZ Analog Unb |
| 61 | P15[5] | GPIO [unused] | | | HiZ Analog Unb |
| 62 | P2[0] | LsbA[0] | Software In/Out | Strong drive | HiZ Analog Unb |
| 63 | P2[1] | LsbA[1] | Software In/Out | Strong drive | HiZ Analog Unb |
| 64 | P2[2] | LsbA[2] | Software In/Out | Strong drive | HiZ Analog Unb |
| 65 | P2[3] | LsbA[3] | Software In/Out | Strong drive | HiZ Analog Unb |
| 66 | P2[4] | LsbA[4] | Software In/Out | Strong drive | HiZ Analog Unb |
| 67 | VDDIO2 | VDDIO2 | Power | | |
| 68 | P2[5] | LsbA[5] | Software In/Out | Strong drive | HiZ Analog Unb |

Abbreviations used in Table 3 have the following meanings:
- HiZ Analog Unb = Hi-Z Analog Unbuffered
- Dgtl In = Digital Input
- HiZ digital = High impedance digital
- Dgtl Out = Digital Output
- OD, DL = Open drain, drives low

## 2.2 Hardware Ports

Table 4 contains information about the pins on this device in device port order. (No connection ["n/c"], power and dedicated pins have been omitted.)

Table 4. Device Ports

| Port | Pin | Name | Type | Drive Mode | Reset State |
|------|-----|------|------|------------|-------------|
| P0[0] | 48 | D[0] | Dgtl In | Strong drive | HiZ Analog Unb |
| P0[1] | 49 | D[1] | Dgtl In | Strong drive | HiZ Analog Unb |
| P0[2] | 50 | D[2] | Dgtl In | Strong drive | HiZ Analog Unb |
| P0[3] | 51 | D[3] | Dgtl In | Strong drive | HiZ Analog Unb |
| P0[4] | 53 | D[4] | Dgtl In | Strong drive | HiZ Analog Unb |
| P0[5] | 54 | D[5] | Dgtl In | Strong drive | HiZ Analog Unb |
| P0[6] | 55 | D[6] | Dgtl In | Strong drive | HiZ Analog Unb |
| P0[7] | 56 | D[7] | Dgtl In | Strong drive | HiZ Analog Unb |
| P1[0] | 11 | Debug:SWD_IO | Reserved | | |
| P1[1] | 12 | Debug:SWD_CK | Reserved | | |
| P1[2] | 13 | ExtBus[6] | Software Input | HiZ digital | HiZ Analog Unb |
| P1[3] | 14 | Debug:SWV | Reserved | | |
| P1[4] | 15 | ExtBus[3] | Dgtl In | Strong drive | HiZ Analog Unb |
| P1[5] | 16 | ExtBus[2] | Software In/Out | Strong drive | HiZ Analog Unb |
| P1[6] | 18 | ExtBus[1] | Dgtl In | Strong drive | HiZ Analog Unb |
| P1[7] | 19 | ExtBus[0] | Software In/Out | Strong drive | HiZ Analog Unb |
| P12[0] | 38 | ExtBus[4] | Software Output | OD, DL | HiZ Analog Unb |
| P12[1] | 39 | ExtBus[5] | Software Input | HiZ digital | HiZ Analog Unb |
| P12[2] | 46 | ExtBus[8] | Software Output | OD, DL | HiZ Analog Unb |
| P12[3] | 47 | ExtBus[7] | Dgtl Out | Strong drive | HiZ Analog Unb |
| P12[4] | 3 | RxSysTerminal | Dgtl In | HiZ digital | HiZ Analog Unb |
| P12[5] | 4 | TxSysTerminal | Dgtl Out | Strong drive | HiZ Analog Unb |
| P12[6] | 20 | SIO [unused] | | | HiZ Analog Unb |
| P12[7] | 21 | SIO [unused] | | | HiZ Analog Unb |
| P15[0] | 27 | GPIO [unused] | | | HiZ Analog Unb |
| P15[1] | 28 | GPIO [unused] | | | HiZ Analog Unb |
| P15[2] | 40 | GPIO [unused] | | | HiZ Analog Unb |
| P15[3] | 41 | GPIO [unused] | | | HiZ Analog Unb |
| P15[4] | 60 | GPIO [unused] | | | HiZ Analog Unb |
| P15[5] | 61 | GPIO [unused] | | | HiZ Analog Unb |
| P15[6] | 22 | USB IO [unused] | | | HiZ Analog Unb |
| P15[7] | 23 | USB IO [unused] | | | HiZ Analog Unb |
| P2[0] | 62 | LsbA[0] | Software In/Out | Strong drive | HiZ Analog Unb |
| P2[1] | 63 | LsbA[1] | Software In/Out | Strong drive | HiZ Analog Unb |
| P2[2] | 64 | LsbA[2] | Software In/Out | Strong drive | HiZ Analog Unb |
| P2[3] | 65 | LsbA[3] | Software In/Out | Strong drive | HiZ Analog Unb |

2 Pins

| Port | Pin | Name | Type | Drive Mode | Reset State |
|------|-----|------|------|------------|-------------|
| P2[4] | 66 | LsbA[4] | Software In/Out | Strong drive | HiZ Analog Unb |
| P2[5] | 68 | LsbA[5] | Software In/Out | Strong drive | HiZ Analog Unb |
| P2[6] | 1 | LsbA[6] | Software In/Out | Strong drive | HiZ Analog Unb |
| P2[7] | 2 | LsbA[7] | Software In/Out | Strong drive | HiZ Analog Unb |
| P3[0] | 29 | MsbA[0] | Dgtl In | Strong drive | HiZ Analog Unb |
| P3[1] | 30 | MsbA[1] | Dgtl In | Strong drive | HiZ Analog Unb |
| P3[2] | 31 | MsbA[2] | Dgtl In | Strong drive | HiZ Analog Unb |
| P3[3] | 32 | MsbA[3] | Dgtl In | Strong drive | HiZ Analog Unb |
| P3[4] | 33 | MsbA[4] | Dgtl In | Strong drive | HiZ Analog Unb |
| P3[5] | 34 | MsbA[5] | Dgtl In | Strong drive | HiZ Analog Unb |
| P3[6] | 36 | MsbA[6] | Dgtl In | Strong drive | HiZ Analog Unb |
| P3[7] | 37 | MsbA[7] | Dgtl In | Strong drive | HiZ Analog Unb |

Abbreviations used in Table 4 have the following meanings:
- Dgtl In = Digital Input
- HiZ Analog Unb = Hi-Z Analog Unbuffered
- HiZ digital = High impedance digital
- OD, DL = Open drain, drives low
- Dgtl Out = Digital Output

## 2.3 Software Pins

Table 5 contains information about the software pins on this device in alphabetical order. (Only software-accessible pins are shown.)

Table 5. Software Pins

| Name | Port | Type | Reset State |
|------|------|------|-------------|
| D[0] | P0[0] | Dgtl In | HiZ Analog Unb |
| D[1] | P0[1] | Dgtl In | HiZ Analog Unb |
| D[2] | P0[2] | Dgtl In | HiZ Analog Unb |
| D[3] | P0[3] | Dgtl In | HiZ Analog Unb |
| D[4] | P0[4] | Dgtl In | HiZ Analog Unb |
| D[5] | P0[5] | Dgtl In | HiZ Analog Unb |
| D[6] | P0[6] | Dgtl In | HiZ Analog Unb |
| D[7] | P0[7] | Dgtl In | HiZ Analog Unb |
| Debug:SWD_CK | P1[1] | Reserved | |
| Debug:SWD_IO | P1[0] | Reserved | |
| Debug:SWV | P1[3] | Reserved | |
| ExtBus[0] | P1[7] | Software In/Out | HiZ Analog Unb |
| ExtBus[1] | P1[6] | Dgtl In | HiZ Analog Unb |
| ExtBus[2] | P1[5] | Software In/Out | HiZ Analog Unb |
| ExtBus[3] | P1[4] | Dgtl In | HiZ Analog Unb |
| ExtBus[4] | P12[0] | Software Output | HiZ Analog Unb |
| ExtBus[5] | P12[1] | Software Input | HiZ Analog Unb |
| ExtBus[6] | P1[2] | Software Input | HiZ Analog Unb |
| ExtBus[7] | P12[3] | Dgtl Out | HiZ Analog Unb |
| ExtBus[8] | P12[2] | Software Output | HiZ Analog Unb |
| LsbA[0] | P2[0] | Software In/Out | HiZ Analog Unb |
| LsbA[1] | P2[1] | Software In/Out | HiZ Analog Unb |
| LsbA[2] | P2[2] | Software In/Out | HiZ Analog Unb |
| LsbA[3] | P2[3] | Software In/Out | HiZ Analog Unb |
| LsbA[4] | P2[4] | Software In/Out | HiZ Analog Unb |
| LsbA[5] | P2[5] | Software In/Out | HiZ Analog Unb |
| LsbA[6] | P2[6] | Software In/Out | HiZ Analog Unb |
| LsbA[7] | P2[7] | Software In/Out | HiZ Analog Unb |
| MsbA[0] | P3[0] | Dgtl In | HiZ Analog Unb |
| MsbA[1] | P3[1] | Dgtl In | HiZ Analog Unb |
| MsbA[2] | P3[2] | Dgtl In | HiZ Analog Unb |
| MsbA[3] | P3[3] | Dgtl In | HiZ Analog Unb |
| MsbA[4] | P3[4] | Dgtl In | HiZ Analog Unb |

2 Pins

| Name | Port | Type | Reset State |
|------|------|------|-------------|
| MsbA[5] | P3[5] | Dgtl In | HiZ Analog Unb |
| MsbA[6] | P3[6] | Dgtl In | HiZ Analog Unb |
| MsbA[7] | P3[7] | Dgtl In | HiZ Analog Unb |
| RxSysTerminal | P12[4] | Dgtl In | HiZ Analog Unb |
| TxSysTerminal | P12[5] | Dgtl Out | HiZ Analog Unb |

Abbreviations used in Table 5 have the following meanings:
- Dgtl In = Digital Input
- HiZ Analog Unb = Hi-Z Analog Unbuffered
- Dgtl Out = Digital Output

For more information on reading, writing and configuring pins, please refer to:
- Pins chapter in the System Reference Guide
  - CyPins API routines
- Programming Application Interface section in the cy_pins component datasheet

# 3 System Settings

## 3.1 System Configuration

Table 6. System Configuration Settings

| Name | Value |
|---|---|
| Device Configuration Mode | Compressed |
| Enable Error Correcting Code (ECC) | False |
| Store Configuration Data in ECC Memory | True |
| Instruction Cache Enabled | True |
| Enable Fast IMO During Startup | True |
| Unused Bonded IO | Allow but warn |
| Heap Size (bytes) | 0x80 |
| Stack Size (bytes) | 0x0800 |
| Include CMSIS Core Peripheral Library Files | True |

## 3.2 System Debug Settings

Table 7. System Debug Settings

| Name | Value |
|---|---|
| Debug Select | SWD+SWV (serial wire debug and viewer) |
| Enable Device Protection | False |
| Embedded Trace (ETM) | False |
| Use Optional XRES | False |

## 3.3 System Operating Conditions

Table 8. System Operating Conditions

| Name | Value |
|---|---|
| Variable VDDA | False |
| VDDA (V) | 5.0 |
| VDDD (V) | 5.0 |
| VDDIO0 (V) | 5.0 |
| VDDIO1 (V) | 5.0 |
| VDDIO2 (V) | 5.0 |
| VDDIO3 (V) | 5.0 |
| Temperature Range | 0C - 85/125C |

# 4 Clocks

The clock system includes these clock resources:
- Four internal clock sources increase system integration:
  - 3 to 74.7 MHz Internal Main Oscillator (IMO) ±1% at 3 MHz
  - 1 kHz, 33 kHz, and 100 kHz Internal Low Speed Oscillator (ILO) outputs
  - 12 to 80 MHz clock doubler output, sourced from IMO, MHz External Crystal Oscillator (MHzECO), and Digital System Interconnect (DSI)
  - 24 to 80 MHz fractional Phase-Locked Loop (PLL) sourced from IMO, MHzECO, and DSI
- Clock generated using a DSI signal from an external I/O pin or other logic
- Two external clock sources provide high precision clocks:
  - 4 to 25 MHz External Crystal Oscillator (MHzECO)
  - 32.768 kHz External Crystal Oscillator (kHzECO) for Real Time Clock (RTC)
- Dedicated 16-bit divider for bus clock
- Eight individually sourced 16-bit clock dividers for the digital system peripherals
- Four individually sourced 16-bit clock dividers with skew for the analog system peripherals
- IMO has a USB mode that synchronizes to USB host traffic, requiring no external crystal for USB. (USB equipped parts only)

Figure 3. System Clock Configuration
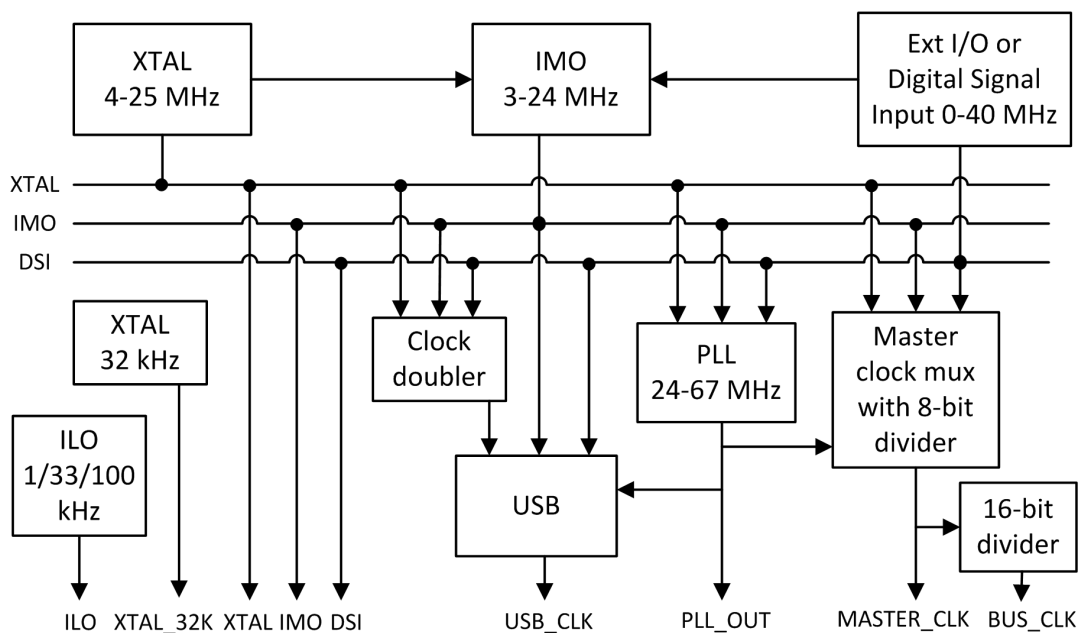
## 4.1 System Clocks

Table 9 lists the system clocks used in this design.

Table 9. System Clocks

| Name | Domain | Source | Desired Freq | Nominal Freq | Accuracy (%) | Start at Reset | Enabled |
|------|--------|--------|--------------|--------------|--------------|----------------|---------|
| PLL_OUT | DIGITAL | IMO | 48 MHz | 48 MHz | ±1 | True | True |
| MASTER_CLK | DIGITAL | PLL_OUT | ? MHz | 48 MHz | ±1 | True | True |
| BUS_CLK | DIGITAL | MASTER_CLK | ? MHz | 24 MHz | ±1 | True | True |
| IMO | DIGITAL | | 3 MHz | 3 MHz | ±1 | True | True |
| ILO | DIGITAL | | ? MHz | 1 kHz | -50,+100 | True | True |
| USB_CLK | DIGITAL | PLL_OUT | 48 MHz | ? MHz | ±0 | False | False |
| XTAL | DIGITAL | | 20 MHz | ? MHz | ±0.1 | False | False |
| XTAL 32kHz | DIGITAL | | 32.768 kHz | ? MHz | ±0 | False | False |
| Digital Signal | DIGITAL | | ? MHz | ? MHz | ±0 | False | False |

## 4.2 Local and Design Wide Clocks

Local clocks drive individual analog and digital blocks. Design wide clocks are a user-defined optimization, where two or more analog or digital blocks that share a common clock profile (frequency, etc) can be driven from the same clock divider output source.

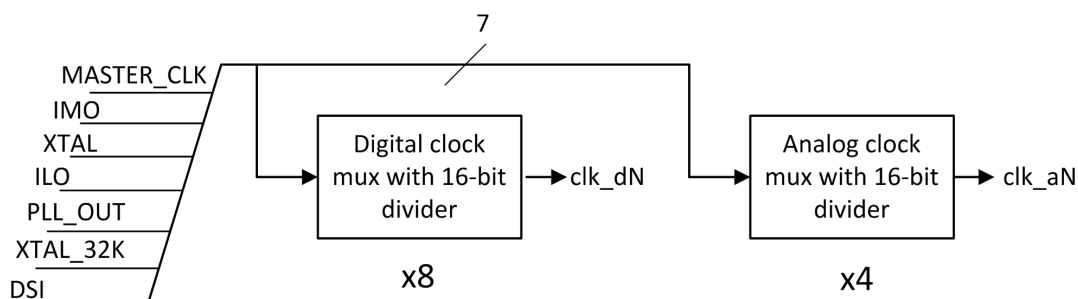Figure 4. Local and Design Wide Clock Configuration



Table 10 lists the local clocks used in this design.

Table 10. Local Clocks

| Name | Domain | Source | Desired Freq | Nominal Freq | Accuracy (%) | Start at Reset | Enabled |
|------|--------|--------|--------------|--------------|--------------|----------------|---------|
| CPUCLK_FAST | DIGITAL | MASTER_CLK | ? MHz | 24 MHz | ±1 | True | True |
| SysTerminal_-IntClock | DIGITAL | MASTER_CLK | 76.8 kHz | 76.8 kHz | ±1 | True | True |
| CPU_CLK | DIGITAL | ILO | 100 Hz | 100 Hz | -50,+100 | True | True |

For more information on clocking resources, please refer to:
- Clocking System chapter in the PSoC 5 Technical Reference Manual
- Clocking chapter in the System Reference Guide
  - ○ CyPLL API routines
  - ○ CyIMO API routines
  - ○ CyILO API routines

4 Clocks

- o CyMaster API routines
- o CyXTAL API routines

# 5 Interrupts and DMAs

## 5.1 Interrupts

This design contains the following interrupt components: (0 is the highest priority)

Table 11. Interrupts

| Name | Priority | Vector |
|---|---|---|
| ISR_SYS_IOREQ | 1 | 0 |
| SysTerminal_-RXInternalInterrupt | 2 | 1 |
| SysTerminal_-TXInternalInterrupt | 3 | 2 |

For more information on interrupts, please refer to:
- Interrupt Controller chapter in the PSoC 5 Technical Reference Manual
- Interrupts chapter in the System Reference Guide
  - o CyInt API routines and related registers
- Datasheet for cy_isr component

## 5.2 DMAs

This design contains no DMA components.

# 6 Flash Memory

PSoC 5 devices offer a host of Flash protection options and device security features that you can leverage to meet the security and protection requirements of an application. These requirements range from protecting configuration settings or Flash data to locking the entire device from external access.

Table 12 lists the Flash protection settings for your design.

Table 12. Flash Protection Settings

| Start Address | End Address | Protection Level |
|---|---|---|
| 0x0 | 0x3FFFF | U - Unprotected |

Flash memory is organized as rows with each row of flash having 256 bytes. Each flash row can be assigned one of four protection levels:
- U - Unprotected
- F - Factory Upgrade
- R - Field Upgrade
- W - Full Protection

For more information on Flash memory and protection, please refer to:
- Flash Protection chapter in the PSoC 5 Technical Reference Manual
- Flash and EEPROM chapter in the System Reference Guide
  - CyWrite API routines
  - CyFlash API routines

# 7 Design Contents

This design's schematic content consists of the following schematic sheet:

## 7.1 Schematic Sheet: Page 1

Figure 5. Schematic Sheet: Page 1
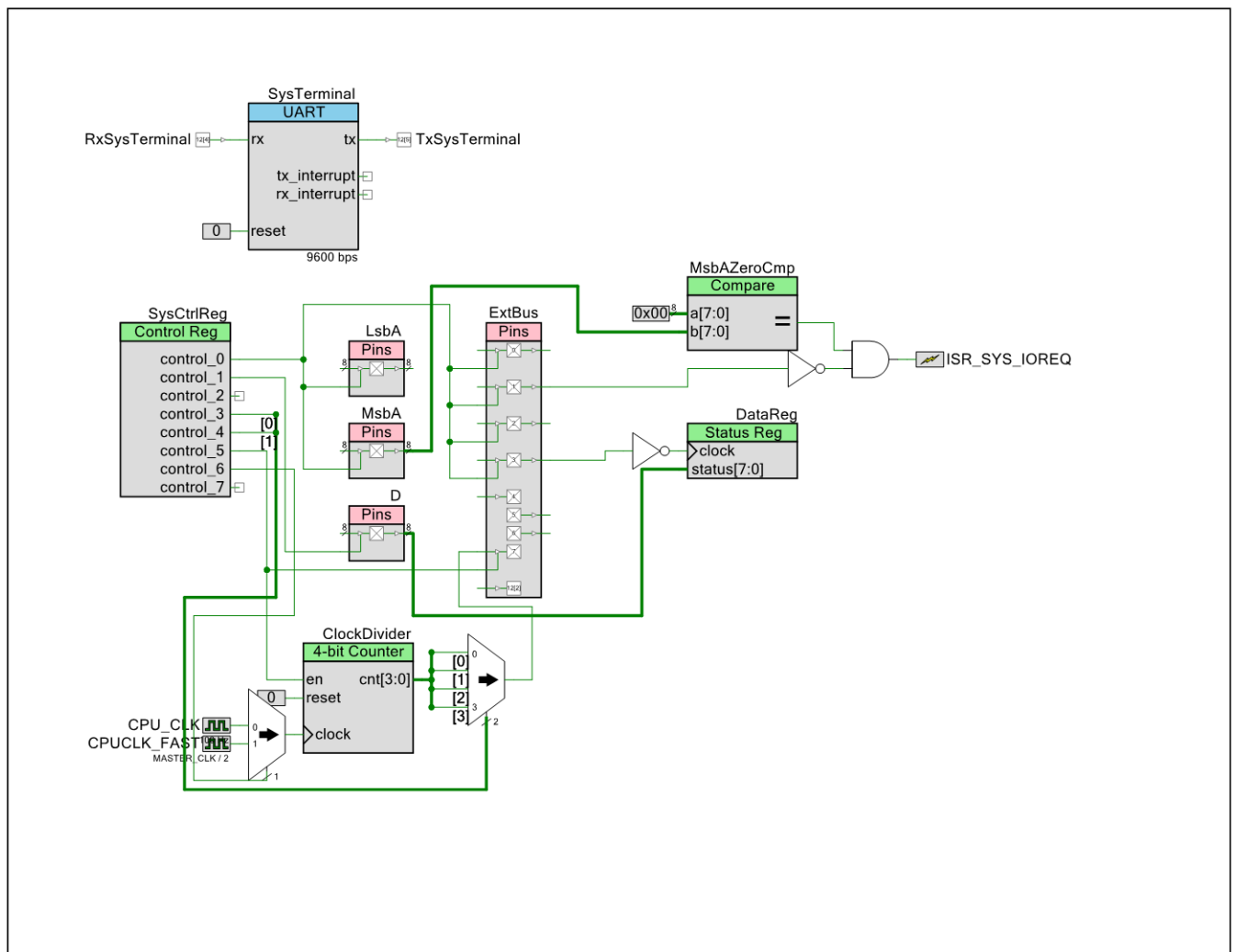


This schematic sheet contains the following component instances:
- Instance ClockDivider (type: BasicCounter_v1_0)
- Instance DataReg (type: CyStatusReg_v1_90)
- Instance MsbAZeroCmp (type: DigitalComp_v1_0)
- Instance SysCtrlReg (type: CyControlReg_v1_80)
- Instance SysTerminal (type: UART_v2_50)

# 8 Components

## 8.1 Component type: BasicCounter [v1.0]

### 8.1.1 Instance ClockDivider

**Description: Basic Counter**
**Instance type: BasicCounter [v1.0]**
**Datasheet: online component datasheet for BasicCounter**

Table 13. Component Parameters for ClockDivider

| Parameter Name | Value | Description |
|---|---|---|
| Width | 4 | Width of the counter. Must be between 2 and 32. |

## 8.2 Component type: CyControlReg [v1.80]

### 8.2.1 Instance SysCtrlReg

**Description: The Control Register allows the firmware to set values for to use for digital signals.**
**Instance type: CyControlReg [v1.80]**
**Datasheet: online component datasheet for CyControlReg**

Table 14. Component Parameters for SysCtrlReg

| Parameter Name | Value | Description |
|---|---|---|
| Bit0Mode | DirectMode | Defines bit 0 mode |
| Bit1Mode | DirectMode | Defines bit 1 mode |
| Bit2Mode | DirectMode | Defines bit 2 mode |
| Bit3Mode | DirectMode | Defines bit 3 mode |
| Bit4Mode | DirectMode | Defines bit 4 mode |
| Bit5Mode | DirectMode | Defines bit 5 mode |
| Bit6Mode | DirectMode | Defines bit 6 mode |
| Bit7Mode | DirectMode | Defines bit 7 mode |
| BitValue | 0 | Defines bit value |
| BusDisplay | false | Displays the output terminals as bus |
| ExternalReset | false | Shows the reset terminal |
| NumOutputs | 8 | Defines the number of outputs needed (1-8) |

## 8.3 Component type: CyStatusReg [v1.90]

### 8.3.1 Instance DataReg

**Description: The Status Register allows the firmware to read values from digital signals.**
**Instance type: CyStatusReg [v1.90]**
**Datasheet: online component datasheet for CyStatusReg**

Table 15. Component Parameters for DataReg

| Parameter Name | Value | Description |
|---|---|---|
| Bit0Mode | Sticky (Clear on Read) | Bit Mode for Bit 0 of the Status Register |
| Bit1Mode | Sticky (Clear on Read) | Bit Mode for Bit 1 of the Status Register |
| Bit2Mode | Sticky (Clear on Read) | Bit Mode for Bit 2 of the Status Register |
| Bit3Mode | Sticky (Clear on Read) | Bit Mode for Bit 3 of the Status Register |
| Bit4Mode | Sticky (Clear on Read) | Bit Mode for Bit 4 of the Status Register |
| Bit5Mode | Sticky (Clear on Read) | Bit Mode for Bit 5 of the Status Register |
| Bit6Mode | Sticky (Clear on Read) | Bit Mode for Bit 6 of the Status Register |
| Bit7Mode | Sticky (Clear on Read) | Bit Mode for Bit 7 of the Status Register |
| BusDisplay | true | Displays the input terminals as bus |
| Interrupt | false | Shows the interrupt terminal |
| MaskValue | 0 | Defines the value of the interrupt mask |
| NumInputs | 8 | Defines the number of status inputs (1-8) |

## 8.4 Component type: DigitalComp [v1.0]

### 8.4.1 Instance MsbAZeroCmp

**Description: Digital Comparator**
**Instance type: DigitalComp [v1.0]**
**Datasheet: online component datasheet for DigitalComp**

Table 16. Component Parameters for MsbAZeroCmp

| Parameter Name | Value | Description |
|---|---|---|
| CmpType | = | Comparison used to generate output. |
| Width | 8 | Width of a and b terminals. Must be between 1 and 32. |

## 8.5 Component type: UART [v2.50]

### 8.5.1 Instance SysTerminal

**Description: Universal Asynchronous Receiver Transmitter**
**Instance type: UART [v2.50]**
**Datasheet: online component datasheet for UART**

Table 17. Component Parameters for SysTerminal

| Parameter Name | Value | Description |
|---|---|---|
| Address1 | 0 | This parameter specifies the RX Hardware Address #1. |
| Address2 | 0 | This parameter specifies the RX Hardware Address #2. |
| BaudRate | 9600 | Sets the target baud rate. |

| Parameter Name | Value | Description |
|---|---|---|
| BreakBitsRX | 13 | Specifies the break signal length for the RX (detection) channel. |
| BreakBitsTX | 13 | Specifies the break signal length for the TX channel. |
| BreakDetect | false | Enables the break detect hardware. |
| CRCoutputsEn | false | Enables the CRC outputs. |
| EnIntRXInterrupt | true | Enables the internal RX interrupt configuration and the ISR. |
| EnIntTXInterrupt | true | Enables the internal TX interrupt configuration and the ISR. |
| FlowControl | None | Enable the flow control signals. |
| HalfDuplexEn | false | Enables half duplex mode on the RX Half of the UART module. |
| HwTXEnSignal | false | Enables the external TX enable signal output. |
| InternalClock | true | Enables the internal clock. This parameter removes the clock input pin. |
| InterruptOnTXComplete | false | This is an Interrupt mask used to enable/disable the interrupt on 'TX complete' event. |
| InterruptOnTXFifoEmpty | true | This is an Interrupt mask used to enable/disable the interrupt on 'TX FIFO empty' event. |
| InterruptOnTXFifoFull | false | This is an Interrupt mask used to enable/disable the interrupt on 'TX FIFO full' event. |
| InterruptOnTXFifoNotFull | false | This is an Interrupt mask used to enable/disable the interrupt on 'TX FIFO not full' event. |
| IntOnAddressDetect | false | Enables the interrupt on hardware address detected event by default |
| IntOnAddressMatch | false | Enables the interrupt on hardware address match detected event by default |
| IntOnBreak | false | Enables the interrupt on break signal detected event by default |
| IntOnByteRcvd | true | Enables the interrupt on RX byte received event by default |
| IntOnOverrunError | false | Enables the interrupt on overrun error event by default |
| IntOnParityError | false | Enables the interrupt on parity error event by default |
| IntOnStopError | false | Enables the interrupt on stop error event by default |
| NumDataBits | 8 | Defines the number of data bits. Values can be 5, 6, 7 or 8 bits. |
| NumStopBits | 1 | Defines the number of stop bits. Values can be 1 or 2 bits. |
| OverSamplingRate | 8 | This parameter defines the over sampling rate. |

| Parameter Name | Value | Description |
|---|---|---|
| ParityType | None | Sets the parity type as Odd, Even or Mark/Space |
| ParityTypeSw | false | This parameter allows the parity type to be changed through software by using the WriteControlRegister API |
| RXAddressMode | None | Configures the RX hardware address detection mode |
| RXBufferSize | 256 | The size of the RAM space allocated for the RX input buffer. |
| RXEnable | true | Enables the RX in the UART |
| TXBitClkGenDP | true | When enabled, this parameter enables the TX clock generation on DataPath resource. When disabled, TX clock is generated from Clock7. |
| TXBufferSize | 128 | The size of the RAM space allocated for the TX output buffer. |
| TXEnable | true | Enables the TX in the UART |
| Use23Polling | false | Allows the use of 2 out of 3 polling resources on the RX UART sampler. |

# 9 Other Resources

The following documents contain important information on Cypress software APIs that might be relevant to this design:

- Standard Types and Defines chapter in the [System Reference Guide](#)
  - Software base types
  - Hardware register types
  - Compiler defines
  - Cypress API return codes
  - Interrupt types and macros
- Registers
  - The full PSoC 5 register map is covered in the [PSoC 5 Registers Technical Reference Manual](#)
  - Register Access chapter in the [System Reference Guide](#)
    - § CY_GET API routines
    - § CY_SET API routines
- System Functions chapter in the [System Reference Guide](#)
  - General API routines
  - CyDelay API routines
  - CyVd Voltage Detect API routines
- Power Management
  - Power Supply and Monitoring chapter in the [PSoC 5 Technical Reference Manual](#)
  - Low Power Modes chapter in the [PSoC 5 Technical Reference Manual](#)
  - Power Management chapter in the [System Reference Guide](#)
    - § CyPm API routines
- Watchdog Timer chapter in the [System Reference Guide](#)
  - CyWdt API routines
- Cache Management
  - Cache Controller chapter in the [PSoC 5 Technical Reference Manual](#)
  - Cache chapter in the [System Reference Guide](#)
    - § CyFlushCache() API routine