Design Project #4 – XOR Gate

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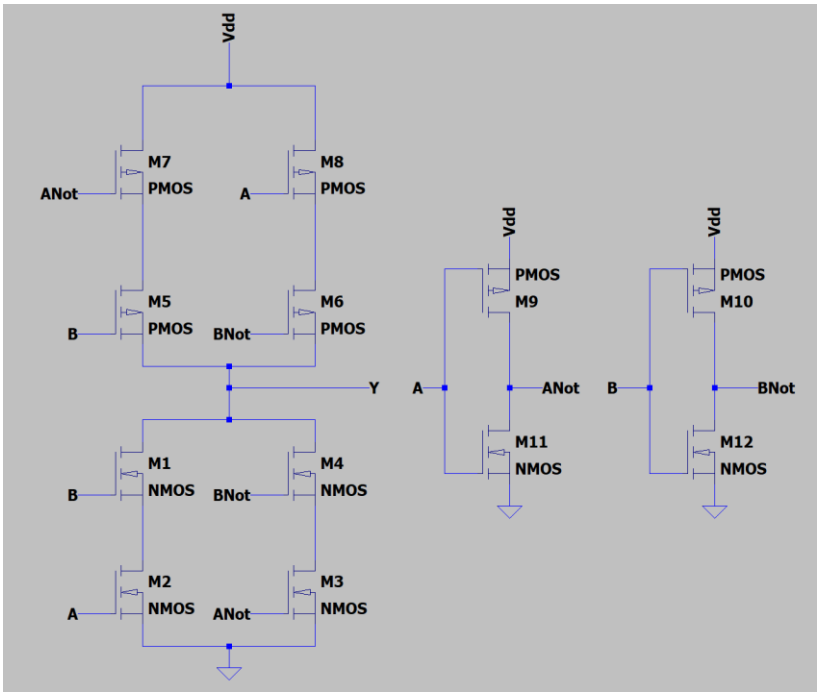
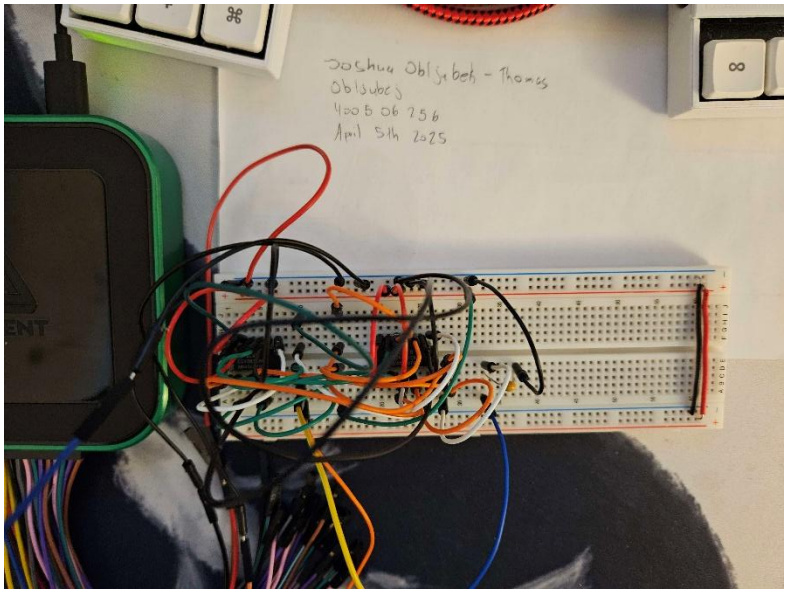
Circuit Schematic



Physical Implementation



Ideal Sizing

In a CMOS XOR gate, achieving symmetrical switching behavior is essential for maintaining signal integrity and minimizing delay. This is accomplished by adjusting the width-to-length (W/L) ratio of the transistors to equalize the resistance in the pull-up network (PUN) and pull-down network (PDN). PMOS transistors, which form the PUN, naturally exhibit higher resistance due to their lower carrier mobility compared to NMOS transistors in the PDN. To counterbalance this, PMOS devices must be sized wider.

In this design, both the PUN and PDN contain two transistors in series on the longest conduction path. As a result, the total resistance through each network scales with the number of series transistors, and the sizing must account for this. Assuming a typical PMOS to NMOS resistance ratio of 2.5:1 for balanced rise and fall times, and considering two devices per path, the overall ratio required becomes:

$$\frac{2 * W_{PMOS}}{2 * W_{NMOS}} = \frac{5}{2} = 2.5$$

This ensures that both high-to-low and low-to-high transitions occur with roughly the same delay. Therefore, the ideal sizing requires each PMOS transistor to have 2.5 times the width of an NMOS transistor to ensure timing symmetry and efficient operation.

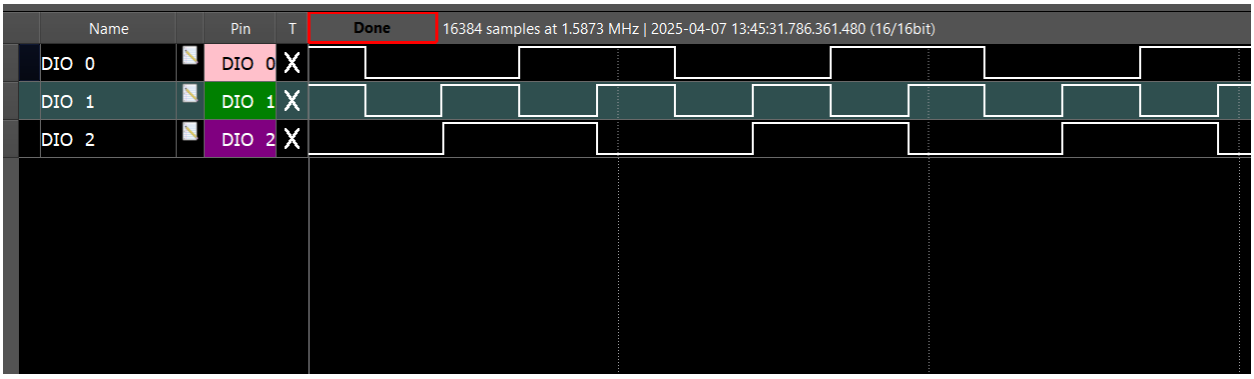
Explanation of Ideal Sizing

In practice, implementing this ideal sizing depends on the available components. For this project, the XOR gate was constructed using two MC14007 MOSFET arrays, each containing 3 PMOS and 3 NMOS devices. The devices in this chip are pre-packaged with fixed geometries, meaning the W/L ratios cannot be physically modified.

Due to this constraint, ideal transistor sizing could not be directly implemented in hardware. All transistors were used at their default sizes. As a result, the PMOS transistors could not be widened relative to the NMOS transistors. This imbalance typically causes slower rising edges (due to PMOS resistance) and faster falling edges (from NMOS), which affects timing consistency. This is reflected in the measured propagation delays from the timing tests, where TPLH and TPHL showed a noticeable difference.

Despite this, the circuit still functions correctly as an XOR gate, and the deviations in voltage levels and delay are within acceptable bounds for discrete implementation. The theoretical sizing remains useful for understanding performance trade-offs and would be critical for custom IC or VLSI design, where transistor dimensions can be adjusted freely.

Functional Digital Testing



To verify correct XOR behavior, the circuit was connected to the Analog Discovery 3's DIO pins, with inputs A and B driven using digital waveforms and the output observed using the logic analyzer. The XOR logic is defined by the equation:

$$V_{out} = A \oplus B = A\overline{B} + \overline{A}B$$

This expression ensures that the output is high (logic 1) only when exactly one input is high. The truth table was verified by toggling inputs through all four input combinations:

- A = 0, B = 0 → V_{out} = 0
- A = 0, B = 1 → V_{out} = 1
- A = 1, B = 0 → V_{out} = 1
- A = 1, B = 1 → V_{out} = 0

All transitions matched the expected XOR output, confirming functional correctness at the logic level.

Static Level testing

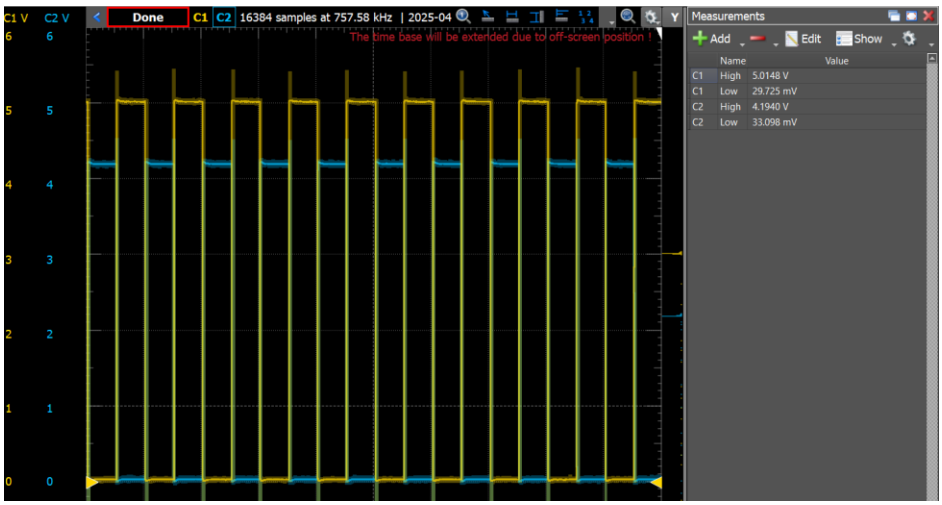


Figure 1: A input sinusoid, B input 5V

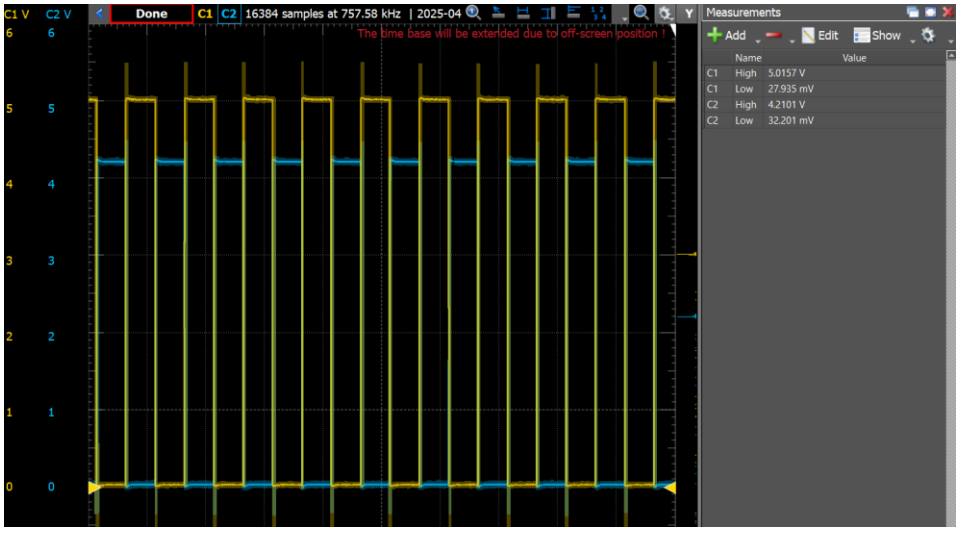


Figure 2: B input sinusoid, A input 5V

Test	Observations
A input is sinusoidal at 0-5V B input is 5V	$V_H = 4.1940V$ $V_L = 33.098$ mV
A input is 5V B input is sinusoidal at 0-5V	$V_H = 4.2101V$ $V_L = 27.935$ mV

Static level testing was performed by fixing one input at logic high (5V) while toggling the other with a square wave oscillating between 0 and 5V. This method isolates each input's effect and allows for accurate measurement of the output voltage levels (High and Low).

From the oscilloscope readings:

- V_H values were 4.1940V and 4.2101V, resulting in a percent difference of only 0.38%, indicating consistent high output levels
- V_L values were 33.098mV and 27.935mV, with a percent difference of 16.9%, which is large due to the small magnitudes involved. Minor deviations near 0V appear proportionally significant

These results indicate that the circuit is mostly symmetrical.

Timing

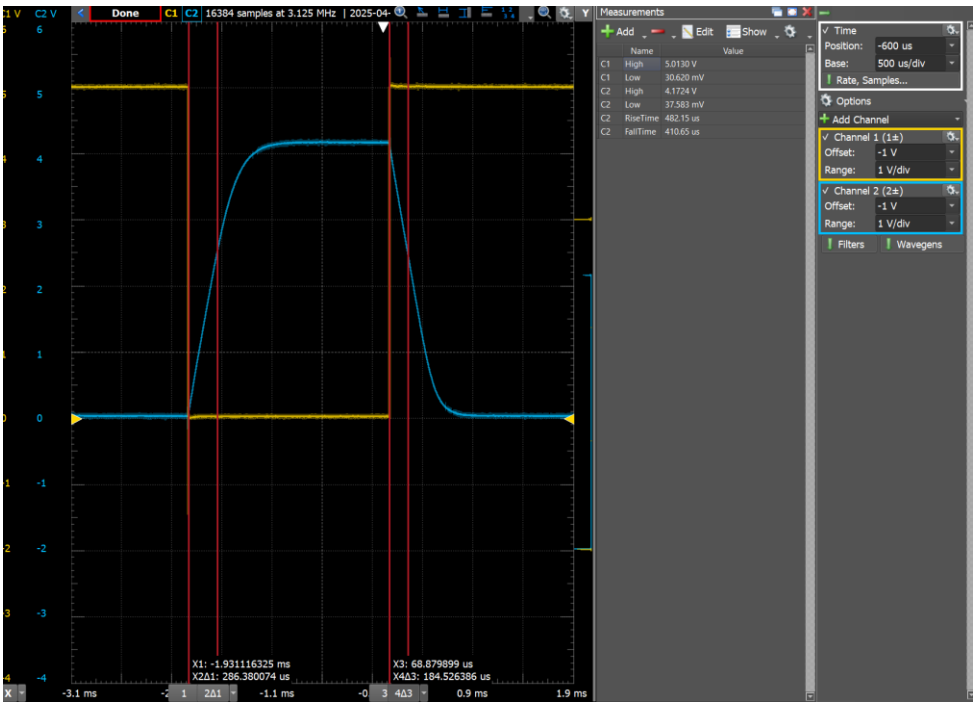


Figure 3: Circuit demonstrating the rise/fall times, TPLH, TPHL

To evaluate the dynamic performance of the XOR gate, one input was held at a constant 5V while the other was driven with a square wave (0–5V). A 100 nF capacitor was connected at the output to simulate a load, allowing for clearer observation of rise and fall transitions on the oscilloscope.

The key timing parameters measured were:

- T_{PLH} (propagation delay from low to high): 286us from graph
- T_{PLH} (propagation delay from low to high): 184us from graph
- T_P (Average propagation delay): $\frac{T_{PLH}+T_{PHL}}{2} = 235us$
- Rise Time = 482.15us
- Fall Time = 410.65us

The larger T_{PLH} compared to T_{PHL} is expected due to the mismatch in PMOS and NMOS sizing. Since PMOS transistors have higher resistance, the rising edge is slower. This imbalance confirms the impact of non-ideal sizing in hardware, as described earlier. Nonetheless, the gate transitions are clearly defined and consistent, demonstrating acceptable performance for discrete logic operation.

Bonus

Circuit Schematic

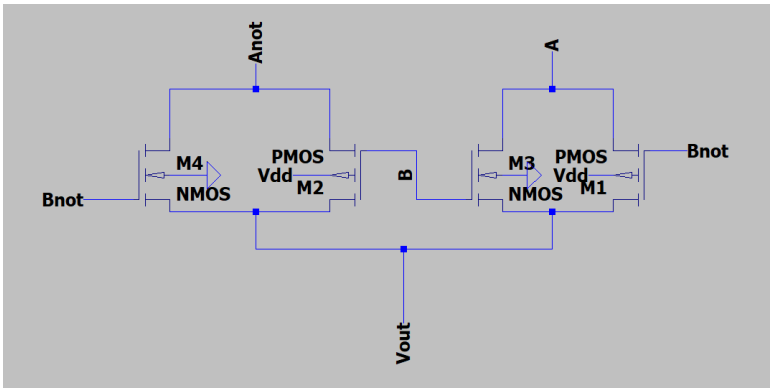


Figure 4: Circuit schematic for bonus

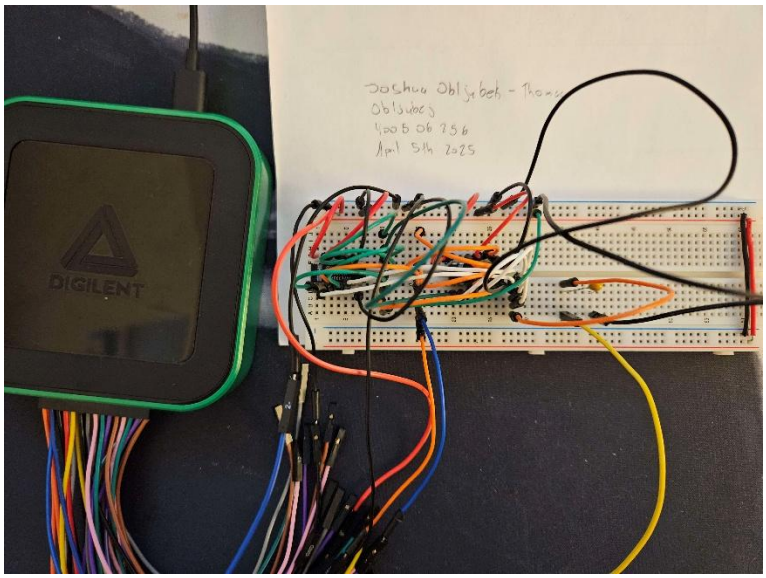


Figure 5: Physical Implementation

Functional Digital Testing

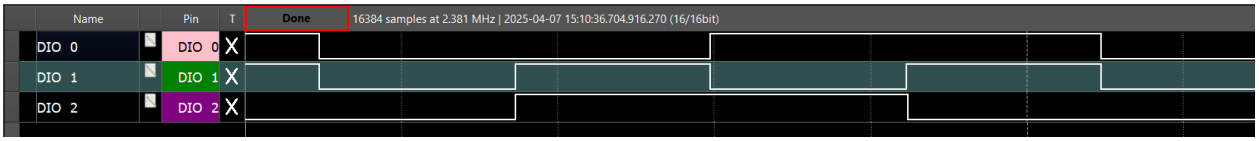


Figure 6: A --> DIO0, B --> DIO1, Vout --> DIO2

An XOR gate was also implemented using an alternative method based on pass transistor logic, which reduces the transistor count by using NMOS transistors to selectively pass logic levels based on control signals. The circuit schematic follows the structure:

$$V_{out} = A \oplus B = A\overline{B} + \overline{A}B$$

But rather than combining pull-up and pull-down networks like in the standard CMOS, this design uses NMOS pass gates to selectively transmit input values depending on the control signal states. This approach allows for a 8-transistor implementation.

Physically building the circuit on a breadboard and analyzing with the AD3 logic analyzer demonstrated identical results to the first part.

Static Level testing

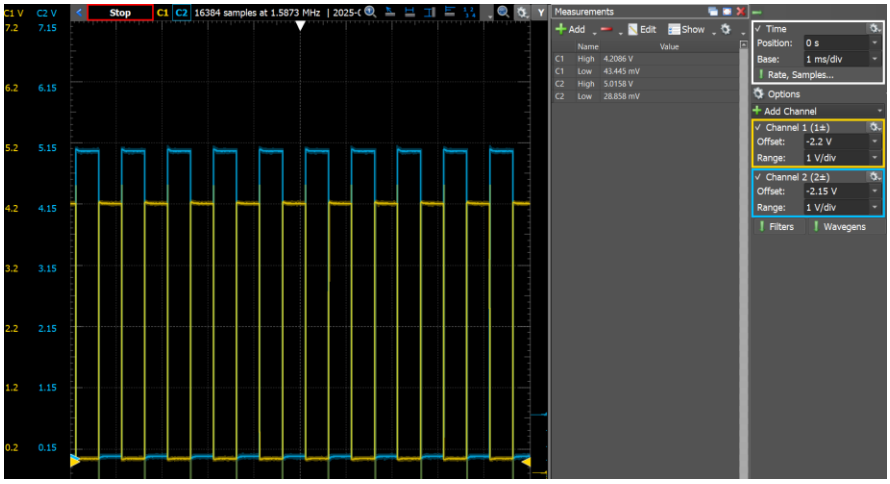


Figure 7: A input sinusoid, B input 5V

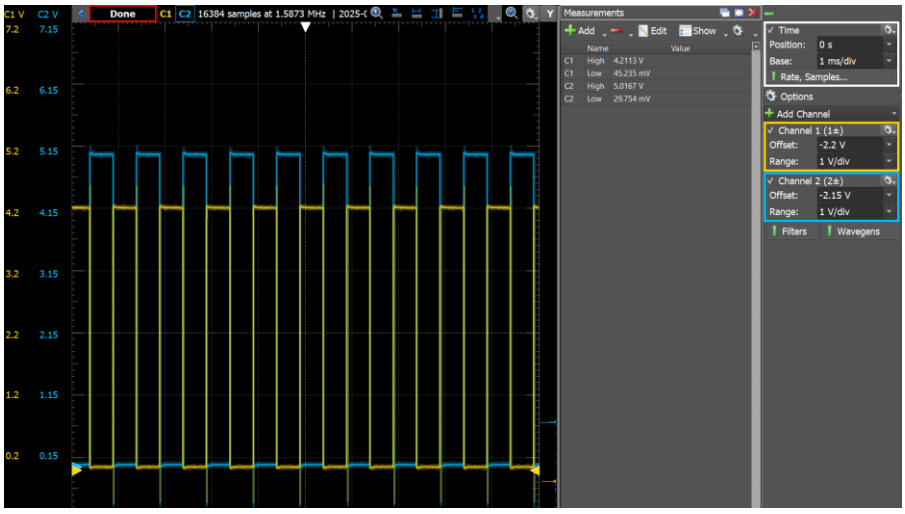


Figure 8: B input sinusoid, A input 5V

Test	Observations
A input is sinusoidal at 0-5V B input is 5V	$V_H = 4.2066V$ $V_L = 28.858$ mV
A input is 5V B input is sinusoidal at 0-5V	$V_H = 4.2113V$ $V_L = 29.754$ mV

Static level testing was performed by fixing one input at logic high (5V) while toggling the other with a square wave oscillating between 0 and 5V. This method isolates each input's effect and allows for accurate measurement of the output voltage levels (High and Low).

From the oscilloscope readings:

- V_H values were 4.2066V and 4.2113V, resulting in a percent difference of only 0.11%, indicating consistent high output levels
- V_L values were 28.858mV and 29.754mV, with a percent difference of 3.06%, which is larger due to the small magnitudes involved. Minor deviations near 0V appear proportionally significant

These results indicate that the circuit is mostly symmetrical.

Timing

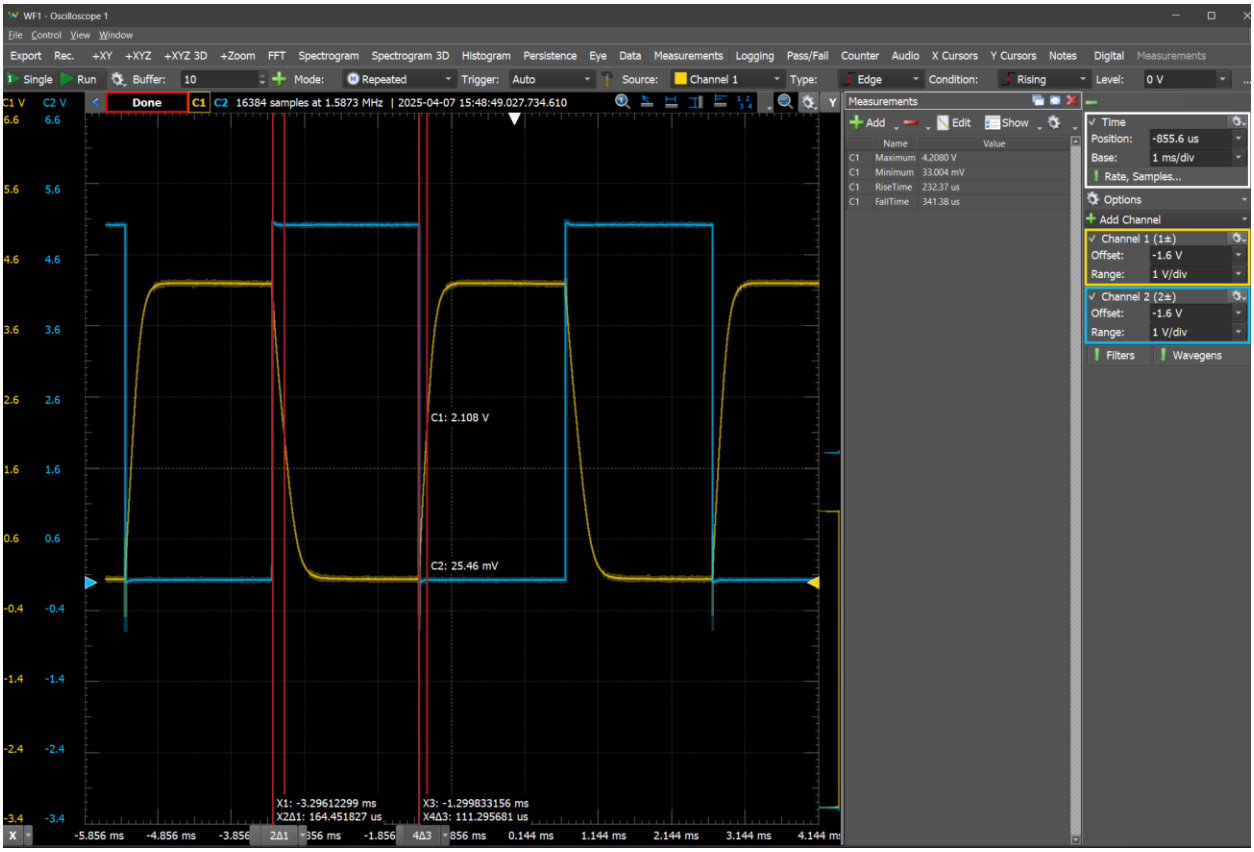


Figure 9: Circuit demonstrating the rise/fall times, TPLH, TPHL

Timing measurements were repeated with a 100nF capacitor on the output:

- Rise time: 232.37us
- Fall time: 341.38us
- T_{PLH}: 111.29us
- T_{PHL}: 164.45us
- T_P = 137.5us

Compared to the CMOS implementation (235 µs), the pass-transistor XOR showed significantly faster switching performance. However, it may suffer from threshold voltage drop issues when passing a full logic high through NMOS-only paths, which wasn't a major issue in this case due to the strong 5V input levels used.