Design Project #2 – Voltage Controlled Switch

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Ideal Switches

Switches are vital in the analysis of electrical and computer engineering. In transient and steady state analysis with capacitors and inductors, physical switches were used to trigger transient behavior. This report implements two distinct voltage controlled switches for faster and more precise switching behavior. The first switch is a simple switch with two terminals V1, and V2, and a control terminal causing for an open or short circuit. The second switch acts as a multiplexer with terminals V1, Va, Vb, and control.

Several idealities of an ideal switch include:

- The ability for the switch to open completely. This means the switch should be able to have an infinite resistance when open and there is no current from VA → VB.
- The ability for the switch to close completely. This means that the switch should have no resistance or current flow and VA = VB.
- The switch should be bidirectional. With the circuits we have been using in RC/RL circuit analysis, there are many times when the current reverses across the switch.
- The switch should work for any inputs and loads from V1 and V2.

Qualitative descriptions of non-idealities

- When a switch is fully open, it should ideally behave like an open circuit with infinite resistance across the terminals. However, using MOSFETS to make the switch will always result in some current leakage since they are not ideal.
- When a switch is fully closed, it should ideally behave like an open circuit with no resistance across the terminals. However, in practice, any circuit design, even a wire has some associated resistance and voltage drop.
- While the switch should be fully bidirectional. This ideality is not possible due to the asymmetrical nature of MOSFET devices. Even having two in parallel with each other to account for both directional cases, an inverted signal is required leading to even more non-idealities.
- Any switch using MOSFET devices cannot work for any inputs of V1 and V2 since they will reach saturation and cutoff regions.

Quantitative descriptions of non-idealities

- Ron measures the non-ideality when the switch is ON
- Ioff measures the non-ideality when the switch is OFF
- A percent difference calculation for the resistance between forwards and backwards direction is used to quantitatively analyze the bidirectionality of the circuit
- Maximum and minimum values for V1 and V2 measure the voltage range of the circuit.

Test Plan

Switch Type 1	Switch Type 2
To measure Ron and Ioff we can use a test voltage at V1 of 3V DC and a load resistor of 200K ohms at V2 to measure the voltage drop across the resistor and switch. Using ohms law, we are able to calculate the current across the resistor and then the resistance of the switch. To measure the range of V1 and V2, a timed DC sweep with values ranging form 0V to +5V and a load resistor of 200KΩ, we are able to observe the range of values the switch is able to operate in. To measure the bidirectionality of the switch resistance, test 1 will be performed a second time but with the two terminals flipped. The percent difference is then calculated to quantitatively analyze the bidirectionality of the switch.	The same three tests can be applied to switch two as well, with slightly modified implementations. For the first test of 3V DC at V1, we will add a load resistance of 200KΩ at Va and Vb. This allows us to calculate the current across both resistors, then the on resistance current of the switch in both cases. To measure the range of V1, Va, and Vb, a timed DC sweep at V1 from 0V to +5V can be implemented with a load resistance of 200k at both Va and Vb can be used to observe the range of values the switch is able to operate in. To measure the bidirectionality of the switch in both V1-Va and V1-Vb, test 1 will be performed a second time but with the inputs flipped. Meaning there will be two DC voltage inputs of 3V DC at Va and Vb and a load resistor of 200kΩ at V1. This then allows us to calculate the percent difference between the forwards and backwards direction resistances.

Switch Type 1

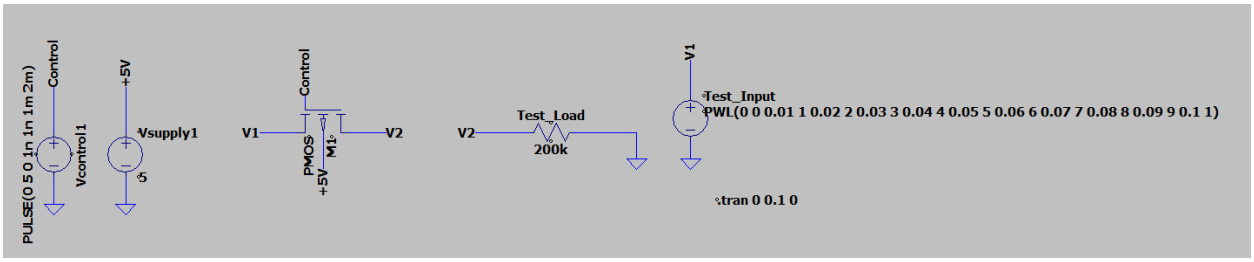

Figure 1 Circuit Schematic of the Design

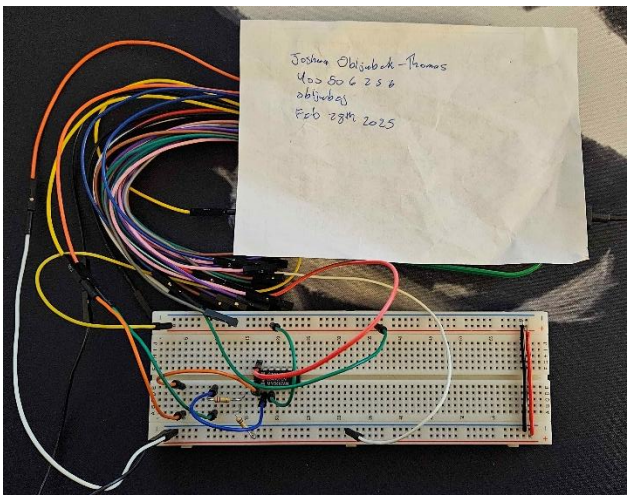

Figure 2 Physical Implementation

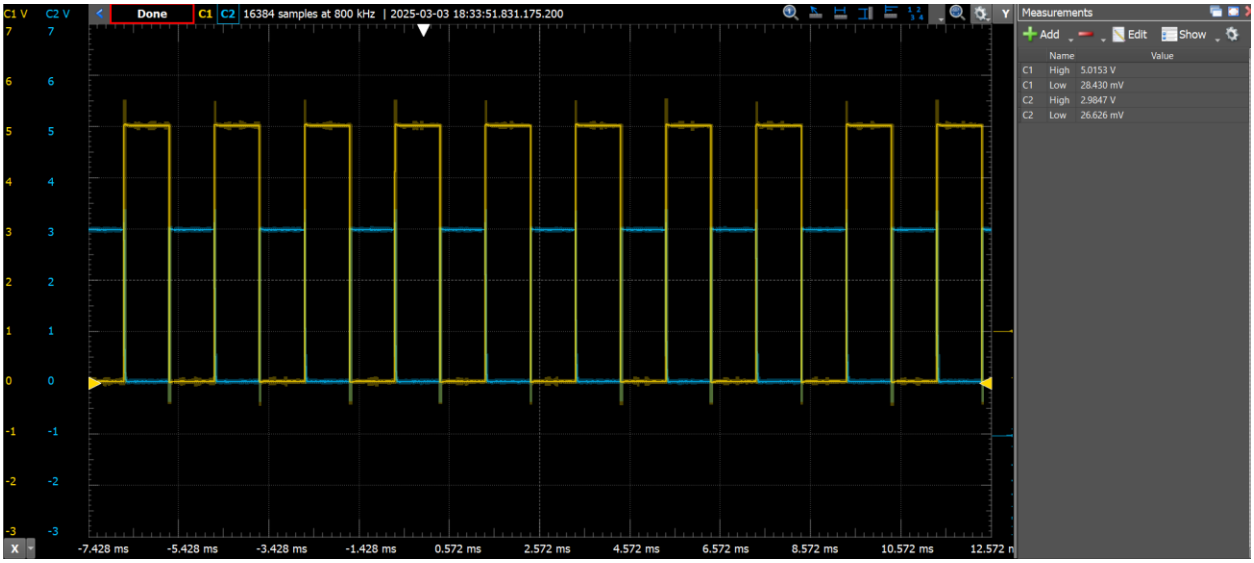

Figure 3 Input of 3V and load of 200k in Forward Direction

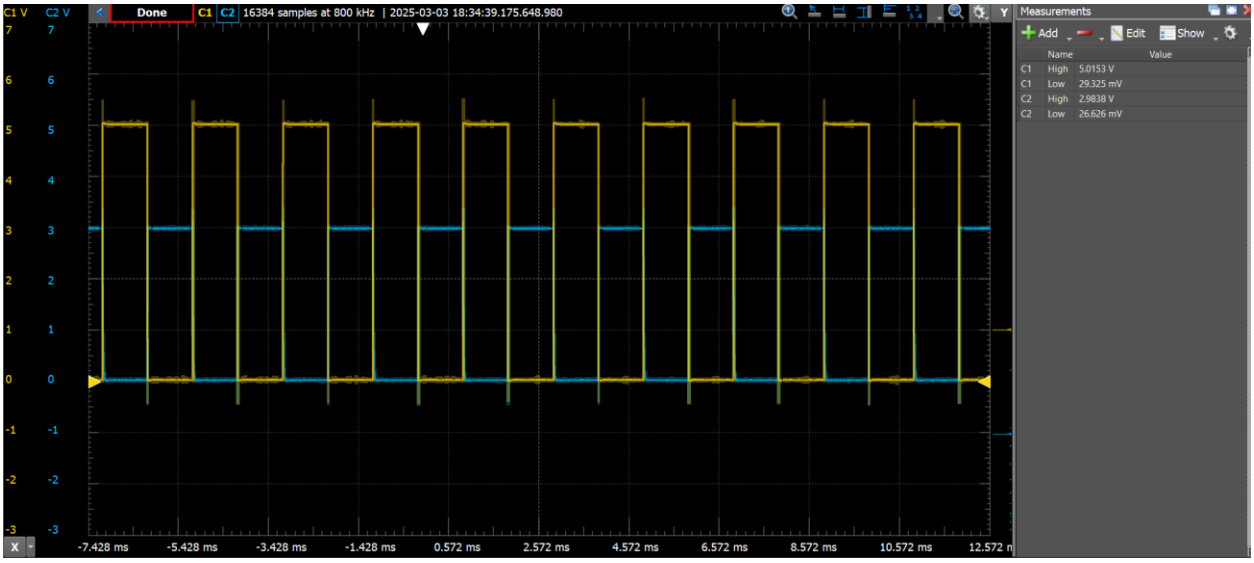

Figure 4 Input of 3V and load of 200k in Reverse Direction

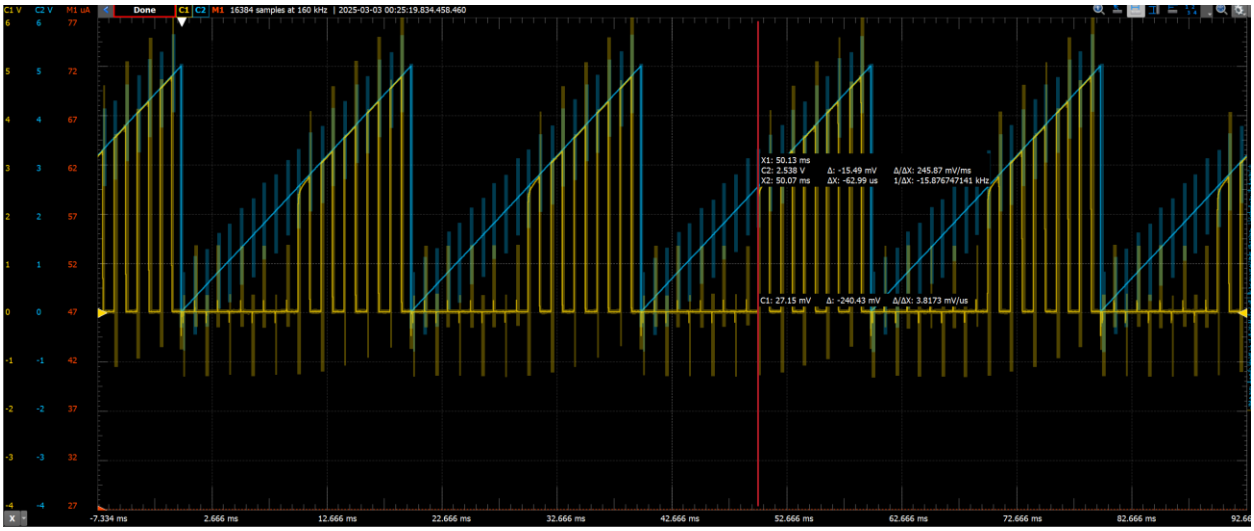

Figure 5 Timed DC Sweep Input from 0-5V

Test Results

Non-Ideality	Measurement	Value
R_{on} forwards	V_R = 2.9847V V_{switch} = 0.0153V	$R_{switch} = \frac{200000*V_{switch}}{V_R}$ R_{switch} = 1025.22 Ω
R_{on} backwards	V_R = 2.9856V V_{switch} = 0.0144V	$R_{switch} = \frac{200000*V_{switch}}{V_R}$ R_{switch} = 964.63 Ω
I_{off} forwards	V_{Roff} = 26.626mV	$I_{off F} = \frac{V_R}{200000}$ $I_{off F}$ = 13.3uA
I_{off} backwards	V_R = 26.626mV	$I_{off F} = \frac{V_R}{200000}$ $I_{off F}$ = 13.3uA
Bidirectionality		$p = \frac{\lvert R_{forward}-R_{backward}\rvert}{\lvert R_{forward}+R_{backward}\rvert/2} * 100\%$ p = 6.09%
Minimum and Maximum voltages	V_{max} = 4.98V V_{min} = 2.538V	V_{max} = 4.98V V_{min} = 2.538V

Results Comparison

Switch type 1 is designed to have two terminals, V1 and V2, a control voltage that connects the two terminals when it is set to 0V, and a supply voltage of 5V. Testing the circuit in Figure 1 based on the testing plan allowed for the quantification of the non-idealities of switch type 1.

The first for the circuit had V1 as a 3V DC input supply and a V2 as a load resistor of 200KΩ. This resulted in an on-state resistance of approximately 1025Ω, meaning that during the on state the switch will behave as a 1025Ω resistor rather than a wire. Ideally, this resistance would be 0Ω, however this is not possible in practice due to the characteristics of a PMOS transistor.

With the same test of a 3V DC input supply and load resistor of 200KΩ, the off current is found to be 13.3uA. In an ideal case, the circuit would behave as an open circuit and I_{off} would be 0. However, this is again not possible in practice due to the real-world characteristics of a PMOS transistor.

Repeating the same first test but in the reverse direction resulted in an on resistance of 964.63Ω and an off current of 13.3uA, leading to a percent resistance difference of 6.09%. In an ideal case, this value would be 0%, but as the design used a single MOSFET, bidirectional behavior is limited by asymmetry in the MOSFET construction.

Finally, a timed DC sweep of V1 with a load resistance of 200k proved that the operating input voltage range is from 2.538V to 4.98V. In an ideal case, this would have infinite range, however due to the construction of the PMOS, an input voltage lower than 2.538V results in cutoff and a voltage higher than 4.98V results in saturation.

Design Trade-offs

Several trade-offs were made in the design of this circuit. This design uses a singular MOSFET leading to a much lower cost-per-unit and a much simpler complexity. However, some trade offs of the circuit include limited bidirectionality. While still very good at 6% difference, using a single PMOS limits bidirectional behavior due to asymmetry in the MOSFET construction. Another possible solution for this circuit is to use two PMOS transistors and an NMOS transistor. The NMOS transistor and a pull-down resistor would act as the inverted input to the second PMOS transistor. This results in a perfect bidirectional design. However, this also leads to much higher complexity and cost-per-unit implementation. Overall, the chosen design prioritizes lower cost-per-unit and simplicity while making some compromises.

Switch Type 2

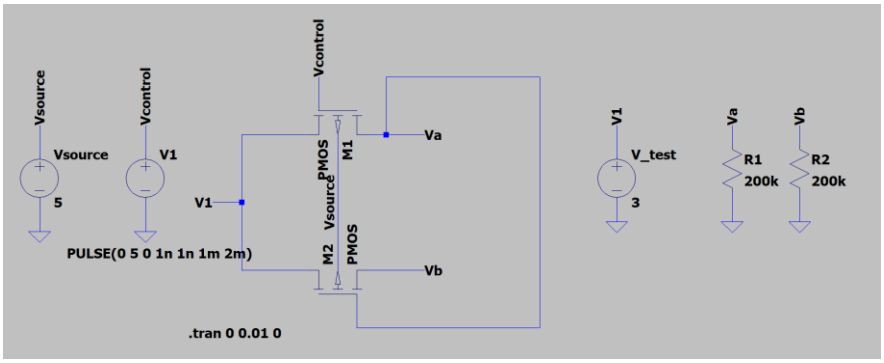

Figure 6 Circuit Schematic of the Design

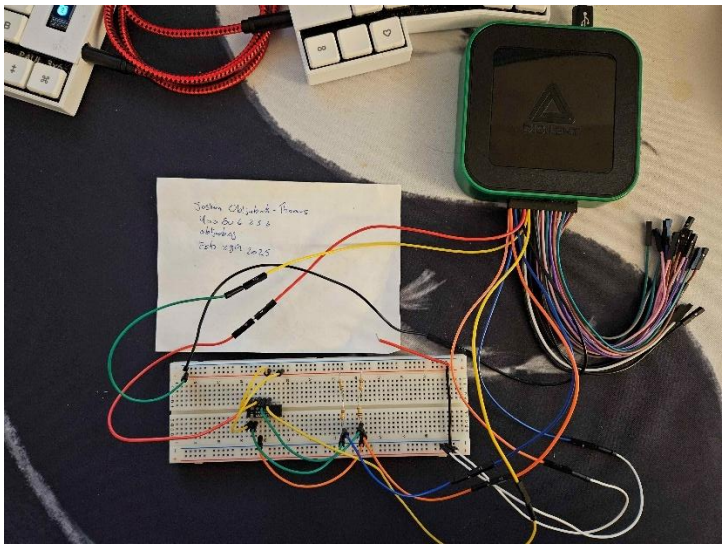

Figure 7 Physical Implementation

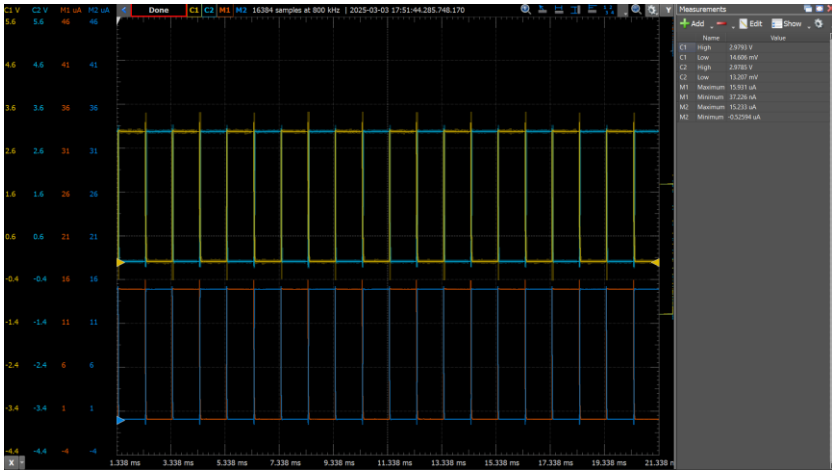

Figure 8 3V Input at V1 and Load of 200K at Va and Vb forwards direction

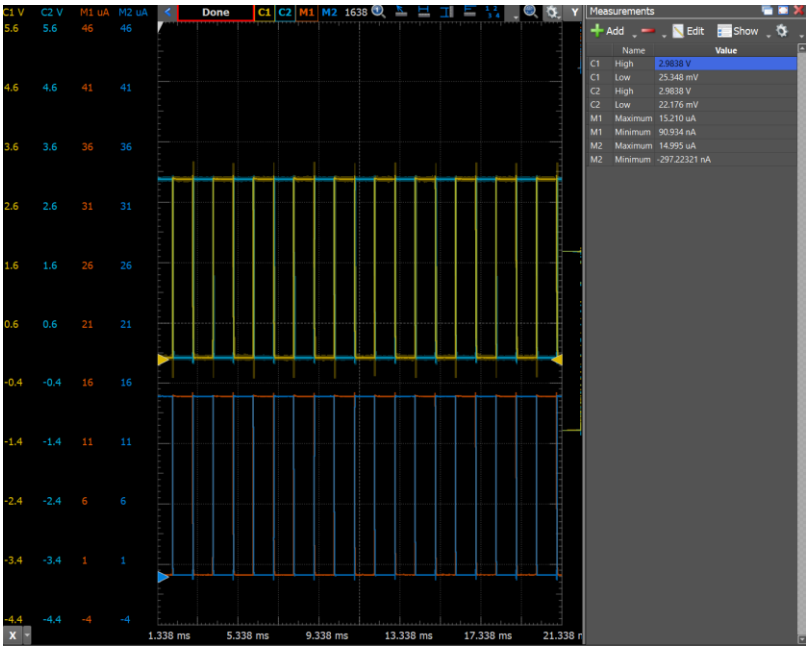

Figure 9 Input at V1 and Load of 200K at Va and Vb backwards direction

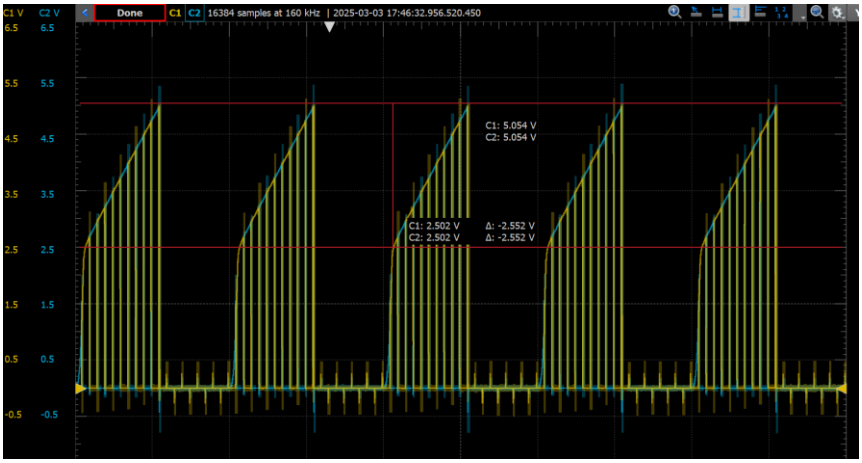

Figure 10 Timed DC sweep from 0-5V

Test Results

Non Ideality	Measurements	Value
Ron Forwards (A)	V_R = 2.9793V V_{Switch} = 0.0207V	$R_{switch} = \frac{200000*V_{switch}}{V_R}$ R_{switch} = 1392.53Ω
Ron Backwards (A)	V_R = 2.9838V V_{Switch} = 0.0162 V	$R_{switch} = \frac{200000*V_{switch}}{V_R}$ R_{switch} = 1085.86 Ω
Ron Forwards (B)	V_R = 2.9785V V_{Switch} = 0.0215V	$R_{switch} = \frac{200000*V_{switch}}{V_R}$ R_{switch} = 1443.67Ω
Ron Backwards (B)	V_R = 2.9838V V_{Switch} = 0.0162 V	$R_{switch} = \frac{200000*V_{switch}}{V_R}$ R_{switch} = 1085.86 Ω
Ioff Forwards (A) Ioff Backwards (A)	Math function on graph	$I_{off F}$ = 37.226nA $I_{off B}$ = 90.934nA
Ioff Forwards (B) Ioff Backwards (B)	Math function on graph	$I_{off F}$ = 0.052594uA $I_{off B}$ = -297.22 uA
Bidirectionality (A)		$p = \frac{\lvert R_{forward} - R_{backward} \rvert}{\lvert R_{forward} + R_{backward} \rvert / 2} * 100\%$ p = 24.7%
Bidirectionality (B)		$p = \frac{\lvert R_{forward} - R_{backward} \rvert}{\lvert R_{forward} + R_{backward} \rvert / 2} * 100\%$ p = 28.2%
Minimum and Maximum voltages	V_{max} = 5.054V V_{min} = 2.502V	V_{max} = 5.054V V_{min} = 2.502V

Results Comparison

Switch type 2 is designed to have three terminals, V1, Va, and Vb, a control voltage that acts as a multiplexer between V1 and Va/Vb, and a supply voltage of 5V. Testing the circuit in Figure 6 based on the testing plan allowed for the quantification of the non-idealities of switch type 2.

The first for the circuit had V1 as a 3V DC input supply and a V2 as a load resistor of 200KΩ. This resulted in an on-state resistance of approximately 1085.65Ω for V1-Va, meaning that during the on state the switch will behave as a 1085.65Ω resistor rather than a wire. This also resulted in an on-state resistance of approximately 1443.67Ω for V1-Vb, meaning that during the on state, the switch will behave as a 1443.65Ω resistor rather than a wire. Ideally, both resistances would be 0Ω, however this is not possible in practice due to the characteristics of a PMOS transistor. It should also be noted that the

resistance from V1-Vb seems to be higher than the resistance from V1-Va. This is caused by the varying gate of the second PMOS transistor.

With the same test of a 3V DC input supply and load resistor of 200KΩ, the off current is found to be 37.226nA for V1-Va and 0.052594uA from V1-Vb. In an ideal case, the circuit would behave as an open circuit and I_{off} would be 0. However, this is again not possible in practice due to the real-world characteristics of a PMOS transistor.

Repeating the same first test but in the reverse direction resulted in an on resistance of 1085.86 Ω and an off current of 90.934nA for V1-Va, leading to a percent resistance difference of 24.7% from V1-Va. Additionally, the resistance form V1-Vb in the reverse direction is measured to be 1085.86Ω with a current of 297.22 uA leading to a percent resistance difference of 28.2% from V1-Vb. In an ideal case, this value would be 0% for both V1-Va and V1-Vb, however, due to the implementation of a feedback wire to the gate of the second PMOS transistor, the circuit has poor bidirectional symmetry.

Finally, a timed DC sweep of V1 with a load resistance of 200k proved that the operating input voltage range is from 2.502V to 5.054V for both V1-Va and V1-Vb. In an ideal case, this would have infinite range, however due to the construction of the PMOS, an input voltage lower than 2.502V results in cutoff and a voltage higher than 5.054V results in saturation.

Design Trade Offs

The chosen solution prioritizes a low cost-per-unit construction and a simpler design since it only uses two PMOS transistors. This allows for the switch to implement most of the idealities of a low Ron, low Ioff, and a wide range of minimum and maximum voltages. However, due to the limited number of MOSFET's and the feedback wire to the gate of the second, it does not demonstrate good bidirectional behavior. Using more MOSFETS, with similar implementation as explain in circuit type 1 would result in much better bidirectionality. However, this would lead to a much higher cost-per-unit and a more complex design. Furthermore, another implementation could use both a PMOS and an NMOS architecture to allow for bidirectionality. While in theory this sounds perfect, through testing it is found that the NMOS had much more restrictions and the inconsistency in the outputs.