Design Project #5 – ADC

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Summary

This project focused on creating a 3-bit DAC using a binary-weighted resistor network and two inverting op-amps. The circuit converts 3-bit digital inputs into proportional analog voltages with a full-scale range of 5 V. After testing, the DAC showed accurate performance with low gain error, minimal offset, and consistent step sizes, confirming the design worked as intended.

Design

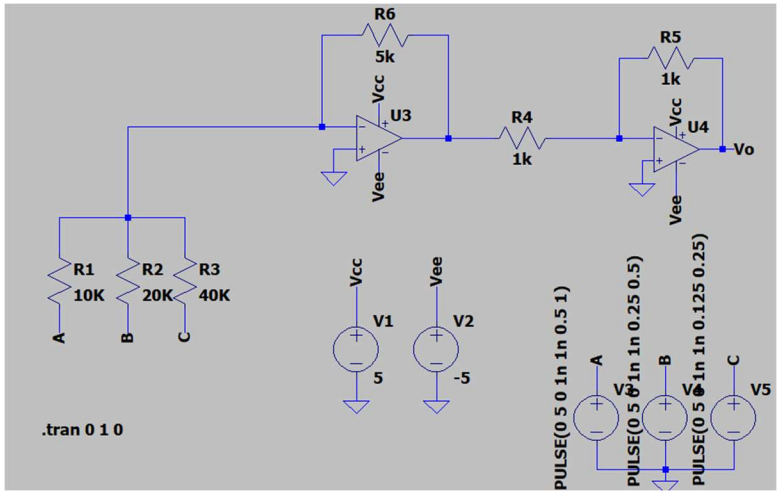

Figure 1: Circuit Schematic

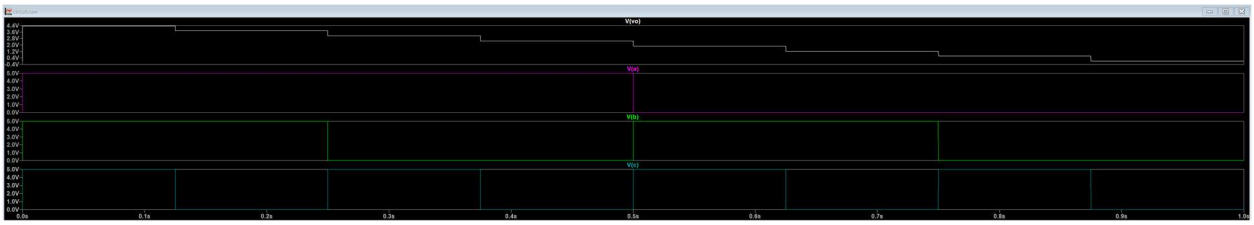

Figure 2: Simulation Testing

This DAC implementation uses a pair of inverting op-amps to build a 3-bit binary-weighted converter. The digital inputs accept values of either 0 volts or 5 volts and are connected through resistors with values chosen in a 1:2:4 ratio for proper binary weighting. Specifically, the resistors used are 10k, 20k, and 40k, connected from each input bit to a common node at the inverting terminal of the first op-amp. This configuration allows each bit to contribute a proportional current, which the op-amp sums and converts into a voltage based on the feedback resistance, set at 5k in the circuit. Since this stage inverts the signal, a second inverting op-amp is added as a unity gain buffer to correct the polarity and isolate the output from the rest of the system.

The circuit implements a 3-bit binary-weighted DAC using an op-amp summing configuration. Each bit input is associated with a resistor chosen in a binary-weighted ratio of 1:2:4 (10kΩ, 20kΩ, 40kΩ), allowing the current contribution from each input to reflect its binary weight. The inverting op-amp stage (U3) sums these currents at its inverting input and converts them into a voltage using the feedback resistor R_f=5kΩ. The output of this stage follows the equation:

$$V_{o1} = -R_F * (\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3})$$

Substituting the resistor values and logic voltages (0 V or 5 V), this formula was used to calculate the expected output for each of the 8 digital input combinations. Since the first op-amp inverts the signal, a second inverting op-amp (U4) with equal input and feedback resistors (1kΩ) is used to restore a non-inverted output. The final output voltage is thus positive and proportional to the binary input, scaled according to the resistor ratios and supply voltage.

The design of this circuit is heavily inspired from the “4-bit DAC using op-amp” circuit from “circuitfever.com” [1]. Their circuit is effectively demonstrates the functionality of U3 in the circuit I designed, and expresses the analog values as a negative number.

Measurement and analysis

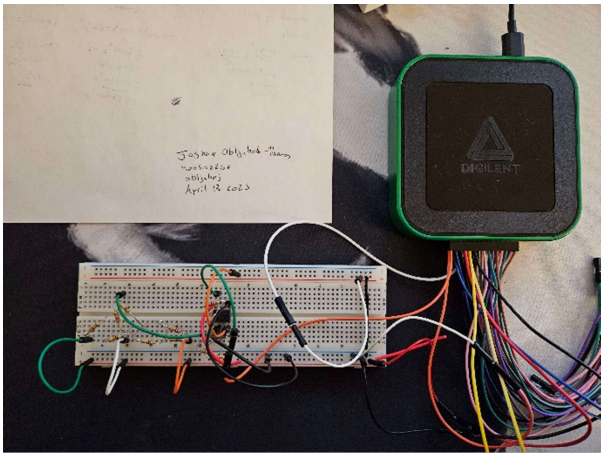

Figure 3: Image of physical implementation

Testing this circuit, it would have been ideal to use either the wavegen or the digital I/O pins on the ad3. Unfortunately there are only two channels for the wavegen and the digital I/O pins can only output +3.3V, not our circuits logical high of +5V. To test this, the inputs were connected with wires to either the +5V power supply or the GND terminal. Following is a few examples of the circuit working with inputs of 000 corresponding to 0V, 010 corresponding to 1.25V, 110 corresponding to 3.75V, and 111 corresponding to 4.375V.

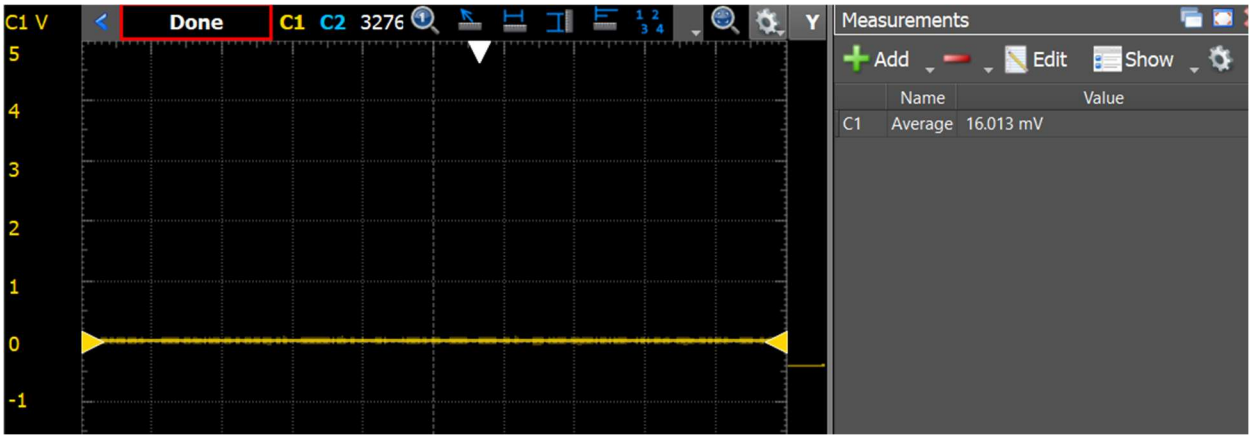

Figure 4: Input of 000

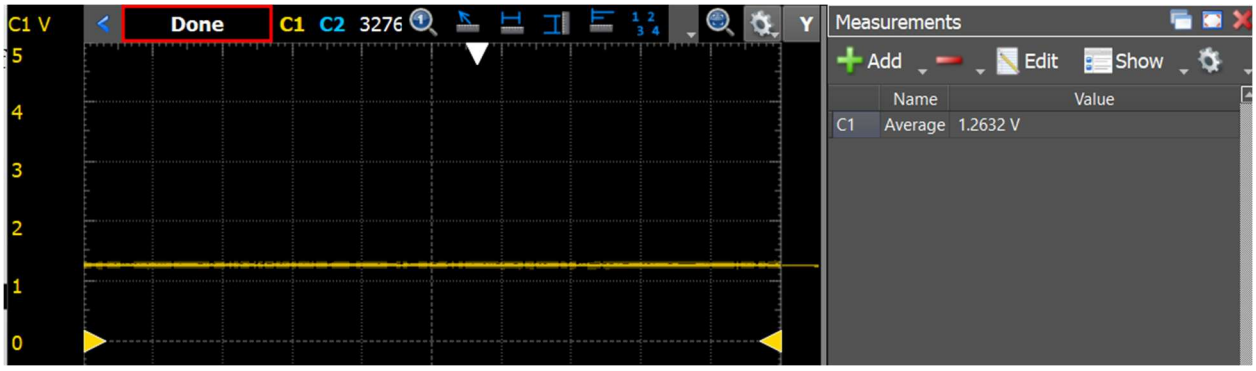

Figure 5: Input of 010

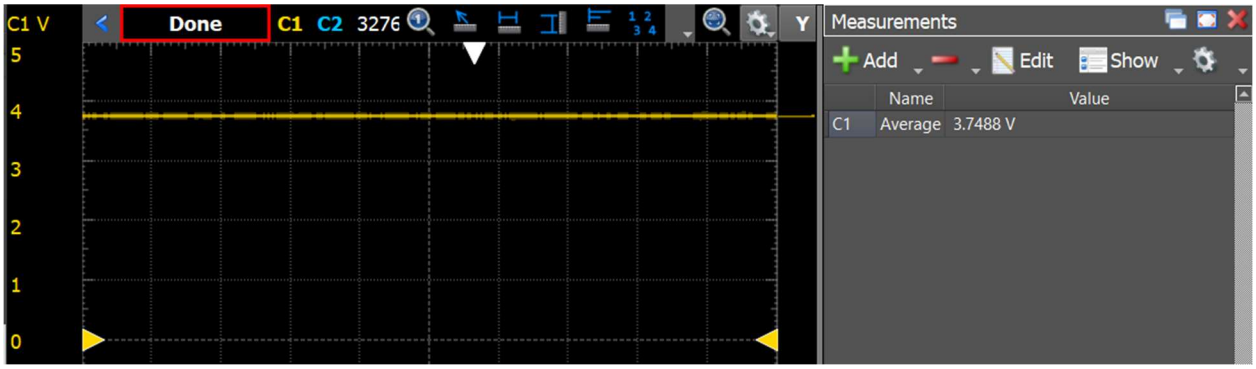

Figure 6: Input of 110

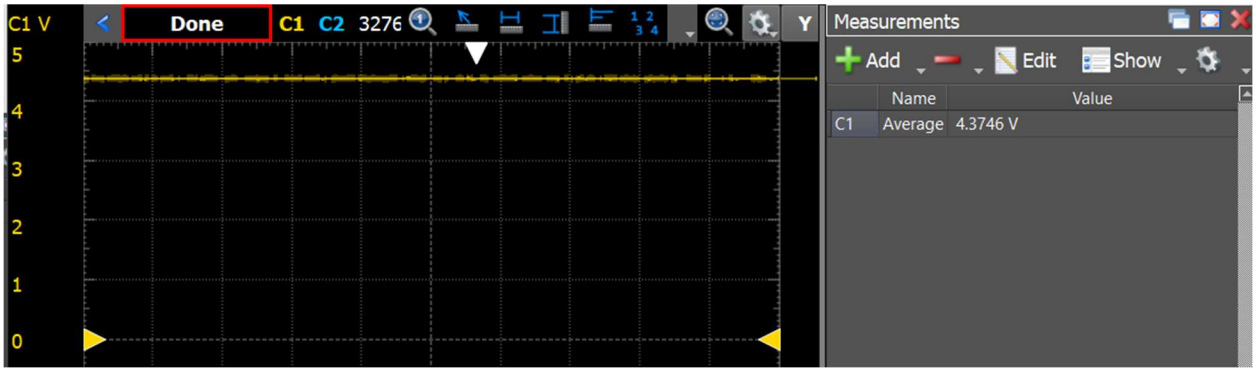

Figure 7: Input of 111

Gain Error

Gain error quantifies the deviation in the slope of the actual DAC output from the ideal transfer function. It reflects how closely the DAC output scales with the digital input, and is typically measured by comparing the actual output at or near full-scale input against the ideal output. In our case, an input of 111 (binary for 7) corresponds to the full-scale range. The ideal output for this input, assuming a full-scale voltage V_{FS} = 5V, is:

$$\frac{7}{8}5V = 4.375$$

However, the measured output was 4.3746V. The gain error is calculated as:

$$Gain\ Error = \frac{4.3746V - 4.375V}{5V} = -0.01\%$$

This small negative gain error indicates the DAC output is slightly compressed relative to the ideal, possibly due to resistor tolerance or loading effects in the circuit.

Maximum DNL

Differential non-linearity (DNL) measures the deviation between the actual step size and the ideal step size of a DAC. Ideally, each increment in the digital input should result in a uniform voltage increase. DNL is used to detect missing codes or non-uniform transitions, which can cause distortion in analog output.

To measure the maximum DNL, we compared the largest actual voltage step between two consecutive digital codes to the ideal step size. For a 3-bit DAC with a full-scale output of 5V, the ideal step size is:

$$\frac{5V}{8} = 0.625V$$

The largest measured step was 0.6254V, leading to a DNL of:

$$DNL = \frac{0.6254 - 0.625}{0.625} = 0.064\%$$

This low DNL value suggests that the DAC produces consistently spaced outputs with minimal deviation, and no missing codes were observed.

Offset Error

Offset error refers to the output voltage of the DAC when the input code is zero. Ideally, the output for a digital input of 000 should be exactly 0 volts. Any deviation from zero at this input level indicates an offset error, which can result from factors such as resistor mismatches, op-amp input bias currents, or small leakage currents in the circuit.

For this DAC, the output measured at input 000 was 16.013 mV. This small positive offset means that even when the digital input is at its minimum, the output does not reach ground. Although this offset is relatively minor, it effectively shifts the entire output range and can impact accuracy in precision applications. As a percentage of the full-scale voltage of 5 volts, the offset error is:

$$Offset\ Error = \frac{16.013mV}{5V} = 0.32\%$$

This result indicates that the circuit performs well, but improvements could be made by using more precise components or incorporating offset correction techniques.

Discussion

The small gain, offset, and differential non-linearity errors observed in this DAC can be mainly attributed to resistor tolerances and slight imperfections in the op-amps. The use of 5% tolerance resistors introduces minor mismatches in the weighted current contributions, which can slightly shift output levels and cause small deviations from ideal step sizes. The op-amps themselves may also introduce offset voltages or bias currents that influence the final output, especially near zero input where the offset error was most visible.

Despite these non-idealities, the errors were all within acceptable limits. The gain error was nearly zero, the offset error was around 16 mV, and the maximum DNL was only 0.064%, indicating no missing codes or major linearity issues. Overall, the circuit performed reliably under the given constraints and produced the expected 3-bit DAC behavior. If higher accuracy were needed, resistor matching could be improved by selecting tighter tolerance components or using a laser-trimmed resistor network. Additionally, offset trimming techniques or more precise op-amps could further reduce the error margins.

Through my research, I also found an R to 2R DAC implementation, which uses a repeating ladder of only two resistor values, R and 2R, to generate the analog output [2]. This approach simplifies resistor matching, improves accuracy in higher bit designs, and is often preferred for its scalability and ease of layout. However, for a simple 3 bit DAC, the binary weighted design was easier to implement using the available components in the lab kit and required fewer connections, making it a more practical choice for this project.

References

[1] “4-bit DAC using op-amp,” 4 bit DAC using op-amp - Circuit Fever, https://circuitfever.com/4-bit-dac-using-op-amp (accessed Apr. 13, 2025).

[2] W. Storr, “R-2R digital-to-analogue converter (R-2R DAC),” Basic Electronics Tutorials, https://www.electronics-tutorials.ws/combination/r-2r-dac.html (accessed Apr. 13, 2025).