ElecEng 2CF4
Assignment 1 Report 2

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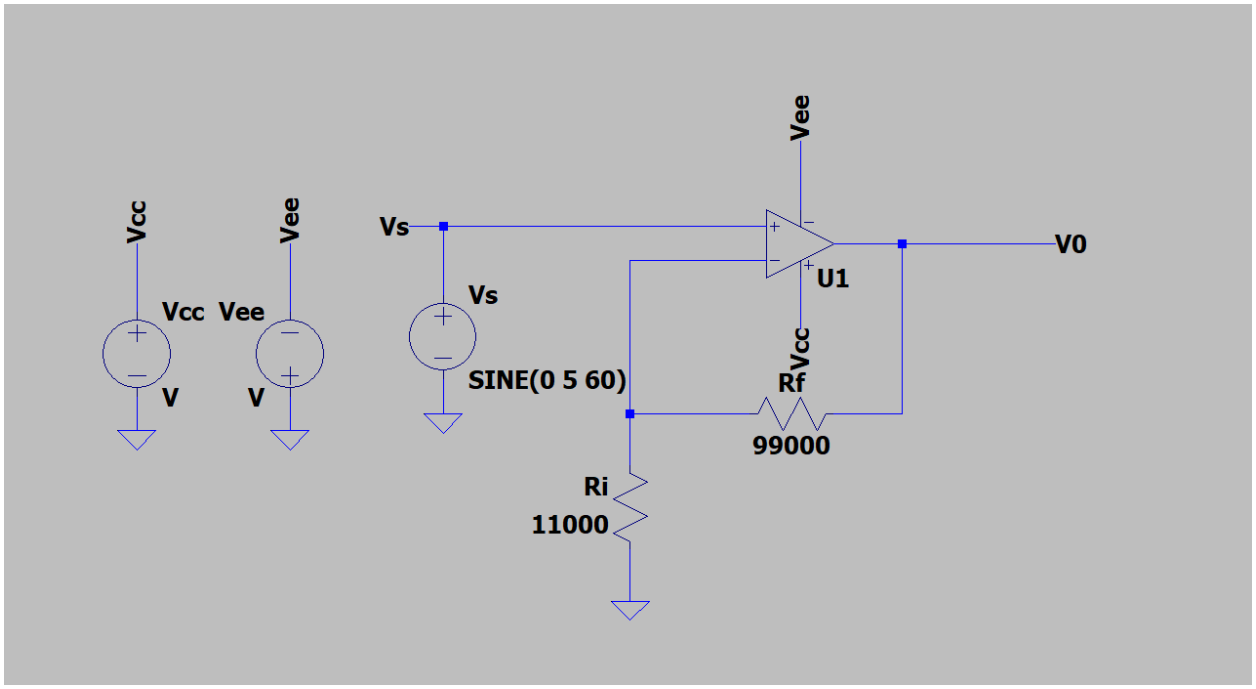
2.A.

1. **Image of Schematic**

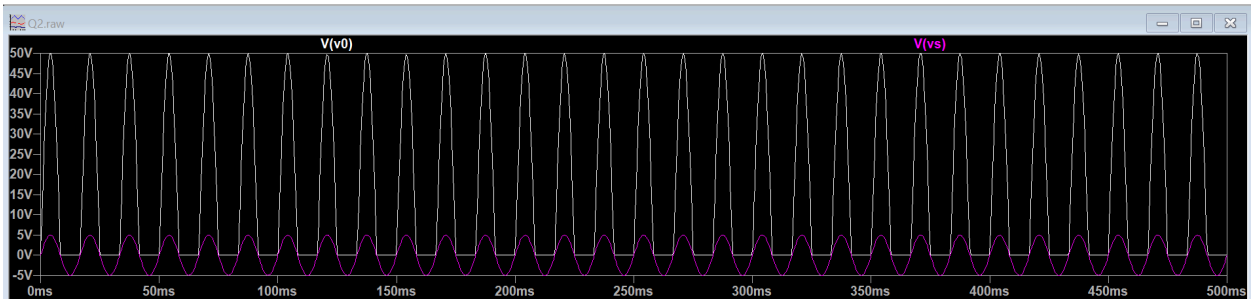


2. **Spice Netlist**

```
* C:\Users\Josh\Documents\COMPENG\Y2S2\2CF3\Asignment1\Q2.asc
Rf V0 N001 99000
Ri 0 N001 11000
X§U1 Vs N001 Vcc Vee V0 level2 Avol=1Meg GBW=10Meg Slew=10Meg Ilimit=25m Rail=0
Vos=0 En=0 Enk=0 In=0 Ink=0 Rin=500Meg
Vcc Vcc 0 V
Vee 0 Vee V
Vs Vs 0 SINE(0 5 60)
.lib UniversalOpAmp2.lib
.backanno
.end
```

2.B.

1. **Plot of Vo and Vs as a function of time**



2. **Spice Netlist**

```
* C:\Users\Josh\Documents\COMPENG\Y2S2\2CF3\Asignment1\Q2.asc
Rf V0 N001 99000
Ri 0 N001 11000
X§U1 Vs N001 Vcc Vee V0 level2 Avol=1Meg GBW=10Meg Slew=10Meg Ilimit=25m Rail=0
Vos=0 En=0 Enk=0 In=0 Ink=0 Rin=500Meg
Vcc Vcc 0 100
Vee 0 Vee 0
Vs Vs 0 SINE(0 5 60)
.tran 0 0.5 0
.lib UniversalOpAmp2.lib
.backanno
.end
```

3. **State whether your circuit achieved the desired gain of 10**

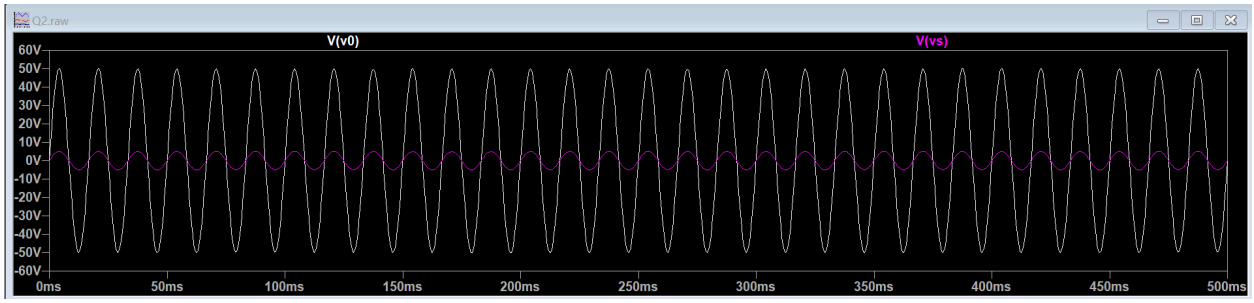
The circuit achieved the desired gain of 10. However, the limits of the power supplies cause for the output to be clipped due to saturation.

4. **State whether it is operating in a nonlinear regime. Justify your statement.**

The circuit is operating in a nonlinear way because Vo doesn't fully follow the Vs during the negative half-cycles. This happens because the negative terminal of the op-amp is 0, so it can't produce negative voltages due to saturation. While the positive half-cycles are amplified as expected with a gain of 10, the negative half-cycles are cut off at 0 V, leading to clipping and nonlinearity.

2.C.

1. **Plot of Vo and Vs as a function of time**



2. **Spice Netlist**

```
* C:\Users\Josh\Documents\COMPENG\Y2S2\2CF3\Asignment1\Q2.asc
Rf V0 N001 99000
Ri 0 N001 11000
X§U1 Vs N001 Vcc Vee V0 level2 Avol=1Meg GBW=10Meg Slew=10Meg Ilimit=25m Rail=0
Vos=0 En=0 Enk=0 In=0 Ink=0 Rin=500Meg
Vcc Vcc 0 100
Vee 0 Vee 100
Vs Vs 0 SINE(0 5 60)
.tran 0 0.5 0
.lib UniversalOpAmp2.lib
.backanno
.end
```

3. **State whether your circuit achieved the desired gain of 10.**

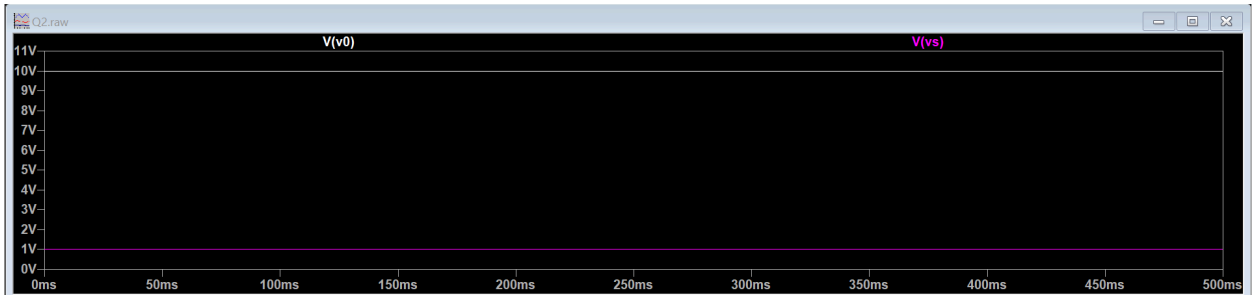
The circuit achieves the gain of 10 at all times.

4. **State whether it is operating in a linear or a nonlinear regime. Justify your statement.**

The circuit operates in a linear regime because Vo follows Vs with the correct gain of 10 for both positive and negative cycles. The two power rails being set at +100 and -100 provide enough range for the op-amp to amplify the signal without clipping, ensuring linear behavior.

2.D.

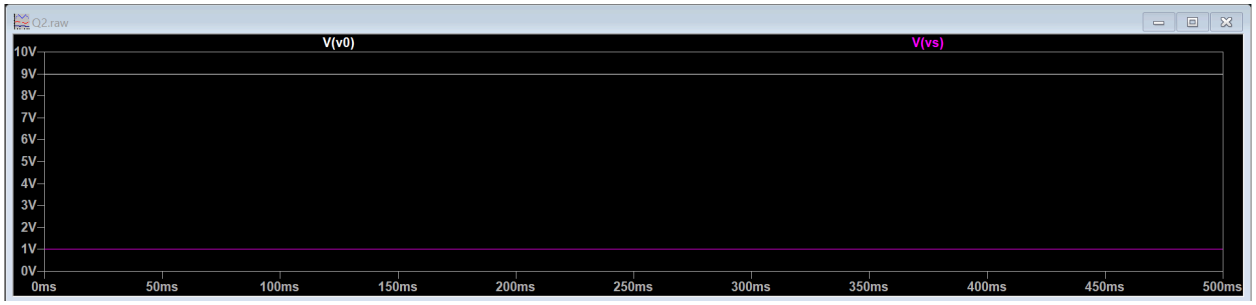
1. **Plot of Vo and Vs for the case of Ao = 10^6**



2. **Spice Netlist for the case of Ao = 10^6**

```
Rf V0 N001 99000
Ri 0 N001 11000
X§U1 Vs N001 Vcc Vee V0 level2 Avol=1Meg GBW=10Meg Slew=10Meg Ilimit=25m Rail=0
Vos=0 En=0 Enk=0 In=0 Ink=0 Rin=500Meg
Vcc Vcc 0 100
Vee 0 Vee 100
V1 Vs 0 1
.tran 0 0.5 0
.lib UniversalOpAmp2.lib
.backanno
.end
```

3. **Plot of Vo and Vs for the case of Ao = 100**



4. **Netlist for the case of Ao = 100**

```
* C:\Users\Josh\Documents\COMPENG\Y2S2\2CF3\Asignment1\Q2.asc
Rf V0 N001 99000
Ri 0 N001 11000
X§U1 Vs N001 Vcc Vee V0 level2 Avol=100 GBW=10Meg Slew=10Meg Ilimit=25m Rail=0
Vos=0 En=0 Enk=0 In=0 Ink=0 Rin=500Meg
Vcc Vcc 0 100
Vee 0 Vee 100
V1 Vs 0 1
.tran 0 0.5 0
.lib UniversalOpAmp2.lib
.backanno
.end
```

5. **State the simulated circuit gain in the case when Ao = 100.**

Observed gain = 9

6. **State the gain error in percentage compared to the ideal gain of 10.**

Percent difference = (observed - true)/true = (9-10)/10 = 10%