ElecEng 2CF4
Assignment 2 Report 1

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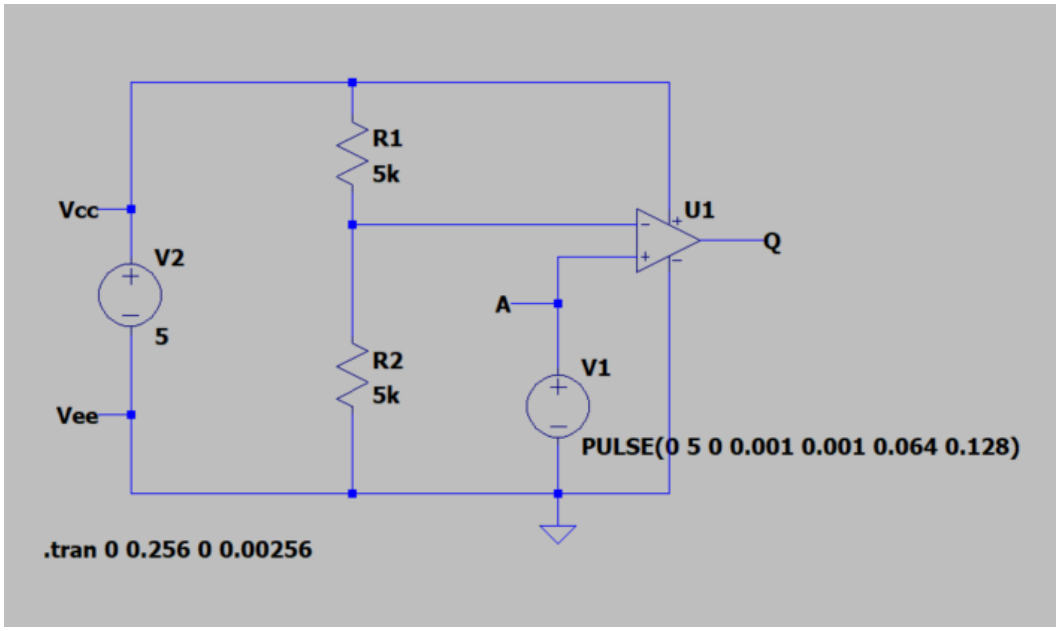
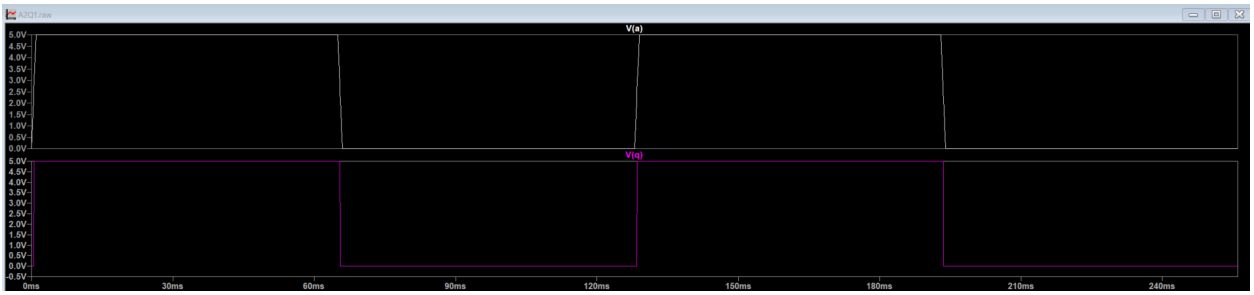
Exercise 1: Simulate a Buffer in LTspice

1.



2.



3.

```
* C:\Users\Josh\Documents\COMPENG\Y2S2\2CF3\Assignment2\A2Q1.asc
V1 A 0 PULSE(0 5 0 0.001 0.001 0.064 0.128)
X§U1 A N001 Vcc 0 Q level2 Avol=1Meg GBW=10Meg Slew=10Meg Ilimit=25m Rail=0 Vos=0
En=0 Enk=0 In=0 Ink=0 Rin=500Meg
V2 Vcc 0 5
R1 Vcc N001 5k
R2 N001 0 5k
.tran 0 0.256 0 0.00256
.lib UniversalOpAmp2.lib
.backanno
.end
```

4. A2Q1.asc

5. **Comment on whether the simulation results match the expected behavior, including a description of the expected behavior and any differences or anomalies (glitches) in the simulation results.**

The simulation matches the expected behavior with no glitches. The circuit was designed to output high when Va > 2.5V and low otherwise.

6. **Explain how you derived the two resistors' values.**

Since we know the top node (Vcc) == 5V and the bottom node is grounded at 0V I derived the two resistor values with voltage division.

$$5V - \left(\frac{R_1}{R_1 + R_2}\right)(5V) = 2.5V$$

$$0V + \left(\frac{R_2}{R_1 + R_2}\right)(5V) = 2.5V$$

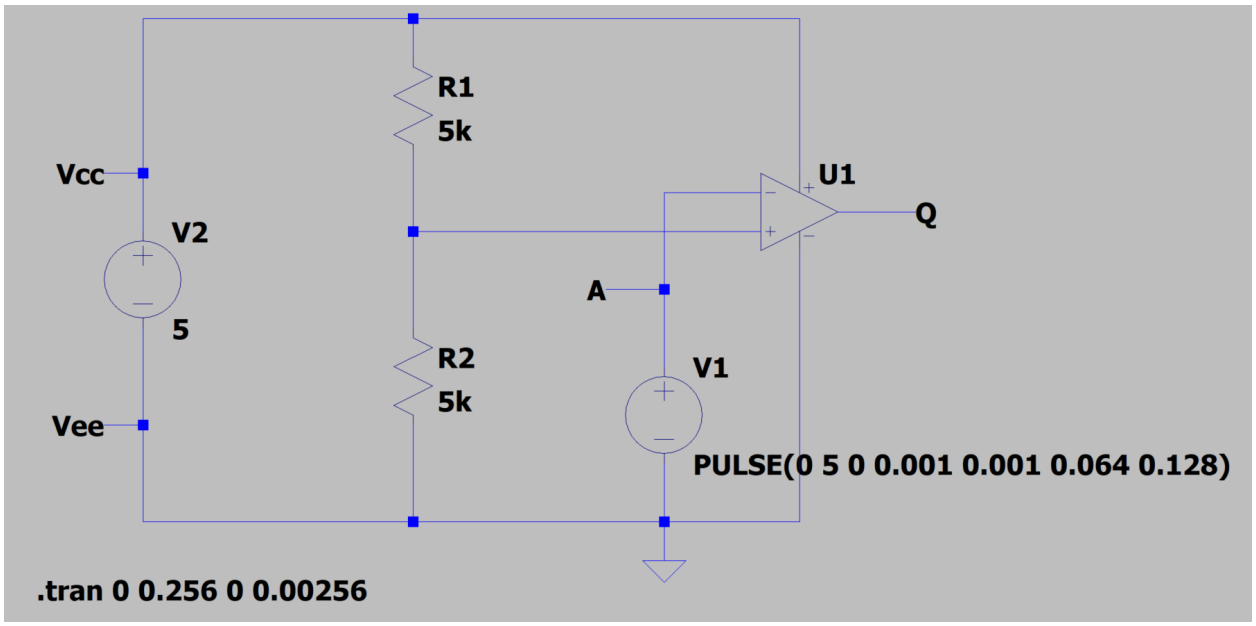
$$R_1 = R_2$$

7. **It was noted that a unit-gain amplifier is not suitable as a buffer because we would like the output to be either voltage high or low even if the input voltage is intermediate. Comment on why this behavior is desirable.**

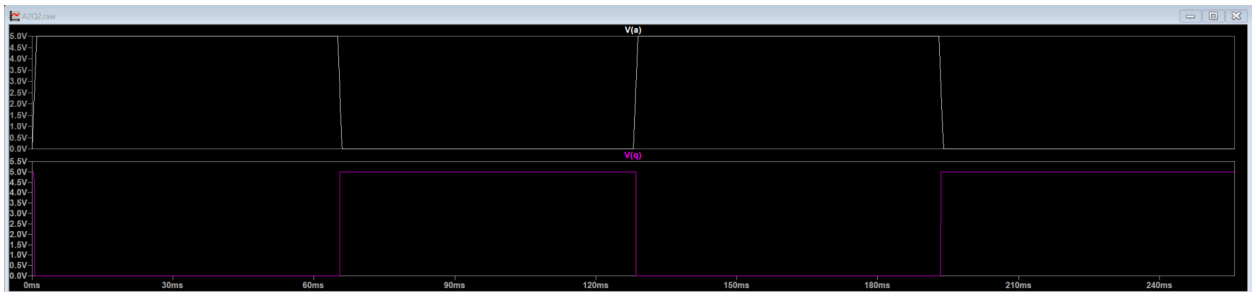
A unit-gain amplifier isn't ideal as a digital buffer because its output mirrors the input voltage linearly. This means an intermediate input voltage results in an intermediate output voltage, which is problematic for digital systems. Digital circuits rely on distinct high and low voltage levels to represent logic states. This clear separation is important for accurate timing (sharp transitions), minimizing noise interference, ensuring correct logic interpretations, and avoiding unpredictable circuit behavior.

Exercise 2: Simulate a NOT Gate in LTspice

1.



2.



3.

```
* C:\Users\Josh\Documents\COMPENG\Y2S2\2CF3\Assignment2\A2Q2.asc
V1 A 0 PULSE(0 5 0 0.001 0.001 0.064 0.128)
X§U1 N001 A Vcc 0 Q level2 Avol=1Meg GBW=10Meg Slew=10Meg Ilimit=25m Rail=0 Vos=0
En=0 Enk=0 In=0 Ink=0 Rin=500Meg
V2 Vcc 0 5
R1 Vcc N001 5k
R2 N001 0 5k
.tran 0 0.256 0 0.00256
.lib UniversalOpAmp2.lib
.backanno
.end
```

4. A2Q2.asc

5. **Comment on whether the simulation results match the expected behavior, including a description of the expected behavior and any differences or anomalies (glitches) in the simulation results.**

The simulation matches the expected behavior with no glitches. The circuit was designed to output high when Va < 2.5V and low otherwise.

6. **Explain why swapping the driving voltages of the inverting and non-inverting inputs turned the non-inverting buffer of Exercise 1 into an inverting buffer.**

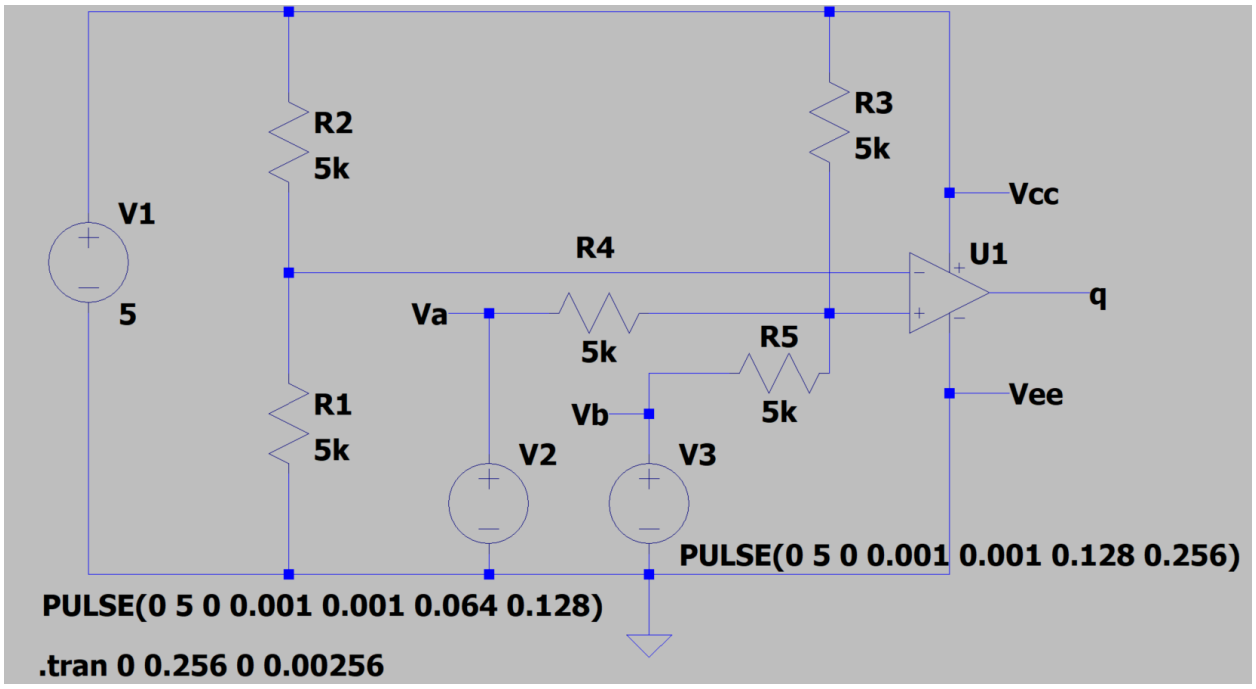
By reversing the op-amp's driving voltages, the non-inverting terminal becomes the reference voltage, fixed at 2.5V. The op-amp outputs 5V whenever the non-inverting terminal's voltage exceeds that of the inverting terminal. For instance, if the inverting terminal (Va) is at 0V, the non-inverting terminal (2.5V) is higher, resulting in a 5V output.

7. **Include the output requirement for the NOT gate. It is not necessary to show its derivation.**

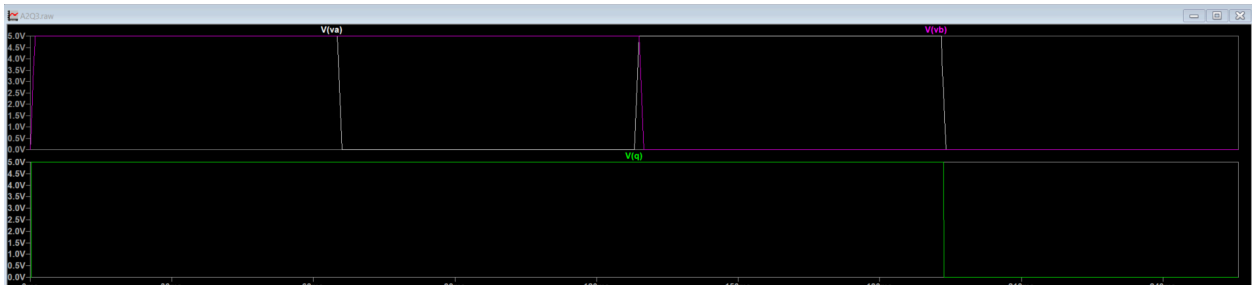
$$V_Q = \begin{cases} 0V, & V_A > 2.5V \\ 5V, & V_A < 2.5V \end{cases}$$

Exercise 3: Simulate an OR Gate in LTspice

1.



2.



3.

```
* C:\Users\Josh\Documents\COMPENG\Y2S2\2CF3\Assignment2\A2Q3.asc
V1 Vcc 0 5
V2 Va 0 PULSE(0 5 0 0.001 0.001 0.064 0.128)
V3 Vb 0 PULSE(0 5 0 0.001 0.001 0.128 0.256)
R1 N001 0 5k
R2 Vcc N001 5k
R3 Vcc N002 5k
R4 N002 Va 5k
R5 N002 Vb 5k
X§U1 N002 N001 Vcc 0 q level2 Avol=1Meg GBW=10Meg Slew=10Meg Ilimit=25m Rail=0
Vos=0 En=0 Enk=0 In=0 Ink=0 Rin=500Meg
```

.tran 0 0.256 0 0.00256
.lib UniversalOpAmp2.lib
.backanno
.end

4. A2Q3.asc
5. **Comment on whether the simulation results match the expected behavior, including a description of the expected behavior and any differences or anomalies (glitches) in the simulation results.**

The simulation results generally match the expected behavior, where the output is low when (5V+Va+Vb) < 2.5V and high otherwise. However, some glitches are observed. Specifically, when 1.5V < Va = Vb < 2.5V during hte rising/falling edges, the output Q goes high, which is not expected.

6. **Analyze the node (i.e., with Kirchhoff's current law) at the non-inverting input of the op-amp to prove that V+ = V̄ = (VCC + VA + VB)/3 if all three resistors branching from it have the same value R.**

Assume all currents exit the node V+.

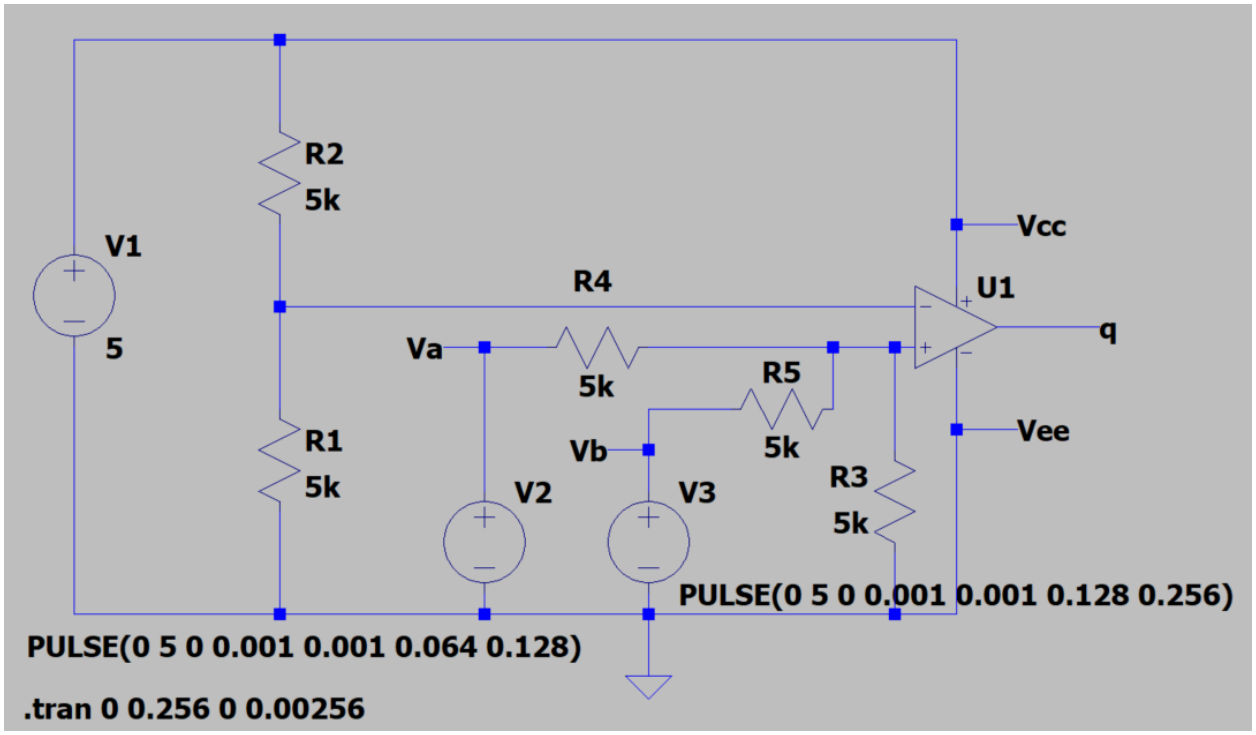
$$\text{At } V^+ = \bar{V}:$$
$$I_{V_{cc}} + I_{V_a} + I_{V_b} = 0$$
$$\text{If } R_1 = R_2 = R_3 = R$$
$$\left(\frac{V^+ - V_{cc}}{R}\right) + \left(\frac{V^+ - V_a}{R}\right) + \left(\frac{V^+ - V_b}{R}\right) = 0$$
$$3V^+ - V_{cc} - V_A - V_B = 0$$
$$3V^+ = V_{cc} + V_A + V_B$$
$$V^+ = \bar{V} = \frac{V_{cc} + V_A + V_B}{3}$$

7. **Include the output requirement for Vout of the OR gate, depending on V̄ .**

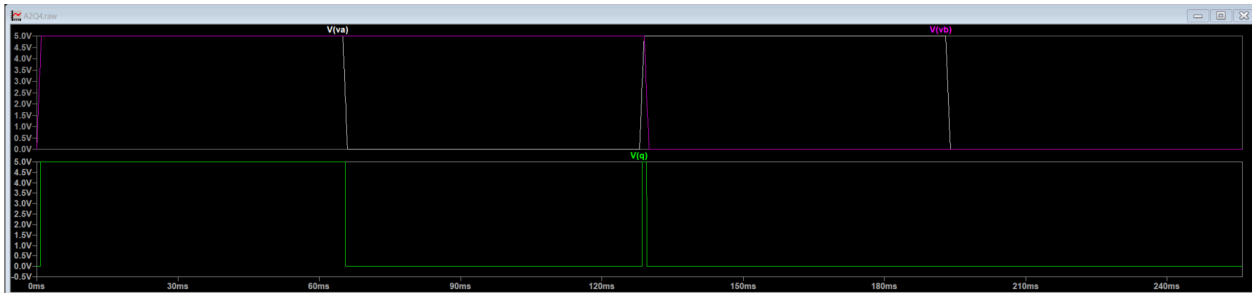
$$V_Q = \begin{cases} 0V, & V_A < 2.5V \\ 5V, & V_A > 2.5V \end{cases}$$

Exercise 4: Simulate an AND Gate in LTspice

1.



2.



3.

```
* C:\Users\Josh\Documents\COMPENG\Y2S2\2CF3\Assignment2\A2Q4.asc
V1 Vcc 0 5
V2 Va 0 PULSE(0 5 0 0.001 0.001 0.064 0.128)
V3 Vb 0 PULSE(0 5 0 0.001 0.001 0.128 0.256)
R1 N001 0 5k
R2 Vcc N001 5k
R3 0 N002 5k
R4 N002 Va 5k
R5 N002 Vb 5k
```

X§U1 N002 N001 Vcc 0 q level2 Avol=1Meg GBW=10Meg Slew=10Meg Ilimit=25m Rail=0 Vos=0 En=0 Enk=0 In=0 Ink=0 Rin=500Meg
.tran 0 0.256 0 0.00256
.lib UniversalOpAmp2.lib
.backanno
.end

4. A2Q4.asc
5. **Comment on whether the simulation results match the expected behavior, including a description of the expected behavior and any differences or anomalies (glitches) in the simulation results.**

Similar to exercise 3, the simulation results generally match the expected behavior, where the output is low when (0V+Va+Vb)/3 < 2.5V and high otherwise. However, some glitches are observed. Specifically, on the rising edge of Va and the falling edge of Vb, there is a momentary switch on Q since it satisfies the implemented equation where (0V+Va+Vb)/3 > 2.5V leads to a logical high output.

6. **A NAND gate is an AND gate with its output inverted. Of course, it can be made by cascading an AND gate and a NOT gate, but suggest how it might instead be designed with a single op-amp.**

A NAND gate can be implemented using a single op-amp by modifying the AND gate circuit, similar to the approach used in Exersize 2 for creating a NOT gate. It can be noted that the Vout requirement for the AND gate:

$$V_Q = \begin{cases} 0V, & V_A < 2.5V \\ 5V, & V_A > 2.5V \end{cases}$$

is identical to what we had in Exersize 1. By reversing the op-amp's driving voltages, the non-inverting terminal becomes the reference voltage, fixed at 2.5V. The op-amp outputs 5V whenever the non-inverting terminal's voltage exceeds that of the inverting terminal. For instance, if the inverting terminal (Va) is at 0V, the non-inverting terminal (2.5V) is higher, resulting in a 5V output. Thus, the design effectively combines the functionality of both the NOT and AND gates within a single op-amp.