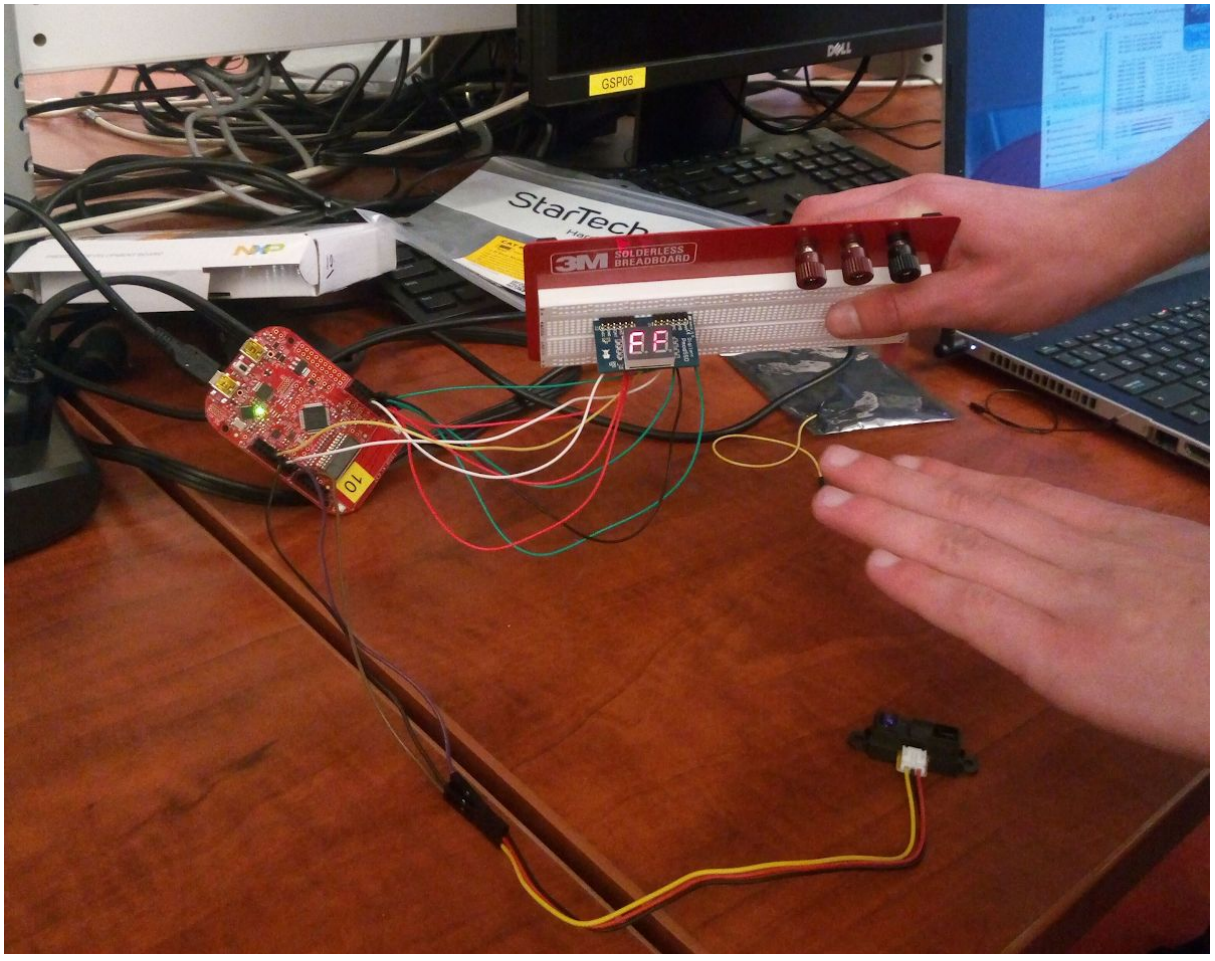
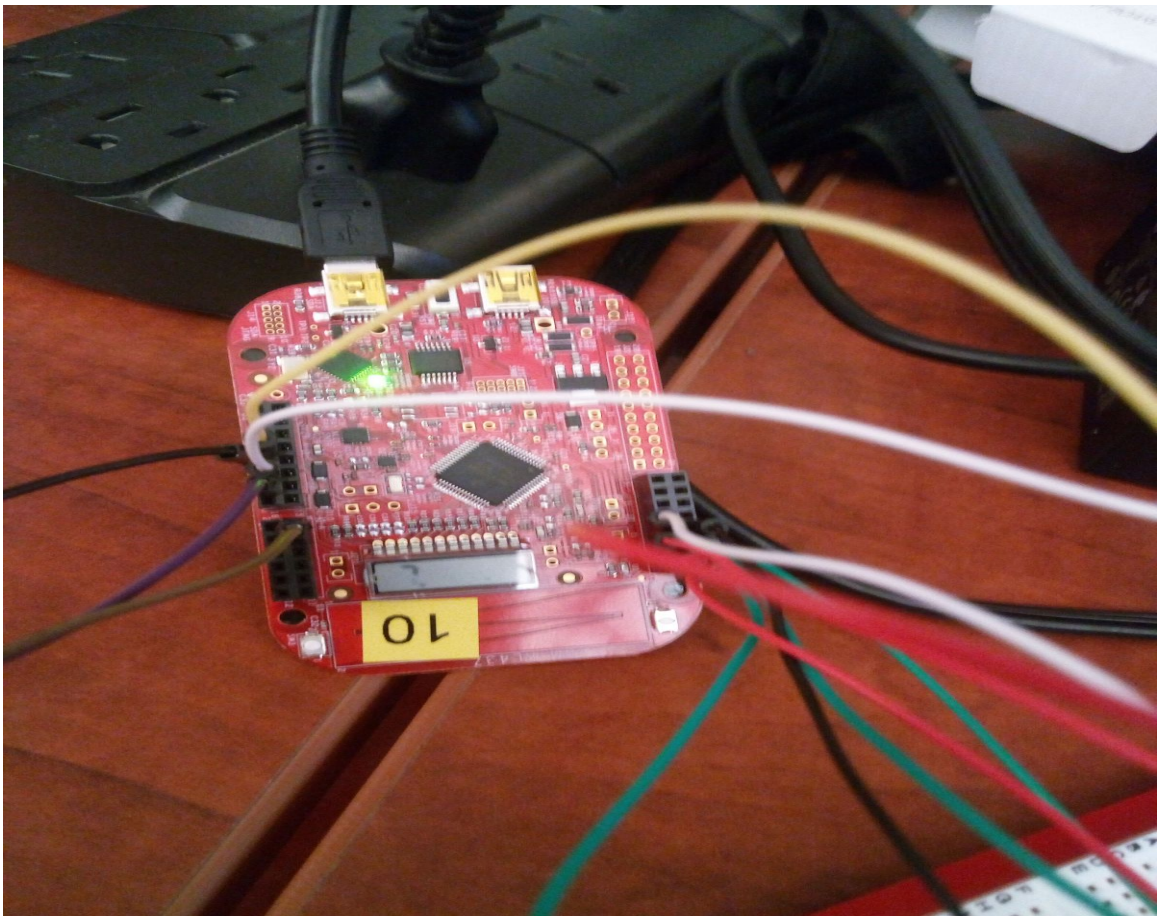
EECS 3215
Digital Logic Design
Lab 6
Michael Founk 213641204
Sean O’Brien 213735741

Problem Statement

The purpose of this lab is to configure the ADC unit on the FRDM board in order to do some signal processing. The lab can be considered two separate tasks, the first of which is to setup the infrared sensor, configure the ADC unit and assign a pin as input to receive the sensor data. The second task of the lab is to convert the sensor data to a form which is can be displayed using two seven segment display digits, and drive the output to the display (each segment of the display is powered by a seperate cable, so the C code must drive the output accordingly).





Top-Level Design

The design of our code to solving this problem is straightforward. We enable the clock to all of the ports we will need, as well as set the pins we will utilize to GPIO mode. We followed the instruction in the lab document, and utilized the reference manual to set the ADC unit properly. The pin receiving the IR data was assigned as an input and the pins driving the display were assigned as outputs. The main loop of our program waits for the conversion to complete before proceeding, and when the data is ready it splits the 8-bits (from ADC settings) of received data into two parts, msb and lsb. These 4-bit sequences drive the two different digits of the display. The seven segment decoder follows the typical convention, and the pins are driven by registers being set and cleared. The digit being displayed is

rapidly switched due to a pin on the board being set or cleared after each digit displays its value.

Code

```
#include <stdio.h>
#include "board.h"
#include "peripherals.h"
#include "pin_mux.h"
#include "clock_config.h"
#include "MKL43Z4.h"
#include "fsl_debug_console.h"
#include <stdlib.h>
/* TODO: insert other include files here. */

/* TODO: insert other definitions and declarations here. */

/*
 * @brief   Application entry point.
 */

void delay(unsigned int mseconds){
        int c, d;

        for (c = 1; c <= 200; c++){
            for(d = 1; d <= 200; d++)
            {

            }
        }
    }

int main(void) {
    /* Init board hardware. */
//     BOARD_InitBootPins();
//     BOARD_InitBootClocks();
//     BOARD_InitBootPeripherals();
//     /* Init FSL debug console. */
//     BOARD_InitDebugConsole();

    SIM->SCGC6 |= 1<<27u;
    SIM->SCGC5 |= SIM_SCGC5_PORTE_MASK;
    SIM->SCGC5 |= SIM_SCGC5_PORTA_MASK;
    SIM->SCGC5 |= SIM_SCGC5_PORTB_MASK;
    SIM->SCGC5 |= SIM_SCGC5_PORTC_MASK;
    SIM->SCGC5 |= SIM_SCGC5_PORTD_MASK;


    ADC0->SC1[0] &= 0xFFFFFFC0;  // 000000; // DIFF and ADCH
    ADC0->CFG1   &= 0xFFFFFFF3; // Mode
    ADC0->CFG2   &= 0xFFFFFFEF; // Muxsel
    PTE->PDDR = 0<<20u; // set PTE as input
```

```
PORTA->PCR[1] = 0x100;
PORTA->PCR[2] = 0x100;
PORTD->PCR[3] = 0x100;
PORTA->PCR[12] = 0x100;
PORTB->PCR[18] = 0x100;
PORTB->PCR[19] = 0x100;
PORTC->PCR[0] = 0x100;
PORTC->PCR[4] = 0x100;

//first four segments
PTA->PDDR |= 1<<1u; //A
PTA->PDDR |= 1<<2u; //B
PTD->PDDR |= 1<<3u; //C
PTA->PDDR |= 1<<12u; //D
//next four segments
PTB->PDDR |= 1<<18u; //E
PTB->PDDR |= 1<<19u; //F
PTC->PDDR |= 1<<0u; //G
PTC->PDDR |= 1<<4u; //selector bit


int lsb = 0;
int msb = 0;

while(1) {

    ADC0->SC1[0] &= 0xFFFFFFC0; // DIFF and ADCH

    while((ADC0->SC1[0] >> 7u) != 0b1) {}
    delay(1000);
    lsb = ADC0->R[0] % 16;
    msb = ADC0->R[0] >> 4;
    printf("This is our thing: %i\n", ADC0->R[0]);

    PTC->PCOR |= 1<<4u;

    if(lsb == 0)
    {
        PTA->PSOR |= 1<<1u; //A
        PTA->PSOR |= 1<<2u; //B
        PTD->PSOR |= 1<<3u; //C
        PTA->PSOR |= 1<<12u; //D
        PTB->PSOR |= 1<<18u; //E
        PTB->PSOR |= 1<<19u; //F
        PTC->PCOR |= 1; //G
    }
    else if(lsb == 1)
    {
        PTA->PCOR |= 1<<1u; //A
        PTA->PSOR |= 1<<2u; //B
        PTD->PSOR |= 1<<3u; //C
        PTA->PCOR |= 1<<12u; //D
        PTB->PCOR |= 1<<18u; //E
        PTB->PCOR |= 1<<19u; //F
```

```
    PTC->PCOR |= 1; //G
}
else if(lsb == 2)
{
    PTA->PSOR |= 1<<1u; //A
    PTA->PSOR |= 1<<2u; //B
    PTD->PCOR |= 1<<3u; //C
    PTA->PSOR |= 1<<12u; //D
    PTB->PSOR |= 1<<18u; //E
    PTB->PCOR |= 1<<19u; //F
    PTC->PSOR |= 1; //G
}
else if(lsb == 3)
{
    PTA->PSOR |= 1<<1u; //A
    PTA->PSOR |= 1<<2u; //B
    PTD->PSOR |= 1<<3u; //C
    PTA->PSOR |= 1<<12u; //D
    PTB->PCOR |= 1<<18u; //E
    PTB->PCOR |= 1<<19u; //F
    PTC->PSOR |= 1; //G
}
else if(lsb == 4)
{
    PTA->PCOR |= 1<<1u; //A
    PTA->PSOR |= 1<<2u; //B
    PTD->PSOR |= 1<<3u; //C
    PTA->PCOR |= 1<<12u; //D
    PTB->PCOR |= 1<<18u; //E
    PTB->PSOR |= 1<<19u; //F
    PTC->PSOR |= 1; //G
}
else if(lsb == 5)
{
    PTA->PSOR |= 1<<1u; //A
    PTA->PCOR |= 1<<2u; //B
    PTD->PSOR |= 1<<3u; //C
    PTA->PSOR |= 1<<12u; //D
    PTB->PCOR |= 1<<18u; //E
    PTB->PSOR |= 1<<19u; //F
    PTC->PSOR |= 1; //G
}
else if(lsb == 6){
    PTA->PSOR |= 1<<1u; //A
                                    PTA->PCOR |= 1<<2u; //B
                                    PTD->PSOR |= 1<<3u; //C
                                    PTA->PSOR |= 1<<12u; //D
                                    PTB->PSOR |= 1<<18u; //E
                                    PTB->PSOR |= 1<<19u; //F
                                    PTC->PSOR |= 1; //G
}else if(lsb == 7){
    PTA->PSOR |= 1<<1u; //A
                    PTA->PSOR |= 1<<2u; //B
                    PTD->PSOR |= 1<<3u; //C
```

```
                    PTA->PCOR |= 1<<12u; //D
                    PTB->PCOR |= 1<<18u; //E
                    PTB->PCOR |= 1<<19u; //F
                    PTC->PCOR |= 1; //G
}else if(lsb == 8){
    PTA->PSOR |= 1<<1u; //A
                                PTA->PSOR |= 1<<2u; //B
                                PTD->PSOR |= 1<<3u; //C
                                PTA->PSOR |= 1<<12u; //D
                                PTB->PSOR |= 1<<18u; //E
                                PTB->PSOR |= 1<<19u; //F
                                PTC->PSOR |= 1; //G
}else if(lsb == 9){
    PTA->PSOR |= 1<<1u; //A
                                PTA->PSOR |= 1<<2u; //B
                                PTD->PSOR |= 1<<3u; //C
                                PTA->PSOR |= 1<<12u; //D
                                PTB->PCOR |= 1<<18u; //E
                                PTB->PSOR |= 1<<19u; //F
                                PTC->PSOR |= 1; //G
}else if(lsb == 10){
    PTA->PSOR |= 1<<1u; //A
                                PTA->PSOR |= 1<<2u; //B
                                PTD->PSOR |= 1<<3u; //C
                                PTA->PCOR |= 1<<12u; //D
                                PTB->PSOR |= 1<<18u; //E
                                PTB->PSOR |= 1<<19u; //F
                                PTC->PSOR |= 1; //G
}else if(lsb == 11){
    PTA->PCOR |= 1<<1u; //A
                                PTA->PCOR |= 1<<2u; //B
                                PTD->PSOR |= 1<<3u; //C
                                PTA->PSOR |= 1<<12u; //D
                                PTB->PSOR |= 1<<18u; //E
                                PTB->PSOR |= 1<<19u; //F
                                PTC->PSOR |= 1; //G
}else if(lsb == 12){
    PTA->PSOR |= 1<<1u; //A
                            PTA->PCOR |= 1<<2u; //B
                            PTD->PCOR |= 1<<3u; //C
                            PTA->PSOR |= 1<<12u; //D
                            PTB->PSOR |= 1<<18u; //E
                            PTB->PSOR |= 1<<19u; //F
                            PTC->PCOR |= 1; //G
}else if(lsb == 13){
    PTA->PCOR |= 1<<1u; //A
                                PTA->PSOR |= 1<<2u; //B
                                PTD->PSOR |= 1<<3u; //C
                                PTA->PSOR |= 1<<12u; //D
                                PTB->PSOR |= 1<<18u; //E
                                PTB->PCOR |= 1<<19u; //F
                                PTC->PSOR |= 1; //G
}else if(lsb == 14){
    PTA->PSOR |= 1<<1u; //A
```

```
                                        PTA->PCOR |= 1<<2u; //B
                                        PTD->PCOR |= 1<<3u; //C
                                        PTA->PSOR |= 1<<12u; //D
                                        PTB->PSOR |= 1<<18u; //E
                                        PTB->PSOR |= 1<<19u; //F
                                        PTC->PSOR |= 1; //G
    }else if(lsb == 15){
        PTA->PSOR |= 1<<1u; //A
                                        PTA->PCOR |= 1<<2u; //B
                                        PTD->PCOR |= 1<<3u; //C
                                        PTA->PCOR |= 1<<12u; //D
                                        PTB->PSOR |= 1<<18u; //E
                                        PTB->PSOR |= 1<<19u; //F
                                        PTC->PSOR |= 1; //G
    }
     delay(1000);
    PTC->PSOR |= 1<<4u;

if(msb == 0)
        {
            PTA->PSOR |= 1<<1u; //A
            PTA->PSOR |= 1<<2u; //B
            PTD->PSOR |= 1<<3u; //C
            PTA->PSOR |= 1<<12u; //D
            PTB->PSOR |= 1<<18u; //E
            PTB->PSOR |= 1<<19u; //F
            PTC->PCOR |= 1; //G
        }
        else if(msb == 1)
        {
            PTA->PCOR |= 1<<1u; //A
            PTA->PSOR |= 1<<2u; //B
            PTD->PSOR |= 1<<3u; //C
            PTA->PCOR |= 1<<12u; //D
            PTB->PCOR |= 1<<18u; //E
            PTB->PCOR |= 1<<19u; //F
            PTC->PCOR |= 1; //G
        }
        else if(msb == 2)
        {
            PTA->PSOR |= 1<<1u; //A
            PTA->PSOR |= 1<<2u; //B
            PTD->PCOR |= 1<<3u; //C
            PTA->PSOR |= 1<<12u; //D
            PTB->PSOR |= 1<<18u; //E
            PTB->PCOR |= 1<<19u; //F
            PTC->PSOR |= 1; //G
        }
        else if(msb == 3)
        {
            PTA->PSOR |= 1<<1u; //A
            PTA->PSOR |= 1<<2u; //B
            PTD->PSOR |= 1<<3u; //C
            PTA->PSOR |= 1<<12u; //D
```

```
    PTB->PCOR |= 1<<18u; //E
    PTB->PCOR |= 1<<19u; //F
    PTC->PSOR |= 1; //G
}
else if(msb == 4)
{
    PTA->PCOR |= 1<<1u; //A
    PTA->PSOR |= 1<<2u; //B
    PTD->PSOR |= 1<<3u; //C
    PTA->PCOR |= 1<<12u; //D
    PTB->PCOR |= 1<<18u; //E
    PTB->PSOR |= 1<<19u; //F
    PTC->PSOR |= 1; //G
}
else if(msb == 5)
{
    PTA->PSOR |= 1<<1u; //A
    PTA->PCOR |= 1<<2u; //B
    PTD->PSOR |= 1<<3u; //C
    PTA->PSOR |= 1<<12u; //D
    PTB->PCOR |= 1<<18u; //E
    PTB->PSOR |= 1<<19u; //F
    PTC->PSOR |= 1; //G
}
else if(msb == 6){
    PTA->PSOR |= 1<<1u; //A
                                    PTA->PCOR |= 1<<2u; //B
                                    PTD->PSOR |= 1<<3u; //C
                                    PTA->PSOR |= 1<<12u; //D
                                    PTB->PSOR |= 1<<18u; //E
                                    PTB->PSOR |= 1<<19u; //F
                                    PTC->PSOR |= 1; //G
}else if(msb == 7){
    PTA->PSOR |= 1<<1u; //A
                    PTA->PSOR |= 1<<2u; //B
                    PTD->PSOR |= 1<<3u; //C
                    PTA->PCOR |= 1<<12u; //D
                    PTB->PCOR |= 1<<18u; //E
                    PTB->PCOR |= 1<<19u; //F
                    PTC->PCOR |= 1; //G
}else if(msb == 8){
    PTA->PSOR |= 1<<1u; //A
                                    PTA->PSOR |= 1<<2u; //B
                                    PTD->PSOR |= 1<<3u; //C
                                    PTA->PSOR |= 1<<12u; //D
                                    PTB->PSOR |= 1<<18u; //E
                                    PTB->PSOR |= 1<<19u; //F
                                    PTC->PSOR |= 1; //G
}else if(msb == 9){
    PTA->PSOR |= 1<<1u; //A
                                    PTA->PSOR |= 1<<2u; //B
                                    PTD->PSOR |= 1<<3u; //C
                                    PTA->PSOR |= 1<<12u; //D
                                    PTB->PCOR |= 1<<18u; //E
```

```
                                        PTB->PSOR |= 1<<19u; //F
                                        PTC->PSOR |= 1; //G
        }else if(msb == 10){
            PTA->PSOR |= 1<<1u; //A
                                        PTA->PSOR |= 1<<2u; //B
                                        PTD->PSOR |= 1<<3u; //C
                                        PTA->PCOR |= 1<<12u; //D
                                        PTB->PSOR |= 1<<18u; //E
                                        PTB->PSOR |= 1<<19u; //F
                                        PTC->PSOR |= 1; //G
        }else if(msb == 11){
            PTA->PCOR |= 1<<1u; //A
                                        PTA->PCOR |= 1<<2u; //B
                                        PTD->PSOR |= 1<<3u; //C
                                        PTA->PSOR |= 1<<12u; //D
                                        PTB->PSOR |= 1<<18u; //E
                                        PTB->PSOR |= 1<<19u; //F
                                        PTC->PSOR |= 1; //G
        }else if(msb == 12){
            PTA->PSOR |= 1<<1u; //A
                                    PTA->PCOR |= 1<<2u; //B
                                    PTD->PCOR |= 1<<3u; //C
                                    PTA->PSOR |= 1<<12u; //D
                                    PTB->PSOR |= 1<<18u; //E
                                    PTB->PSOR |= 1<<19u; //F
                                    PTC->PCOR |= 1; //G
        }else if(msb == 13){
            PTA->PCOR |= 1<<1u; //A
                                        PTA->PSOR |= 1<<2u; //B
                                        PTD->PSOR |= 1<<3u; //C
                                        PTA->PSOR |= 1<<12u; //D
                                        PTB->PSOR |= 1<<18u; //E
                                        PTB->PCOR |= 1<<19u; //F
                                        PTC->PSOR |= 1; //G
        }else if(msb == 14){
            PTA->PSOR |= 1<<1u; //A
                                        PTA->PCOR |= 1<<2u; //B
                                        PTD->PCOR |= 1<<3u; //C
                                        PTA->PSOR |= 1<<12u; //D
                                        PTB->PSOR |= 1<<18u; //E
                                        PTB->PSOR |= 1<<19u; //F
                                        PTC->PSOR |= 1; //G
        }else if(msb == 15){
            PTA->PSOR |= 1<<1u; //A
                                        PTA->PCOR |= 1<<2u; //B
                                        PTD->PCOR |= 1<<3u; //C
                                        PTA->PCOR |= 1<<12u; //D
                                        PTB->PSOR |= 1<<18u; //E
                                        PTB->PSOR |= 1<<19u; //F
                                        PTC->PSOR |= 1; //G
        }

}
```