University of South Australia
Division of STEM

Engineering Honours Project A (**ENGG 4009**)

Assessment 3A - Preliminary Report

RF FPGA CHANNELISATION

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University of South Australia

Disclaimer

I declare the following to be my own work, unless otherwise referenced, as defined by the University's policy on plagarism.

Kane O'Brien (110268293)

I declare that I have viewed the Academic Integrity Module and have passed the Module. I understand what Academic Integrity means and what Academic Misconduct is.

Kane O'Brien (110268293)

1 Introduction

In the 1860's Maxwell formulated theories of electro-magnetic propagation through free space. Since then, radio has been a constantly evolving field. Due to the proliferation of radio communication, the Radio Frequency (RF) spectrum is approaching saturation, making it difficult to find free space to communicate. This is managed by separating the spectrum into channels, requiring a radio with the ability to tune to different frequencies in order to observe different transmissions. Utilising digital signals, issues inherent to radio transmissions can be mitigated; signal integrity can be preserved in noisy environments, and error detection and correction can be integrated into the process. Digital channelisation is a fundamental part of modern communication technologies such as mobile (GSM, 3G, 4G, 5G) and WiFi. Without the growth of digital computing and digital signal processing, radio would still be a primative process in the analogue domain. Hardware required for digital radio is smaller, cheaper and far more efficient, consequently allowing these technologies to exist. Digital channelisation is currently performed on purpose-built hardware, but advances in hardware technologies and Field Programmable Gate Array (FPGA) density have encouraged the growth of Software Defined Radio (SDR) and the ability observe larger portions of the spectrum. Currently, there is no 'open-source' channeliser technology available or implemented; the following research is to build a framework supportive of an open source channeliser.

2 Background

When radio is thought of in everyday terms, it is often the car radio that comes to mind, listening to music and news - or perhaps the CB radio (citizens band) used by truck drivers and caravaners alike. Radio is a technology based in the electro-magnetic spectrum, with many applications including voice communication, music, TV, data transfer, and other radio developments such as RADAR (Radio Detection And Ranging) and radiographic imaging. Due to the proliferation of radio technology, the electro-magnetic spectrum is approaching saturation, making it difficult to find free space to communicate. In order to manage the spectrum and avoid unintentional interference, structured radio channels have been designated by governing bodies around the world.

In the past, channelisation was an analogue process, tuning complex electronic circuitry to match a given frequency, filter out the 'side-bands' (undesired channels) to receive only the desired channel. Practically, this enabled communication on one frequency, and the receiver would need to be tuned each time a different channel was desired. In order to receive multiple channels, duplication of electronic circuitry is required - increasing complexity and cost of implementation. Radio is inherently analogue due to physical constraints however, Analogue-to- Digital (ADC) and Digital- to- Analogue (DAC) converters exist enabling operation of digital computing solutions in the radio domain. Modern ADC hardware has suitably high sampling rates to allow sampling directly from the HF (High Frequency, 3-30MHz) radio spectrum. Digital Signal Processing (DSP) techniques can then be used to perform channelisation on a digital data stream.

The digital channelisation process requires several separate data streams to be processed, before recombination in order to form a final output; the processing should be performed in a cohesive manner, for which parallel computing solutions are appropriate (Harris, Dick & Rice, 2003). Graphics Processor Units (GPU) and Field Programmable Gate Array (FPGA) circuitry were designed for highly parallel computing, and their capability can be leveraged for digital channelisation. Mathematically, channelisation is well understood (Harris, 2004), and implemented heavily in digital mobile communications (GSM, 3G, 4G, 5G, WiFi). Current implementations of channelisers are proprietary and this research serves to develop an open-source, freely available SDR channeliser foundation for future research and provide a channeliser for the radio community.

3 Aims and Objectives

Aims

The aim of this research is to develop an understanding of digital signal processing techniques required for radio frequency channelisation, leveraging prior approaches and utilising open-source software.

Objectives

1. Investigate literature to determine prior approaches and available software tools.
2. Develop a channeliser simulator to gain an understanding of digital signal processing techniques.
3. Design a channeliser for implementation on an FPGA.
4. Evaluate the performance of the FPGA based channeliser on supplied hardware in order to determine functionality.

4 Proposed Research Plan

The scope of this research ensures that the research methodology is a mixed approach. Each objective requires a different procedure and methodology, and has been organised by objective

Objective 1: Investigate the literature to determine prior approaches and available software tools. The methodology required for this objective is qualitative literature review and consultation with industry supervisors. This study will first review the digital signal processing (DSP) algorithms involved in channelisation to develop an understanding of process. The study will then focus on previous approaches and available programming packages in order to determine a suitable method for implementation. Journals of particular interest are *"IEEE Transactions on Microwave Theory and Techniques"* and *"IEEE Transactions on Signal Processing"*; further, research articles and books authored by 'F.J. Harris' are significant. This research shall be conducted in March - April 2021.

Objective 2: Develop a channeliser simulator to gain an understanding of digital signal processing techniques. Using MATLAB and/or Simulink, a channeliser simulator shall be modelled in order to validate the design and produce quantitative data. The simulator will be validated with test signals to quantify performance. An analysis will be performed on effects of common radio challenges - high peak-to-average-power ratio (PAPR), poor signal-noise ratio (SNR), quantisation error. This research shall be conducted throughout April – August 2021.

Objective 3: Design a channeliser for implementation on an FPGA. Using High Level Synthesis (HLS) tools or Hardware Defined Language (HDL) a hardware model of the channeliser simulator will be realised. The HLS/HDL channeliser can be quantitatively tested in FPGA simulation, and the analysis process developed in objective 2 can be followed, comparing the results to ensure performance is within allowable limits set in consultation with supervisors. This research shall be conducted in August – October 2021.

Objective 3: Evaluate the performance of the FPGA based channeliser in order to determine functionality. The HLS/HDL channeliser will be implemented to a dedicated FPGA/SDR (software defined radio) board. A defined set of test procedures will be developed with input from industry supervision. The FPGA channeliser will be validated quantitatively to test for consistency with previous analysis, and compliance with industry supervisor design specifications. This research shall be conducted in October – November 2021.

5 References

Harris, FJ 2004, *Multirate Signal Processing for Communication Systems*, 1st edn., Prentice Hall PTR, Upper Saddle River, New Jersey.

Harris, FJ, Dick, C & Rice, M 2003, *Digital receivers and transmitters using polyphase filter banks for wireless communications*, *IEEE Transactions on Microwave Theory and Techniques*, vol. 51, no. 4, pp. 1395–1412.

6 Attachments

Remember to attach your Minutes of Supervisor Meetings.

RF FPGA CHANNELISATION - ENGINEERING HONOURS PROJECT A (ENGG 4009)

MEETING MINUTES

Purpose:	Kick-off meeting for Honours Project, RF FPGA Channelisation
Date:	Tuesday, 9/3/21
Time:	10am - 11am
Location:	MLK-P1-38
Facilitator:	Professor Kutluyil Dogancay
Signed:	Kutluyil Dogancay Digitally signed by Kutluyil Dogancay Date: 2021.03.10 14:29:19 +10'30'
Attendees:	
Jeffrey Wojtiuk	
Kutluyil Dogancay	
Kane O'Brien	

Report from previous week:

Discussion, Issues:

- De-scoping of project from the initial outlaid project for individual project
- Quantization problem in moving from analogue/ floating to a fixed-point processing
- SNR, ADC bit resolution and effects
- MATLAB multilevel QPSK QAM and OFDM signals (high peak-averages)
    - Raised cosine pulses
- FPGA hardware implementation is still the end target and motivation.
- Spectral Noise Density
- How much SNR loss for what Bitrate (BER/SNR – floating point is the best case scenario; compare to fixed point)
- Quantise spectrum, recover (channelise) signals (look at fixed point) (FixedPointToolbox) (Compare fixed to float point)
- Measure SNR, attempt recovery, but ideally the effect of noise on the channel can be measured at the SNR level.

Actions:	**Responsible:**
• **Develop sample signals in MATLAB that can be used throughout the project** • **Generate gaussian white noise. Generate to a controllable power level.** • **Modulate these and simulate a RF spectrum**	

RF FPGA CHANNELISATION - ENGINEERING HONOURS PROJECT A (ENGG 4009)

MEETING MINUTES

Purpose:	2nd weekly meeting for Honours Project, RF FPGA Channelisation
Date:	Tuesday, 16/3/21
Time:	10am – 11:30am
Location:	MLK-P1-38
Facilitator:	Professor Kutluyil Dogancay
Signed:	Kutluyil Dogancay Digitally signed by Kutluyil Dogancay Date: 2021.03.17 00:06:42 +10'30'
Attendees:	
Jonathon Harvey	
Kutluyil Dogancay	
Kane O'Brien	

Report from previous week:

A little overwhelmed leaving the initial meeting, but I've connected all the dots and understands where the technology sits, feeling much better about the project overall however understanding a steep learning curve still approaching.

Obtained a reference book from TAFESA – Multirate Signal Processing for communication system (Fredric J Harris) - this is also highly recommended by Jonathon, as well as any papers and linked/ refered literature from Harris.

Discussion, Issues:

- Discussed the new scope of the project
- Discussed the research paper, how channelisation math works, Key terms that will develop a good deal of material to be understood/ researched (Polyphase channeliser/ FIR filter/ CIC filter. There is a book on the subject of 'python modulation' to be found.
- Discussed tools and software to be used for the new project
    - Python Modulation blocks
    - FM/AM generation can be done in Simulink. IQ data can be generated and saved for later, or processed on generation.
    - Blade RF 2.0 SDR is hardware target for stretch goal; plan to look at some documentation for the processors onboard.
- LMA happy to simulate with fixed frequency tones initially, happy to see basic fm signal simulation being used for encoding. QPSK / FSK encoding also encouraged. BladeRF SDR can record fullrate 16(18?)bit I/Q signal, can use to obtain 1-3 audio channel. this can be used to test the simulation at a later date – able to physically listen to the output (triple J) although audio delays may be difficult to hear physically.
- Data transfer of (abcdefg…) in binary is acceptable, will need to look at pulse shapes if doing binary data.
- Ideally simulate hardware before implementation (Python C++ libraries available)
- Areas of interest for literature (Review current libraries, FFT (feasibility onboard fpga vs. known implementations), Implementation method (VHDL/HLS[intel compiler/blackbox HLS] Matlab HDL Coder)

Actions:	**Responsible:**
• Kane to continue understanding the theory / maths involved. • Kutlu send some lecture notes from DSP course around Multirate, previous assignments that are on topic and helpful • Kane to setup a MS teams group to allow communication & collaborative file sharing • Kane to provide Jonathon access to GitHub – where comments and direction can be made and provided. • Kane to arrange further meetings with Kutlu to catch up on the math/ some content that exists in different elective subjects.	