University of South Australia
Division of STEM

Engineering Honours Project A (**ENGG 4009**)

Assessment 3B - Research Proposal

Effective Radio Channelisation using Polyphase Digital Signal Processing Techniques

Student:
Kane O'BRIEN
obrkw001@mymail.unisa.edu.au
110268293

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Supervisors:
Professor Kutluyıl Doğançay
Dr. Jeffrey Wojtiuk
Jonathon Harvey

LOCKHEED MARTIN

University of South Australia

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Kane O'Brien (110268293)

I declare that I have viewed the Academic Integrity Module and have passed the Module. I understand what Academic Integrity means and what Academic Misconduct is.

Kane O'Brien (110268293)

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1 Introduction

A radio channel is a small slice of the Radio Frequency (RF) spectrum upon which a signal can be broadcast. In order to maximise the spectrum, channels are placed at different frequencies; channelisation is the process of matching a transmitter and receiver in order to allow communication. A polyphase channeliser is a digital signal processing technique which filters multiple signals and returns them to 'baseband' in seperate channels, for further processing. The purpose of this research is to determine the efficacity of polyphase channelisation on Field Programmable Gate Array (FPGA) hardware. The research aims to answer questions in the constraints of analytical vs. numerical solutions to the polyphase channelisation theory by exploring the effects upon the signal paths in computer simulation, and hardware implementation. Channelisation theory is explored from motivation to prior approach, exploring digital filter and multirate-sampling techniques in order to simulate a critically sampled and over-sampled filter bank in software and hardware.

2 Background

Polyphase channelisation was mathematically explored as an application of multi-rate sampling in the 1980's by Crochiere, and 1990's by Harris to provide a more computationally efficient solution for multi-channel digital recieving. Current technologies utilise the Fast Fourier Transform (FFT) to isolate channels, Application Specific Integrated Circuitry (ASIC) is highly efficient in channelisation through evolution of technology. Polyphase filtering provides specific advantages that could be profound for the digital communication industry if implemented however silicon technology limitations have hindered application. Whilst the mathematical problem is solved, the literature surrounding polyphase channelisation has not advanced and refers back to itself as the FFT is generally considered sufficient for current technologies.

2.1 Phase and Gain Imbalance from Polyphase Channeliser

Modern digital communications rely on many channels multiplexed in frequency and phase; two phase-orthogonal channels –*In-phase, I and Quadrature-phase, Q* – are utilised and the effects of polyphase signal processing upon the orthogonality and require exploration. Digital modulation requires initally dividing the signal into words, before applying a scheme such as Quadrature Amplitude Modulation (QAM); most schemes are described in the complex plane shown by equation (1) where A and B are the I and Q coefficients (Rohde & Schwarz nd.). Commonly seen in Asynchronus Digital Subscriber Line (ADSL), QAM will have a constellation above 4096 bits requiring a high Signal to Noise Ratio (SNR) per Shannons theorem (Tanenbaum & Wetherall 2014). Frequency Division Multiplexing (FDM) and Orthogonal-FDM (OFDM) are utilised to decompose the QAM constellation over multiple frequencies. i.e. a QAM-1024 can be deconstructed to 4xQAM-256 channels,

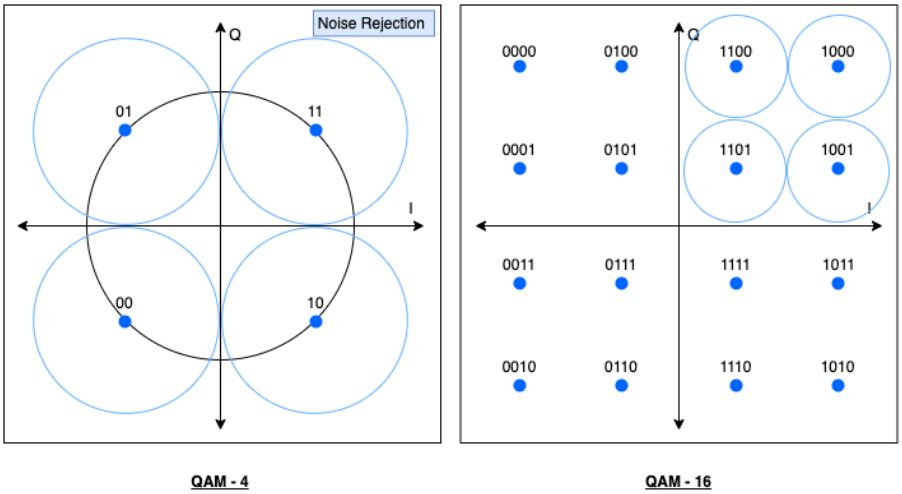

Figure 1: Example QAM4 and QAM16 constellations showing noise rejection rings.

the overall bit-rate remains unchanged but Shannons SNR requirement decreases, shown in Figure (1). Polyphase channelisation seperates channels through processing of spectral information before decomposition through the Discrete Fourier Transform (DFT) collapses the spectrum, efficently returning the channels. The effect of polyphase channelisation upon IQ signals gain imbalance and orthogonality shift has not been explored as the pure mathematical models of Crochiere & Rabiner (1983) and Harris (2004, 2021) constrain this error to 0, therefore require exploration.

$$\begin{aligned} \hat{x}_{(t)} &= A\cos(2\pi f_c t) - jB\sin(2\pi f_c t) \\ &= Ce^{-j2\pi f_c t} \end{aligned} \tag{1}$$

2.2 Digital Polyphase Filter Bank

Polyphase channeliser is a parallel process whilst Fast Fourier Transform (FFT) is a serial process which may provide advantages to communication technology in hardware implementation. The RF spectrum is inherently analogue, Digital to Analogue (DAC) and Analogue to Digital Converters (ADC) which enable the receiver to operate on digital signals; by sampling frequency is dictated by the Nyquist sampling critereon, with ADC of the early 2000's capable of operating in the *'low to mid 100's of megahertz'* - modern ADC capable of frequencies over 6 GHz (Harris, Dick & Rice 2003; Analog Devices 2016). This is suitable for Intermediate Frequency (IF) and RF receivers, simplifying the electronics. Figure 2 represents the theoretical model, however due to the IQ signal, Figure 3 is more realistic.

By nature of the digital data stream, the Discrete Fourier Transform (DFT) is common to most channeliser implementations to convert signals between time and frequency domain. The DFT (equation 2) is the principle transform, however is generally decomposed into the Fast Fourier Transform (FFT) - (Radix_2 Cooley-Tukey FFT algorithm), limited to

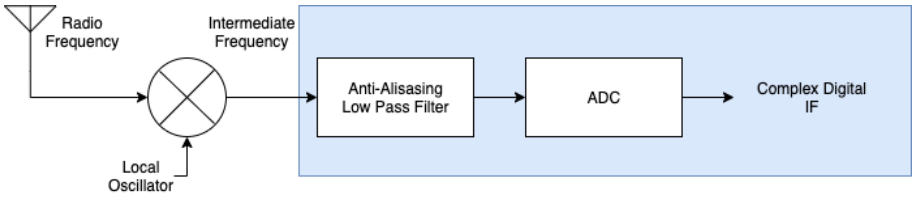

Figure 2: Example of digital radio receiver.

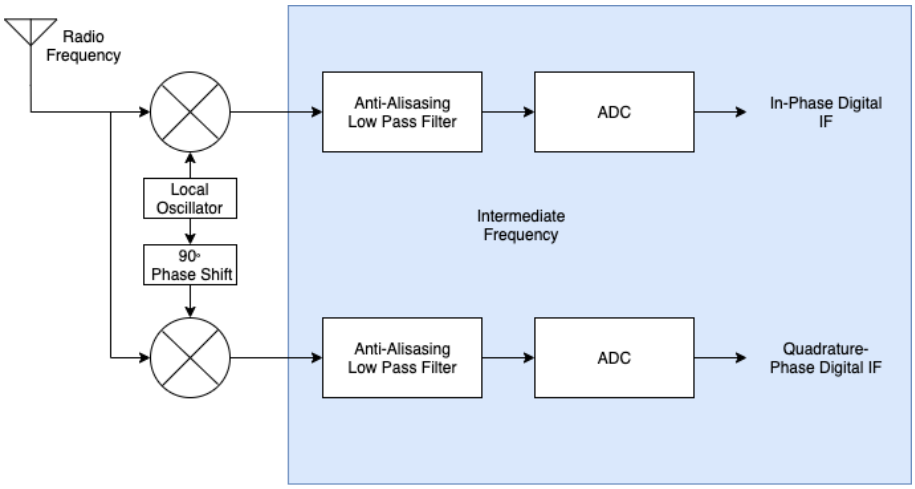

Figure 3: Realistic digital radio reciever.

N_2 substitution of N. The DFT outputs n 'frequency bins' seperated by $\frac{k}{N}$, where each bin is a channel containing IQ signal, with a fixed filter response (Proakis & Manolakis 2014).Conversely a polyphase filter bank can be built through an input commutator and multi-rate signal processing techniques, resulting in multiple 'arms' each with different spectral information, due to a $1/F_s$ phase shift. Each arm is then run through a decomposed prototype filter as shown by equation 3 (Harris 2021). In order maintain congruency between arms, the filter must be linear and time invariant, such as a Finite Impulse Response (FIR) filter (Crochiere & Rabiner 1983). The polyphase filter bank results in constructive and destructive summation when the spectral information is realigned through a DFT/ FFT, resulting in the de-multiplexed channels as outputs.

$$X_k = \sum_{n=0}^{N-1} x_n e^{-j2\pi kn/N} \tag{2}$$

Multirate sampling techniques are used to adjust the sampling rate, however decimation further results in spectral imaging which provides a further advantage over the DFT process, as the output is provided directly to baseband, as shown in Figure 4 (Crochiere & Rabiner 1983; Harris 2004, 2021). By implementing the polyphase channeliser similarly to Figure 5, a parallel process is obtained, with a smaller FFT resulting in a more efficient channeliser.

$$y[n] = \sum_{k=0}^{N-1} h[k]x[n-k] \tag{3}$$

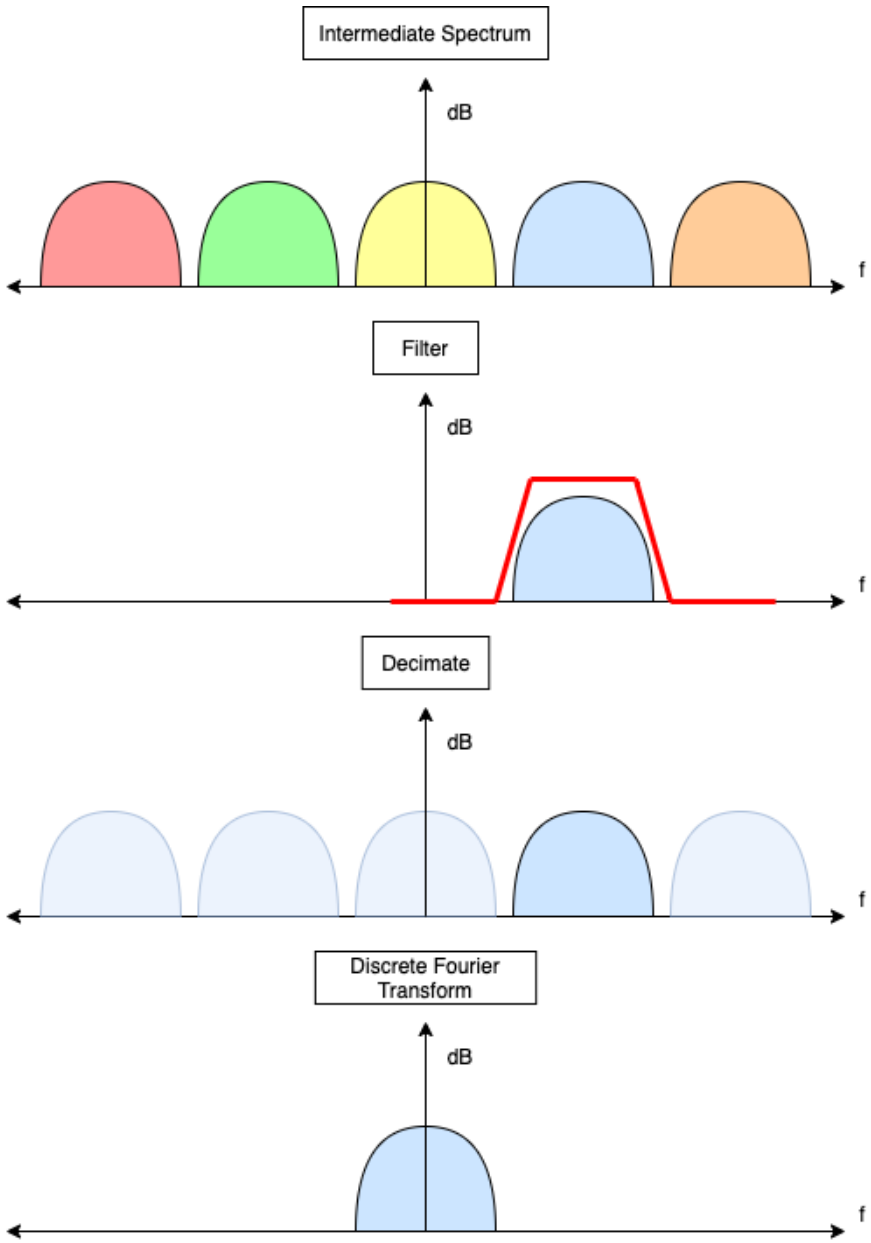

Figure 4: Spectrum before and after filtering, followed by imaging through DFT

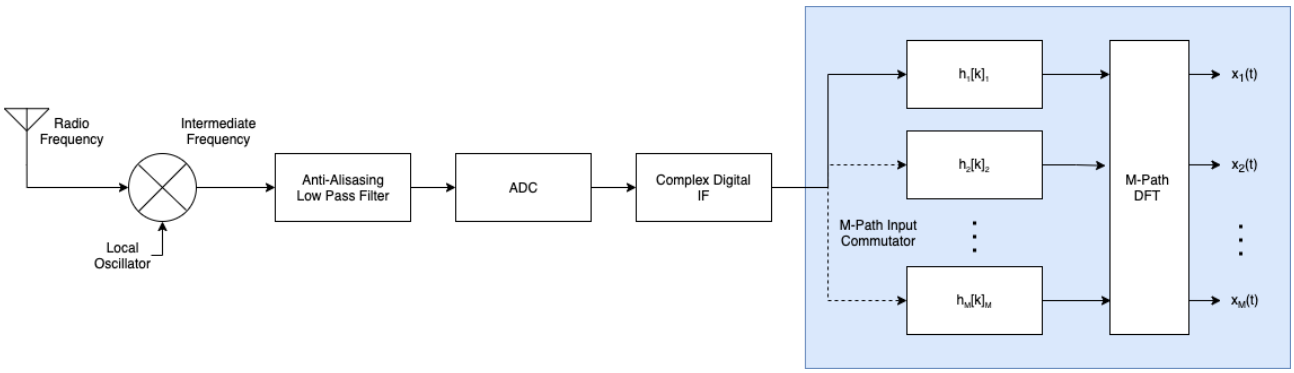

Figure 5: Derived polyphase channeliser

The general case of a polyphase channeliser is an over-sampled polyphase filter, colloquially referred as 'Weighted Overlapped and Add' (WOLA), in which the decimation factor is less than the critical value ($M < K$), allowing managed channel overlap to minimise spectral leakage (Crochiere & Rabiner 1983). Crochiere & Rabiner (1983) suggest WOLA to be more capable in an multi-dimensional processing problem rather than one dimensional data of an RF timeseries, however Pritsker, Shan Neoh, Cheung et al. (nd.) dispute this, and provide a framework for WOLA+FFT implementation onto an FPGA, requiring further research in the hardware hardware implementation.

2.3 Prior Approaches

Technology has evolved with high clock rates to support FFT channelisation within ASIC and RFSoC, ubiquitious however not generic of flexible in use. Harris, Dick & Rice (2003) has explored the performance of polyphase channelisation through quantitatively through numeric simulation and proof of concept. Pritsker, Shan Neoh, Cheung et al. (nd.) have explored the oversampled case using quantitative methodology, providing a framework for FPGA integration through use of proprietary High Level Synthesis (HLS) tools. Honours student George (2005) and PhD student Shin (2017) used similar qualitative methodologies for the polyphase channelisation component of their research, however both were limited by technology at the time. George (2005) was able to implement a polyphase channeliser on an FPGA, however the FPGA (Altera Cyclone II) of the time was limited in application due to limited internal logic elements, reducing filter length and lack of IQ signal. Shin (2017) was later able to implement a polyphase channeliser to an unknown modern Graphics Processor Unit (GPU), noting the GPU hardware is more flexible in a runtime environment.

The explored literature points to a polyphase channeliser producing a more effective FFT process, able to process a wider bandwidth with improved spectral leakage and higher harmonic rejection however, a recognised issue is due to the digital domain; floating point logic elements on FPGA's are typically limited on consumer level hardware and fixed point logic results in quantisation error (George 2005; Shin 2017; Harris 2004, 2021). Explored briefly in the literature, the dynamic range and effective noise floor of a signal are tightly intertwined with the digital signal path however it is a recognised research gap, Harris, Dick & Rice (2003) calculate the limit of spectral artifacts to levels of -5dB/bit (12bit ADC provides -60dB, 16bit ADC provides -80dB), whilst Pritsker, Shan Neoh, Cheung et al. (nd.) provides no assumption to the noise floor of the system, however recognise quantisation error in floating-point to fixed-point conversion.

2.4 Knowledge Gap

There is a clear knowledge gap in polyphase channelisation implementation. The literature review stage revealed limited modern research papers, however strong lineage back to the works of Crochiere & Rabiner (1983) and Harris, Dick & Rice (2003). Whilst mathematically,

the polyphase channeliser provides many advantages in comparison to the current FFT channelisation, technology has provided limitations and lead to FFT based channelisers being more prominent in practice; provided sufficient technology advances the polyphase filter may be able to provide a more energy efficient, lower latency solution to an everyday application in digital communication.

George (2005) is the most relevant source for FPGA implementation, however did not provide any quantitative data that could be used to answer the research questions. Efficent synthesis and characterisation of a WOLA type channeliser is a recognised knowledge gap, Pritsker, Shan Neoh, Cheung et al. (nd.) provided a framework that could make the implementation possible, however only as a computer model. The effects of digital bit depth (word length) and continuous quantisation errors in fixed point implementation throughout the digital signal path is a recognised gap in the literature and requires exploration.

3 Aims and Objectives

3.1 Aims

The aim of this research is to develop an understanding of digital signal processing techniques required for radio frequency channelisation, leveraging prior approaches and utilising open-source software.

3.2 Objectives

1. Develop a channeliser simulator to gain an understanding of digital signal processing techniques
2. Design a channeliser for implementation on an Field Programmable Gate Array (FPGA)
3. Evaluate the performance of the FPGA based channeliser on supplied hardware in order to determine functionality
4. Determine the effects of the channeliser in the Frequency Domain Multiplexed (FDM) case

4 Methodology and Methods

The scope of this research ensures that the research methodology is a mixed approach. Each objective requires a different procedure and methodology, and has been organised by objective

4.1 Methodology

Objective 1: Develop a channeliser simulator to gain an understanding of digital signal processing techniques. Using MATLAB, a channeliser simulator shall be modelled in order to validate the design and produce quantitative data. The simulator should operate in floating point and adjustable bit-depth fixed point and will provide a quantitative set of results in quantisation error, fixed point precision, and accumulated error as the Finite Impulse Response (FIR) filter-tap length increases and accumulated error from rounding vs truncation for later analysis.

Objective 2: Design a channeliser for implementation on an Field Programmable Gate Array (FPGA). The channeliser will first be deconstructed into logical blocks, before using Very High Speed Integrated Circuit Hardware Description Language (VHDL) to model, simulated and validate with generated test data. The method will include VHDL simulation to be conducted in a 'Docker container' with 'GHDL'; each logical block can be input a data stream from a text file, and can output a text file. Output data can be quantitativly analysed and compared with the software simulation from objective 1 for validation.

Objective 3: Evaluate the performance of the FPGA based channeliser on supplied hardware in order to determine functionality. Using Intel Quartus, the VHDL code can be synthesised, required hardware logic elements and timing can be observed. The supplied FPGA is an Intel Cyclone 5. The 3rd objective will require as much input data as possible to be channelised; the Quartus synthesis will determine final channels able to be received based on the number of hardware logic elements available and through final place-and-route. After implementation, the performance of the radio can be measured both qualitatively if audio stations are listened to, and quantitatively processing raw data in MATLAB.

Objective 4: Determine the effects of the channeliser in the Frequency Domain Multiplexed (FDM) case. Digital signals using Quadrature Phase Shift Keying (QPSK) or 16-QAM are heaviliy effected by poor Signal to Noise Ratio (SNR), poor Peak to Average Ratio (PAPR) and Gain and Phase imbalances; FDM signals will be measured on a per-channel basis to qualitatively determine the effect of polyphase channelisation in the specific FDM case, to determine qualitative metrics including Bit Error Rate (BER) and Constellation Noise.

5 Ethics & Workplace Health and Safety

5.1 Human Research Ethics

Human research ethics are an important consideration for all research projects. During the definition of the research proposal no human research has been recognised therefore no approval has been sought. At any stage during the research project if human research component is discovered, the appropriate applications will be made before proceeding.

5.2 Workplace Health and Safety

Workplace health and safety is an important consideration for any research endeavour. During the research proposal, several hazards were identified and controlled through risk assessment procedures in accordance with the Workplace Health and Safety Act and Regulations. Table 1 provides the hazard assessment, whilst Figure 6 provides the risk analysis matrix required for assessment. At any stage, if further risks are identified, they shall be assessed and controlled appropriately.

Risk Assessment Matrix

Low Risk = 1 - 4
Medium Risk = 5 - 12
High Risk = 13 - 25

			Consequences				
			Negligible	Minor	Moderate	Significant	Severe
			1	2	3	4	5
Likelihood	Very Unlikely	1	1	2	3	4	5
	Unlikely	2	2	4	6	8	10
	Possible	3	3	6	9	12	15
	Likely	4	4	8	12	16	20
	Very Likely	5	5	10	15	20	25

Figure 6: Risk assessment score matrix

Risk Assessment for Radio Frequency Channelisation Project

Hazard	Hazard Effect	Risk Level	Controls	Residual Risk
Design and programming				
Time spent on computer	Repetitive Strain Injuries	10	• Regular stretches • Warm up • Take regular breaks • Regular change work positions	2
Ergonomic position concerns	Undue stress on body	10	Align workstation to meet ergonomic standards	2
Test and verification				
Use of hand tools	• Injury to self • Damage to work surfaces • Damage to property	12	• Work within Safe Operating Procedures • Wear required personal protective equiptment	1
Demonstration and presentation				
Electromagnetic Emissions	• Burns • Damage to transmitter circuitry • RF interference with other equiptment	15	• Transmit in controlled areas following S.O.P • Ensure connections are terminated correctly • Use appropriate cables and attenuators	1
Cables between equiptment	Slips, trips and falls	7	• Ensure cables are clearly marked and appropriately fixed • Bunt off area to minimise traffic	2

Table 1: Identified Hazards and Controls

6 Logistics & Budget

Recognised within the Methodology section, the research shall be undertaken in two major stages - software simulation, and hardware test and verification; the required software and hardware have been seperated into tables 2 and 3 respectively. The required hardware is to be provided by Lockheed Martin Australia, and therefore the required budget for the project is $0.00.

Software Requirements for Simulation and Firmware Generation

Software	Supplier	O/S?	Cost	Subtotal
Atom Text Editor	atom.io	Yes	$ 0	$ 0
Docker	docker.com	No	$ 0	$ 0
GHDL Simulator	ghdl.free.fr	Yes	$ 0	$ 0
GNU Radio	gnuradio.org	Yes	$ 0	$ 0
GTKwave	gtkwave.sourceforge.net	Yes	$ 0	$ 0
MATLAB	Mathworks Australia, UniSA Licence	No	x	x
Quartus Lite 20.1	Intel	No	$ 0	$ 0
O/S = Open Source, x = unknown cost			**Total:**	$ 0

Table 2: Required parts for software simulation and firmware generation

Hardware / Material Requirements for Test and Verification

Part	Supplier	Cost	Qty.	Supplied?	Subtotal
PC/ Laptop	Student	x	1	Yes, Student	x
BladeRF 2.0 Ax9	Nuand	$ 950	1	Yes, LMA	$ 950
USB 3.0 SS Cable	Varies	$ 10	1	Yes, LMA	$ 10
Extra requirements for live transmission / demonstration purposes					
BladeRF/ other SDR transmitter	Nuand	$ 950	1	Yes, LMA	$ 950
USB 3.0 SS Cable	Varies	$ 10	1	Yes, LMA	$ 10
SMA -30dB Attenuator	Mini-Circuits	$ 50	1	Yes, LMA	$ 50
SMA-SMA Cable	Mini-Circuits	$ 10	2	Yes, LMA	$ 20
x = unknown cost				**Total:**	$ 1990

Table 3: Required parts for test, verification and live demonstration

7 Timetable

The proposed timeline for the research project is as shown in Figure 7. This is subject to change as required time is estimated and course requirements from ENGG4011 are not yet confirmed.

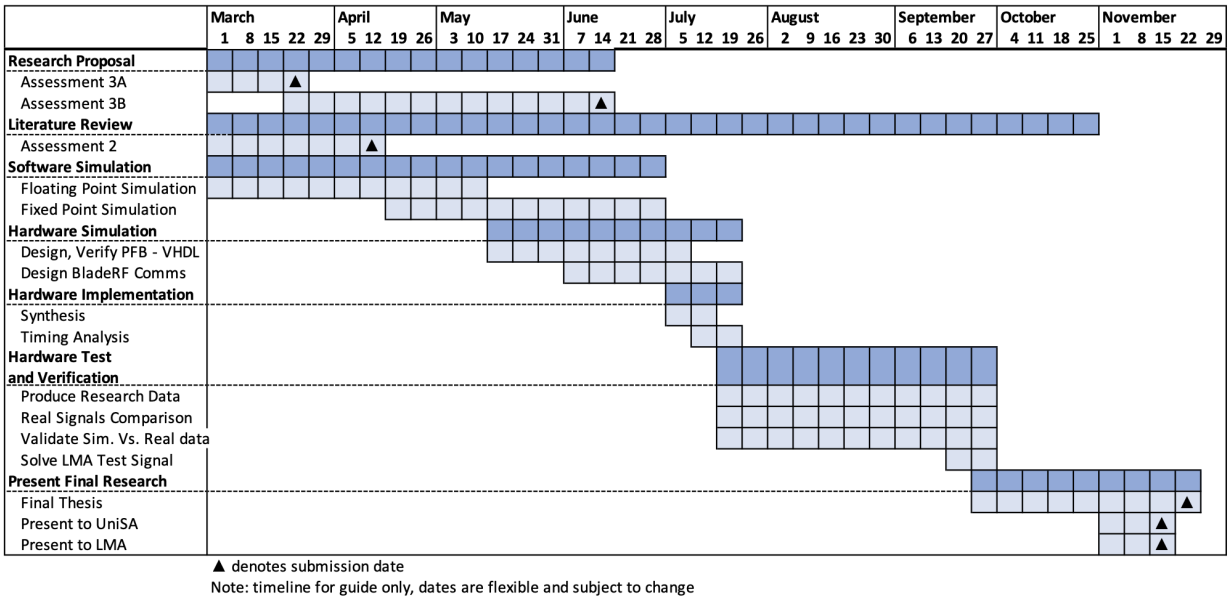

Figure 7: Proposed timeline for research project.

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