xidoo_datapath:U0

Aload	
Asel[1..0]	
IRload	
Input[7..0]	Aeq0
JMPmux	Apos
MemWr	IR[2..0]
Meminst	Output[7..0]
PCload	
Sub	
clock	
reset	

SWT[7..0]

LEDs[7..0]

CLK

RST

fsm_control:U1

	Aload
Aeq0	Asel[1..0]
Apos	Halt
Enter	IRload
clock	JMPmux
ir[2..0]	MemWr
reset	Meminst
	PCload
	Sub

Enter

Halt