STN2120

Multiprotocol OBD to UART Interpreter
Datasheet

OBD SOLUTIONS

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1.0 Overview

This datasheet summarizes the features of the STN2120 device. It is not intended as a comprehensive reference source. To complement the information in this datasheet refer to the **"STN1100 Family Reference and Programming Manual".** Please see the OBD Solutions website (www.obdsol.com) for the latest version of the STN1100 Family Reference Manual.

The STN2120 is an OBD to UART interpreter IC designed to provide bi-directional half-duplex communication with the vehicle's On-Board Diagnostic system (OBD-II). It supports all legislated OBD-II protocols, as well as two proprietary networks: GM Single Wire CAN (GMLAN), and Ford Medium Speed CAN (MS CAN).

A wealth of information can be obtained by tapping into the OBD bus, including the status of the malfunction indicator light (MIL), diagnostic trouble codes (DTCs), inspection and maintenance (I/M) information, freeze frames, VIN, hundreds of real-time parameters, and more.

The STN2120 is fully compatible with the *de facto* industry standard ELM327 command set. Based on a 16-bit processor core, the STN2120 offers more features and better performance than any other ELM327 compatible IC.

2.0 Feature Highlights

- **Stable, field-tested firmware**
- Fully **compatible with the ELM327** AT command set
- Fully **backwards compatible with the STN1110** command set
- **Extended** ST **command set**
- **UART interface** (baud rates from 62 bps to 8 Mbps[1])
- Secure **bootloader** for easy firmware updates
- Support for **all legislated OBD-II protocols:**
  - ISO 15765-4 (CAN)
  - ISO 14230-4 (Keyword Protocol 2000)
  - ISO 9141-2 (Asian, European, Chrysler vehicles)
  - SAE J1850 VPW (GM vehicles)
  - SAE J1850 PWM (Ford vehicles)
- Support for **non-legislated OBD protocols:**
  - ISO 15765
  - ISO 11898 (raw CAN)
  - GMLAN Single Wire CAN (GMW3089)
  - Ford Medium Speed CAN (MS CAN)
- Support for the heavy-duty **SAE J1939 OBD protocol**
- Superior **automatic protocol detection** algorithm
- **Large message buffer**
- Sophisticated **PowerSave Sleep/Wakeup Triggers**
- Available in **QFN** package
- **RoHS** compliant

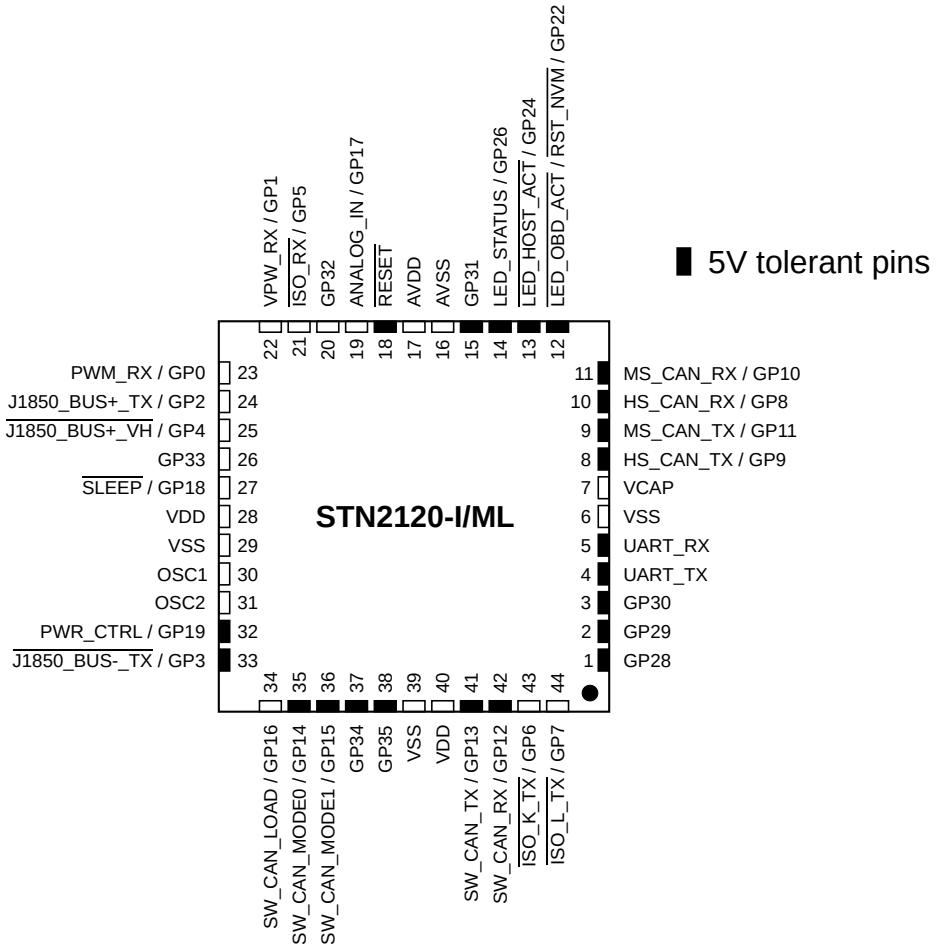
Note 1: Maximum theoretical baud rate. Actual maximum baud rate is application dependent and may be limited by driver hardware.

3.0 Typical Applications

- Vehicle telematics
- Fleet management and tracking applications
- Usage-based insurance (UBI)
- OBD data loggers
- Automotive diagnostic scan tools and code readers
- Digital dashboards

4.0 Pinout

44-Pin QFN[1]



Note 1. The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

4.1 Pinout Summary

Table 1: Pinout Summary

Pin #	Pin Name	Pin Type	Pin Description
1	GP28	5V, 8x	General purpose I/O pin
2	GP29	5V, 4x	General purpose I/O pin
3	GP30	5V, 4x	General purpose I/O pin
4	UART_TX	OD, 5V, 4x	UART transmit output
5	UART_RX	I, 5V, 4x	UART receive input
6	VSS	P	Ground reference for logic and I/O pins
7	VCAP	P	CPU logic filter capacitor connection
8	HS_CAN_TX / GP9	OD, 5V, 8x	High-speed CAN transmit output
9	MS_CAN_TX / GP11	OD, 5V, 8x	Medium-speed CAN transmit output
10	HS_CAN_RX / GP8	I, 5V, 8x	High-speed CAN receive input
11	MS_CAN_RX / GP10	I, 5V, 8x	Medium-speed CAN receive input
12	$\overline{\text{LED\_OBD\_ACT}}$ / $\overline{\text{RST\_NVM}}$ / GP22	OD/I, 5V, 4x	Active low OBD activity LED output *and* active low input to reset non-volatile settings to factory defaults
13	$\overline{\text{LED\_HOST\_ACT}}$ / GP24	O, 4x	Active low host activity LED output
14	LED_STATUS / GP26	O, 8x	Status LED output
15	GP31	5V, 8x	General purpose I/O pin
16	AVSS	P	Analog ground reference
17	AVDD	P	Analog positive supply
18	$\overline{\text{RESET}}$	I, 5V	Active low device reset input
19	ANALOG_IN / GP17	A	Analog voltage measurement input
20	GP32	4x	General purpose I/O pin
21	$\overline{\text{ISO\_RX}}$ / GP5	I, 4x	Active low ISO 9141/ISO 14230 K-line input
22	VPW_RX / GP1	I, 4x	SAE J1850 VPW receive input
23	PWM_RX / GP0	I, 4x	SAE J1850 PWM receive input
24	J1850_BUS+_TX / GP2	O, 4x	SAE J1850 Bus+ transmit output
25	$\overline{\text{J1850\_BUS+\_VH}}$ / GP4	O, 4x	SAE J1850 PWM/VPW Bus+ high voltage select output
26	GP33	4x	General purpose I/O pin
27	$\overline{\text{SLEEP}}$ / GP18	I, 4x	External sleep control input
28	VDD	P	Positive supply for logic and I/O pins
29	VSS	P	Ground reference for logic and I/O pins
30	OSC1	I	16.000 MHz oscillator crystal input
31	OSC2	O	16.000 MHz oscillator crystal output
32	PWR_CTRL / GP19	OD, 4x	External power control output
33	$\overline{\text{J1850\_BUS-\_TX}}$ / GP3	O, 4x	Active low SAE J1850 Bus- transmit output

Pin #	Pin Name	Pin Type	Pin Description
34	SW_CAN_LOAD / GP16	O, 8x	Single-wire CAN high-speed tool load enable output
35	SW_CAN_MODE0 / GP14	OD, 8x	Single-wire CAN transceiver operating mode selection output 0
36	SW_CAN_MODE1 / GP15	OD, 8x	Single-wire CAN transceiver operating mode selection output 1
37	GP34	5V, 4x	General purpose I/O pin
38	GP35	5V, 4x	General purpose I/O pin
39	VSS	P	Ground reference for logic and I/O pins
40	VDD	P	Positive supply for logic and I/O pins
41	SW_CAN_TX / GP13	OD, 4x	Single-wire CAN transmit output
42	SW_CAN_RX / GP12	I, 5V, 4x	Single-wire CAN receive input
43	$\overline{\text{ISO\_K\_TX}}$ / GP6	O, 8x	Active low ISO 9141/ISO 14230 K-line output
44	$\overline{\text{ISO\_L\_TX}}$ / GP7	O, 8x	Active low ISO 9141/ISO 14230 L-line output
PAD		–	Thermal pad

Legend:

I	– Schmitt trigger input with CMOS levels	O	– digital output	4x	– 4x source/sink driver
A	– analog input	OD	– open drain output	8x	– 8x source/sink driver
P	– power pin	5V	– 5 volt tolerant pin		

4.2 Detailed Pin Descriptions

ANALOG_IN

Analog voltage measurement input (AVDD max). By default, this input is calibrated for an external 62 kΩ/10 kΩ voltage divider connected to battery positive. Connect to AVSS if unused.

AVDD

Analog positive supply. Must be connected to VDD or an external voltage reference (between VDD - 0.3V or 3.0V, whichever is greater and VDD + 0.3V or 3.6V, whichever is less). AVDD may be decoupled from digital supply by connecting it to VDD via a 10 Ω resistor or a small (10 µH – 47 µH) inductor.

AVSS

Analog ground reference. Must be connected to analog "clean" ground (between VSS - 0.3V and VSS + 0.3V) or VSS.

GPx

General purpose pins. Can be configured as output or input, open-drain, and can have internal pull-ups or pull-downs. If configured for open-drain, do not leave floating. Connect to VSS if unused.

HS_CAN_RX

High-speed CAN receive input. Compatible with 3.3V and 5V logic. Pull up to VDD if unused.

HS_CAN_TX

High-speed CAN transmit output. Open drain – requires a pull-up to VDD or 5V. This pin has an 8x current rating (see Table 6 "Output Pin DC Specifications"). Pull-up value depends on CAN baud rates used and the trace length (higher resistor values can be used with lower baud rates and shorter traces); recommended value is 1 kΩ. Pull up to VDD via 100 kΩ resistor if unused.

$\overline{\text{ISO\_K\_TX}}$

Active low ISO 9141/ISO 14230 K-line output. When the pin is logic high, K-line should be low. This pin has an 8x current rating (see Table 6 "Output Pin DC Specifications"). Leave unconnected if unused.

$\overline{\text{ISO\_L\_TX}}$

Active low ISO 9141/ISO 14230 L-line output. When the pin is logic high, L-line should be low. This pin has an 8x current rating (see Table 6 "Output Pin DC Specifications"). Leave unconnected if unused.

$\overline{\text{ISO\_RX}}$

Active low ISO 9141/ISO 14230 K-line receive input. When K-line is high (recessive), this pin should be at a logic low level. Connect to VSS if unused.

J1850_BUS+_TX

SAE J1850 Bus+ transmit output. When the pin is high, Bus+ should be high (dominant). This pin has a 4x current rating (see Table 6 "Output Pin DC Specifications"). Leave unconnected if unused.

$\overline{\text{J1850\_BUS-\_TX}}$

Active low SAE J1850 Bus- transmit output. When the pin is high, Bus- should be low (dominant). This pin has a 4x current rating (see Table 6 "Output Pin DC Specifications"). Leave unconnected if unused.

$\overline{\text{J1850\_BUS+\_VH}}$

The firmware uses this pin to control the voltage level of the SAE J1850 PWM/VPW Bus+ supply. When the PWM protocol is selected, it outputs a logic high to switch the supply voltage to a nominal 5V. When the VPW protocol is selected, it outputs a logic low to switch the supply voltage to a nominal 8V. This pin has a 4x current rating (see Table 6 "Output Pin DC Specifications"). Leave unconnected if unused.

$\overline{\text{LED\_HOST\_ACT}}$

Active low host activity LED output. This pin has a 4x current rating (see Table 6 "Output Pin DC Specifications"). Leave unconnected if unused.

$\overline{\text{LED\_OBD\_ACT}}$ / $\overline{\text{RST\_NVM}}$

Active low OBD activity LED output and active low input to reset NVM to factory defaults. This pin has a 4x current rating (see Table 6 "Output Pin DC Specifications"). Must be pulled up to VDD via a 100 kΩ resistor for proper device operation.

LED_STATUS

Status LED output. This pin will output constant high when the device is running and will output low with 5 ms high pulses every 3 seconds when in sleep mode. This pin has an 8x current rating (see Table 6 “Output Pin DC Specifications”). Leave unconnected if unused.

MS_CAN_RX

Medium-speed CAN receive input. Compatible with 3.3V and 5V logic. Pull up to VDD if unused.

MS_CAN_TX

Medium-speed CAN transmit output. Open drain – requires a pull-up to VDD or 5V. Pull-up resistor value depends on CAN baud rates used and the trace length (higher resistor values can be used with lower baud rates and shorter traces); recommended value is 1 kΩ (1.5 kΩ, if pulled up to 5V). This pin has an 8x current rating (see Table 6 “Output Pin DC Specifications”). Pull up to VDD via 100 kΩ resistor if unused.

OSC1, OSC2

16.000 MHz oscillator crystal connection.

PAD

The metal plane on the bottom of the device (QFN package only). It is not connected to any pins internally. Connect to VSS externally.

PWM_RX

SAE J1850 PWM receive input. When the SAE J1850 bus is in the recessive state (Bus+ is low, Bus- is high), this pin should be at a logic low level. When the SAE J1850 bus is in the dominant (Bus+ is high) state, this pin should be at a logic high level. Connect to VSS if unused.

PWR_CTRL

External power control output. Used to switch external circuitry into low-power (sleep) state. Polarity can be configured in firmware; default configuration is active high (logic low = sleep mode). Open drain – requires a pull-up to VDD or 5V; be mindful of the fact that the pull-up will draw current in low-power state. This pin has a 4x current rating (see Table 6 “Output Pin DC Specifications”). Pull down to VSS via 100 kΩ resistor if unused.

$\overline{\text{RESET}}$

Device reset input. A logic low pulse (min 2 µs) on this pin will reset the device. Apply a continuous logic low to hold the device in reset. If your circuit does not use this functionality, pull up this pin to VDD.

$\overline{\text{SLEEP}}$

External sleep control input. When enabled in firmware, puts the device into low-power sleep mode. Polarity of this pin can be configured in firmware; default configuration is active low. Pull up to VDD if unused.

SW_CAN_LOAD

Single-wire CAN high-speed tool load enable output. The pin outputs logic high when high-speed tool load is enabled via the STCSWM command. This pin has an 8x current rating (see Table 6 “Output Pin DC Specifications”). Leave unconnected if unused.

SW_CAN_MODE0, SW_CAN_MODE1

Single-wire CAN transceiver operating mode selection outputs. Connect to MODE0, MODE1 pins of a single-wire CAN transceiver IC. Open drain – require pull-ups to VDD or 5V; recommended value is 10 kΩ. These pins have 8x current ratings (see Table 6 “Output Pin DC Specifications”). Both pins are driven low in sleep mode – it is recommended to pull up to a switched power to reduce power consumption during sleep. Leave unconnected if unused.

SW_CAN_RX

Single-wire CAN receive input. Compatible with 3.3V and 5V logic. Pull up to VDD if unused.

SW_CAN_TX

Single-wire CAN transmit output. Open drain – requires a pull-up to VDD or 5V. Pull-up resistor value depends on CAN baud rates used and the trace length (higher resistor values can be used with lower baud rates and shorter traces); recommended value is 1 kΩ (1.5 kΩ, if pulled up to 5V). This pin has a 4x current rating (see Table 6 “Output Pin DC Specifications”). Pull up to VDD via 100 kΩ resistor if unused.

UART_RX

UART receive input. Compatible with 3.3V and 5V logic.

UART_TX

UART transmit output. Open drain – requires a pull-up to VDD or 5V. This pin has a 4x current rating (see Table 6 “Output Pin DC Specifications”). Pull-up value depends on UART baud rate and the trace length (higher resistor values can be used with lower baud rates and shorter traces); typical value is 1 kΩ (1.5 kΩ, if pulled up to 5V).

VCAP

CPU logic filter capacitor connection. Connect to a low-ESR (< 1 Ω) tantalum or ceramic capacitor. Minimum value is 4.7 µF; typical value is 10 µF.

VDD

Positive 3.0 – 3.6V supply for logic and I/O pins.

VPW_RX

SAE J1850 VPW receive input. When the SAE J1850 Bus+ is in the recessive (low) state, this pin should be at a logic low level. When the SAE J1850 Bus+ is in the dominant (high) state, this pin should be at a logic high level. Connect to VSS if unused.

VSS

Ground reference for logic and I/O pins.

5.0 Guidelines for Getting Started with STN2120

5.1 Basic Connection Requirements

Getting started with the STN2120 IC requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names, which must always be connected:

- All **VDD and Vss** pins (see Section 5.2 “Decoupling Capacitors”)
- **AVDD and AVss** pins (see Section 5.2 “Decoupling Capacitors” and Section 5.3 “AVDD and AVSS Pins”)
- **VCAP** (see Section 5.4 “Internal Voltage Regulator Filter Capacitor”)
- $\overline{\textbf{RESET}}$ pin (see Section 5.5 “Device Reset Pin”)
- **OSC1 and OSC2** pins (see Section 5.6 “Oscillator Pins”)
- $\overline{\textbf{RST\_NVM}}$ pin (see Section 5.7 “NVM Reset Input”)
- **Open Drain Output Pull-ups** (see Section 5.8 “Open Drain Outputs”)

5.2 Decoupling Capacitors

You must use decoupling capacitors on every pair of power supply pins, such as VDD, VSS and AVDD, AVSS. Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** Recommendation of 1 µF, 10-20V. This capacitor should be a low-ESR and have resonance frequency in the range of 20 MHz and higher. It is recommended that ceramic capacitors be used.
- **Placement on the printed circuit board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended to place the capacitors on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within ¼” (6 mm) in length.
- **Handling high frequency noise:** If the board is experiencing high frequency noise, upward of tens of MHz, add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 µF to 0.001 µF. Place this second capacitor next to the primary decoupling capacitor.
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum thereby reducing PCB track inductance.

5.2.1 Tank Capacitors

On boards with power traces running longer than six inches in length, use a tank capacitor for integrated circuits, including the STN2120, to supply a local power source. The value of the tank capacitor should be determined based on the trace resistance that connects the power supply source to the device, and the maximum current drawn by the device in the application. In other words, select the tank capacitor so that it meets the acceptable voltage sag at the device. Typical values range from 4.7 µF to 47 µF.

5.3 AVDD and AVSS Pins

As a minimum, AVDD must be connected directly to VDD and AVSS must be connected directly to VSS.

It is recommended that AVDD be connected to to VDD via a 10 Ω resistor or a small (10 µH – 47 µH) inductor.

AVSS should be connected to the electrically cleanest ground net (plane). For best results, analog circuitry should have a separate ground plane with a point connection to VSS ground plane as close as possible to the AVSS pin.

5.4 Internal Voltage Regulator Filter Capacitor

A low-ESR (< 1 Ω) capacitor is required on the VCAP pin, which is used to stabilize the internal voltage regulator output voltage. The VCAP pin must not be connected to VDD, and must have a capacitor between 4.7 µF and 10 µF, 16V connected to ground. The type can be ceramic or tantalum. Refer to Section 7.2 “Electrical Characteristics” for additional information. The placement of this capacitor should be close to the VCAP pin. It is recommended that the trace length not exceed ¼” (6 mm).

5.5 Device Reset Pin

$\overline{\text{RESET}}$ pin must be logic high for STN2120 to run. If this pin is not controlled by the host controller, it must be connected to VDD.

It is recommended to pull up $\overline{\text{RESET}}$ pin to VDD via a 10 kΩ resistor.

5.6 Oscillator Pins

The oscillator circuit should be placed on the same side of the board as the device. Also, place the oscillator circuit close to the oscillator pins, not exceeding one-half inch (12 mm) distance between them. The load capacitors should be placed next to the oscillator itself, on the same side of the board. Use a grounded copper pour around the oscillator circuit to isolate them from surrounding circuits. The grounded copper pour should be routed directly to the STN2120 ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed.

5.7 NVM Reset Input

$\overline{\text{RST\_NVM}}$ pin must be pulled up to V_{DD} via a 100 kΩ resistor for proper device operation.

5.8 Open Drain Outputs

All open drain outputs (as specified in section 4.1) that are in use must be pulled up to V_{DD} or 5V. Specifically, UART_TX pin must be pulled up in order to be able to communicate with the device. See section 4.2 “Detailed Pin Descriptions” for more information.

5.9 Unused Inputs and Unused Open Drain Outputs

None of the unused inputs or unused open drain outputs (as specified in section 4.1) should be left unconnected. The STN2120 is a CMOS integrated circuit. Leaving any of its inputs or open drain outputs floating may result in IC damage.

Unused open drain outputs can only be terminated with a resistor connected to V_{DD} or 5V. Unused inputs can be terminated via a resistor or direct connection to V_{SS} or V_{DD}.

Unused inputs and open drain outputs should be connected as shown in Table 2. See section 4.2 “Detailed Pin Descriptions” and section 6.1 “Recommended Minimum Connection” for more information.

Table 2: Recommended Unused Input and Open Drain Output Connections

Pin Number	Pin Name	Level
1	GP28	L(5)
2	GP29	L(5)
3	GP30	L(5)
4	UART_TX	H(2)
5	UART_RX	H
8	HS_CAN_TX	H(2)
9	MS_CAN_TX	H(2)
10	HS_CAN_RX	H
11	MS_CAN_RX	H
12	$\overline{\text{LED\_OBD\_ACT}}$ / $\overline{\text{RST\_NVM}}$	H(2)
15	GP31	L(5)
18	$\overline{\text{RESET}}$	H
19	ANALOG_IN	L(1)
20	GP32	L(5)
21	$\overline{\text{ISO\_RX}}$	L(1)
22	VPW_RX	L(1)
23	PWM_RX	L(1)
26	GP33	L(5)
27	$\overline{\text{SLEEP}}$	H
32	PWR_CTRL	L(3)
35	SW_CAN_MODE0	—(4)
36	SW_CAN_MODE1	—(4)
37	GP34	L(5)
38	GP35	L(5)
41	SW_CAN_TX	H(2)
42	SW_CAN_RX	H

Note 1. These inputs may be connected to either V_{DD} or V_{SS}. However, the preferred level is shown.

2. These open drain outputs cannot be connected to V_{DD} directly. They can only be connected to V_{DD} or 5V via a resistor.

3. This open drain output should not be connected to V_{SS} directly. For reduced current consumption during sleep, when unused, this output should be connected to V_{SS} via a resistor.

4. These open drain outputs are driven low when the single-wire CAN channel is not selected. Therefore, they can be left unconnected if single wire CAN is not used.

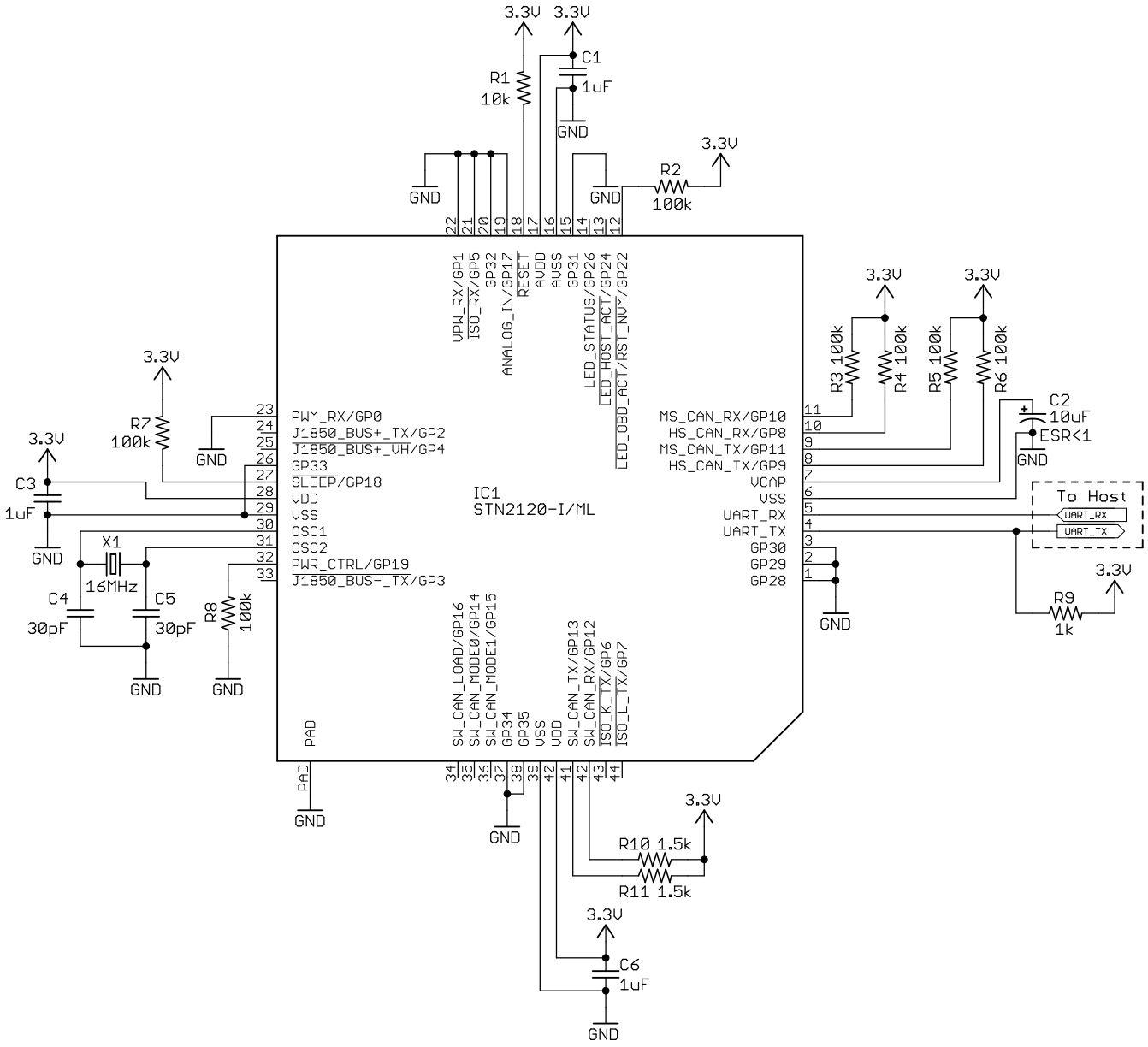
5. General purpose I/O pins are configured as inputs by default. When unused, these inputs may be connected to either V_{DD} or V_{SS}.

6.0 Reference Schematics

6.1 Recommended Minimum Connection

Figure 1 shows the recommended minimum of components necessary to get the STN2120 to operate reliably, while minimizing power consumption. It is not a practical circuit; it is intended as a reference to show what to do with unused pins. Refer to the detailed pin descriptions (section 4.2) for more information.

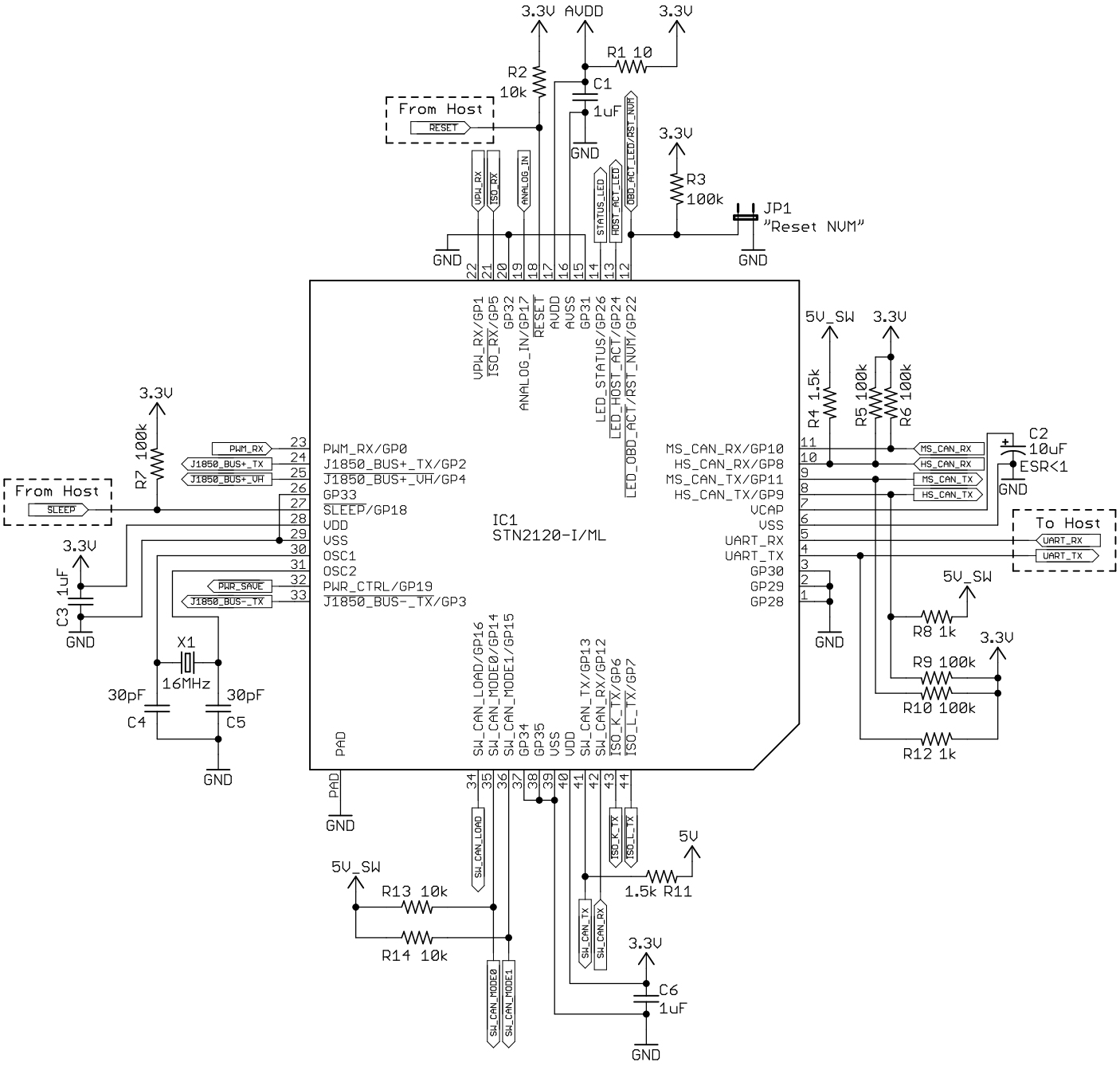
Figure 1 – Recommended Minimum Connection



6.2 Typical Configuration

This section contains schematics showing the typical configuration for the various circuit blocks. Pay special attention when choosing substitutes for components with specific part numbers, to make sure they have the same or better characteristics. Components without specific part numbers are generic. Use good engineering practices and common sense to make sure the specific parts you choose are appropriate for your application.

Figure 2 – STN2120 IC



Important: Connect the voltage sense before the protection/filter circuitry. D1, D3, R15, and the internal diode should protect the IC, if there is a voltage spike.

Figure 3 – Voltage Sense

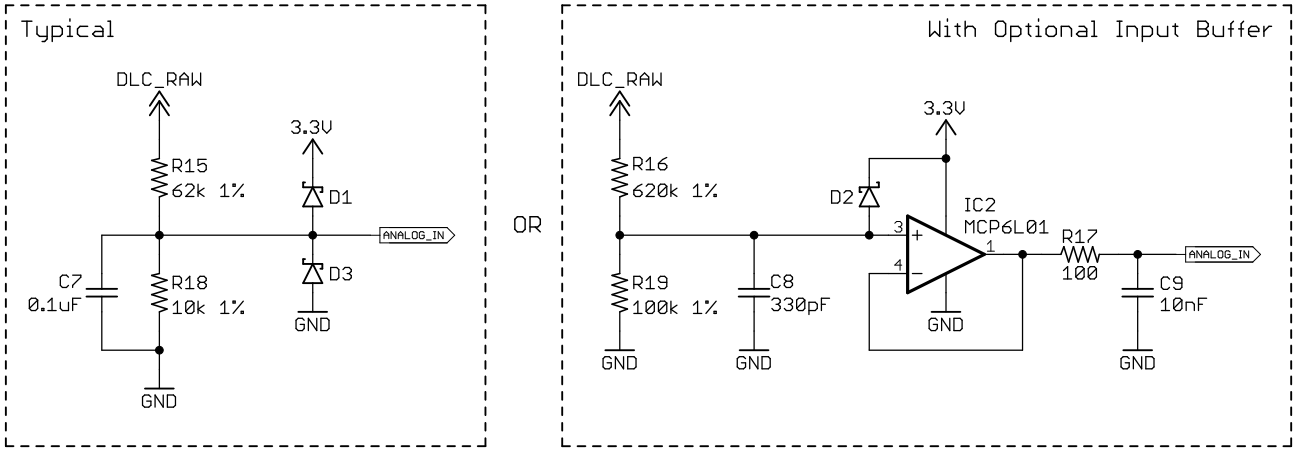


Figure 4 – LEDs

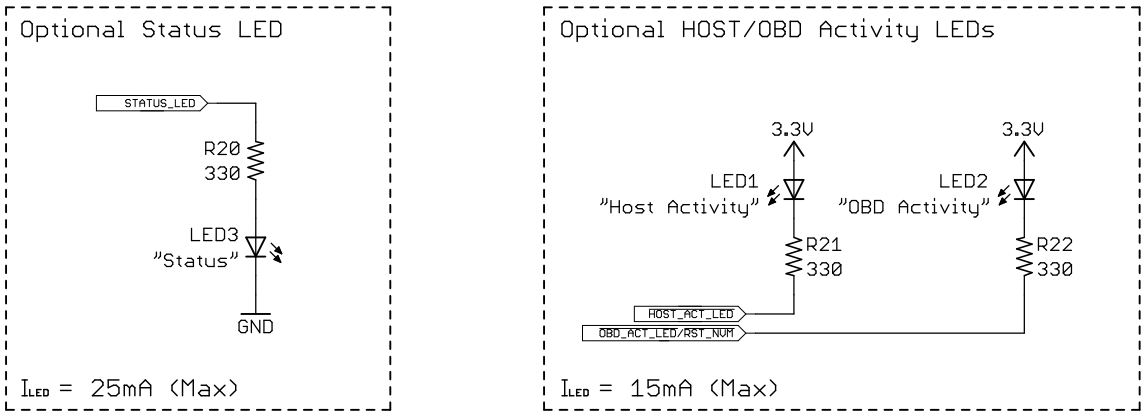


Figure 5 – OBD Port Connector

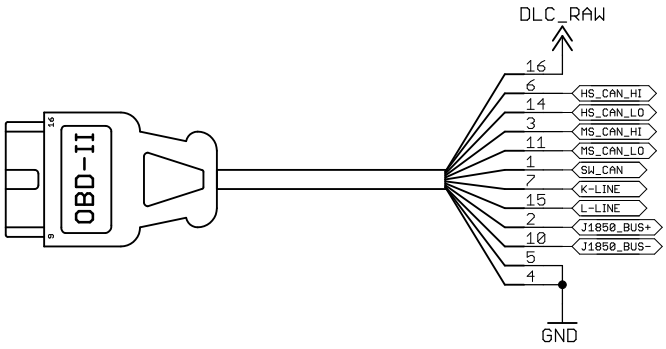


Figure 6 – Over-Voltage Protection

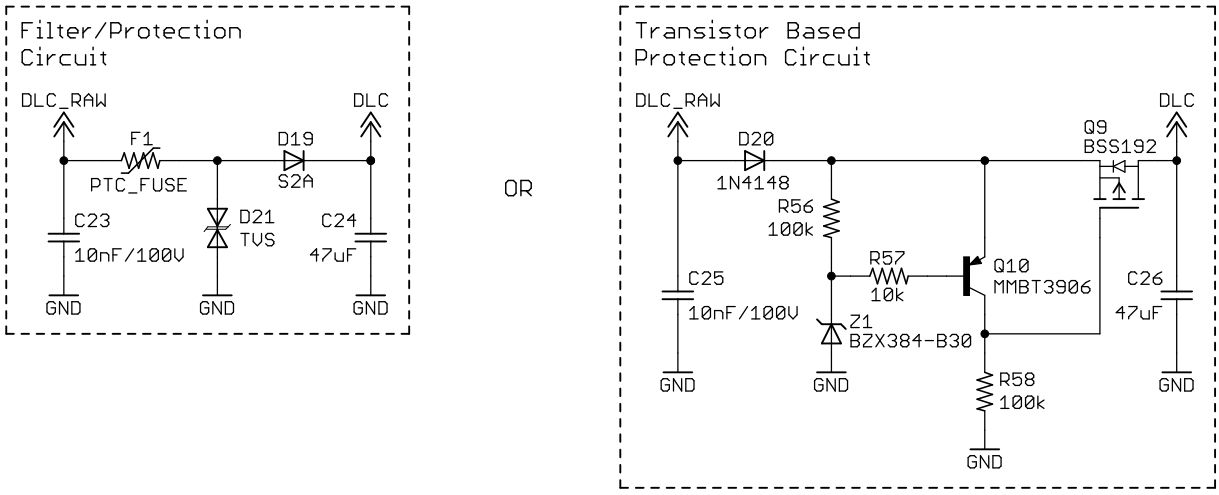


Figure 7 – Power Supplies

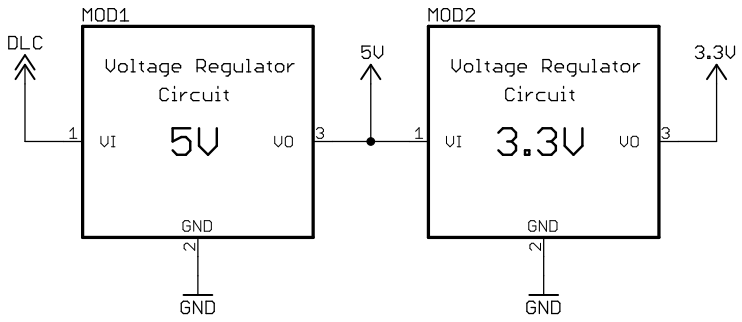


Figure 8 – Switched Power Control

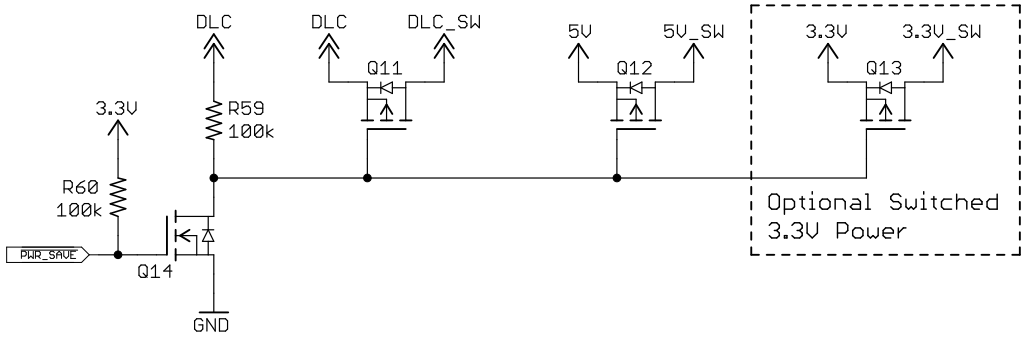


Figure 9 – ISO 9141/ISO 14230 Transceiver

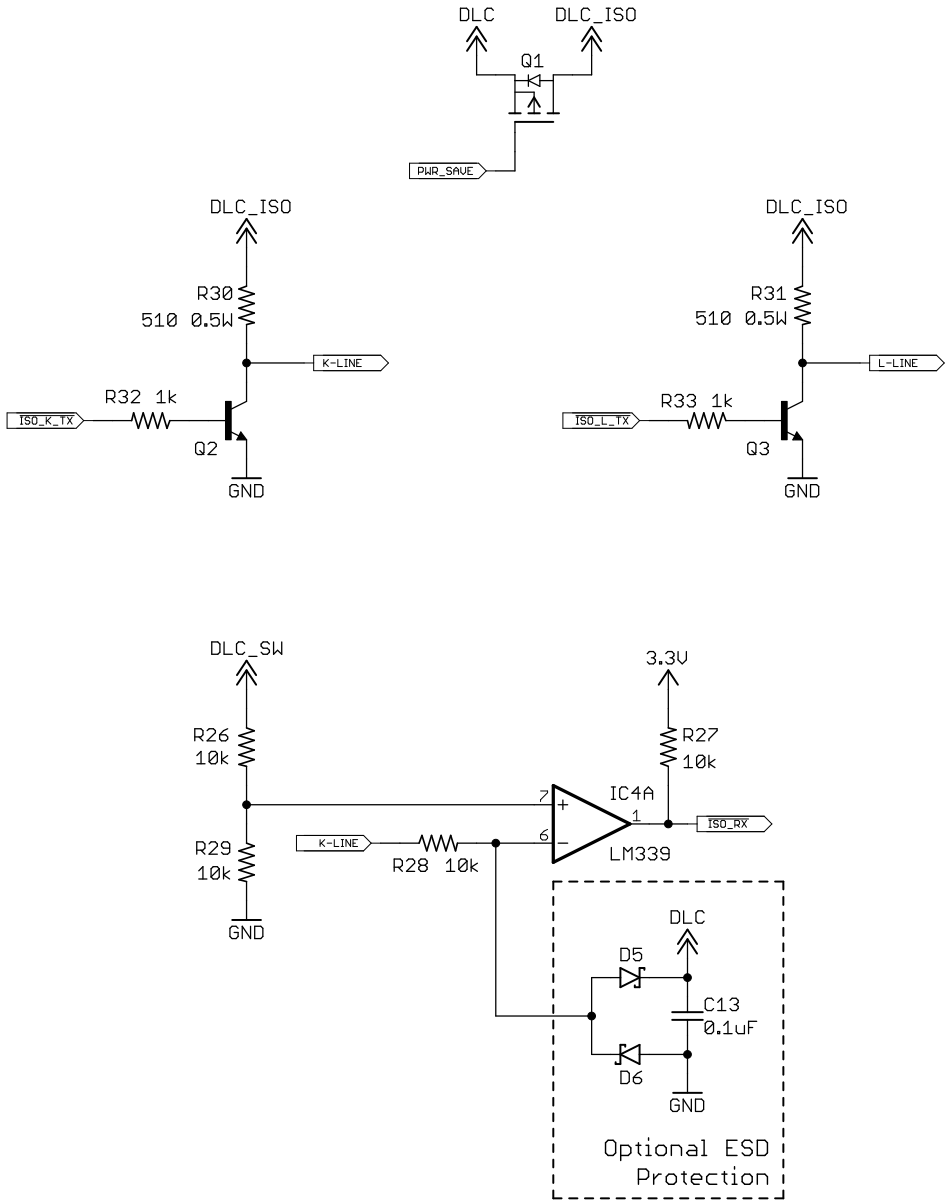


Figure 10 – High Speed CAN Transceiver

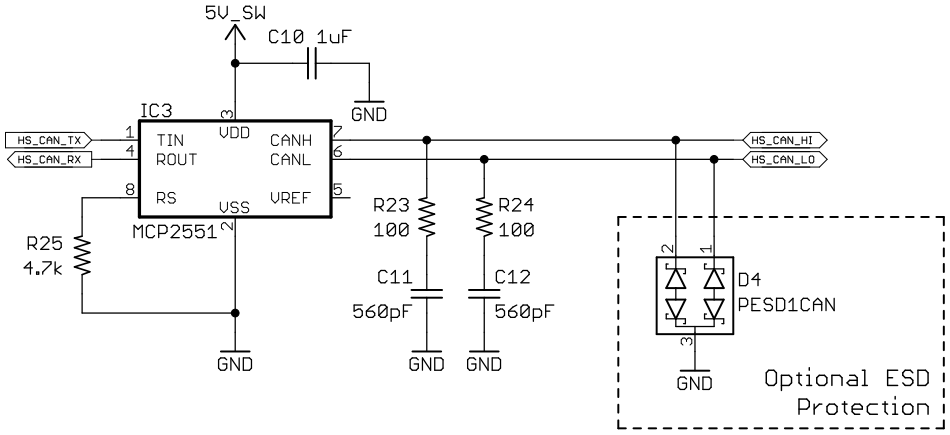


Figure 11 – Medium Speed CAN Transceiver

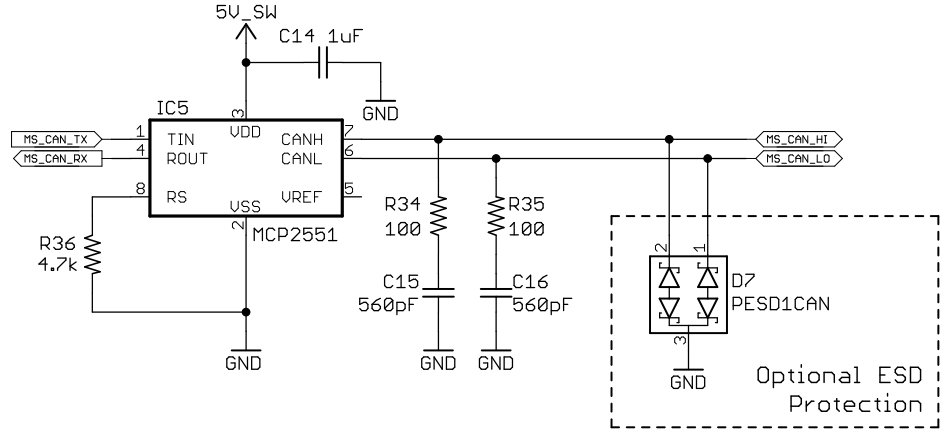
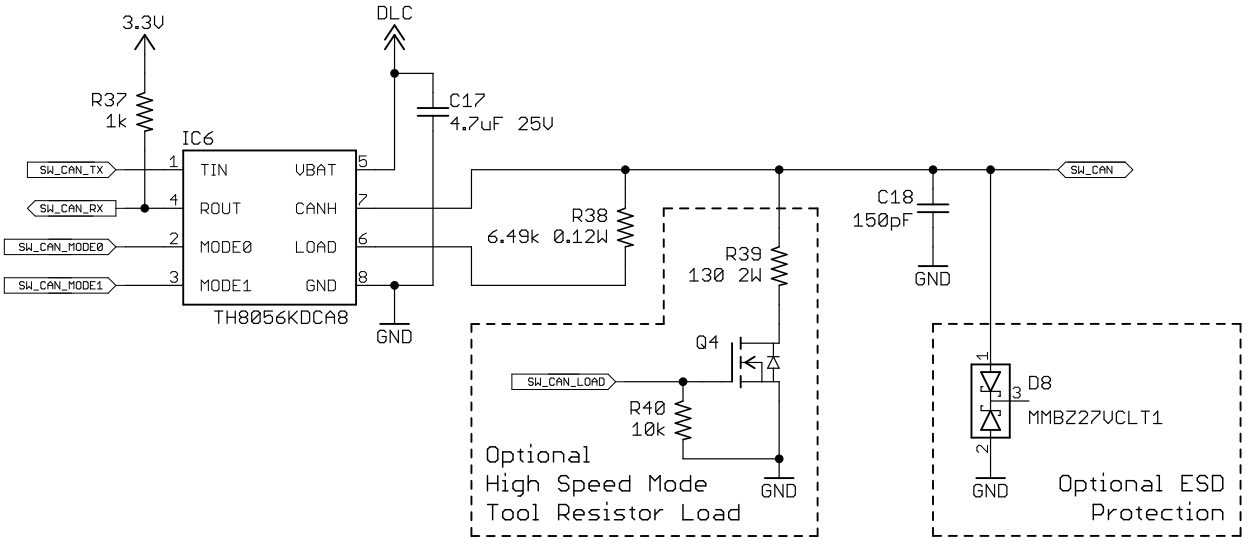
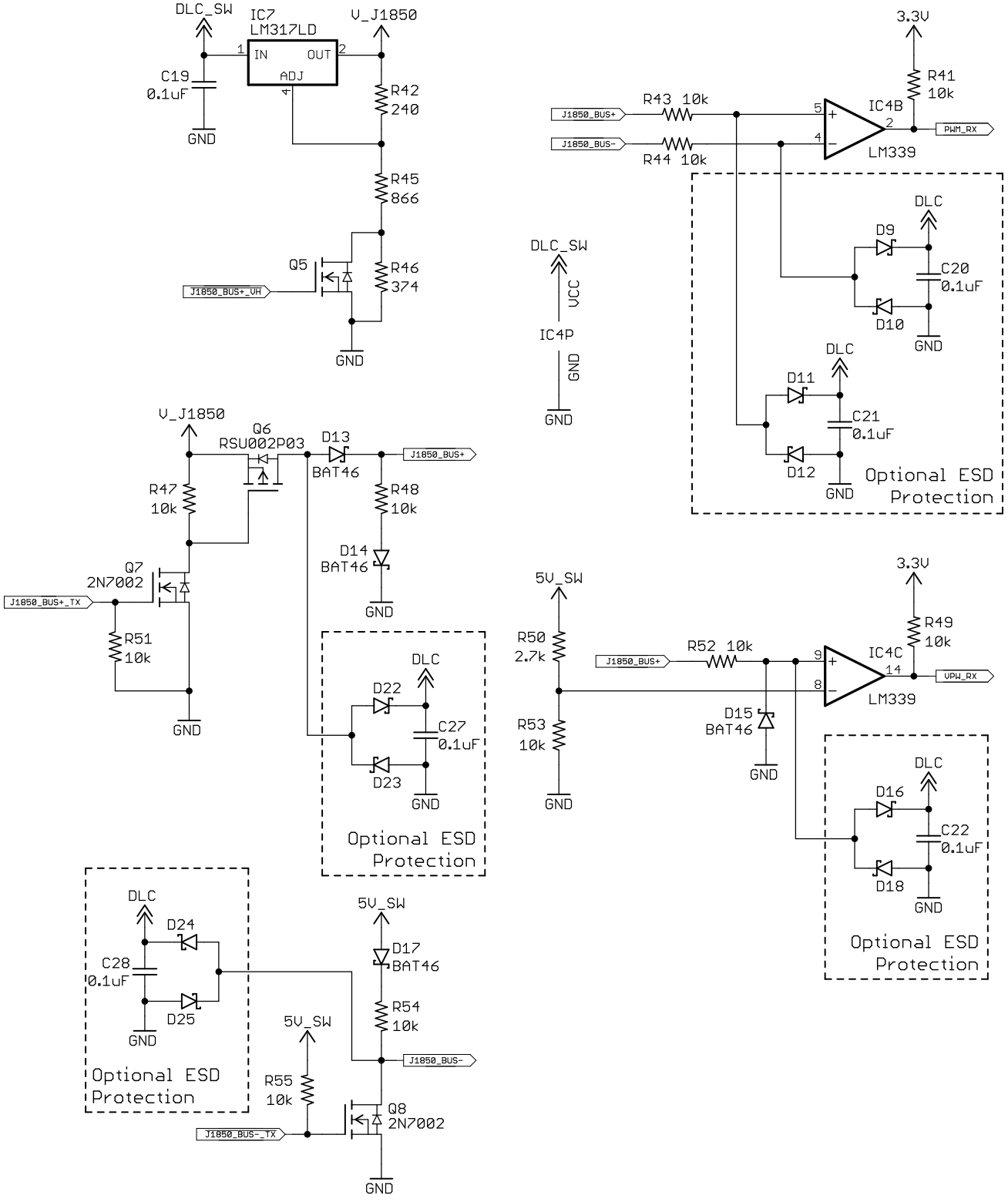


Figure 12 – Single Wire CAN Transceiver



Important: Q6, Q7, and Q8 can only be substituted with transistors that have the same or better switching characteristics. OK to substitute fast-switching silicon diodes (e.g., 1N4148) for D13, D14, and D17. Also, note that the comparator IC4 is powered from DLC_SW to ensure signals remain within its common mode range.

Figure 13 – SAE J1850 Transceiver



7.0 Electrical Characteristics

This section provides an overview of the STN2120 electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

The STN2120 is based on the dsPIC33EP256GP504 device from Microchip Technology. For more detailed device specifications or clarification, refer to Microchip documentation, available at http://www.microchip.com.

7.1 Absolute Maximum Ratings (1)

Ambient temperature under bias ..... -40°C to +125°C
Storage temperature ..... -65°C to +150°C
Voltage on V_{DD} with respect to Vss ..... -0.3V to +4.0V
Voltage on any pin that is not 5V tolerant with respect to V_{SS}(2) ..... -0.3V to (V_{DD} + 0.3V)
Voltage on any 5V tolerant pin with respect to V_{SS} when $V_{DD} \geq 3.0V$(2) ..... -0.3V to +5.5V
Voltage on any 5V tolerant pin with respect to V_{SS} when $V_{DD} < 3.0V$(2) ..... -0.3V to 3.6V
Maximum current out of V_{SS} pin ..... 300 mA
Maximum current into V_{DD} pin ..... 300 mA
Maximum current sourced/sunk by any 4x output(3) ..... 15 mA
Maximum current sourced/sunk by any 8x output(3) ..... 25 mA
Maximum current sunk by all outputs ..... 200 mA

Note **1.** Stresses beyond those listed here can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods can affect device reliability.

2. See section 4.0 “Pinout” for the list of 5V tolerant pins.

3. See section 4.1 “Pinout Summary” to determine current rating of individual pins.

7.2 Electrical Characteristics

Table 3: Thermal Operating Conditions

Sym	Characteristic	Min	Typ	Max	Units	Conditions
T_J	**Operating Junction Temperature**	-40	—	+85	°C	
T_A	**Operating Ambient Temperature**	-40	—	+85	°C	

Table 4: Power Specifications

Sym	Characteristic	Min	Typ(1)	Max	Units	Conditions
V_{DD}	**Supply Voltage**	3.0	—	3.6	V	
V_{POR}	**V_{DD} Start Voltage** to ensure internal power-on reset (POR) signal	—	—	V_{SS}	V	
S_{VDD}	**V_{DD} Rise Rate(2)** to ensure internal power-on reset (POR) signal	0.03	—	—	V/ms	0V–1.0V in 0.1s
AV_{DD}	**Analog Supply Voltage**	Greater of V_{DD} – 0.3 or 3.0	—	Lesser of V_{DD} + 0.3 or 3.6	V	

Sym	Characteristic	Min	Typ(1)	Max	Units	Conditions
AVSS	**Analog Ground Reference**	VSS – 0.3	—	VSS + 0.3	V	
VBOR	**Brown-out Reset Voltage**(3) on VDD transition high-to-low	2.65(3)	—	2.95	V	
IDD	**Operating Current**(4)	—	42	63(5)	mA	
IPD	**Average Sleep Current**(4,6)	—	130	265(5)	µA	TA = +25°C
		—	450(5)	800(5)	µA	TA = +85°C
CEFC	**External Filter Capacitor**(7) connected to VCAP pin	4.7	10	—	µF	ESR < 1 Ω

Note
1. Data in Typ column is at 3.3V, 25°C, unless otherwise stated.
2. This spec must be met in order to ensure that a correct internal power-on reset (POR) occurs. It is easily achieved using most common types of supplies, but may be violated if a supply with slowly varying voltage is used, as may be obtained through direct connection to solar cells or some charge pump circuits.
3. This parameter is for design guidance only and is not tested in manufacturing.
4. STN2120 device current only. Does not include any load currents.
5. Values are characterized, but not tested.
6. All wakeup triggers are on and wakeup trigger inputs are in their inactive states.
7. Typical VCAP voltage = 1.8V when VDD ≥ VDDMIN.

Table 5: Input Pin DC Specifications

Sym	Characteristic	Min	Typ	Max	Units	Conditions
VIL	**Input Low Voltage**(3)					
	PWR_CTRL, $\overline{\text{J1850\_BUS-\_TX}}$, GP34, and GP35	VSS	—	0.3 VDD	V	
	All other inputs	VSS	—	0.2 VDD	V	
VIH	**Input High Voltage**					
	non-5V tolerant pins(1)	0.8 VDD	—	VDD	V	
	5V tolerant pins(1)	0.8 VDD	—	5.5	V	
IIPU	**Internal Pull-up Current**	150	250	550	µA	VDD = 3.3V, VPIN = VSS
IIPD	**Internal Pull-down Current**	20	50	100	µA	VDD = 3.3V, VPIN = VDD
VIN	**ANALOG_IN Input Voltage**	AVSS	—	AVDD	V	
RIN	**Recommended ANALOG_IN Voltage Source Impedance**	—	—	200	Ω	
IICL	**Input Low Injection Current**	0	—	-5(3,6)	mA	All pins, except VDD, VSS, AVDD, AVSS, $\overline{\text{RESET}}$, VCAP, and $\overline{\text{ISO\_K\_TX}}$ / GP6
IICH	**Input High Injection Current**	0	—	+5(4,5,6)	mA	All pins, except VDD, VSS, AVDD, AVSS, $\overline{\text{RESET}}$, VCAP, $\overline{\text{ISO\_K\_TX}}$ / GP6 and all 5V tolerant pins
ΣIICT	**Total Input Injection Current** sum of all I/O and control pins	-20(7)	—	+20(7)	mA	Absolute instantaneous sum of all ± input injection currents from all I/O pins (|IICL| + |IICH|) ≤ ΣIICT

Note
1. See section 4.0 “Pinout” for the list of 5V tolerant pins.
2. Negative current is defined as current sourced by the pin.
3. V_{IL} source < (V_{SS} – 0.3). Characterized, but not tested.
4. Non-5V tolerant pins: V_{IH} source > (V_{DD} + 0.3), 5V tolerant pins: V_{IH} source > 5.5V. Characterized, but not tested.
5. Digital 5V tolerant pins cannot tolerate any “positive” input injection current from input sources > 5.5V.
6. Non-zero injection currents can affect the ADC results by approximately 4-6 counts.
7. Any number and/or combination of inputs listed under I_{ICL} or I_{ICH} conditions are permitted, provided the mathematical “absolute instantaneous” sum of the input injection currents from all pins does not exceed the specified limit. Characterized, but not tested.

Table 6: Output Pin DC Specifications

Sym	Characteristic	Min	Typ	Max	Units	Conditions V_{DD} = 3.3V, -40°C ≤ T_A ≤ +85°C
V_{OL}	**Output Low Voltage**(1)					
	4x Sink Driver Pins(2)	—	—	0.4	V	I_{OL} ≤ 6 mA
	8x Sink Driver Pin(2)	—	—	0.4	V	I_{OL} ≤ 12 mA
V_{OH}	**Output High Voltage**(1)					
	4x Source Driver Pins(2)	2.4	—	—	V	I_{OH} ≥ -10 mA
	8x Source Driver Pin(2)	2.4	—	—	V	I_{OH} ≥ -15 mA
V_{OH1}	**Output High Voltage**(1)					
	4x Source Driver Pins(2)	1.5	—	—	V	I_{OH} ≥ -14 mA
		2.0	—	—	V	I_{OH} ≥ -12 mA
		3.0	—	—	V	I_{OH} ≥ -7 mA
	8x Source Driver Pin(2)	1.5	—	—	V	I_{OH} ≥ -22 mA
		2.0	—	—	V	I_{OH} ≥ -18 mA
		3.0	—	—	V	I_{OH} ≥ -10 mA

Note
1. Parameters are characterized, but not tested.
2. See section 4.1 “Pinout Summary” for the output driver current rating designations.

Table 7: I/O Pin Timing Requirements

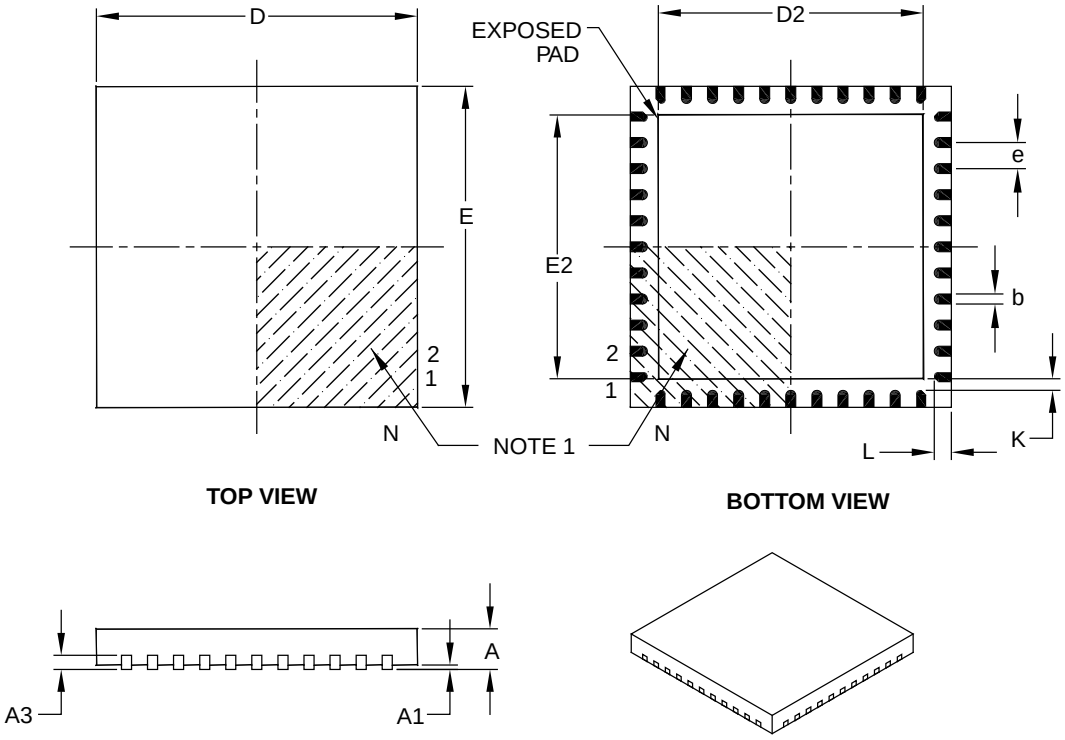
Sym	Characteristic	Min	Typ	Max	Units	Conditions
T_{RST}	**$\overline{\text{RESET}}$ Pulse Width** (low)	2	—	—	µs	
T_{UWM}	**Minimum UART Rx Pulse Width** required for wakeup (user settable)	—	20	—	ns	user setting < 15
		15	—	65,534	µs	user setting ≥ 15
T_{STM}	**Minimum $\overline{\text{SLEEP}}$ Input Time** to stay high before wakeup (user settable)	—	15	—	µs	user setting = 0
		1	—	65,534	ms	user setting > 0

8.0 Packaging Diagrams and Parameters

8.1 QFN (ML) Package

44-Lead Plastic Quad Flat, No Lead Package – 8x8 mm Body

For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		44	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		8.00 BSC	
Exposed Pad Width	E2	6.25	6.45	6.60
Overall Length	D		8.00 BSC	
Exposed Pad Length	D2	6.25	6.45	6.60
Contact Width	b	0.20	0.30	0.35
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	—	—

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

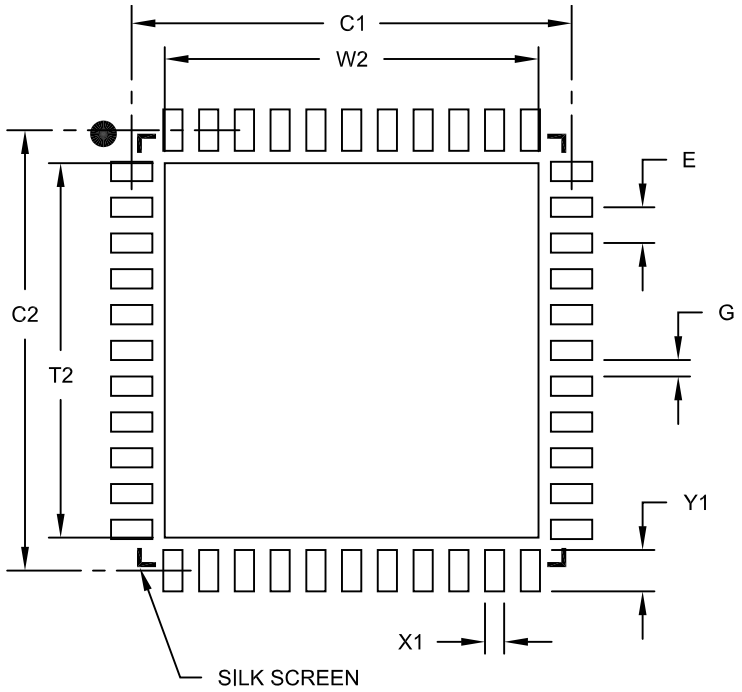
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-103C

8.2 QFN (ML) Land Pattern

44-Lead Plastic Quad Flat, No Lead Package – 8x8 mm Body

For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Optional Center Pad Width	W2	—	—	6.60
Optional Center Pad Length	T2	—	—	6.60
Contact Pad Spacing	C1	—	8.00	—
Contact Pad Spacing	C2	—	8.00	—
Contact Pad Width (x44)	X1	—	—	0.35
Contact Pad Length (x44)	Y1	—	—	0.85
Distance Between Pads	G	0.25	—	—

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2103B

9.0 Ordering Information

TA	Package		Part Number	SKU
-40°C to +85°C	QFN (ML)	Tube	STN2120-I/ML	366201

Appendix A: Revision History

Revision A (October 28, 2015)

Initial release of this document.

Appendix B: Contact Information

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