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Escuela Técnica Superior de Ingenieros de Telecomunicación



MsC. ELECTRONIC SYSTEMS ENGINEERING

MASTER'S DEGREE THESIS

**ANALYSIS & DESIGN OF MEMORY CELLS
HARDENED AGAINST RADIATION**

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TITLE: Analysis and Design of Memory Cells Hardened against Radiation

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Resumen

En este TFM, *Trabajo Fin de Máster*, se exponen las fuentes de radiación y sus efectos en sistemas electrónicos, así como el estudio del estado del arte de las técnicas de endurecimiento de células de memoria volátiles en aplicaciones espaciales. Una vez realizado el estudio del arte, se ha procedido a la implementación de estas técnicas empleando la tecnología CMOS, SGB25 de la empresa IHP con el fin de caracterizar parámetros claves que permitan su clasificación. Para finalizar, se ha realizado el layout de la célula de memoria elegida en el proceso de implementación, con el fin de estudiar su factibilidad en una estructura tipo array.

Palabras claves: Endurecimiento, radiación, espacio, células de memoria, CMOS

Abstract

In this *TFM*, it is exposed the radiation sources and effects on electronics systems, as well as, we have studied the state of the art of hardening techniques in volatile memory cells for space applications. Once we made the state of the art, these techniques has been implemented employing CMOS IHP SGB25 Tecnology with the purpose of study their key parameters to classify these memory cells. Finally, according to the key parameters obtained, a memory cell has been selected to made its layout with the purpose of study this design in a memory array structure.

Key words: Hardening, radiation, space, memory cells, CMOS

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List of Acronyms

- μP : Microprocessor
- ASET: Analogue Single-Event Transient
- ASIC: Application Specific Integrated Circuits
- CME: Coronal Mass Ejection
- ESA: European Space Agency
- ESD: ElectroStatic Discharge
- DRAM: Dynamic RAM
- GEO: GEostationary
- HIT: Heavy-Ion Tolerant
- HW: Hardware
- IC: Integrated Circuits
- LEO: Low Earth Orbit
- LET: Linear Energy Transfer
- LET_m: Linear Energy Transfer threshold
- MBU: Multiple Bit Upset
- MCU: Multiple Cell Upset
- MEO: Medium Earth Orbit
- MTBF: Mean Time Between Failures
- RHBD: Radiation Hardening By Design
- RHPB: Radiation Hardening By Process
- ROM: Read-Only Memory
- SAA: South Atlantic Anomaly

- SE: Soft Error
- SEB: Single Event Burnout
- SEC-DED: Single Event Error Correction - Double Error Detection
- SEE: Single Event Effect
- SEFI: Single Event Functional Interrupt
- SEGR: Single Event Gate Rupture
- SEL: Single Event Latchup
- SET: Single Event Transient
- SEU: Single Event Upset
- SoC: System on Chip
- SRAM: Static RAM
- TID: Total Ionizing Dose
- TMR: Triple Modular Redundancy
- VLSI: Very Large Scale Integration

1 Introduction

The creation of transistor in December 1947 by John Bardeen, Walter House Brattain and Willian Bradford Shockley, and its realization for the first time into an integrated circuit by Jack Kilby in 1958, allowed a huge improvement in electronics and computer fields where entire systems could fit in a hand and have a better performance.

In parallel, the era of space exploration begins after World War II with Sovietic Union and United States competing to be the first nation to explore the space. The first artificial satellite, Sputnik, was launched by Union Sovietic on October 4, 1957. A year later, U.S. launched their first satellite, Explorer 1. On April 12, 1961, Soviet cosmonaut Yuri Gagarin was the first human to fly and orbit the Earth. A few days later, on May 5, 1961, Alan Shepard was the first American to fly into space. This dead heat, became into the first steps in the space exploration field.

Over the years, a wide variety of systems has been benefitted by applications from space exploration. Nowadays there is a huge number of systems that locate their position in space thanks to GNSS satellites, a large number of scientific experiments are carried out 408km above the Earth surface aboard the ISS, or the study of crop fields thanks to images obtained by satellite are some examples of the great applications that exist today thanks to the aerospace field. Moreover, in the last years a huge number of missions are being developing to flyby, orbit, or land into another planets or satellites. These facts, along with the emergence of non-governmental companies interested in both space exploration and exploiting the space from a commercial point of view, has led to a new Space Era is beginning today.

1.1 Motivation

Since NASA Mission Explorer 1 in 1958, where Van Allen belts were detected for the first time [3], the radiation effects in electronics system has been a concern to solve in space applications. Nowadays, the ionizing radiation effects are a huge trouble in the electronic components fiability. These effects are present not only at Aerospacial systems or High-Enery Physics Experiments, where electronic components are going to be exposed in a strong radiativity environment, but also at ground-level applications [4] where radiation proceed from natural sources such as neutrons originated from interaction between cosmic rays and atmosphere, or from particles emission caused by radioactive materiales used in packing and soldering processes.

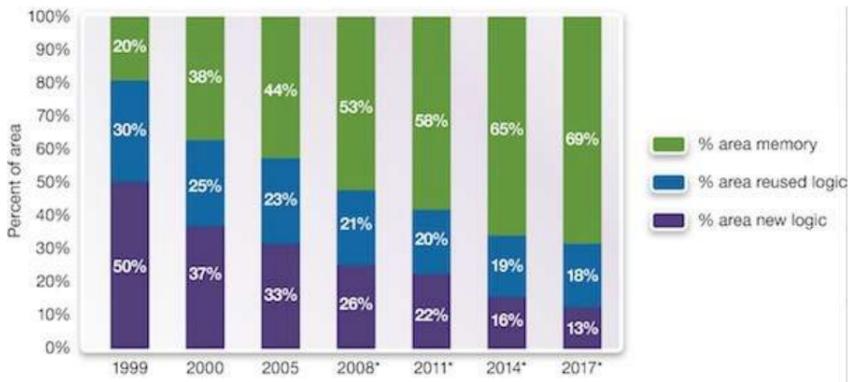


Figure 1.1: Trend of embedded memories area in a SoC

This fact combined with *Semico Research Corporation* report, in which the predominance of SRAM area within the die tends to increase over the years is exposed [5], leading the importance of the study of radiation hardening on memory cells.

1.2 Objectives of this work

The main purpose of this work is to analyze and design hardened memory cells against radiation. To accomplish this overall objective, the following tasks have been implemented:

1. Review about the state of the art of Radiation Hardened memory cells and their features.
2. Understanding of Cadence environment under Linux.
3. Understanding of particle strike double-exponential modelling and simulation technique under the Cadence environment.
4. Implementation & Simulation of various CMOS memory cells at schematic level employing the IHP SGB25 technology.
5. Simulation of radiation effects in various CMOS memory cells at schematic level.
6. Study of radiation robustness of memory cells under test, and normal conditions features to select a memory cell.
7. Layout design of selected memory cell.

1.3 Materials used

This project has been developed through software and bibliographic tools. The work environment has been the Integrated System laboratory of Electronic Engineering department. The following set of software tools has been used:

- Cadence Virtuoso, Microelectronics suite of tools: Schematic Editor L, ADE-XL and Layout Suite XL.
- Spectre language, a Spice variant for Cadence environment, to implement some circuits, analysis and simulations.

- MATLAB and Python scripting to analyze and plot data.

1.3.1 IHP SGB25 Technology

The technology used along this project has been the SGB25, by Germany manufacturer IHP Microelectronics. The SGB25 technology is a 19-mask BiCMOS process which combines a 0.25um CMOS core with 3 types of SiGe:C HBTs. The process offers a 5-layer Al-BEOL, including a MIM capacitor.

1.4 Results overview

In this project, we have studied the radiation effects that lead bit-flips in memory cells as well as different techniques to protect these cells against radiation. Also, we have implemented a set of Radiation-Hardened By Design, RHBD, memory cells using IHP SGB25 Technology with the purpose of comparing its performance and its radiation robustness. According to this point, a RHBD has been selected to develop its layout to compare it with the layout of a non-hardened 6T-SRAM memory cell. A lower area ratio between these memory cells, has been obtained. For this reason we can assure that this RHBD memory cell has a lower area overhead in comparison with the one of a TMR solution.

Also, the following milestones have been developed:

- A study about radiation sources and effects on memory cells is presented.
- A radiation hardened memory cells library has been implemented employing SGB25 IHP Technology.
- A comparison study has been developed according to a set of key parameters selected.

1.5 Project schedule

This work were divided into two parts:

1. *February 2017 - July 2017*: We studied the radiation sources and effects on electronic systems. Both 6T SRAM and HIT memory cells were implemented under SGB25 IHP Technology.

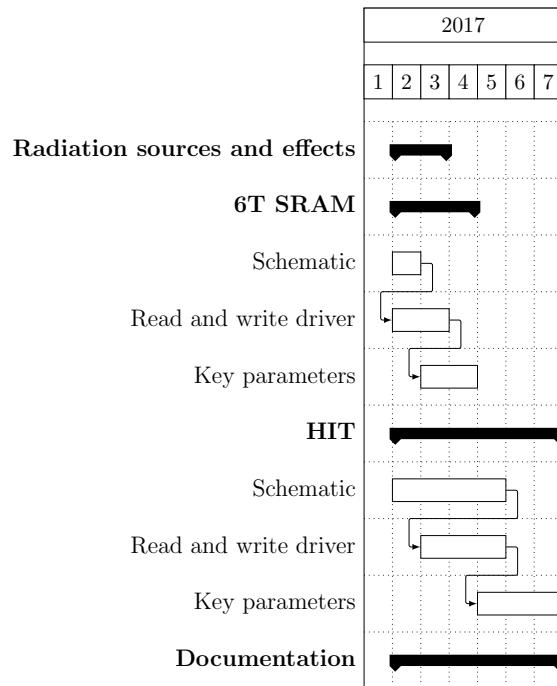


Figure 1.2: Gantt chart between February 2017 and July 2017

2. *February 2018 - July 2018*: In this part, we expanded the scope of the project adding more memory cells to carry out an exhaustive radiation hardened memory cells study.

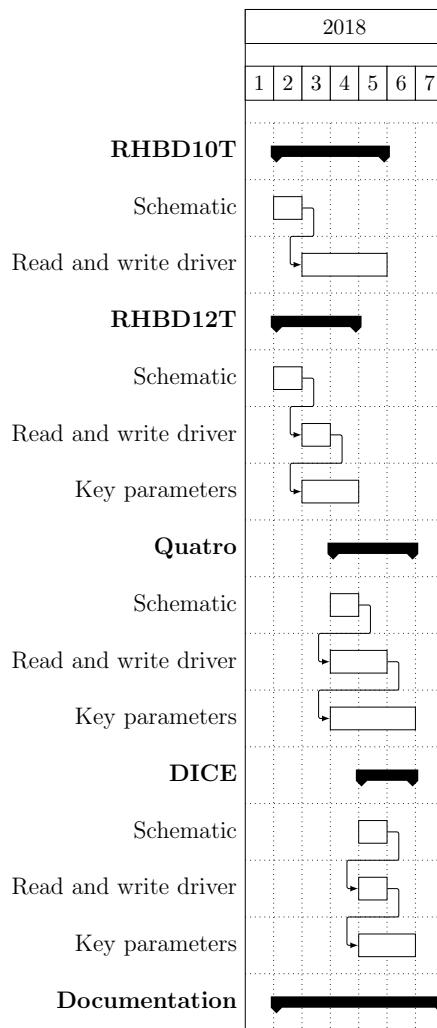


Figure 1.3: Gantt chart between February 2018 and July 2018

According to the previous Gantt charts and a mean time of work in this project of 3h per day, the total time of work is equal to

$$t_{total} = 3 * 30 * 14 = 1260 \text{ hours} \quad (1.1)$$

Radiation Effects on Electronic Systems

In this chapter, the radiation in space environment is explained as well as the radiation effects on electronic devices and its mechanisms and modelling.

2.1 Radiation in Space

The space radiation environment can be classified into two categories: transient particles which include protons and heavy ions of all of the elements of the periodic table, and particles trapped by planetary magnetospheres including electrons, protons and heavy ions.

2.1.1 Galactic Cosmic Rays

Galactic cosmic rays (GCRs) [6] come from outside the solar system but generally from within our Milky Way galaxy and are likely formed by explosive events such as supernova¹. GCRs are atomic nuclei from which all of the surrounding electrons have been stripped away during their high-speed passage through the galaxy. GCRs have probably been accelerated within the last few million years, and have traveled many times across the galaxy, trapped by the galactic magnetic field. As they travel through the very thin gas of interstellar space, some of the GCRs interact and emit gamma rays, which is how we know that they pass through the Milky Way and other galaxies.

2.1.2 Sun

2.1.2.1 Solar flares

A *solar flare* [7] is a sudden and rapid release of magnetic energy that has built up in the solar atmosphere. It can last from a few seconds up to one hour. During this phenomena, radiation is emitted through the entire electromagnetic spectrum from radio waves to X-rays and gamma rays. However, protons and heavy ions should be considered first when analyzing solar flare impacts on integrated circuit reliability.

¹Their true nature being still under researching

2.1.2.2 Coronal Mass Ejections (CME)

A *Coronal Mass Ejection (CME)* [8] is a huge explosion of magnetic field and plasma from Sun's corona over the course of several hours.

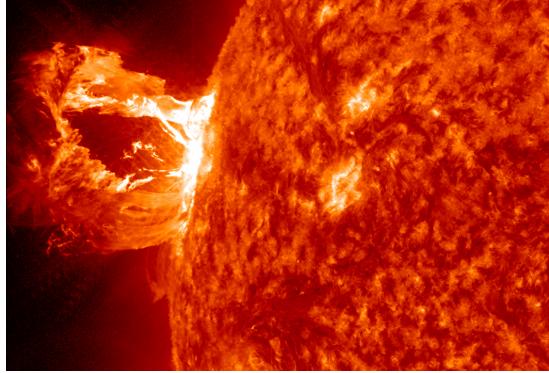


Figure 2.1: Eruption captured by NASA's Solar Dynamics Observatory. April 16, 2012

2.1.2.3 Solar wind

Sun's corona reaches temperatures of up to one million degrees Celsius, leading escaping electrons to the Sun's gravity. As a reaction, protons and heavy ions are ejected in order to maintain the zero electrical charge of the star.

2.1.3 Earth

Also, radiation sources can come from Earth environment due to its magnetic field and atmosphere. This radiation may induce issues to space electronic systems.

2.1.3.1 Van Allen Belts

Van Allen belts are a collection of charged particles, gathered in place by Earth's magnetic field. These radiation belts were discoverable in 1958 by first United States's satellite, Explorer 1. These belts are divided into two regions:

- *Inner belt*: extends from 1000 km to 6000 km above the Earth's surface and is mainly composed by high-energy protons and electrons.
- *Outer belt*: The outer belt spreads from 13000 km to 60000 km above the Earth's surface. Trapped particles are mainly high-energy electrons.

With the purpose of avoid the Van Allen belts radiation effects in satellites orbiting the Earth, it is ensured that its orbits are outside of these zones. However, that belts can swell when the sun becomes more active, extending its influence over several satellites and ISS.

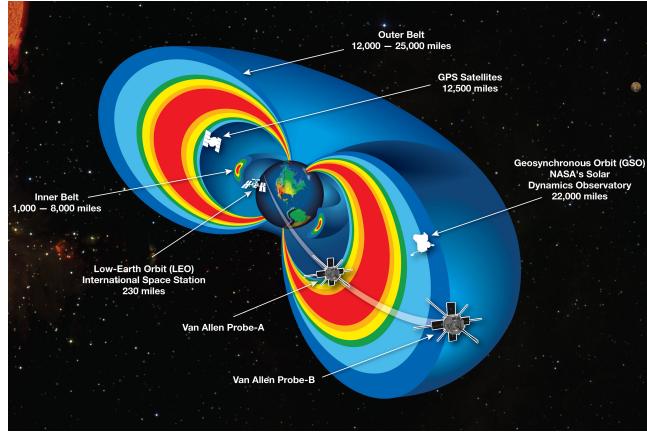


Figure 2.2: Van Allen radiation belts

Furthermore, the tilt of the Earth's magnetic pole from geographic pole and the displacement of the magnetic field from the center cause a dip in the field over the South Atlantic Ocean, resulting in a bulge in the underside of the inner belt, called *South Atlantic Anomaly (SAA)* [9].

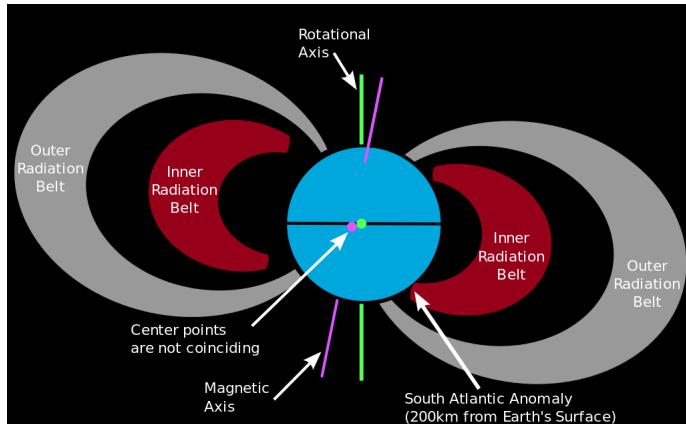


Figure 2.3: Cross-section of Van Allen belts and South Atlantic Anomaly

2.1.3.2 Terrestrial Radiation Sources

Both natural and man-made radiation are present from Earth [10]. Table 2.1 list all these sources of radiation with their annual dose equivalents in units of miliSievert. In microelectronics field, the most important radiation sources are terrestrial and cosmic rays.

Source	Type	Annual Dose
Terrestrial	Natural	0.26
Inhaled radionucleides	Natural	1.0
Internal radionucleides	Natural	0.26
Cosmic radiation	Natural	0.28
Cosmogenic radionuclides	Natural	0.01
Medical diagnostics	Manmade	0.92
Atmospheric weapons testing	Manmade	0.05
Airline travel	Natural 0.03 / passenger	1.6 / crew
Consumer products	Manmade	0.04
Nuclear power	Manmade	<<0.01

Table 2.1: Annual dose from ground radiation in mSv

High-energy cosmic ray particles, mostly protons can create neutrons and secondary particles by spallation reaction on nuclei of atomic gases in Earth's atmosphere in a phenomenon called atmospheric neutrons. The neutron peak flux intensity depends on altitude, latitude and Sun activity.

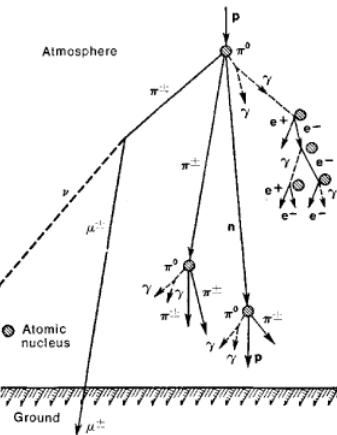


Figure 2.4: Cosmic ray shower

2.2 Radiation Effects

2.2.1 Linear Energy Transfer

Energy is transferred to the medium when a particle interacts with the matter it passes through. The charge deposition capacity, through ionization, is described in terms of *Linear Energy Transfer (LET)* which corresponds to the energy deposition by length unit and depends on the material density ρ :

$$LET = \frac{1}{\rho} \cdot \frac{\Delta E}{\Delta x} \quad (2.1)$$

The deposited energy is given by:

$$\Delta E = \frac{dE}{dx} \cdot \frac{X}{\cos\theta} \quad (2.2)$$

where θ is the ion incident angle.

The minimum LET required for a particle to create a single event, called LET threshold (LET_{th}), occurs when energy deposited is greater than critical energy: $\Delta E > E_c$.

2.2.2 Cumulative Effects

2.2.2.1 Total Ionizing Dose

The ionization dose is deposited by particles passing through the materials constituting the electronic devices causing long term ionizing damages. It primarily impacts insulating layers, which may trap charge or produce interface changes.

2.2.2.2 Displacement Damage

In case that particle interaction doesn't cause a TID effect, the energy deposited in impinging particles displace atoms and creates electrically active defects. The main consequence of displacement damage is a change in the minority carrier lifetimes of semiconductors, and light issues. For this reason, this effect concerns particularly bipolar devices and opto-electronics.

2.2.3 Single Event Effects (SEEs)

SEEs are provoked by charge deposited by a particle striking against the device. These can be classified into two categories [11]:

- *Soft-errors*: These effects lead to change in the signal or stored information.
- *Hard-errors*: These errors can permanently damage the hardware in the same way as in the case of a burnout resulting from a short circuit

2.2.3.1 Soft errors

a. *Single-Event Transient (SET)*

A SET is an energy pulse issued from the ionization of sensitive nodes in electronic devices. It can also propagate in combination logic found CMOS ICs and may be captured by a memory if they occur during a clock edge. In this case a SET may result in an SEU.

b. *Single-Event Upset (SEU)*

This phenomenon, also called bit-flip, occurs when deposited charges, by ions and protons, are collected at sensitive nodes of storage elements such as flip-flops, latches, SRAM cells, etc. SEU may also be the result of an SET being latched on a clock edge after propagating in combinational logic.

The sensitivity to SEU of electronic devices varies according to the technology and several parameters. In particular, reduction of transistor size or supply voltage tends to decrease the critical charge and thus increase the sensitivity to SEE.

c. *Multiple-Bit Upset (MBU) and Multiple-Cell Upset (MCU)*

A single particle can cause multiple bit-flips in a device. Several upsets in a memory word are called MBUs, whereas several upsets in different memory words are referenced as MCUs.

WORD 0	Word 0 bit 0	Word 0 bit 1	Word 0 bit 2	Word 0 bit 3	Word 0 bit 4	Word 0 bit 5	Word 0 bit 6	Word 0 bit 7
WORD 1	Word 1 bit 0	Word 1 bit 1	Word 1 bit 2	Word 1 bit 3	Word 1 bit 4	Word 1 bit 5	Word 1 bit 6	Word 1 bit 7
WORD 2	Word 2 bit 0	Word 2 bit 1	Word 2 bit 2	Word 2 bit 3	Word 2 bit 4	Word 2 bit 5	Word 1 bit 6	Word 2 bit 7

Figure 2.5: Multiple-Bit Upset. Two upset in the same word

WORD 0	Word 0 bit 0	Word 0 bit 1	Word 0 bit 2	Word 0 bit 3	Word 0 bit 4	Word 0 bit 5	Word 0 bit 6	Word 0 bit 7
WORD 1	Word 1 bit 0	Word 1 bit 1	Word 1 bit 2	Word 1 bit 3	Word 1 bit 4	Word 1 bit 5	Word 1 bit 6	Word 1 bit 7
WORD 2	Word 2 bit 0	Word 2 bit 1	Word 2 bit 2	Word 2 bit 3	Word 2 bit 4	Word 2 bit 5	Word 1 bit 6	Word 2 bit 7

Figure 2.6: Multiple-Cell Upset. Two upset in different words

2.2.3.2 Hard errors

a. *Single-Event Functional Interrupt (SEFI)*

When an SEU causes that the device place into a test mode, halt or undefined state, the single event is called Single-Event Functional Interrupt (SEFI). In such cases, a reset of the application or a power off/on is required to recover the full functionality of the system.

IC design tend to increase sensitive to multiple-event upsets by reducing the gaps between transistors, allowing charges deposited by particles to be collected by several sensitive nodes and thus results in SEUs in different memory cells.

b. *Single-Event Latchup (SEL)*

A Single-Event Latchup is the result of the triggering of a parasitic thyristor mainly existing in CMOS circuits and potentially in bipolar devices. When this phenomenon occurs, a high current flows and increases the temperature of the die, until destruction of the structure. This effect can be stopped powering-off the circuit.

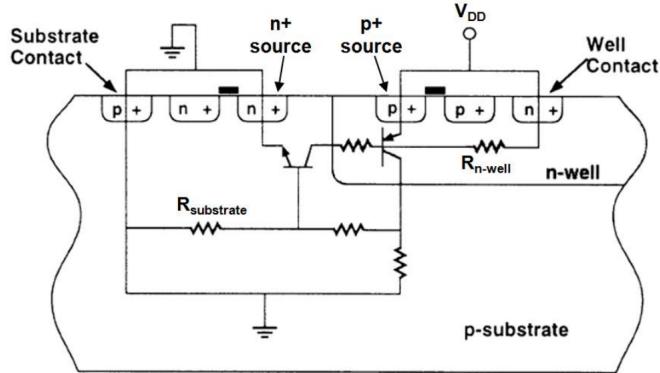


Figure 2.7: Cross-section of an n-well CMOS technology showing parasitic PNPN structure.

c. *Single-Event Burnout (SEB)*

Another type of destructive effect, called Single-Event Burnout, when the source gets forward-biased and the drain-source current is higher than the breakdown voltage of the parasitic structures. This over-current may lead a local overheating able to destroy the device. This phenomenon exists in power MOSFETs devices.

d. *Single-Event Gate Rupture*

Single-Event Gate Rupture occurs when a particle damages or ruptures the gate oxidation insulation of a power MOSFET.

2.2.4 Single Event Effects. Mechanisms and Modelling

Both TID and SEE are radiation effects causes by a particle striking against a MOS devices. In the TID case, trapped charges can lead to a shift in the gate threshold voltages worsening the MOS performances. In the other case, a SEE can lead a bit-flip and loss the stored information. According to the objectives of this work, shown in Section [1.2], the scope of this project is the study of radiation on memory cells, being the main concern to solve the loss of information when a particle strikes against a memory device. For this reason, the focus of this project is on studying and avoiding the SEE in memory cells.

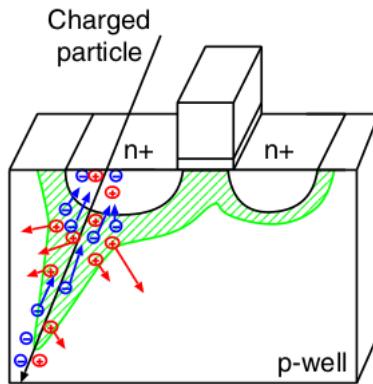


Figure 2.8: Cross-section of particle striking nMOS bulk-transistor with p-well [12].

When a particle strikes against a semiconductor device, electron-hole pairs are created by its ionizing effect along the particle track [12] [13]. Generated electrons in the p-well are collected by drain region of the nMOS transistor by funneling, drift and diffusion [14], while the holes are collected by p-well itself grounded. Thus, the drain output can be flipped by collected electrons transiently leading to $1 \rightarrow 0$ bit-flip. The pMOS transistors behave in much the same way, but in this case the n-well is connected to V_{DD} , so electrons are collected by n-well, while holes are collected in source terminal leading to $0 \rightarrow 1$ transient. For these reasons, in the case of a node with connected by one or more nMOS transistors (pMOS transistors) can lead $1 \rightarrow 0$ ($0 \rightarrow 1$) bit-flips.

At schematic level, this electron-hole movement causes a transient current that flows through transistors with some common node with the transistor where the particle has struck. This transient current provokes a variation in the voltage level on the common node and can cause an SEU.

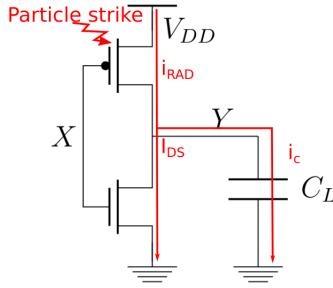


Figure 2.9: Particle striking in CMOS inverter

Applying, to schematic depicts in [Fig. 2.9], the Kirchoff's first law at node Y:

$$i_{RAD}(t) = C \frac{dv_c}{dt} + I_{DS} \quad (2.3)$$

Solving this first-order ODE [15], a double-exponential source [16] [17] is obtained and it has been used to modelling a transient induced by single particle striking against a electronic device. This approach allows to simulate such as $1 \rightarrow 0$ bit as $0 \rightarrow 1$ bit-flips.

$$I(t) = \frac{Q_{coll}}{\tau_2 - \tau_1} \left[\exp\left(-\frac{t - t_{impact}}{\tau_2}\right) - \exp\left(-\frac{t - t_{impact}}{\tau_1}\right) \right] \quad (2.4)$$

Being:

- $Q_{coll} \equiv$ Charge collected
- $t_{impact} \equiv$ Particle impact time
- $\tau_1, \tau_2 \equiv$ Falling and rising time constant respectively.

This model has been implemented in this project through a Spectre script that allows to simulate an SET in the schematic level. Both the falling and rising time has been tuning according to previous studies with this technology.

3 Radiation Hardening on Electronic Systems

An overview over radiation mitigation techniques is introduced. Subsequently, the memory array and memory cells concepts are presented. Finally, the radiation hardened techniques are presented and particular cases of radiation hardened are studied.

3.1 Mitigation techniques

Developing a complete radiation hardened system requires a lot of stages and techniques aiming at mitigation radiation effects in all levels of abstraction from fabrication process, to architecture system level or software level [13].

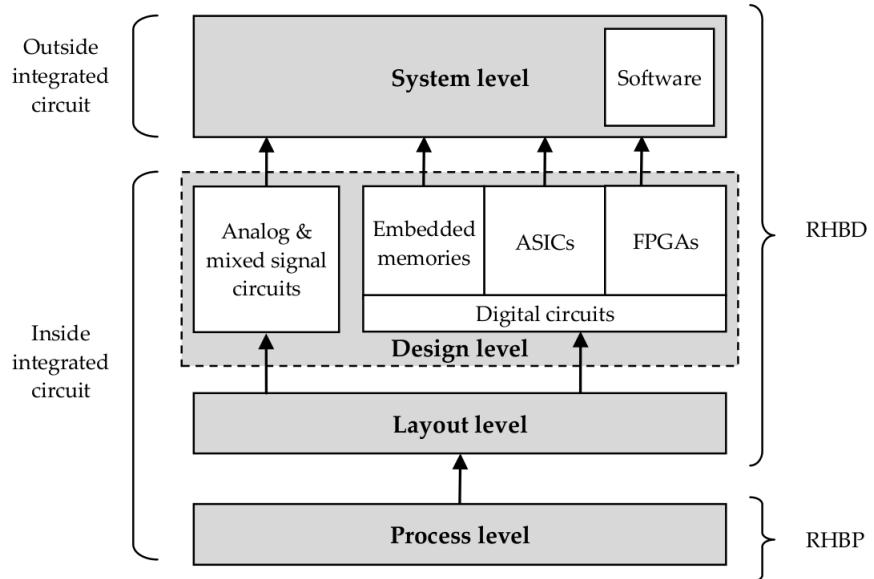


Figure 3.1: Abstraction levels [1]

The process level, also called *Radiation Hardening by Process*, RHBP, just concerns modifications at fabrication processes to reduce the impact of radiation on integrated circuits. Otherwise, the System level, Design level and Layout level are techniques based on TID and SEE mitigation in the design process, being called *Radiation Hardened by Design*, RHBD.

3.1.1 System level

These techniques apply at component level, unit level or embedded software level. Examples of system level solutions to protect electronic systems against radiation effects are:

- *Spatial redundancy*: resources are replicated in order to process the same task in parallel. A voting circuit is in charge of error detection and eventually correction, depending on the number of implemented replicas.
- *Temporal redundancy*: signals are sampled at different instants and a voting circuitry allows rejecting transients and upsets.
- *Information redundancy*: error-detection and error-correction codes are able to protect stored information from radiation effects.

3.1.2 Design level

The techniques devoted to this level are most often dependent to the circuit's nature (digital, analogue or mixed/signal) and/or the circuit's family (ASICs, FGPAs or embedded memory). In Section [3.3] a detailed study of radiation hardened memory cells is exposed.

3.1.3 Layout level

This techniques are based on modifying the transistor's shapes and inserting protection elements in order to reduce mainly TID and SEL phenomena. The main techniques are:

- Enclosed Layout Transistor (ELT)
- Contacts and guard rings

The ELT technique is based on modifying the conventional transistor design avoiding contact between oxide and any p-doped region eliminating current leakage. For this purpose, one of the two nMOS transistor's n+ diffusion can be surrounded by the gate oxide.

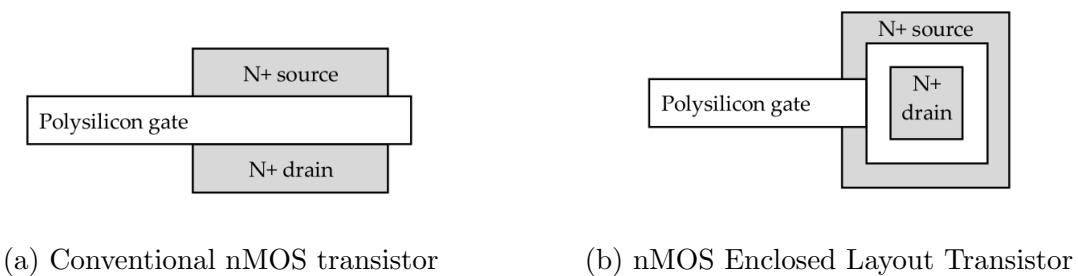


Figure 3.2: nMOS transistor layout comparision

Guard rings [1] form additional collectors for the parasitic transistors. Such collectors are connected either to the positive or negative supply-voltage connection of the integrated circuits. They are placed close to the base-emitter region of the transistor to be protected. As a result, the charge carriers injected into one of the two transistors is diverted largely via these auxiliary collectors to the positive or negative supply-voltage connection.

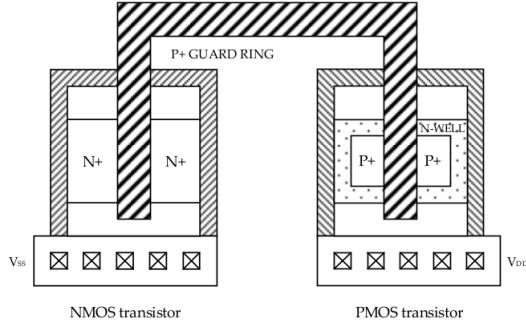


Figure 3.3: CMOS transistors with guard rings [1]

3.1.4 Process level

This level is also called Radiation Hardening By Process (RHBP) and concerns modifications in manufacturing processes in order to reduce the radiation effects on integrated circuits. This goal is achieved by several means such as modifications of the doping profiles in devices and substrates, optimization of deposition processes for insulators and use of specific materials.

As has been mentioned in Subsection [2.2.2.1], the TID phenomenon is associated to charge deposition in insulators, thus degrading their properties. Solutions devoted to reduce the impact of TID focus on modifying insulator's properties and doping levels in active regions nearby interfaces. The Shallow Trench Isolation (STI) is one of the main solutions for TID effects in CMOS technology. However, the SEE are associated to instantaneous failures in active regions and thus can be mitigated by modifications of used materials and/or structures or by using alternative substrates such as Epitaxial layers, Silicon On Insulator (SOI) or Silicon on Sapphire (SOS) [1].

3.2 Memory Arrays

Memory arrays often account for the majority of transistors in a CMOS SoC. Arrays may be divided into categories as shown in the next figure:

- *Content Addressable Memory (CAM)*: determine which address(es) contain stored information that matches a specified key.
- *Serial Access Memory*: is accessed sequentially. Its latency dependent of the stored information position in the sequence.
- *Random Access Memory*: is accessed with an address and has a latency independent of the address.
 - Read / Write Memory: store its information as long as power is applied
 - Read Only Memory: hold data indefinitely.

Focusing on the implementation into IC, CAM is designed to search its entire memory in a single operation being much faster than RAM. Its semiconductor implementation requires a specific comparator system to detect a match between the stored bit and input bit. Furthermore, match outputs from each cell in the data word must be combined to yield a complete data word match

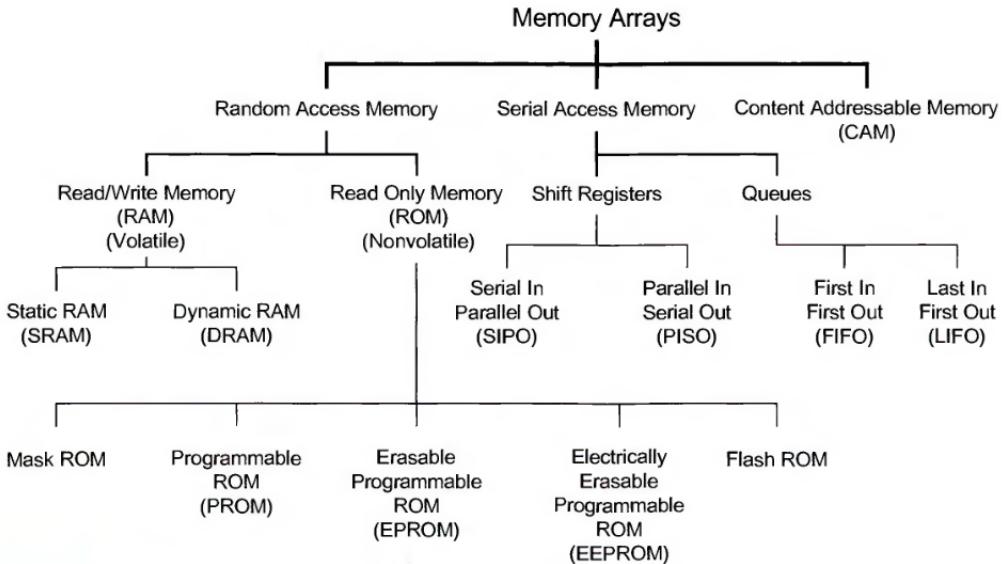


Figure 3.4: Category of memory arrays [18]

signal. The extra circuitry increases power dissipation due to every comparison circuitry is activated each clock cycle. Also, the physical size of the CAM chip is increased which increases its cost.

Latency in Serial Access Memory depends on the position of stored information, in contrast with Random Access Memory where the time to access memories independent of the physical location of the information.

Random Access Memory is classified in *Read/Write Memory*, also called RAM memory, and *Read Only Memory*, also called ROM memory. The main difference between these memories is that a ROM memory has a write time greater than read time, while RAM memory has similar write and read times. Other difference between these memories is RAM memory is *volatile*, which means that retains information while a power supply is applied. Rather, a ROM memory is *non-volatile* holding information indefinitely.

Memory arrays are divided in multiple cells that store a bit of information. In the following figure a 8X1B SRAM memory array is shown:

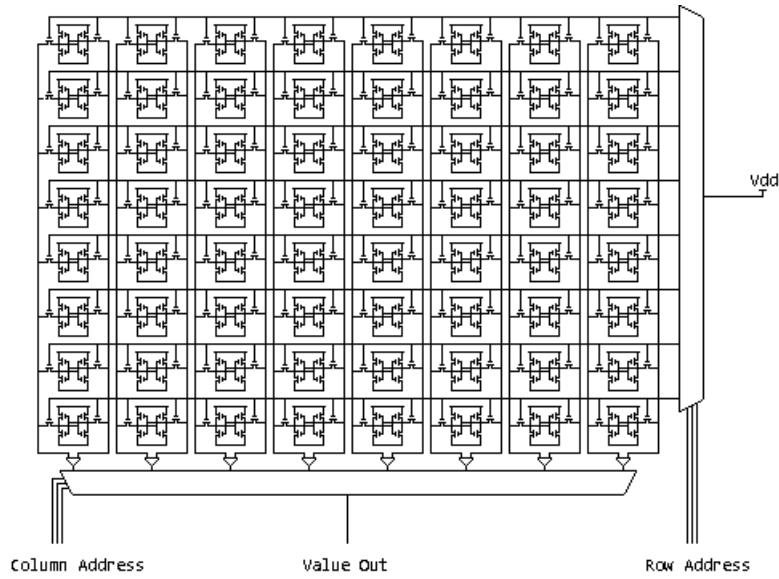


Figure 3.5: SRAM Memory Array

3.2.1 Volatile memories

Read / Write Memory is divided into *Static RAM (SRAM)* and *Dynamic RAM (DRAM)*. The main differences between these cells are that SRAM stores information thanks to a feedback loop, while DRAM uses dynamic storage charge on a capacitor; and SRAM tends to be faster, but much larger, than DRAM.

3.2.1.1 SRAM

A simple SRAM memory cell can be built from two cross-coupled inverters and two pass-transistors, called *6T SRAM*.

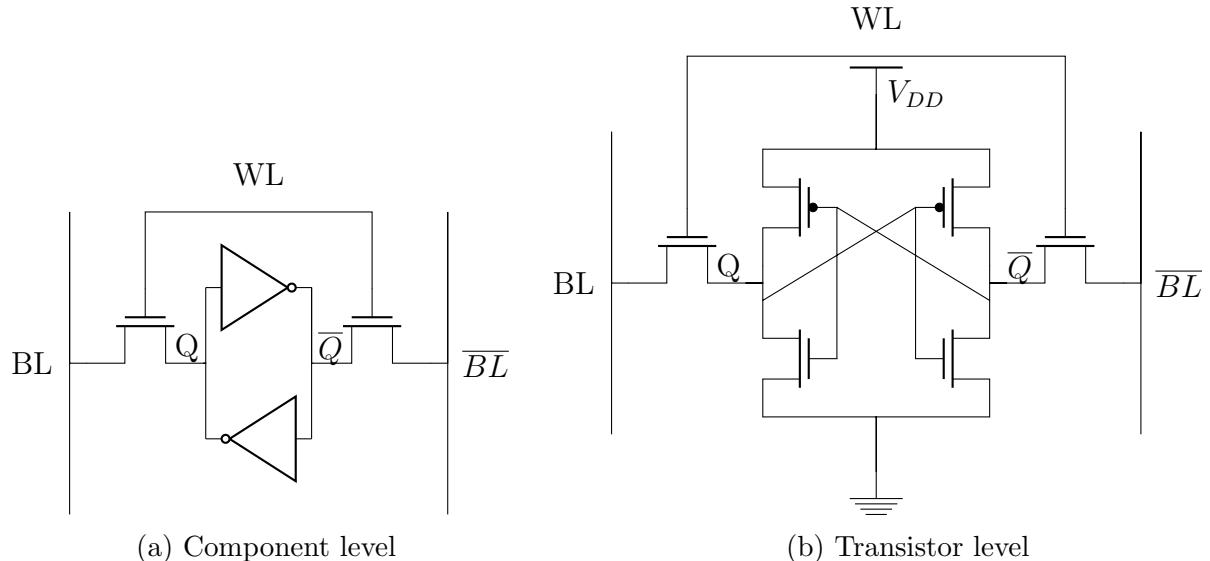


Figure 3.6: 6T SRAM Cell

3.2.1.2 DRAM

A *Dynamic RAM*, DRAM, memory stores its data thanks to a capacitor instead of feedback loop as SRAM. Its IC cell implementation is smaller than SRAM implementation the cell must be periodically read and refreshed so that its contents do not leak away.

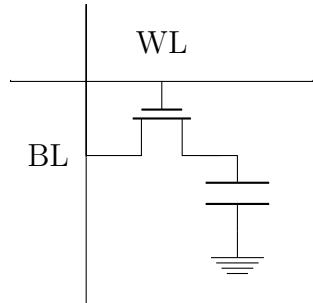


Figure 3.7: DRAM memory cell

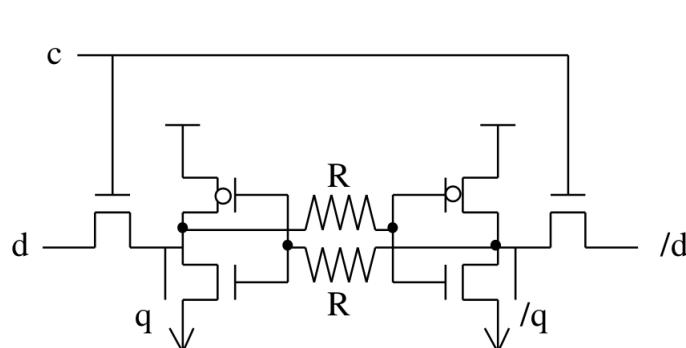
Due to the requirement of extra capacitor component, that is a super-sensitive to radiation effects, this type of memory cells are rarely used in space applications without an extra circuitry.

3.3 Radiation Hardened memory cells

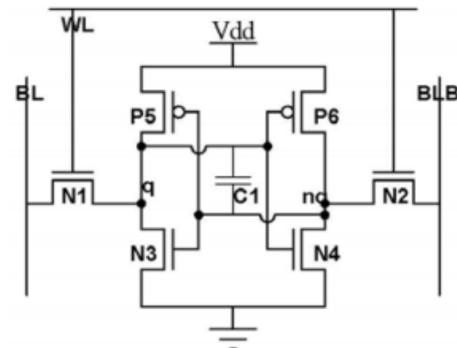
This section will show a radiation hardened memory cells' state of the art in several areas of application.

3.3.1 Resistive and Capacitive Hardening

Early attempts to avoid SEEs on memory cells was made by adding either a resistive or a capacitive [1] element with the purpose of increase their SEU immunity.



(a) Resistor memory cell



(b) Capacitive memory cell

Figure 3.8: Hardened memory cells through resistive and capacitive elements [1]

The main issues of these types of memory cells area a huge speed and area penalty.

3.3.2 Latch Hardening Memory Cells

While Resistive or Capacitive Hardening techniques focus on increase the SEU immunity of the memory cell, this technique is focused on restoring the stored bit after an SEU [19]. For this purpose, these memory cells are based on interconnected couple of latches by regenerative feedback paths[Fig. 3.9].

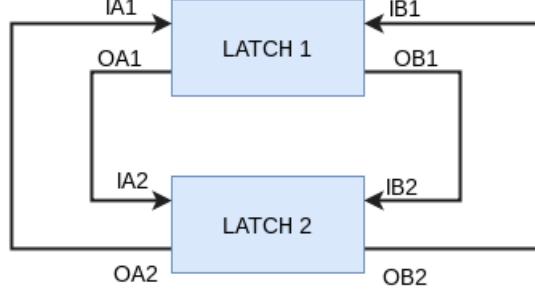


Figure 3.9: Lath Hardenind Memory Cell. General diagram

When the bit is corrupted in a latch by an SEU, it can be restored thanks to the other uncorrupted latch and the regenerative feedback.

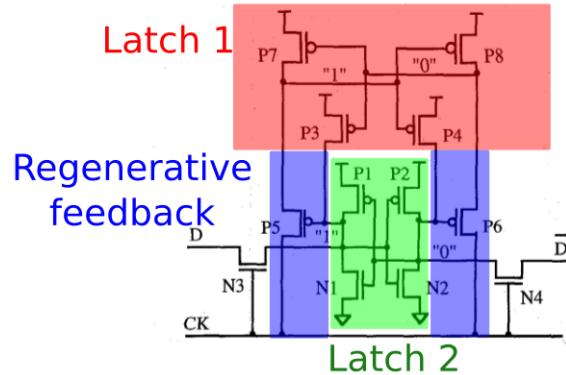


Figure 3.10: Example of Latch Hardening Memory Cell [20]

This type of Radiation Hardened Memory Cells is well-known in literature. For this reason, a particular set of examples has been chosen to encompass all radiation hardened memory cell types based on Latch Hardening Memory Cell:

- RHBD12T
- Quatro
- DICE
- HIT

3.3.2.1 RHBD12T

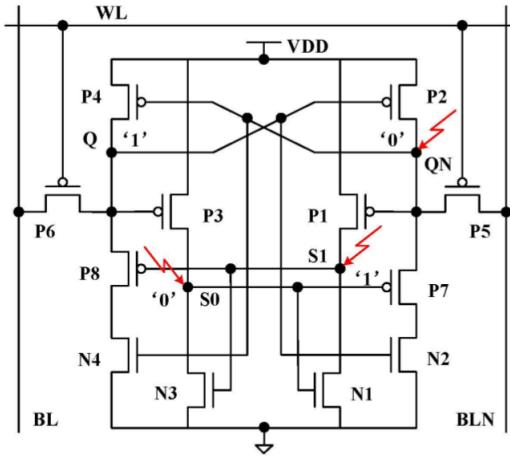


Figure 3.11: RHBD12T Memory Cell [21]

According to Section [2.2.4], in this case [21] the access transistors have been developed through pMOS transistors instead of nMOS transistors. On one hand, this implementation reduces the number of pMOS - nMOS nodes which reduces the number of possible $1 \rightarrow 0$ and $0 \rightarrow 1$ bit-flips at the same node, but it is required a sense amplifier to read the stored bit.

3.3.2.2 Quatro

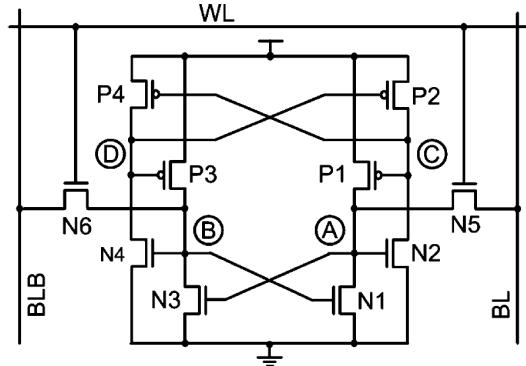
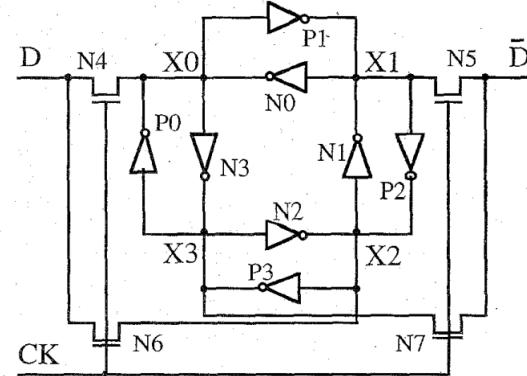


Figure 3.12: Quatro Memory Cell

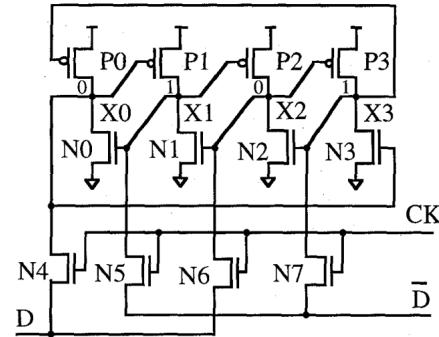
In some cases the radiation effects are faced from point of view of probability. For this reason, there are some RHBD designs that assume a certain probability of failure when a particle strikes against the device. The Quatro memory cell is an example of this. This design offers a great radiation immunity, but it can only recover from $1 \rightarrow 0$ bit-flips.

3.3.2.3 DICE

The *Dual Interlocked Cell* is based on a 4-node redundant structure [1]:



(a) Principle of the DICE memory cell



(b) DICE Transistor level

Figure 3.13: DICE Diagrams [19]

This memory cell is based on the principle called *Dual Node Feedback Control*. Each node is controlled by two adjacent nodes located on the opposite diagonal [19]. It is used in a huge variety of Radiation Hardened Integrated Circuits, such as Aeroflex UT6325 [22].

An example of recovery the stored bit, when a particle strikes against a DICE memory cell in X_0 node, being both X_0 and X_2 at high level and X_1 and X_3 at low level initially, the X_1 node is set to high level through P_1 transistor. When the SET has been vanished, both X_0 node and X_1 nodes recover their initial values through N_3 and N_1 respectively.

3.3.2.4 HIT

The *Heavy Ion Tolerant* [2] is a memory cell developed by the *Laboratoire de Génie Informatique*. This cell is composed of 12 transistors spread out in two nodes connected by feedback paths.

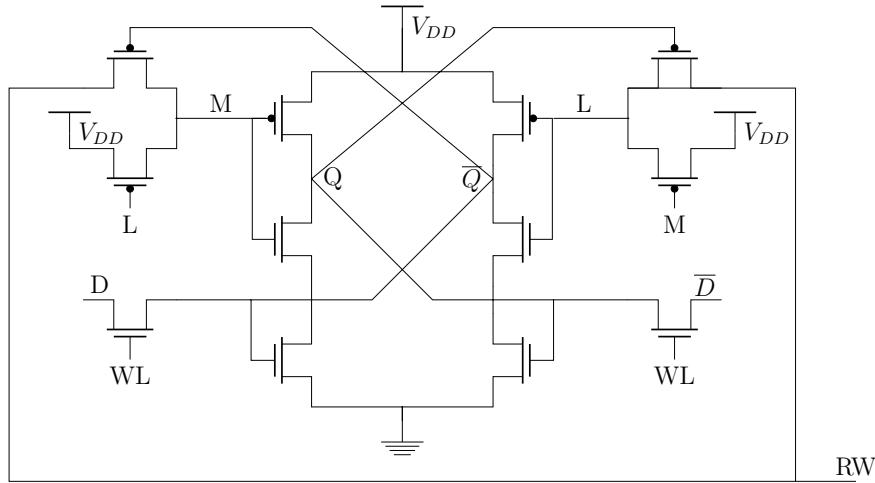


Figure 3.14: HIT memory cell

HIT Memory Cell was used in digital signal processor TSC2102E. This DSP was integrated in the Rosetta Mission launched in 2004 by ESA and landed in Churyumov Gerasimenko comet [1].

4 Implementation Issues

In this chapter we present the different radiation hardened memory cells to implement employing SGB25 IHP Technology and their previous considerations.

4.1 Susceptible nodes

On a single memory cell, all nodes are susceptible to radiation effects causes by the strike of particles. Instead, the bitline nodes (BL and \overline{BL}) and wordline nodes (WL) are shared by multiple memory cells in a memory array structure (Figure [3.5]). Furthermore, the electrical capacity is defined by:

$$C = \frac{dQ}{dV} \quad (4.1)$$

In case of two parallel plates, the capacitance is:

$$C = \epsilon_r \epsilon_0 \frac{S}{d} \quad (4.2)$$

where ϵ_r , dielectric constant, ϵ_0 , vacuum permittivity $\epsilon_0 = 8.854 \cdot 10^{-12} F \cdot m^{-1}$, A , area between the two plates, d , distance between plates.

Moreover, the resistance is directly proportional to the length of the path according to equation:

$$R = \rho \frac{L}{S} \quad (4.3)$$

where ρ is the electrical resistivity, L the path length and S the surface of the path.

For these reasons, these common nodes have a higher capacity and resistance than internal nodes and radiation effects will be diminished when a particle strikes against any of these nodes.

4.2 Sizing memory cells

The starting point for sizing the memory cells has been set the minimum size that allows the correct writing and reading operations. For this purpose, the ratio between transistors have been studied.

Once the minimum size has been determined, the radiation effects has been simulated in all sensitive nodes. When a bit-flip has been detected in the most sensitive node, it has been studied what transistor or transistors are responsible for providing more current to this node in order to resize it and harden the memory cell.

4.3 Temperature range

In this project, without a particular mission to accomplish, it has been supposed the same temperature range as RAD750, a radiation hardened single board computer used in a wide variety of space missions such as Curiosity Mars rover. This temperature range between -55 °C and 125 °C.

4.4 Parameters to measure

The following set of parameters has been selected to be measured to characterize and compare the memory cells:

4.5 Collected charge

This parameter define the robustness of the memory cell under study against radiation. According to equation [2.4], the Q_{coll} is directly proportional to the current caused by a particle strike. The higher Q_{coll} is obtained, better robustness against radiation will have the memory cell.

4.6 Read and Write time

Both parameters measure the speed of the memory cell under study to read a bit from memory, or write a bit into the memory. They have been measured as the time difference between signals that reach 50% of the highest level.

4.7 Simulation methodology

A huge number of memory cells have been simulated in this thesis. To reach correct and comparable results, it has been used a standard simulation methodology in all cases. When a memory cell has been built, a driver that allows read and write to this memory cell has been developed. To simulate both normal operation and radiation effects in the memory cell, a tesbench has been developed for this purpose.

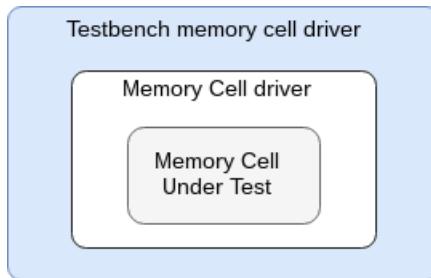
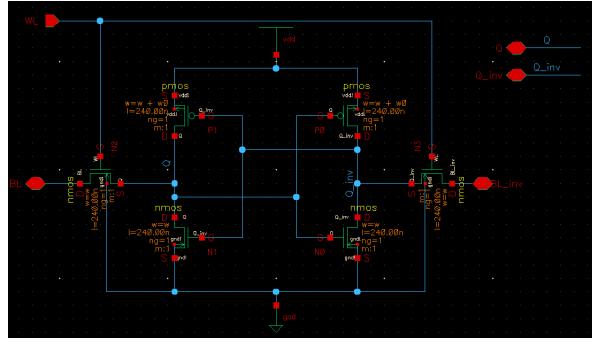
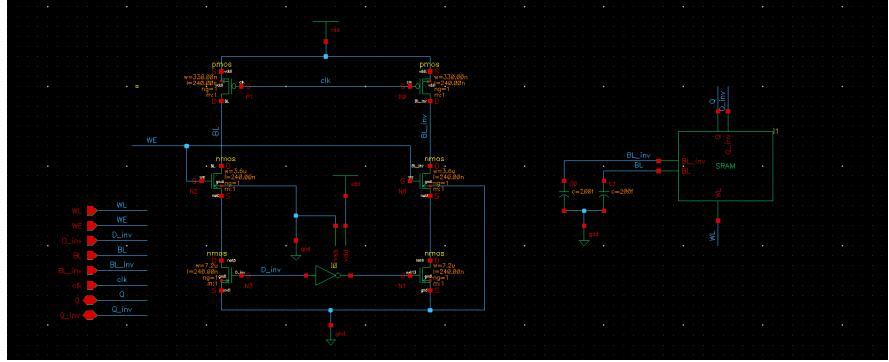


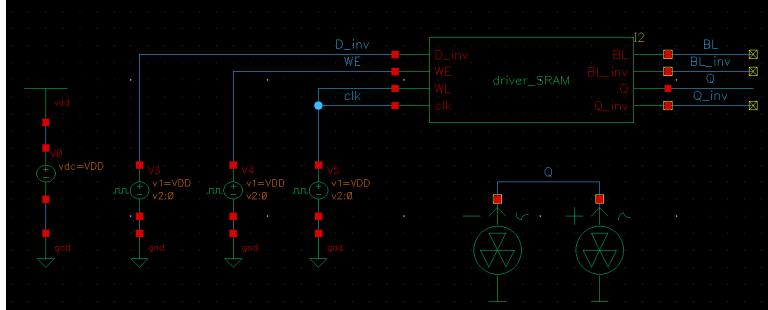
Figure 4.1: Simulation methodology



(a) 6T SRAM transistor view.



(b) 6T SRAM driver.



(c) 6T SRAM Testbench with radiation source.

Figure [4.2a], [Fig. 4.2b] and [Fig. 4.2c] show the different schematics developed in the characterization of 6T-SRAM memory cell. Also, as can be seen in Figure 4.2b, a couple of capacitors has been placed in the bitlines signals in the driver level with the purpose of simulating the capacitance coupling due to multiple memory cells.

4.7.1 Normal operation

In this type of simulation, the operation of memory cell without radiation effects is studied and its key parameters, except the collected charge, Q_{coll} , obtained. The steps to write a bit into the memory cell, or read a bit from memory cell are:

4.7.1.1 Read operation

First, it is necessary to precharge the BL and \overline{BL} . When the operation is enabled by WL signal, the BL is equal to storage node Q and \overline{BL} is equal to \overline{Q} .

4.7.1.2 Write operation

To write $Q = 1$ and $\bar{Q} = 0$, the writer driver within memory driver itself set $BL = 1$ and $\bar{BL} = 0$, respectively, changing the stored data when the operation is enabled by WL signal.

4.7.2 Radiation simulation methodology

We have developed two simulation categories:

- *Normal operation*: The operation of memory cell without radiation effects.
- *Radiation simulation*: Radiation effects are considered in this category, and a study about radiation hardening is presented.

As mentioned previously in Section [2.2.4], a double-exponential current source is added to the *Testbench memory cell driver* [Fig. 4.2c] to simulate a particle striking against a susceptible node. To determine the maximum Q_{coll} allowed by the memory cell, the t_{impact} parameter has been selected to ensure the data value at that time. In case that, an instant after t_{impact} , the stored data has an unexpected value, the Q_{coll} level has lead to a SEU in the node.

This methodology has been implemented, together with the *Corners* simulation and the *Temperature Variation*, through an iterative process to determine the maximum Q_{coll} allowed by the sensitive node of the memory cell: Once the sensitive node has been located and its maximum

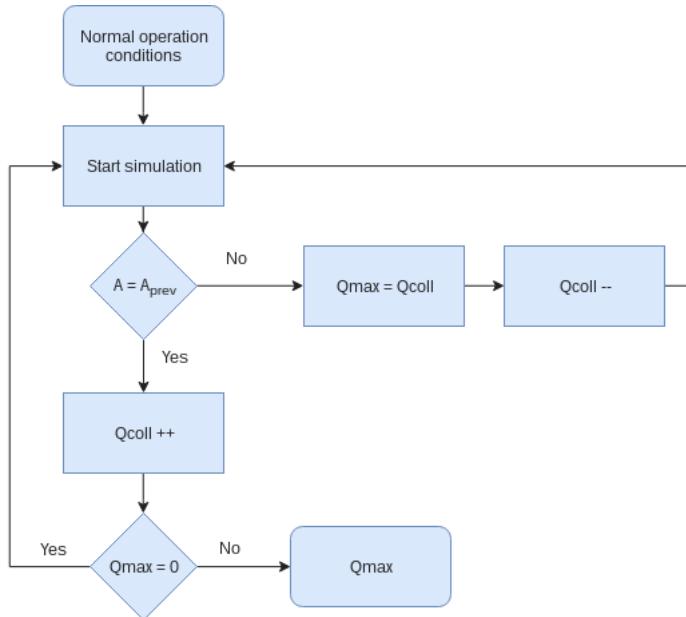


Figure 4.3: $Q_{coll_{max}}$ determination algorithm

charge collected measured, a study of which transistors are responsible of non-restore issue is done with the purpose of resizing and strengthen them.

4.8 Corners and Temperature variation

4.8.1 Corners

When a VLSI system is manufactured, it will suffer variations in their performance due to manufacturing processes. The process corners represent the extreme case of these parameters variations within which the manufacturer ensures ($\approx 99.73\%$ or 3σ) that all manufactured circuits have a better performance than these extreme cases. One naming convention for process corners is to use two-letter designators in the case of carrier mobilities. The first one refers to the nMOS transistor and the second refers to the pMOS transistor.

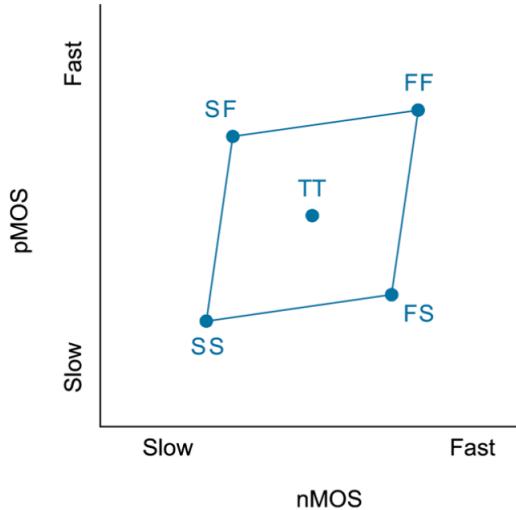


Figure 4.4: Process corners [18]

4.8.2 Temperature variation

It is well-known that temperature causes variations in the behaviour of all electronic systems. In CMOS technologies, a high temperature leads to higher mobility of electrons and holes causing faster devices.

In space applications, each electronic device specification depends on the specific space mission to accomplish due to the huge temperature range from $-235\text{ }^{\circ}\text{C}$ of Lunar Pole Site [23], until $175\text{ }^{\circ}\text{C}$ of Mercury.

4.9 Radiation Hardened Memory Cells Implementation

4.9.1 6T SRAM

The following figure depicts the 6T SRAM at transistor level:

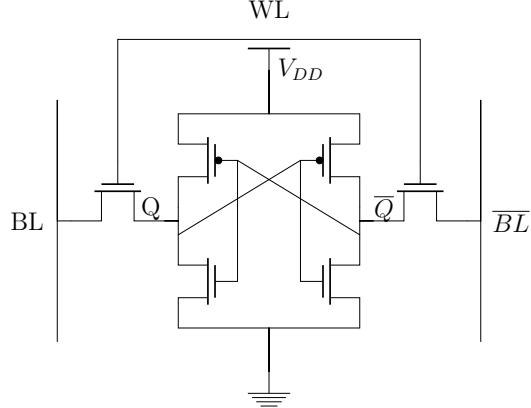


Figure 4.5: 6T SRAM. Transistor level

It is well-known in literature [18] that to write a bit into this memory cell, the pull up pMOS transistors have to be weaker than the access transistors, being this constraint called write stability. Instead, to read data from a 6T SRAM memory cell, the pull-down nMOS transistors have to be stronger than the access transistors, being this constraint called read stability. As show in Figure

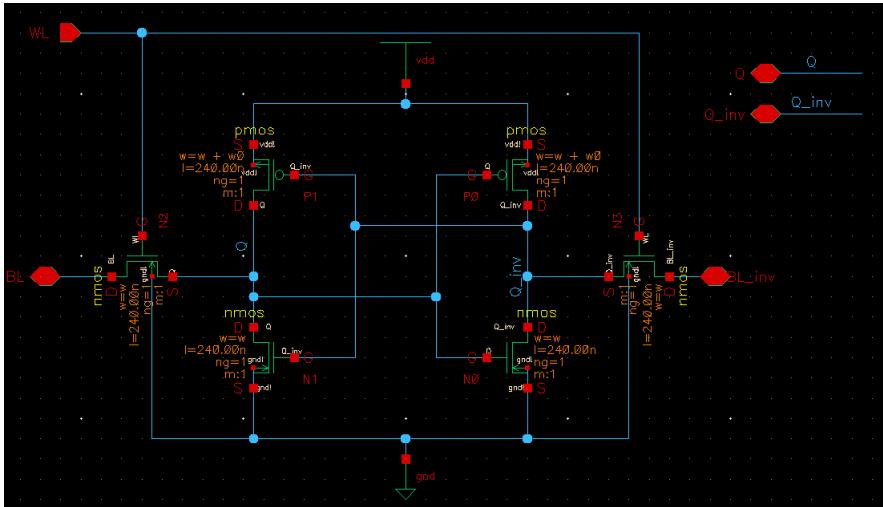


Figure 4.6: Implemented 6T SRAM Memory Cell in Cadence environment using IHP SGB25 Technology

[4.6], the transistor width is set as a parameter w with the purpose of find the optimum width through a parametric sweep simulation.

As it has been mentioned in Section [4.7], it is needed a driver that write into the memory cell as well as read from the memory cell.

This driver is based on a couple of pull-up transistors that precharge the bitlines when clk signal is low. In case of write into the memory cell, the WE signal is high turning on $N0$ and $N2$ transistors. Due to pull-down transistors are stronger than pull-up transistors, the data will be written into memory cell.

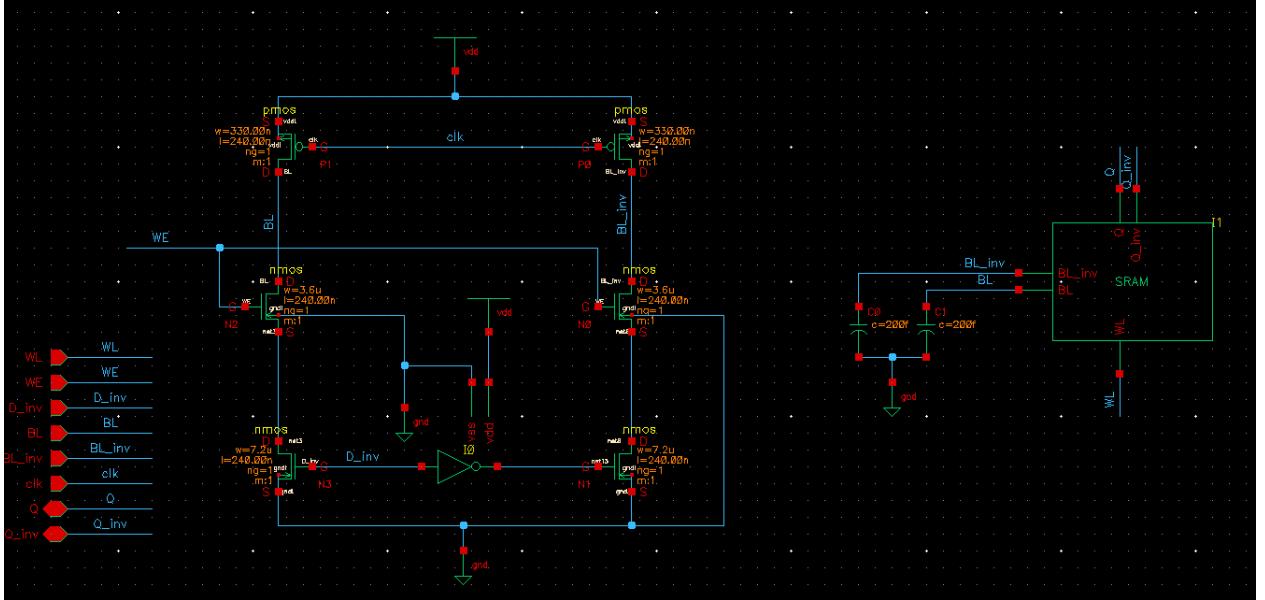


Figure 4.7: SRAM driver

4.9.2 HIT

To build this memory cell under 240 nm IHP SGB25 Technology, it has been used the size details exposed in [2].

Transistors	$w_N(\mu m)$	$L_N(\mu m)$	Transistors	$w_p(\mu m)$	$L_p(\mu m)$
MN1	6.0	1.2	MP1	8.0	1.2
MN2	6.0	1.2	MP2	8.0	1.2
MN3	6.0	1.2	MP3	6.0	1.2
MN4	6.0	1.2	MP4	4.0	1.2
MN5	6.0	1.2	MP5	6.0	1.2
MN6	6.0	1.2	MP6	4.0	1.2

Table 4.1: HIT cell original devices size [2]

The CMOS technology used in [2] is a $1.2 \mu m$ technology. In this way, this sizes have been resized according to the CMOS technology used in this project:

Transistors	$w_N(\mu m)$	$L_N(\mu m)$	Transistors	$w_p(\mu m)$	$L_p(\mu m)$
MN1	0.49	0.24	MP1	0.66	0.24
MN2	0.49	0.24	MP2	0.66	0.24
MN3	0.49	0.24	MP3	0.49	0.24
MN4	0.49	0.24	MP4	0.33	0.24
MN5	0.49	0.24	MP5	0.49	0.24
MN6	0.49	0.24	MP6	0.33	0.24

Table 4.2: HIT cell devices size

The figure [4.8] depicts the HIT cell memory developed. It can be seen that it has been used the channel width as a parameter with the purpose of studying its optimum size and the hardening through resizing.

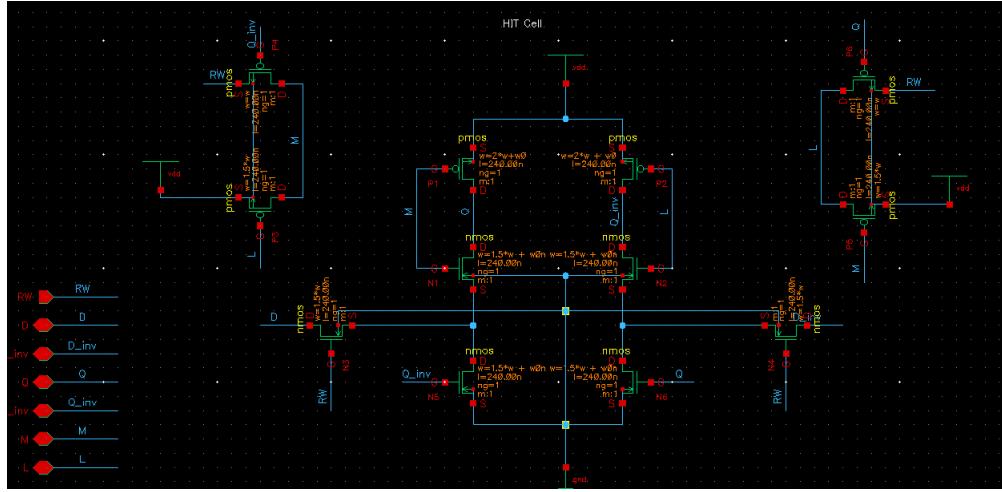


Figure 4.8: HIT memory cell implementation under IHP SGB25 Technology

Similar to the 6T SRAM implementation exposed in the current chapter subsection [4.9.1], it is required a driver that allows both write and read operation as well as a testbench that simulate the entire system.

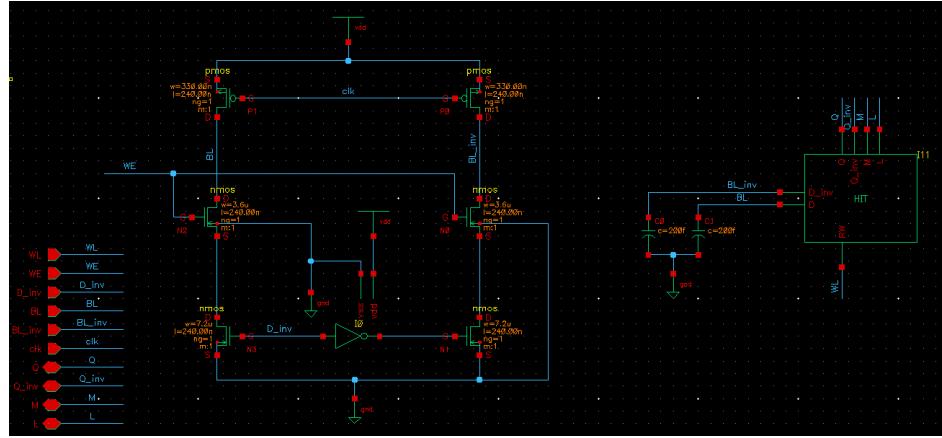


Figure 4.9: HIT driver

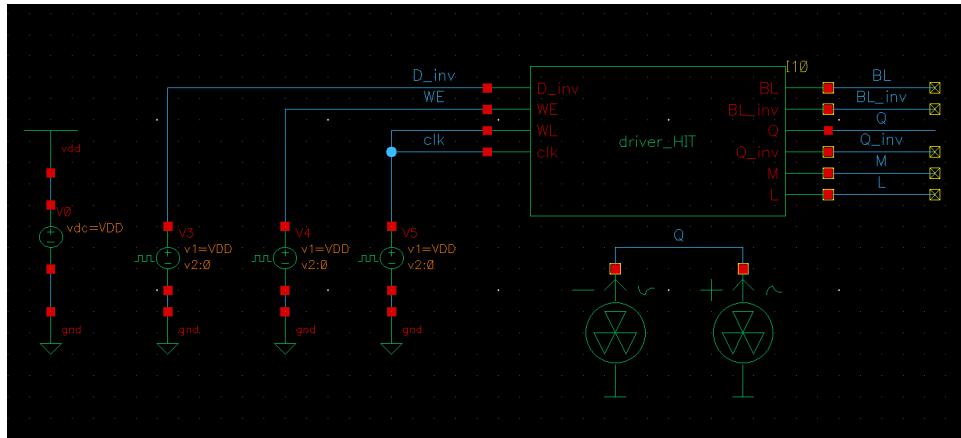


Figure 4.10: HIT testbench driver

4.9.3 DICE

According to [19], this memory cell does not require oversized transistors for its correct operation. In this way, it has been tested the operation with the smallest channel width in all transistors.

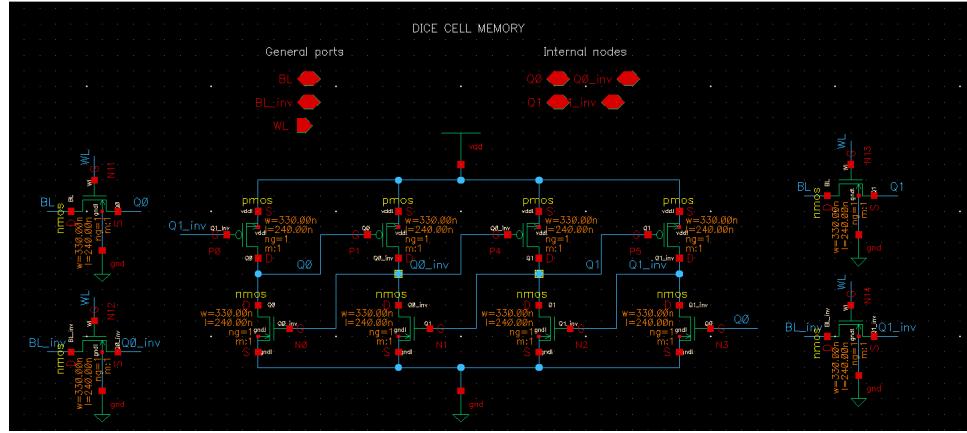


Figure 4.11: DICE schematic

4.9.4 Quatro

This memory cell has been implemented via analysis and parametric sweep simulation to tune a correct sizing of this memory cell.

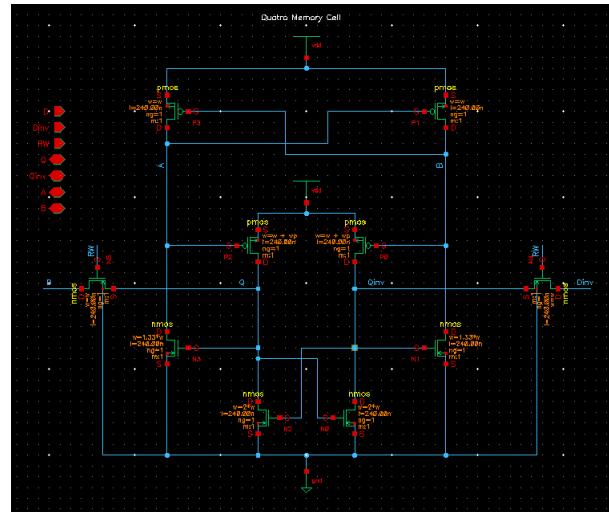


Figure 4.12: Quatro memory cell

5 Experimental Results and Comparison

In this chapter, the obtained results are presented, according to the mentioned in [4.7.2], where simulation methodology was exposed. As well as it is presented the comparison between the radiation hardened memory cells under study. Finally, we select a memory cell and make develop its layout.

5.1 6T SRAM

This memory cell has been used as a reference to be compared to others memory cells. To simulate this memory cell, the following testbench has been developed:

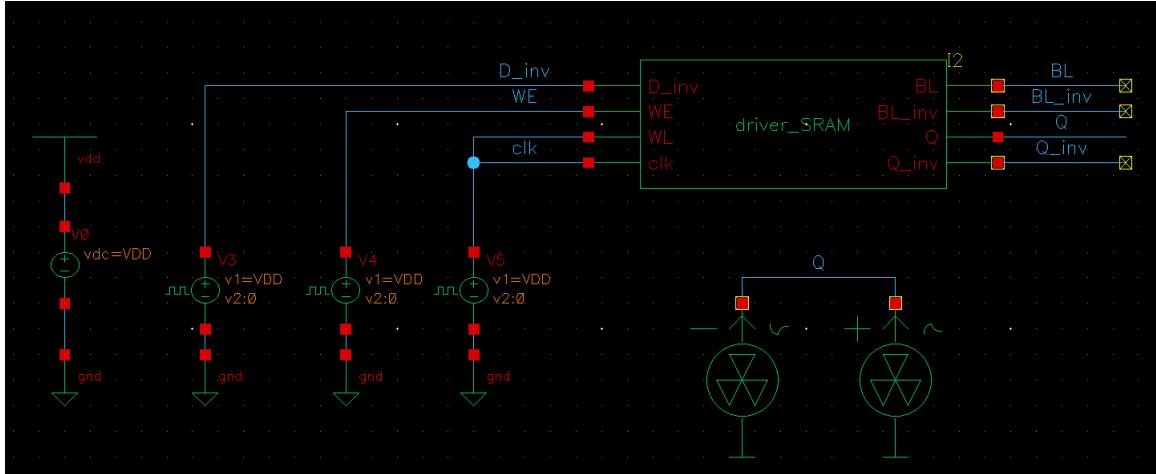


Figure 5.1: Testbench SRAM driver

5.1.1 Normal operation

It has been obtained the following transistor sizing for a correct read and write operations:

	Access transistors	Pull-up transistors	Pull-down transistors
Size	330 nm	330 nm	330nm

Table 5.1: 6T SRAM minimum size

This width channel is the smallest size allowed by IHP SGB25 Technology. This fact seems contradictory to the write stability, as pull-up pMOS transistors have to be weaker than access transistors, and read stability, as well as the pull-down nMOS transistors have to be stronger than access transistors. In the first case, the pull-up pMOS transistors are weaker than access transistors due the difference between carrier mobilities in pMOS and nMOS transistors on this technology. In the other case, the access transistors are weaker than pull-down transistors due to the called *body effect* [18] that diminishes the value of the threshold voltage, weakening these transistors.

The following graph shows the simulation of 6T SRAM normal operation:

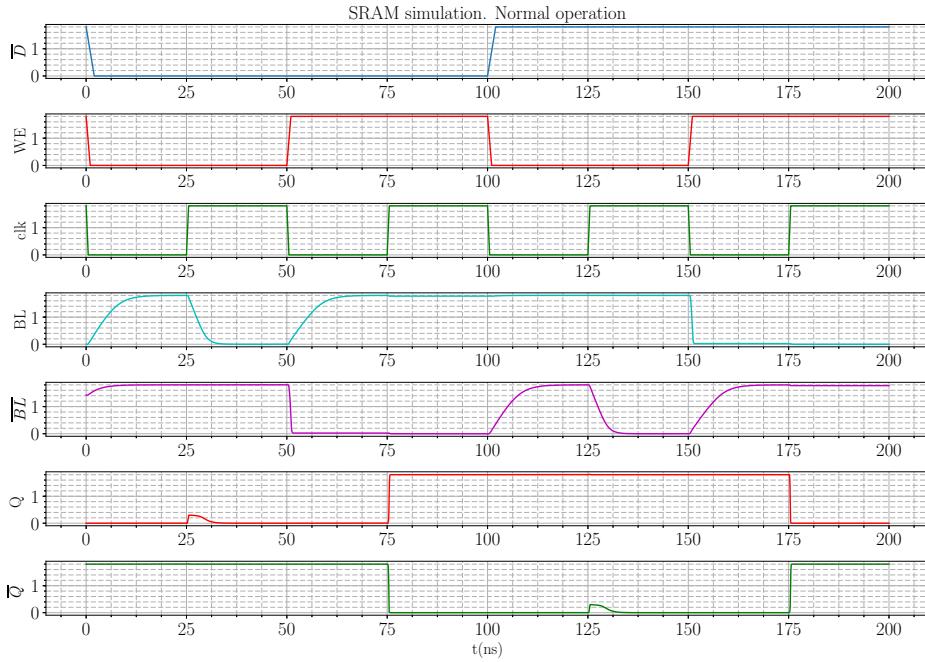


Figure 5.2: 6T SRAM simulation results. Normal operation @ $w = 330$ nm

The obtained parameters that accomplish process corners and within the temperature range are:

<i>Write time(ns)</i>	<i>Read time(ns)</i>	<i>Mean Power(μW)</i>	<i>Peak power(μW)</i>
267.9	3.55	46.54	195.4

Table 5.2: 6T SRAM parameters @ $w = 330$ nm

5.1.2 Radiation simulation

According to equation [2.4], the time of impact of positive SET, t_{impact} , it has been to set to 22 ns and the time of impact of negative SET has been set to 122 ns. In Figure 4.6 can be shown that the susceptible nodes are Q and \bar{Q} . Also, this memory cell has a symmetrical structure, so both nodes have the same radiation robustness as can be demonstrated in the simulations.

The Figure 5.3 shows the simulation results when a particle strikes against the memory cell under study with a collected charge equal to 5 fC.

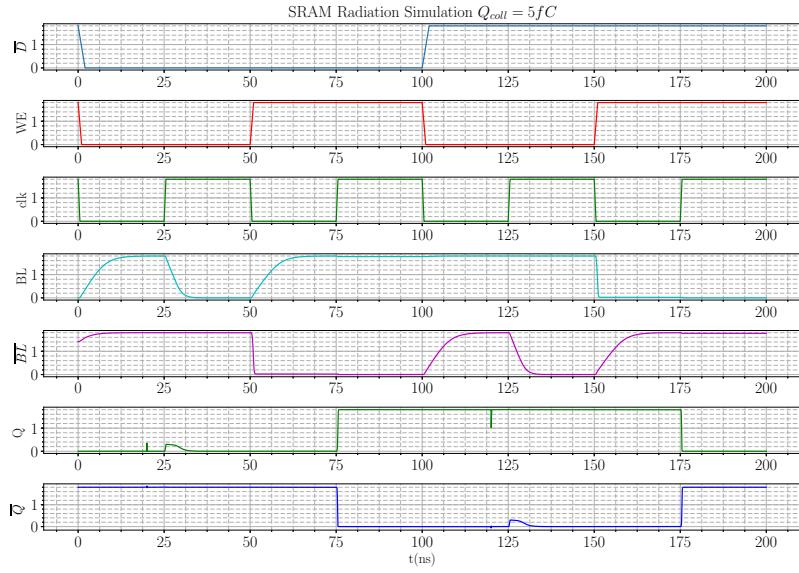


Figure 5.3: SRAM Radiation Simulation. $Q_{coll} = 5 \text{ fC}$.

It can be shown in Q node a positive spike in a time equal to 22 ns, and a negative spike in a time equal to 122 ns due to their respective SET effects. However, these SET don't cause an SEU in Q node.

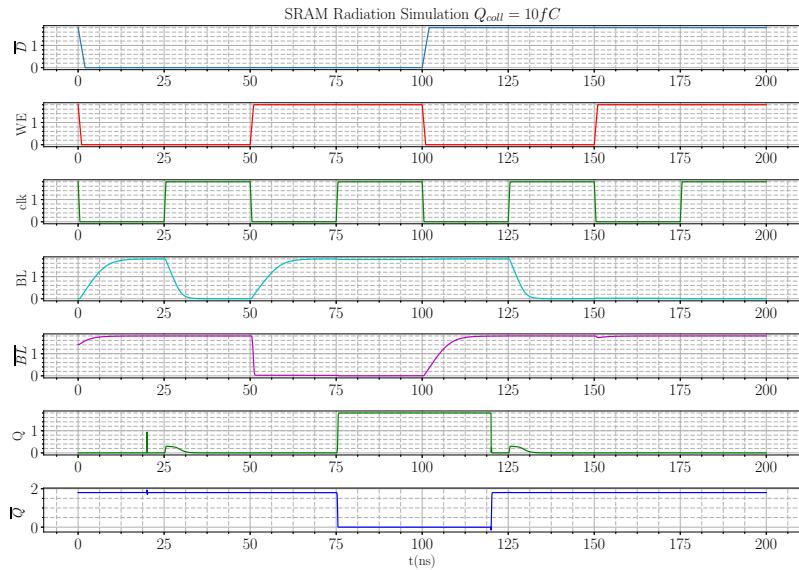
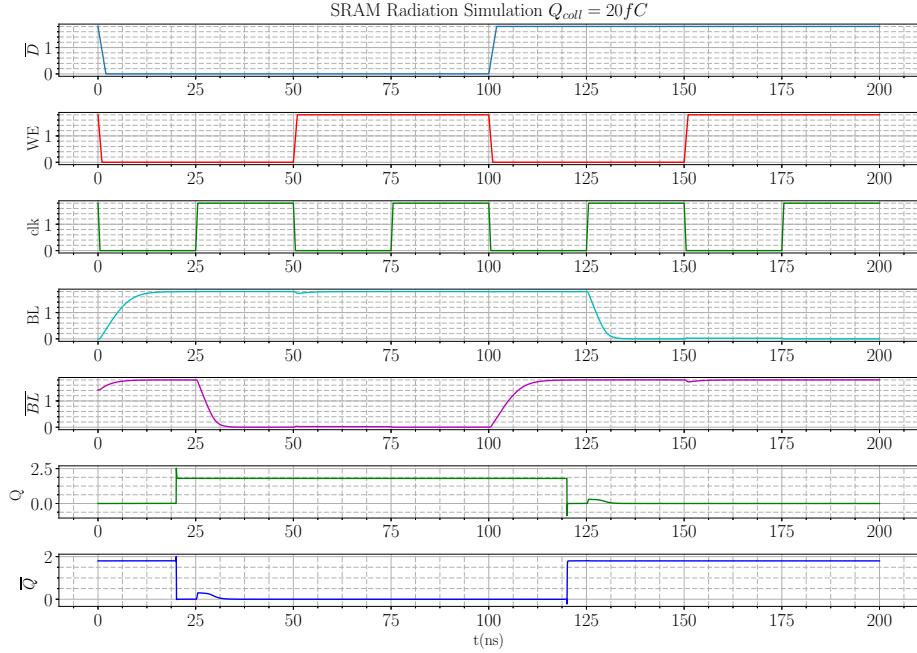


Figure 5.4: SRAM Radiation Simulation. $Q_{coll} = 10 \text{ fC}$.

Instead, the figure [5.4] shows the simulation results with a collected charge equal to 10 fC. In this case, in a time equal to 122 ns, the negative SET has led to a bit-flip in the memory cell, and the bit has been lost. However, the positive negative has not led to a bit-flip.

With a collected charge equal to 20 fC it can be shown that both negative and positive SETs have led to bit-flips in their respective times.



The bottleneck is the minimum value of Q_{coll} that leads into a bit-flip the memory cell. For this reason, it can be affirmed that the maximum collected charge that supports this memory cell is between 5fC and 10 fC under these simulation conditions. To determine the maximum Q_{coll} it has been used the algorithm previously detailed in this chapter subsection 4.7.2, that satisfy all corners and within the specified temperature range. In this way, the maximum collected charge obtained is equal to:

$$Q_{coll,max} = 8.75fC \quad (5.1)$$

This value has been obtained under a temperature equal to 125 $^{\circ}C$ and fs corner, in line with the expected results due to higher temperatures, higher electrons and holes mobility leading to more sensitive to SEE. Also, a fs leads to faster nMOS transistors than pMOS transistors. For this reason, the nMOS is stronger than pMOS in this corner causing a more sensitive node to negative SETs.

5.1.2.1 Radiation hardening through resizing

In an attempt to hardening this memory cell against radiation, the channel width of pMOS transistors has been increased to make pMOS stronger than nMOS in a fs corner. With this purpose, the width of the pMOS transistors in the SRAM have been doubled ($w = 660nm$) and tripled ($w = 990nm$). In both cases, the maximum collected charge tolerated by the memory cell has been found under a temperature of 125 $^{\circ}C$ and fs corner, being the Q_{coll} values:

$$Q_{coll} = 11.75fC \quad (5.2)$$

in the case of $w = 600nm$,

$$Q_{coll} = 15fC \quad (5.3)$$

in the case of $w = 990\text{nm}$.

The parameters obtained in these cases have been:

<i>Write time(ns)</i>	<i>Read time(ns)</i>	<i>Mean Power(μW)</i>	<i>Peak power(μW)</i>
239.5	3.55	46.68	337.49

Table 5.3: 6T SRAM parameters @ $w = 660\text{ nm}$

<i>Write time(ns)</i>	<i>Read time(ns)</i>	<i>Mean Power(μW)</i>	<i>Peak power(μW)</i>
237.1	3.55	46.85	481.5

Table 5.4: 6T SRAM parameters @ $w = 990\text{ nm}$

5.2 HIT

The first Radiation-Hardened Memory cell to introduce its results is the Heavy-Ion Tolerant, HIT [2], memory cell.

5.2.1 Normal operation

The normal operation of this memory cell is shown in Figure [5.5] :

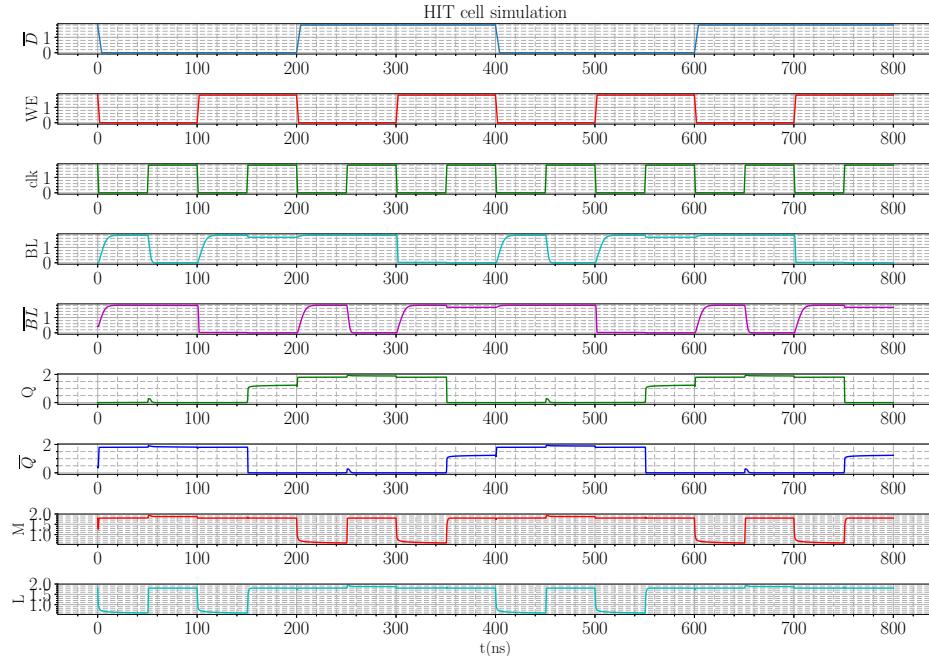


Figure 5.5: Normal operation of HIT cell

Being the obtained parameters to measure:

Write time(ns)	Read time(ns)	Mean Power(μ W)	Peak power(μ W)
907.69	2.594	39.91	724.59

Table 5.5: HIT cell performances

5.2.2 Radiation simulation

In this case, Q and \bar{Q} as well as M and L nodes are simmetrical. As can be seen in Figures [5.6] and [5.7], the Q node are more sensitive to radiation effects than M node, due to in the first case a particle striking against Q node with a collected charge equal to 30 fC create an SEU.

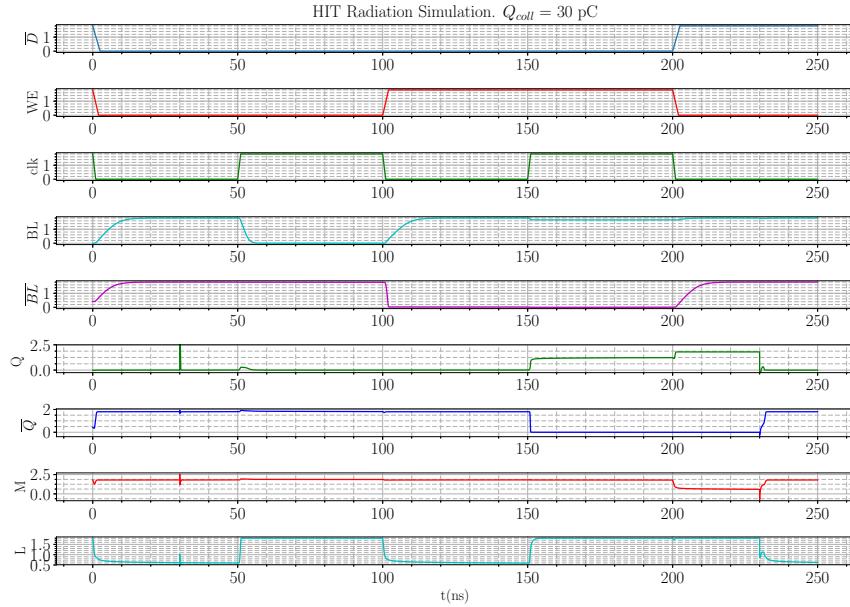


Figure 5.6: HIT memory cell Radiation Simulation in Q node. $Q_{coll} = 30 \text{ pC}$

Following the same procedure used to determine the maximum collected charge in the previous memory cell, it has been obtained in this case:

$$Q_{coll} = 4.5 \text{ pC} \quad (5.4)$$

5.2.2.1 Radiation hardening through resizing

The result previously exposed has been obtained under 125°C and fs corner, in line with the expected results.

To harden this memory cell, the pMOS transistors $P1$ and $P2$ has been resized in order to make them stronger than pull-down nMOS transistors.

When it has been doubled, the maximum collected charge is equal to:

$$Q_{coll} = 9.75 \text{ pC} \quad (5.5)$$

And its parameters:

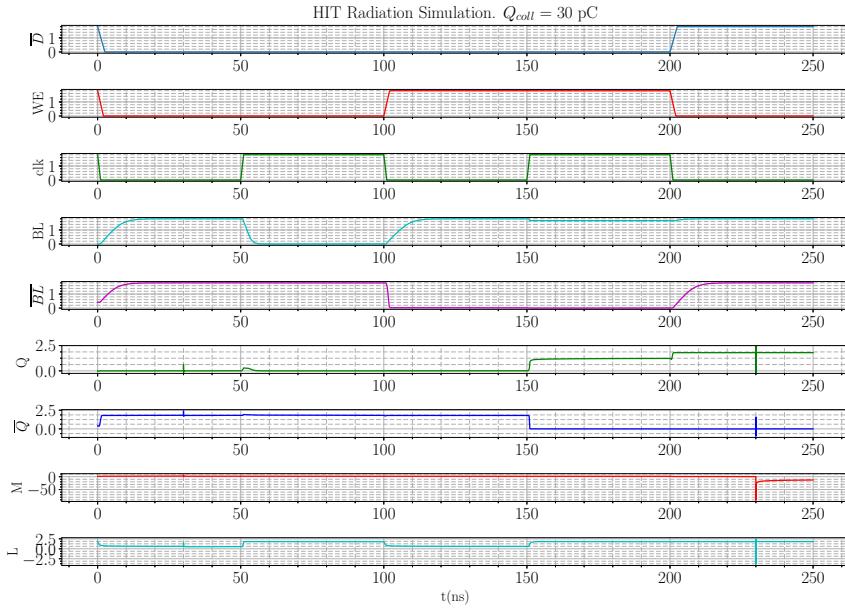


Figure 5.7: HIT memory cell Radiation Simulation in M node. $Q_{coll} = 30 \text{ pC}$

Write time(ns)	Read time(ns)	Mean Power(μW)	Peak power(μW)
972.8	2.594	39.939	726.4

Table 5.6: HIT cell performances with doubled channel width pMOS transistors $P1$ and $P2$

In case of triple the width channel of pMOS transistors, the maximum collected obtained is:

$$Q_{coll} = 21.5 \text{ pC} \quad (5.6)$$

And its key parameters:

Write time(ns)	Read time(ns)	Mean Power(μW)	Peak power(μW)
1047.0	2.594	39.979	725.7

Table 5.7: HIT cell performances with tripled channel width pMOS transistors $P1$ and $P2$

5.3 DICE

5.3.1 Normal operation

In the following figure a *read 0 - write 1 - read 1 - write 0* operation cycle of a DICE memory cell is shown:

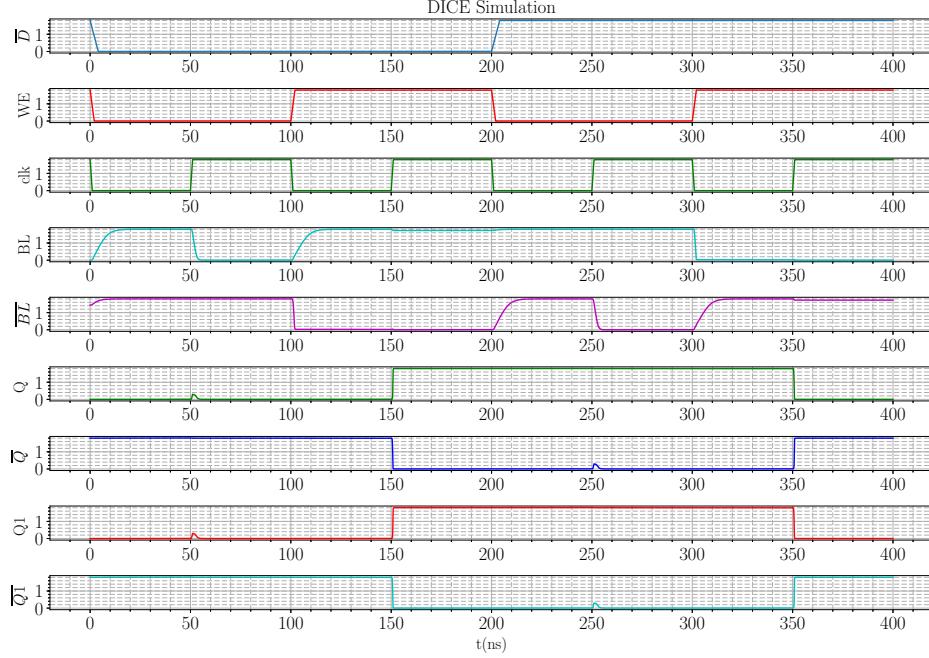


Figure 5.8: Normal operation of DICE memory cell

Being the DICE key parameters:

Write time(ns)	Read time(ns)	Mean Power(μW)	Peak power(μW)
416	1.955	2.2129	326.7

Table 5.8: DICE key parameters

5.3.2 Radiation simulation

As shown in Figure [3.13a], when a particle strikes against an internal node in DICE memory cell, a couple of nodes are affected. According to Figure [4.11], when a particle strikes in Q node leading to a negative SET, the affected node is the \bar{Q} node through $P1$ transistor. However, the affected node is the $Q1$ node through $N3$ transistor when the particle strikes leading to a positive SET.

By this way, we can affirm that the maximum collected charge in the DICE memory cell, with these transistors size, is equal to:

$$Q_{coll} = 161.25 \text{ pC} \quad (5.7)$$

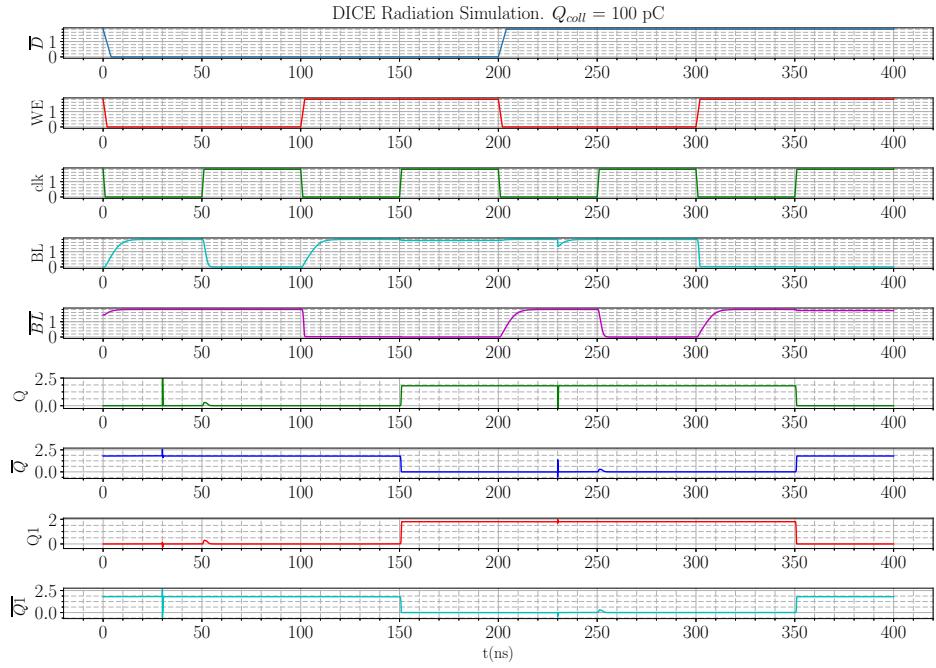


Figure 5.9: DICE memory cell Radiation Simulation. $Q_{coll} = 100 \text{ pC}$

5.3.2.1 Radiation hardening through resizing

According to DICE implementation shown in [4.9.3] and the resizing technique for radiation hardening shown in [4.7.2], the results obtained when we double the DICE memory cells transistors are:

$$Q_{coll} = 215.75 \text{ pC} \quad (5.8)$$

And its key parameters:

Write time(ns)	Read time(ns)	Mean Power(μW)	Peak power(μW)
446.3	1.618	2.2129	398.5

Table 5.9: DICE cell performances with doubled channel width pMOS transistors

And the results obtained in the case of triple the weak transistors:

$$Q_{coll} = 294.75 \text{ pC} \quad (5.9)$$

And its key parameters:

Write time(ns)	Read time(ns)	Mean Power(μW)	Peak power(μW)
482.8	1.5020	2.302	499.29

Table 5.10: DICE cell performances with tripled channel width pMOS transistors

5.4 Quatro

5.4.1 Normal operation

The following graph depicts the results obtained for the normal operation of Quatro memory cell:

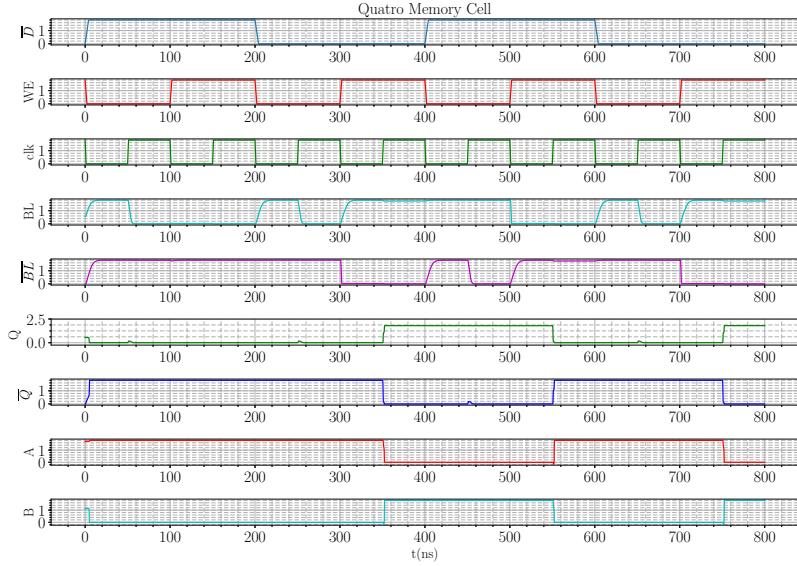


Figure 5.10: Quatro memory cell. Normal operation

Being its key parameters:

Write time(ns)	Read time(ns)	Mean Power(μW)	Peak power(μW)
811.9	3.007	25.339	261.4

Table 5.11: Quatro key parameters

5.4.2 Radiation simulation

As mentioned in Section [3], subsection [3.3.2.2], the memory cell only can recover $1 \rightarrow 0$ bit-flips.

In Figure [5.11] it is shown the results obtained with a collected charge equal to 100 pC. It can be seen that at time equal to 32 ns, the SET has led to an SEU in Q node due to the incapacity of this memory cell to recover this type of SET. However, when the collected charge is equal to 300 pC, the Q node partially loss the information leading to SEU effect as Figure [5.12] depicts.

The maximum collected charge of this memory cell, without modifying the employed size in normal operation, is equal to:

$$Q_{coll} = 111.75 \text{ pC} \quad (5.10)$$

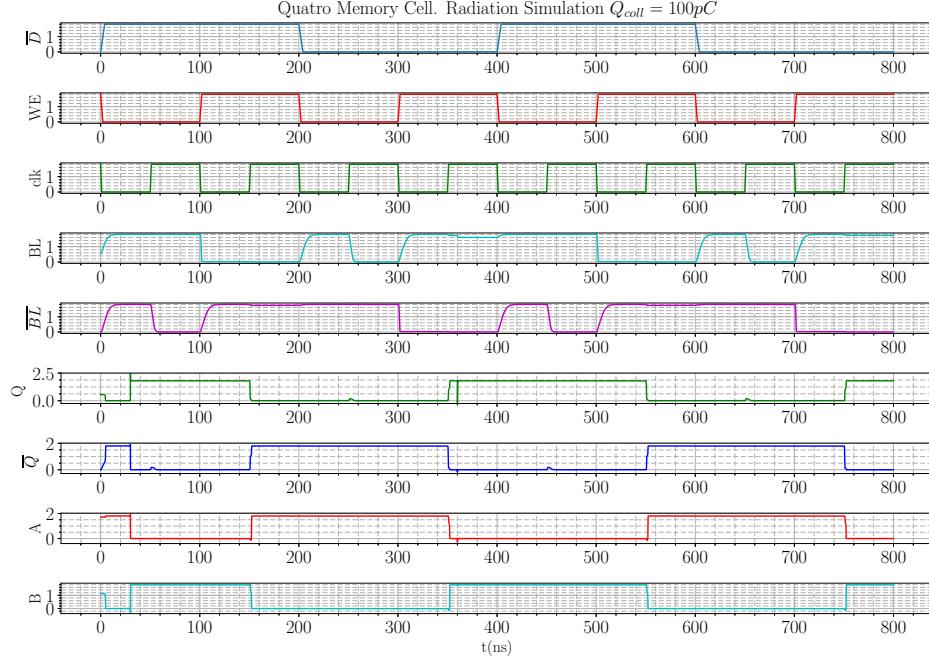


Figure 5.11: Quatro memory cell. Radiation simulation $Q_{coll} = 100 \text{ pC}$

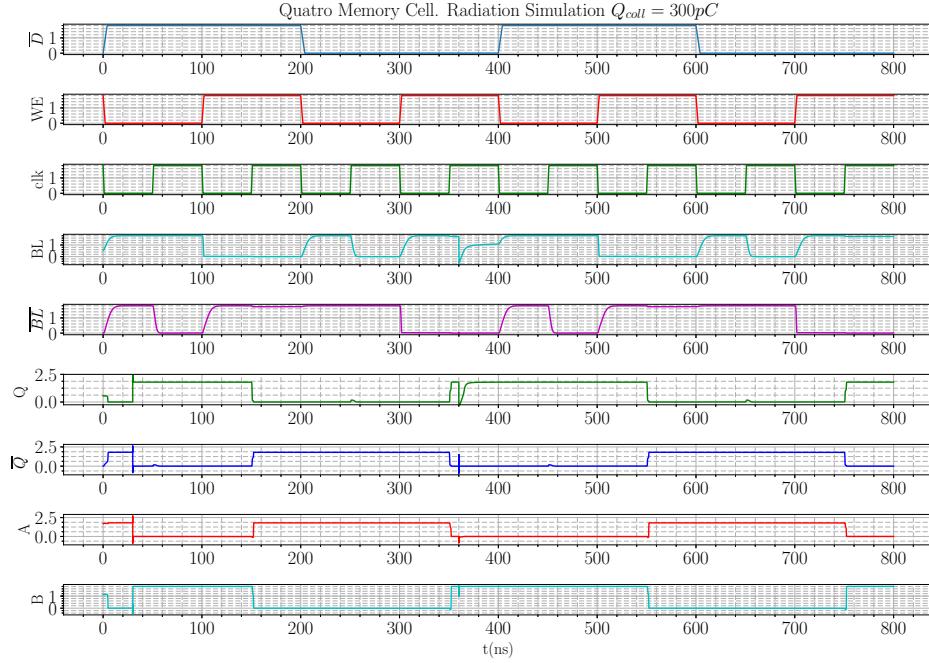


Figure 5.12: Quatro memory cell. Radiation simulation $Q_{coll} = 300 \text{ pC}$

5.4.2.1 Radiation hardening through resizing

According to Quatro implementation [4.9.4], it has been studied the sensitive transistors that leads to an SEU in Q node. The results obtained when these transistors are resized, are:

$$Q_{coll} = 131.25 \text{ pC} \quad (5.11)$$

<i>Write time(ns)</i>	<i>Read time(ns)</i>	<i>Mean Power(μW)</i>	<i>Peak power(μW)</i>
904.69	3.006	35.07	350.0

Table 5.12: Quatro cell performances with doubled channel width

And in the case of tripled these transistors:

$$Q_{coll} = 131.74 \text{ } pC \quad (5.12)$$

<i>Write time(ns)</i>	<i>Read time(ns)</i>	<i>Mean Power(μW)</i>	<i>Peak power(μW)</i>
932.4	3.006	28.25	448.9

Table 5.13: Quatro cell performances with tripled channel width

5.5 Comparison results

In this section, a comparison between the memory cells is presented to choose a memory cell to study its area

5.5.1 Maximum collected charge, $Q_{coll_{max}}$

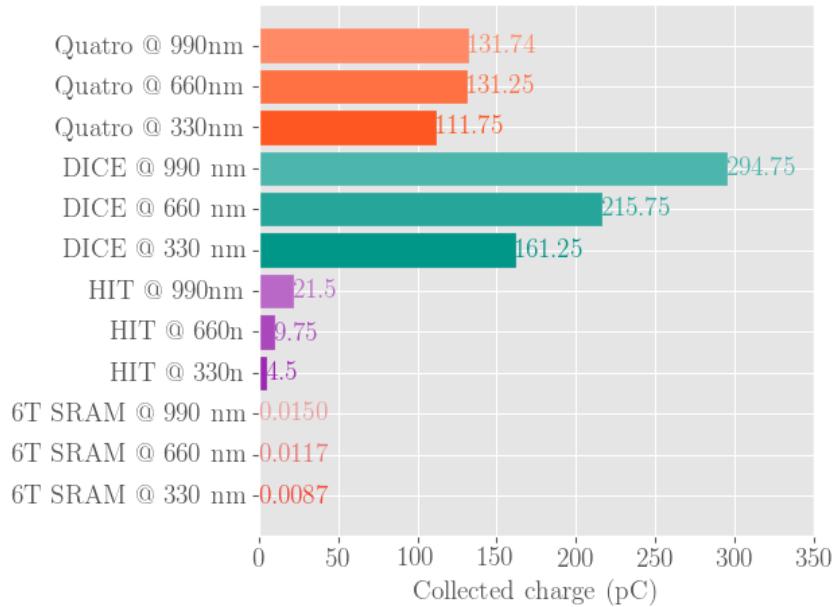


Figure 5.13: Collected charge, Q_{coll} results

The first key parameter measured is the maximum collected charge. As shown in Figure [5.13], the maximum charge collected in a 6T SRAM memory cell is orders of magnitude lower than the rest. The strongest memory cell against radiation, is the DICE memory cell. This fact is due to the radiation hardening is applied at schematic level in this cell. In contrast, the rest of radiation hardened memory cells shown in this project are based on ratioed transistors.

5.5.2 Write and Read time

Figures [5.14] and [5.15] depicts the results obtained for write and read times:

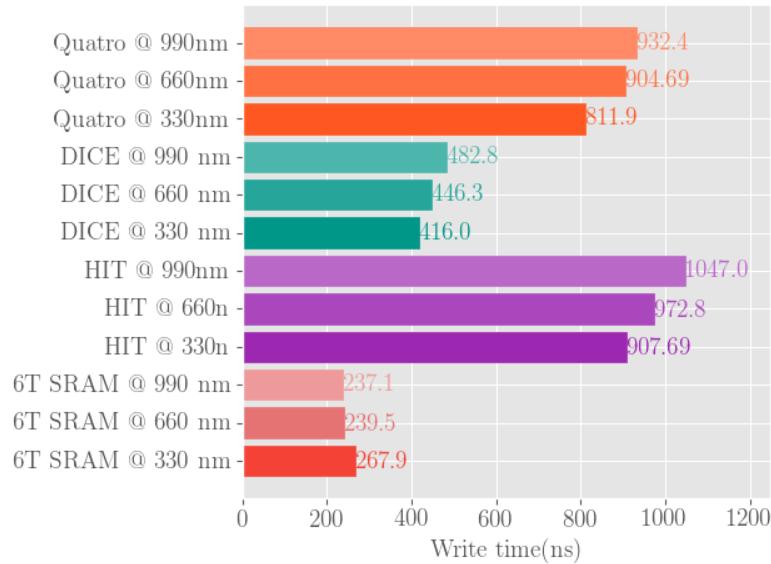


Figure 5.14: Write time comparison

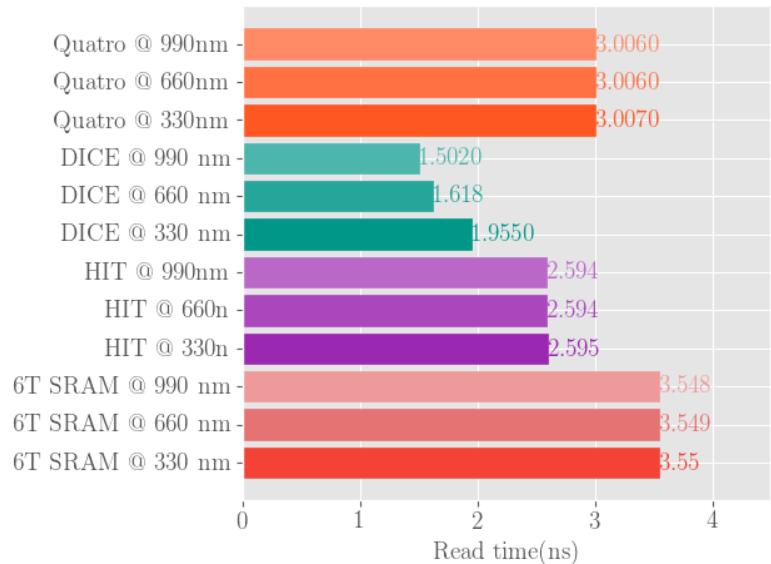


Figure 5.15: Read time comparison

Both HIT and Quatro memory cells have a write time higher than DICE and 6T-SRAM due to its extra radiation hardening circuitry. Instead, the DICE memory cell has a write time similar to the 6T SRAM memory cell because both share the same node capacity.

5.5.3 Power consumption

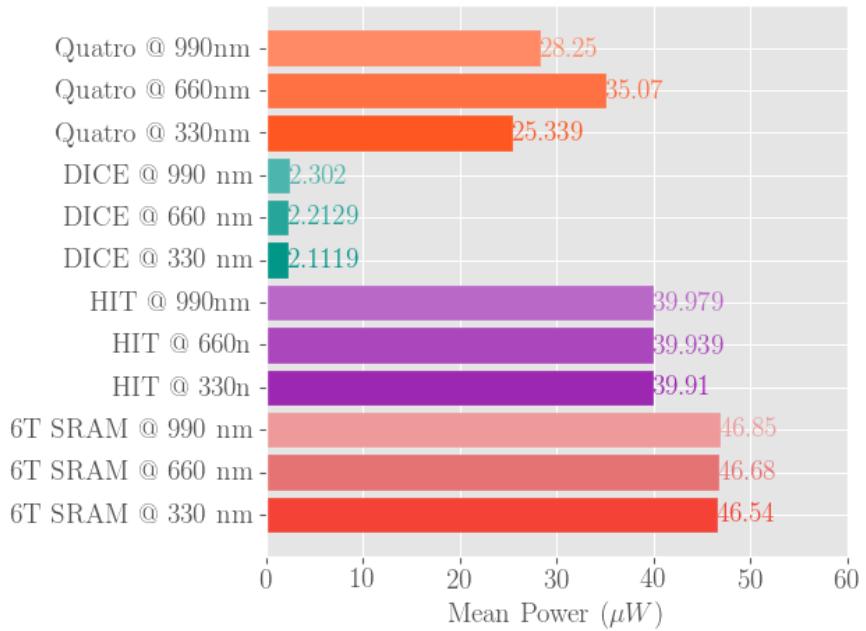


Figure 5.16: Mean power comparison

In Figure [5.16], it can be seen a slight trend to increase the mean power when the memory cells are resized. Also, the DICE is the memory cell with smallest mean power due to its structure [19].

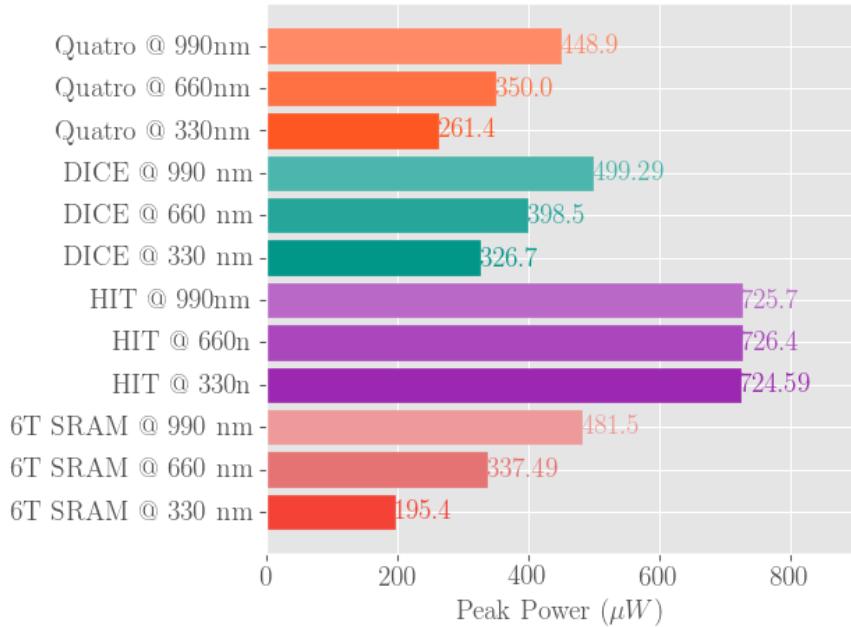


Figure 5.17: Peak power comparison

5.5.4 Area

5.5.4.1 Selected memory cell

According to the results obtained and previously exposed, the HIT has been discarded due to its speed and power overhead. Similarly, the Quatro memory cell has a well radiation hardened performance, but only can recover $1 \rightarrow 0$ bit-flips. Instead, the DICE memory cell is the strongest memory cell under study against radiation. Also, its overhead is not significant and in some cases improves the 6T-SRAM features. For these reason, the DICE memory cell has been selected to compare its area with the standard 6T SRAM.

5.5.4.2 6T-SRAM

In the following figure depicts the layout of a 6T-SRAM memory cell: As shown in previous

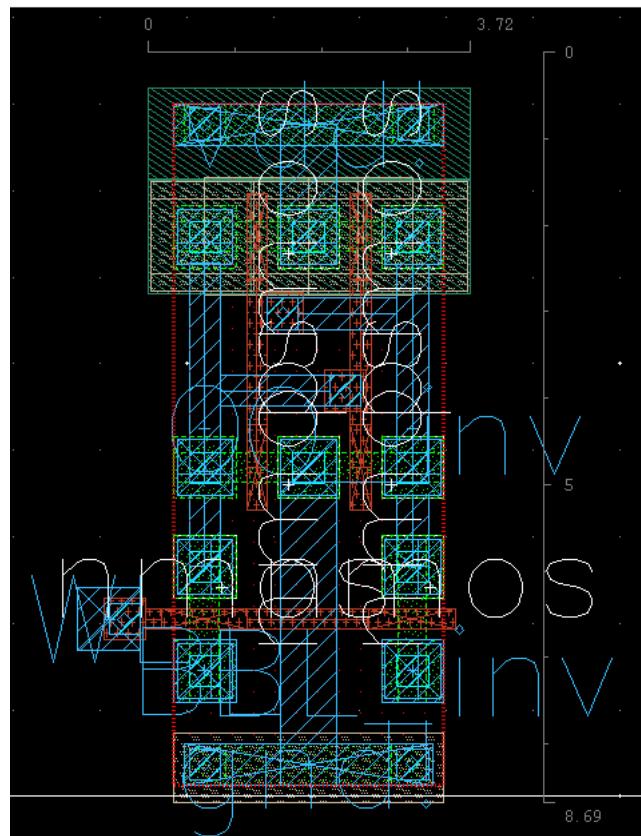


Figure 5.18: 6T SRAM layout

figure, the area of 6T-SRAM memory cell is equal to:

$$Area_{6T-SRAM} = 3.72 \mu m \cdot 8.69 \mu m = 32.33 \mu m^2 \quad (5.13)$$

5.5.4.3 DICE

The layout of DICE memory cell is: And its area is equal to:

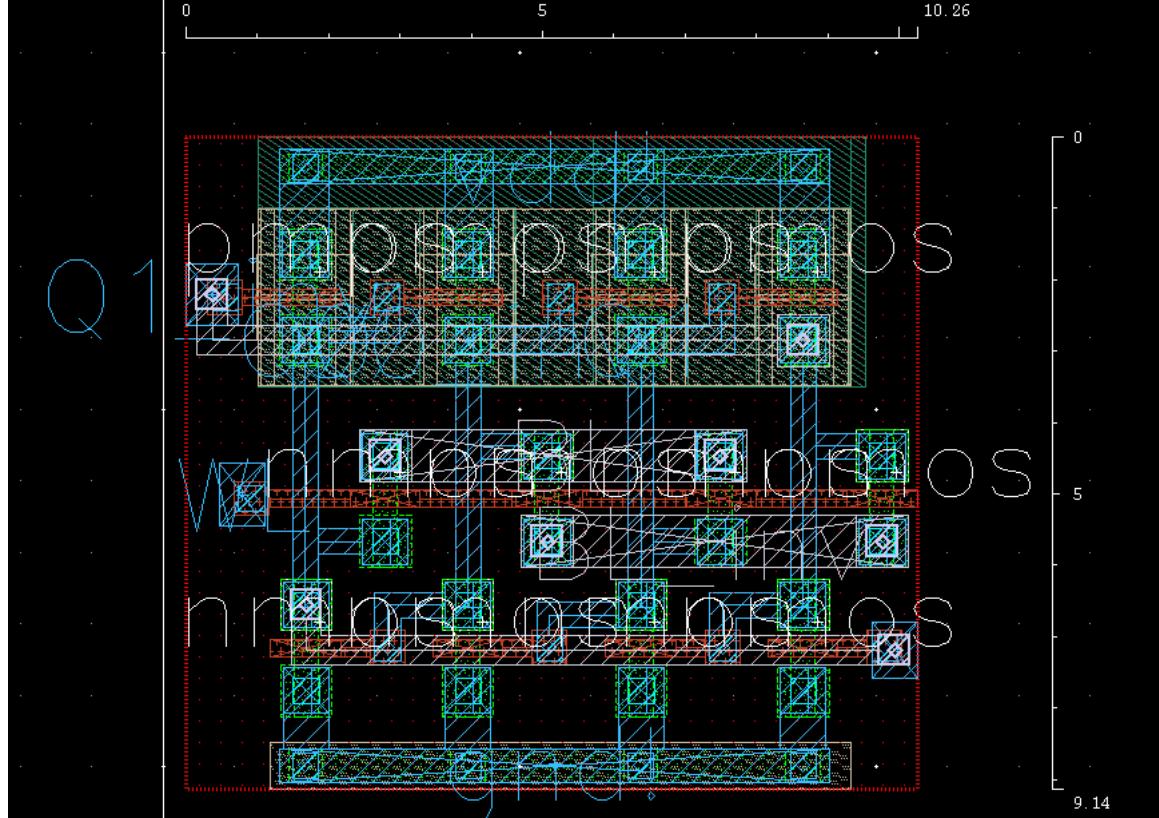


Figure 5.19: DICE layout

$$Area_{DICE} = 10.26 \mu m \cdot 9.14 \mu m = 93.78 \mu m^2 \quad (5.14)$$

Being the ratio between this memory cell and 6T-SRAM:

$$r = \frac{Area_{DICE}}{Area_{6T-SRAM}} = \frac{93.78 \mu m^2}{32.33 \mu m^2} \approx 2.90 \quad (5.15)$$

5.5.4.4 Array memory 2x2

The DICE memory cell can be extend in two dimensions to create a entire memory array easily. In Figure 5.20 is shown a DICE Memory Array of 2x2:

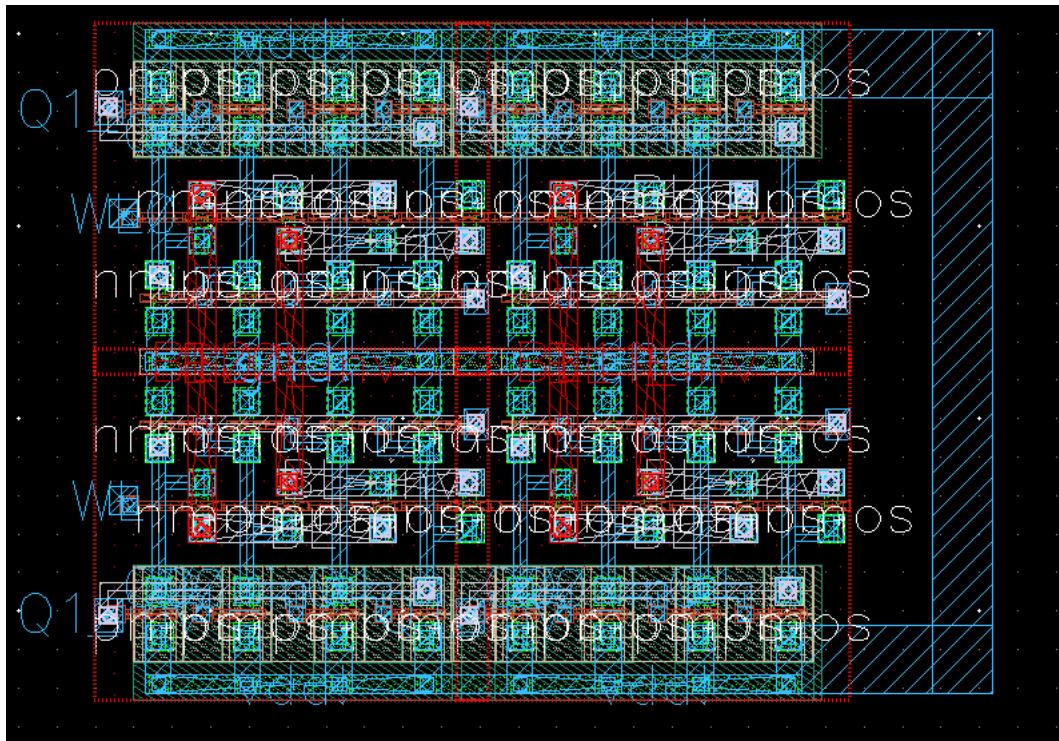


Figure 5.20: DICE 2x2 Memory Array

6 Concluding Remarks and Future Work

6.1 Conclusions

In this project, it has been studied the radiation effects in electronic systems and focusing on radiation effects that lead bit-flips in memory cells. The state-of-art of RHBD memory cells has been analyzed, and implemented a set of this RHBD Memory cells in IHP Technology, SGB25V, with the purpose of comparing its performance and its radiation robustness. Once the different RHBD memory cells has been compared, it has been selected one of them and developed its layout to compare with the layout of 6T-SRAM memory cell. A lower area ratio, r has been obtained, so this implementation has a lower area overhead in comparison with the use of a TMR solution. The performances obtained are consistent with the expected results, [21].

6.2 Future work

- This project is just focus in the radiation-effects in memory cells, but a memory is compound by external circuitry (as shown in [Fig. 3.5]) that is susceptible to radiation effects also. For this reason, a future line of work is the study of radiation effects on external circuitry to harden the entire memory system.
- As mentioned in previous chapters, the radiation hardened systems aimed to space applications, depend on the space mission itself. Another future work is the design of radiation hardened memory cell aimed to a particular mission to optimize.

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