Assignment No. -1

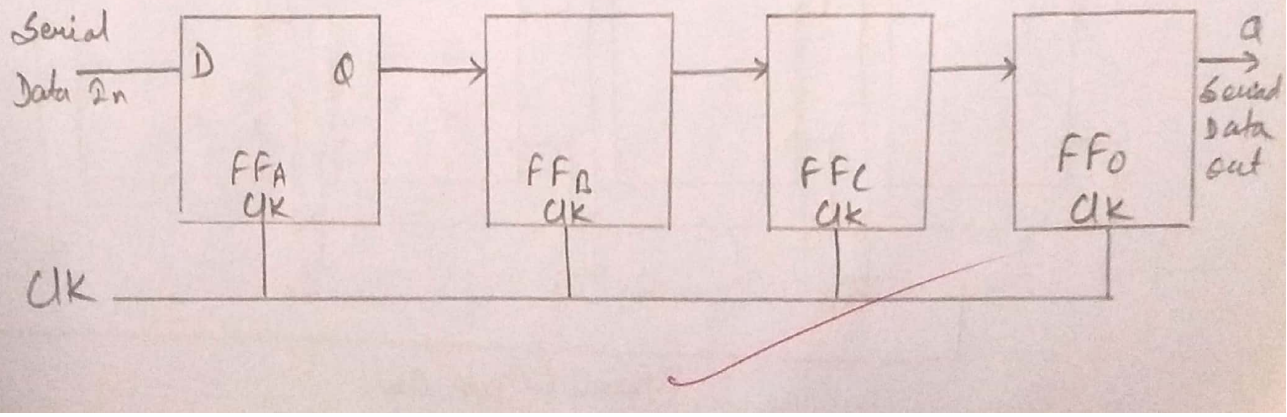
SHIFT REGISTORS

Objective: To design a registor circuit.

Theory: A registor is a group of binary cells suitable for including binary information. The information stored within the registors can be transfered with the help of shift registors. Shift registors are a groups of flip-flops used to store multiple bits of data. The bits stored in such registors can be made to move within and in/out of registors through clock pulses.

Serial In Serial Out Registor (SISO)

The circuit consists of four D-flip-flops connected in a serial manner. All the flip-flops are synchronious with each other since the same clock signal is provided to each flip-flop. The main use of SISO registor is as a delay element.



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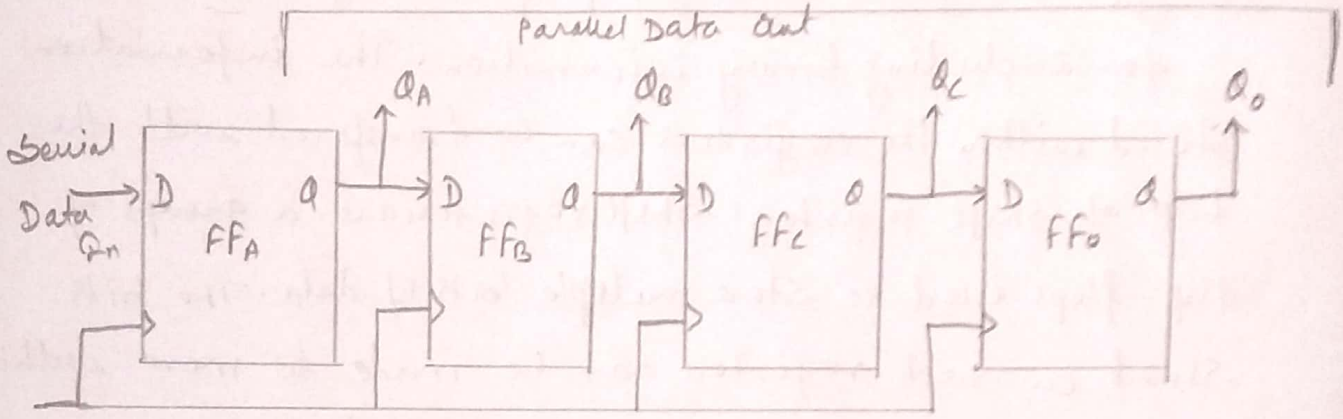
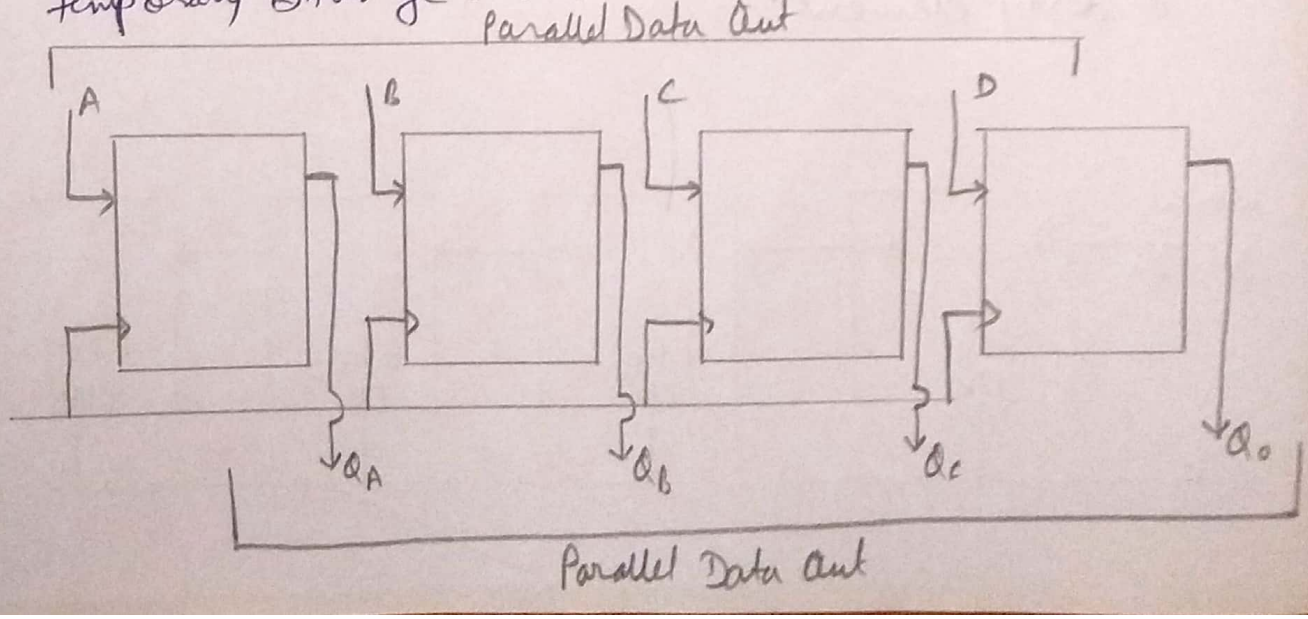
Serial In Parallel Out Register (SIPO)

This shift register allows serial input (one bit after the other through a single data line) and produces a parallel output is known as Serial In Parallel Out register. The main use of SIPO register is to convert Serial Data into Parallel Data.



Parallel In Parallel Out Register (PIPO)

The shift register which allows parallel input to each flip-flop (seperately) and in a simultaneous manner and also produces a parallel output is called Parallel In Parallel Out Shift registers. Its main use is as a temporary storage device.



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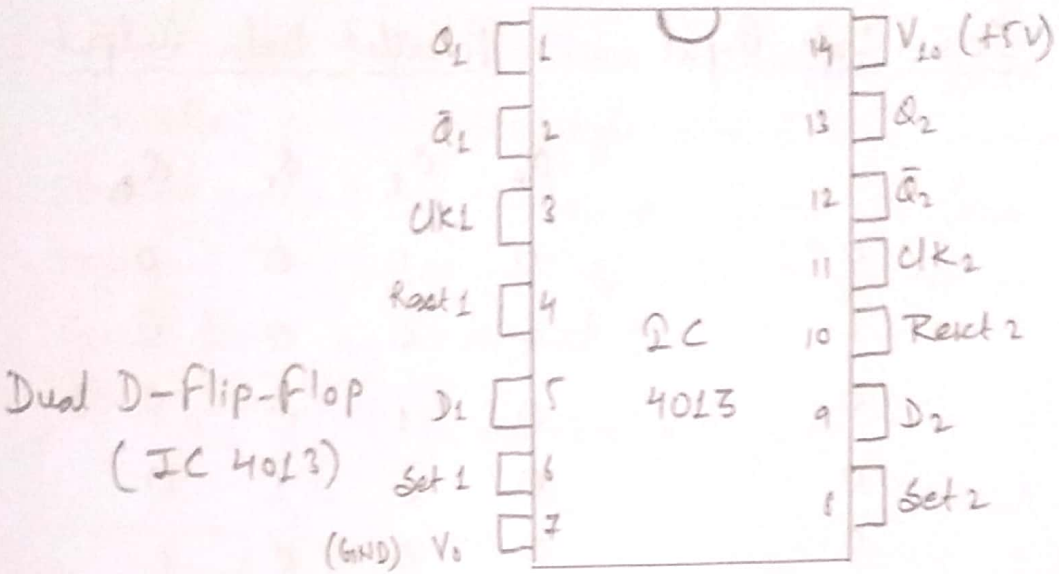
Pin Diagram :



Materials Required :

* Digital Trainer kit
* Wires
* Dual D - flip flop (IC 4013) X2

Verification Table :

* Serial In Serial Out (SISO) Register

Clk	Serial Data Input (D)	Serial Data Output (Q)
0	1	0
1	0	0
2	0	0
3	0	0
4	0	1
5	0	0

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* Serial In Parallel Out (SIPO) Register.

Clk	Serial Data Input	Parallel Data Output			
		Q_A	Q_B	Q_C	Q_D
0	0	0	0	0	0
1	1	1	0	0	0
2	0	0	1	0	0
3	0	0	0	1	0
4	0	0	0	0	1
5	0	0	0	0	0

* Parallel In Parallel Out (PIPO) Register

Clk	Parallel Data Input				Parallel Data Output			
	A	B	C	D	Q_A	Q_B	Q_C	Q_D
0	0	0	0	0	0	0	0	0
1	1	0	0	0	1	0	0	0
2	0	0	0	0	0	1	0	0
3	0	0	0	0	0	0	1	0
4	0	0	0	0	0	0	0	1
5	0	0	0	0	0	0	0	0

Conclusion :-

Registors are a very widely used component and a very integral part of modern day electronics with its applications ranging from holding data instructions and memory address in a CPU to lighting components as well as telecommunication devices.

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Assignment No. – 02 (CO-02)

AIM :- To design of an adder-substractor composite circuit.

Theory :- The 4-bit adder-Sustractor composite circuit performs the operation of both addition and Sustraction. It has two 4-bits inputs $A_3 A_2 A_1 A_0$ and $B_3 B_2 B_1 B_0$. The Mode Select line (M) is connected with the C_{in} of the least significant bit of the Full-adder, is used to perform the operation of addition and sustraction. The XOR gates are used as controlled inverter.

Adders are part of the arithematic and logic unit (ALU).

Components Required :-

1.) IC 4070
2.) IC 4008
3.) Digital Trainer kit
4.) Breadboard
5.) Wires.

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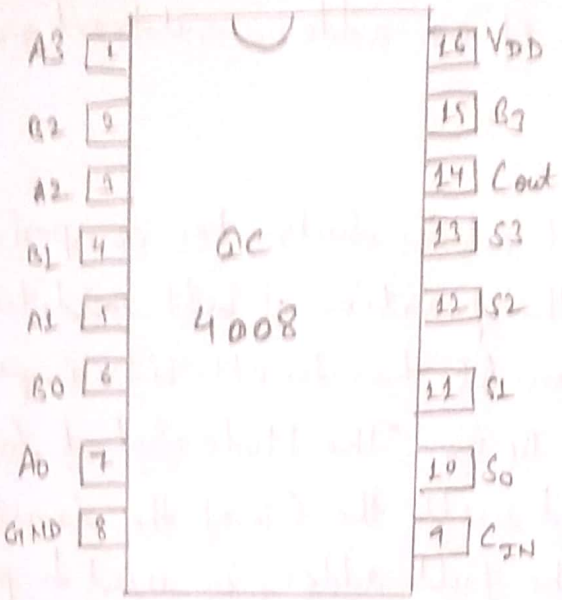
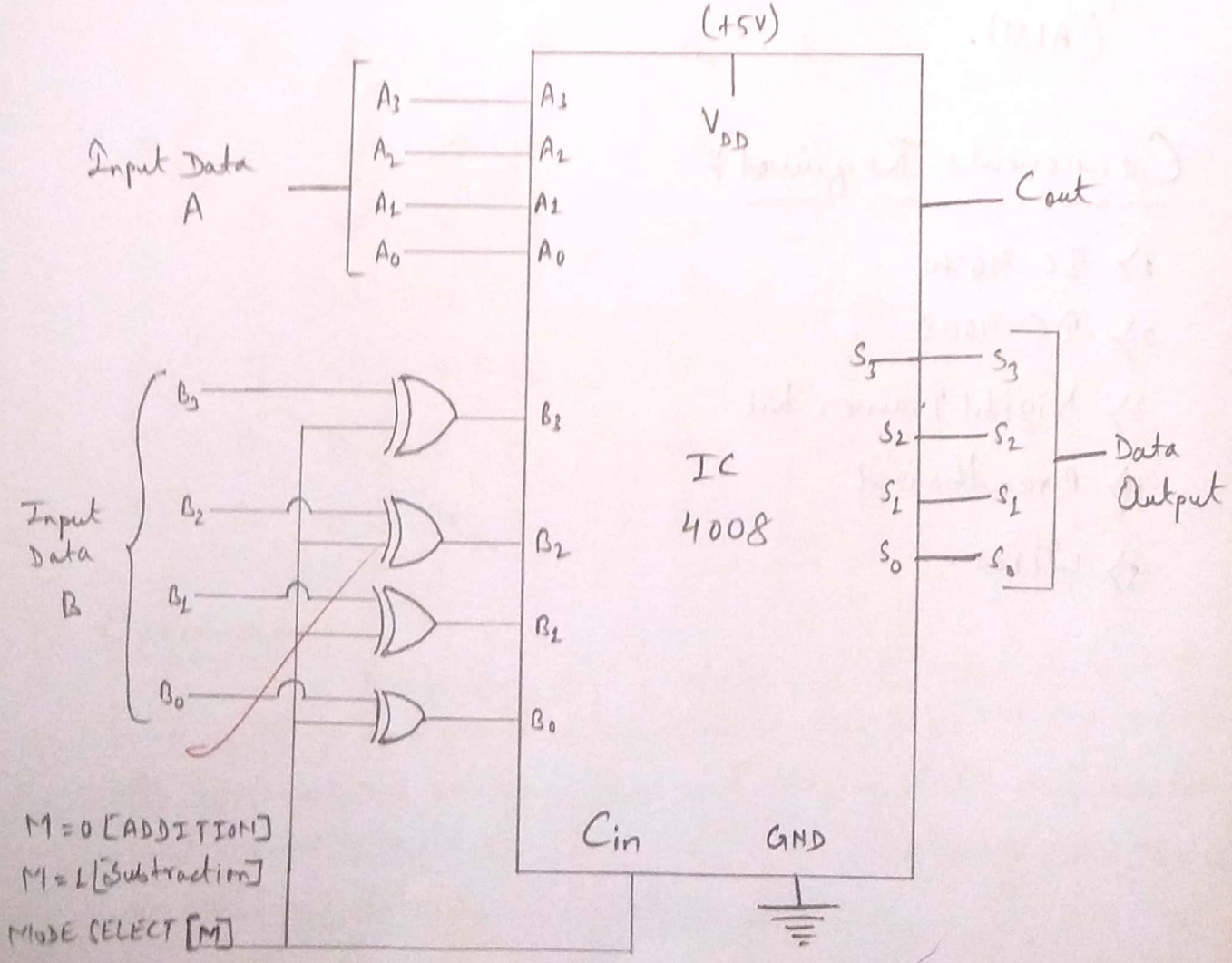
Pin Diagram :-



4-bit Binary Full Adder.

Circuit Diagram :-



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Truth Table :-

Mode Selection	A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0	Cout	S_3	S_2	S_1	S_0
0	0	0	1	0	0	0	1	0	0	0	1	0	0
0	1	0	1	0	1	0	1	0	1	0	1	0	0
0	1	1	0	0	0	0	1	1	0	1	1	1	1
1	1	1	0	0	0	0	1	1	0	1	0	0	1
1	1	0	1	0	0	0	0	1	0	1	0	0	1
1	1	0	0	1	0	0	1	1	0	0	1	0	1

Conclusion :-

4-bit adder-subtractor composite circuit was implemented and truth table is verified.

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Experiment No. – 03.

Objective: To design the circuit for a BCD Adder.

Theory: In computing and electronic systems, binary-coded decimal (BCD) is a class of binary encodings of decimal numbers where each decimal digit is representated by a fixed number of bits. A BCD adder is a circuit that adds two BCD digits in parallel and produces a sum digit which is also in BCD. This circuit includes correction logic. For Sum > 9 the circuit need to add 2's complement of 10_{10} $(0110)_2$ to the uncorrected result $(S_3' S_2' S_1' S_0')$. Correction is also needed when a Carry out (C_0) is generated (for numbers 16-19).

Components Required:

* IC 4008
* IC 4071
* IC 4081
* Digital Trainer kit
* Breadbroad
* Wires.

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Decimal to BCD Table :-

Decimal	Binary Sum					BCD Sum				
	C_{out}'	S_3'	S_2'	S_1'	S_0'	C_{out}	S_3	S_2	S_1	S_0
0		0	0	0	0		0	0	0	0
1		0	0	0	1		0	0	0	1
2		0	0	1	0		0	0	1	0
3		0	0	1	1		0	0	1	1
4		0	1	0	0		0	1	0	0
5		0	1	0	1		0	1	0	1
6		0	1	1	0		0	1	1	0
7		0	1	1	1		0	1	1	1
8		1	0	0	0		1	0	0	0
9		1	0	0	1		1	0	0	1
10		1	0	1	0	1	0	0	0	0
11		1	0	1	1	1	0	0	0	1
12		1	1	0	0	1	0	0	1	0
13		1	1	0	1	1	0	0	1	1
14		1	1	1	0	1	0	1	0	0
15		1	1	1	1	1	0	1	0	1
16	1	0	0	0	0	1	0	1	1	0
17	1	0	0	0	1	1	0	1	1	1
18	1	0	0	1	0	1	1	0	0	0
19	1	0	0	1	1	1	1	0	0	1

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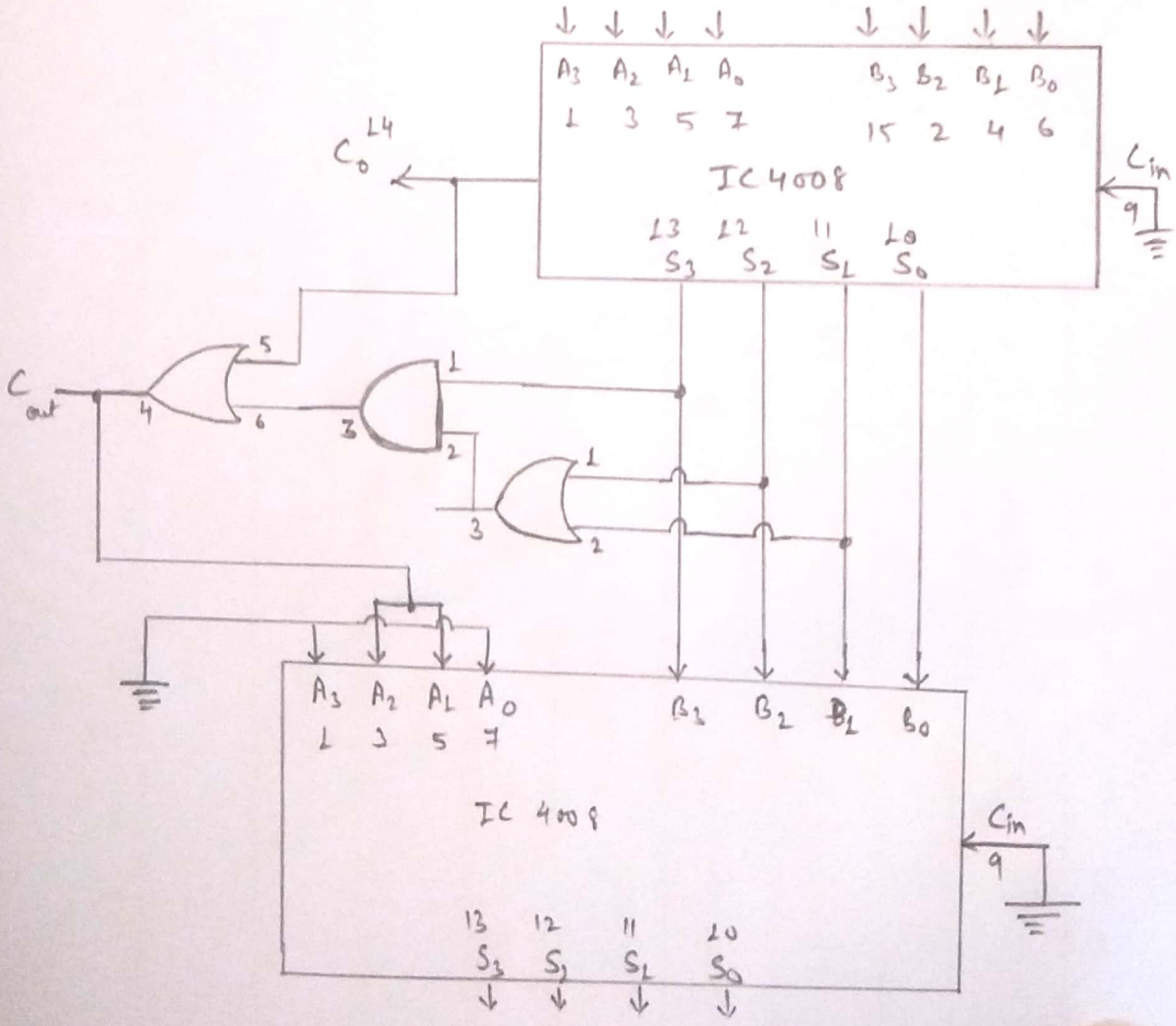
K-map for BCD Adder :-

$S_3'S_2'$ \ $S_1'S_0'$	00	01	11	10
00	0	1	3	2
01	4	5	7	6
11	12	13	15	14
10	8	9	11	10

$$C_{out} = C_0 + S_3' \cdot S_2' + S_3' \cdot S_1'$$

$$C_{out} = C_0 + S_3' \cdot (S_2' + S_1')$$

Circuit Diagram :-



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Truth Table :-

Input								Output				
A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0	Cout	S_3	S_2	S_1	S_0
0	0	1	1	0	0	1	0	0	0	1	0	1
0	0	1	0	0	1	0	0	0	0	1	1	0
1	0	1	0	0	1	0	1	1	0	1	0	1
0	1	1	0	1	1	0	0	1	1	0	0	0

Conclusion :-

BCD adder circuit is made and truth table is verified.

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Experiment No. – 4(a).

TITLE :- Design a Composite Logic Unit using Multiplexer.

Objective :- To design a Composite Logic Unit using a Multiplexer.

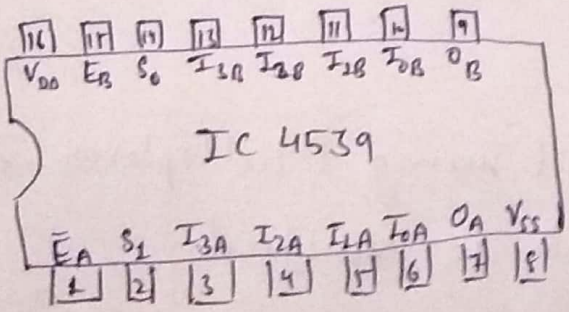
Components Required :-

XOR gate, AND gate, OR gate, NOT gate, Multiplexer.

Theory :-

Logic microoperations are very useful for manipulating individual bits or a portion of word stored in a register. They can be used to change bit value, detect group of bits or insert new bit values into a register. These microoperations require different logic gates to be inserted for each bit or pair of bit in a register to perform the required operation. Although there are several logic micro-operation, most computers use only four AND, OR, XOR and NOT from which all others are derived.

Pin Diagram :-



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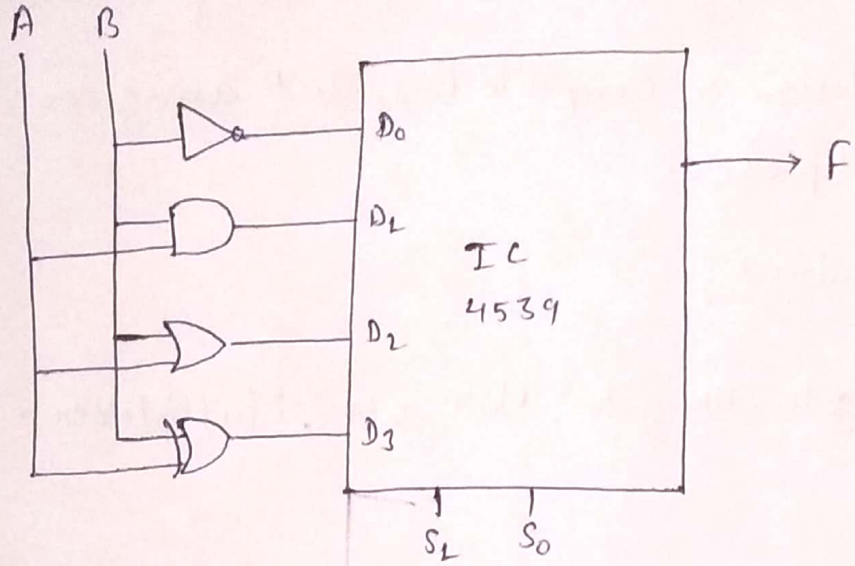
Circuit Diagram :



Observation Table :

Select Lines		Inputs		Output (F)	Operation
S_1	S_0	A	B		
0	0	0	1	0	NOT
0	1	1	1	1	AND
1	0	1	0	1	OR
1	1	0	0	0	XOR
1	1	1	1	0	XOR
0	1	1	0	0	AND.

Conclusion :

Composite Logic Unit using Multiplexer is implemented and observation table is verified.

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Experiment No.- 4(b)

Aim:- To design a 4-bit Composite Arithematic Unit using Multiplexer.

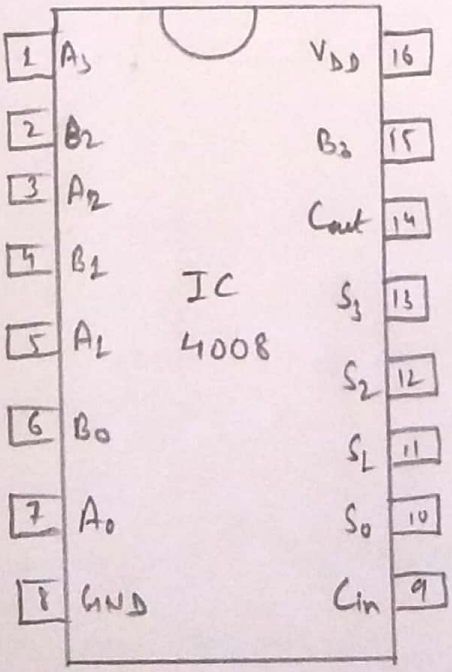
Components Required:-

Trainer kit, NOT Gate (2), 4:1 MUX, IC 4008.

THEORY:-

The Arithematic Unit is also called Arithematic Logic Unit (ALU). It is a part of the CPU. It is often reffered to as Engine of CPU because it allows the computer to perform mathematical calculation. It comprised of many interconnected elements that are designed to perform task.

PIN Diagram:-



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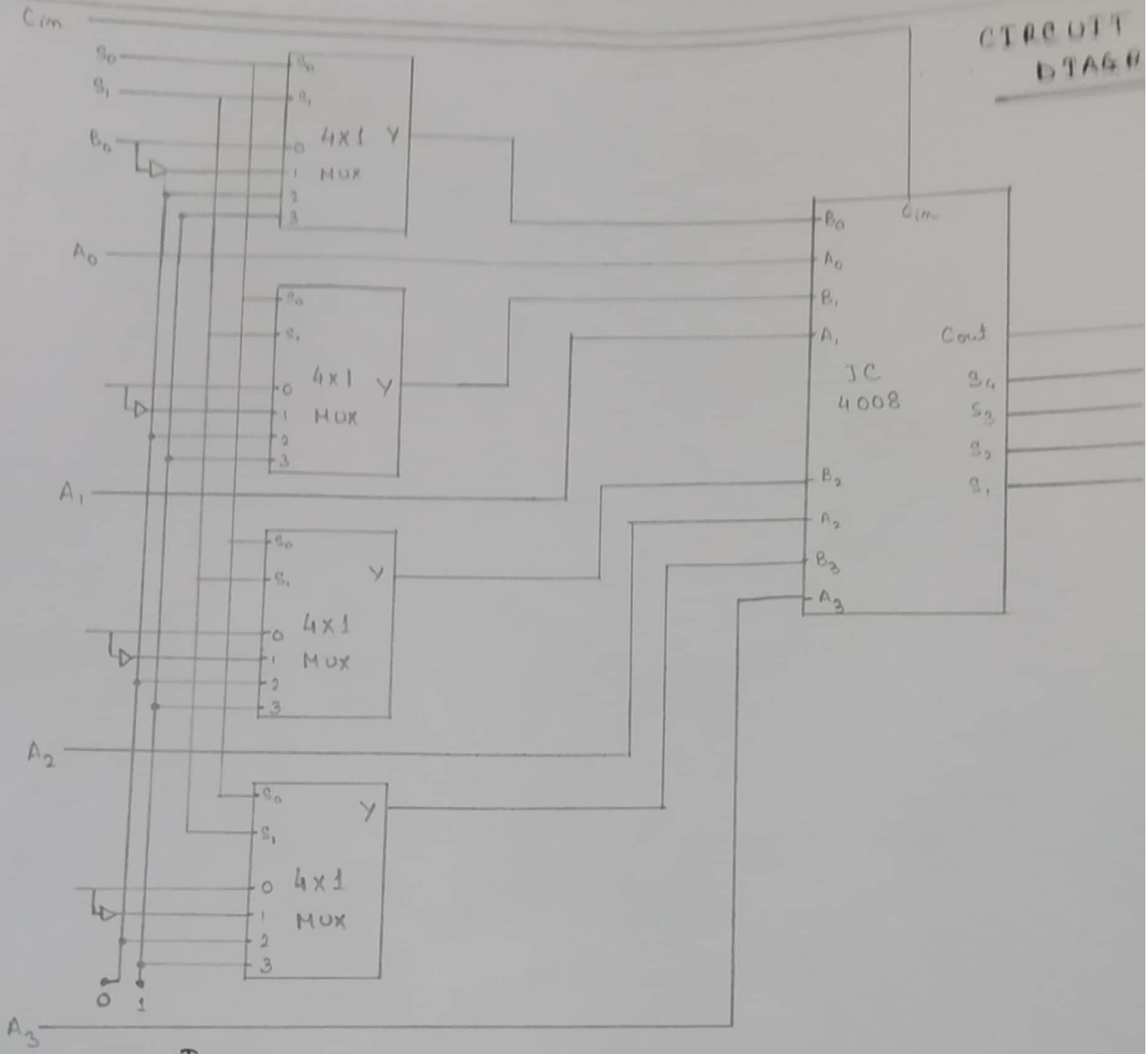
CIRCUIT DIAGRAM



VERIFICATION TABLE

FUNCTION	SELECT INPUTS			INPUT (A)				INPUT (B)				OUTPUT (Y)				
	S_1	S_0	C_{in}	A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0	cout	F_3	F_2	F_1	F_0
Add B to A	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
dd B to A plus 1	0	0	1	1	0	1	0	1	0	1	0	0	1	0	0	1
dd 1's complement B to A	0	1	0	0	0	1	1	0	0	1	0	1	1	0	0	1
dd 2's complement f B to A	0	1	1	1	0	0	1	1	1	1	1	0	1	1	0	1
ransfer A	1	0	0	0	1	1	0	0	1	0	1	1	1	1	0	1
ncrement A	1	0	1	0	1	1	0	0	1	0	1	0	0	1	1	1
crement A	1	1	0	1	1	0	1	1	0	1	0	1	1	1	1	0
ansfer A	1	1	1	1	1	0	0	1	0	1	1	0	1	1	0	0

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Truth Table :-

Function	Select Inputs			Input (A)				Input (B)				Output (F)				
	S_1	S_0	C_{in}	A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0	C_{out}	F_3	F_2	F_1	F_0
Add B to A	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Add B to A plus 1	0	0	1	1	0	1	0	1	0	1	0	0	1	0	0	1
Add 1's complement of B to A	0	1	0	0	0	1	1	0	0	1	0	1	1	0	0	1
Add 2's complement of B to A	0	1	1	1	0	0	1	1	1	1	1	0	1	1	0	1
Transfer A	1	0	0	0	1	1	0	1	1	0	1	1	1	1	0	1
Increment A	1	0	1	1	1	1	0	1	1	0	1	0	0	1	1	1
Decrement A	1	1	0	0	1	0	1	1	1	0	1	0	1	1	1	0
Transfer A	1	1	1	1	1	0	0	0	0	1	1	0	1	1	0	0

Conclusion :-

4 bit ~~arith~~ Arithmetic logic unit using Multiplexer is implemented and hence, the truth is verified.

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