MT3620
Datasheet

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Document Revision History

Revision	Date	Description
0.5	19 September 2017	Initial release.
0.6	28 September 2017	Revisions.
0.61	2 November 2017	Revisions.
0.62	7 November 2017	Revisions.
0.63	8 November 2017	Minor revisions.
0.64		
0.65	27 November 2017	Minor revisions.
0.66	19 December 2017	Revisions.
0.67	20 December 2017	Revisions.
0.68	29 December 2017	Revisions.
0.69	2 January 2018	Reviewed changes and fixed typographical errors.
0.70	2 January 2018	Clarifications and edits.
0.71	15 January 2018	Accepted changes, deleted comments; refined GPIO section.
0.72	19 January 2018	Altered minimum battery backup voltage to 2.5v.
0.73	19 January 2018	Simplified power consumption table.
0.74	9 February 2018	Update the Wi-Fi 2.4G/5G specification table.
0.75	16 March 2018	Listed 1.2kbps UART support and changed ADC reference minimum from 1.6V to 1.8V.
0.76	4 April 2018	Removed references to A0 and fixed a couple of typos.
09.77	5 April 2018	Fixed formatting errors in WiFi performance section. Moved SERVICE UART pins to correct section of pin description table.
0.78	24 May 2018	Fixed Wi-Fi channel bandwidth mismatched statement.
1.0	10 September 2019	Refined for public release
1.1	25 September 2019	Correct operation temperature range and update current consumption data
1.2	25 December 2019	Update Crystal Oscillator requirement

Table of Contents

Figure / Table List

1 System Overview

1.1 General Description

MT3620 is a highly integrated single chip tri-core MCU designed to meet the requirements of modern, robust internet-connected devices. It leverages the Microsoft Azure Sphere security architecture to provide an unprecedented level of security to connected device manufacturers. For the lifetime of the device the Azure Sphere system provides device authentication and attestation, supports remote over-the-air software updates to maintain security in the face of evolving attacks, and automates error logging and reporting. Please refer to the "Azure Sphere Platform Overview" document from Microsoft for more information.

MT3620 features an application processor subsystem based on an ARM Cortex-A7 core which runs at up to 500MHz. The chip also includes two general purpose ARM Cortex-M4F I/O subsystems, each of which runs at up to 200MHz. These subsystems were designed to support real-time requirements when interfacing with a variety of on-chip peripherals including UART, I2C, SPI, I2S, and ADC. They are completely general-purpose Cortex-M4F units which may be tailored to specific application requirements. On-chip peripherals may be mapped to any of the three end-user accessible cores, including the CA7.

In addition to these three end-user accessible cores, MT3620 contains a security subsystem with its own dedicated CM4F core for secure boot and secure system operation. There is also a Wi-Fi subsystem controlled by a dedicated N9 32-bit RISC core. This contains a 1x1 dual-band 802.11a/b/g/n radio, baseband and MAC designed to support both low power and high throughput applications without placing computational load on the user-accessible cores.

MT3620 also includes over 5MB of embedded RAM, split among the various cores. There is a fully-integrated PMU and a real-time clock. Flash memory is integrated in the MT3620 package; see section 1.4 for ordering information. Please refer to the "Azure Sphere MT3620 Support Status" document from Microsoft for information about how much memory and which hardware features are available to end-user applications. Only hardware features supported by the Azure Sphere system are available to MT3620 end-users.

1.2 Main Features

1.2.1 Platform

- ARM Cortex A7 with NEON and FPU support and 64kB L1 instruction cache, 32kB L1 data cache, 256kB L2 cache, and 4MB system memory for the Azure Sphere operating system and user applications; ideal for high-level user code
- Two general purpose ARM Cortex M4 cores, each with 192kB TCM, 64kB SRAM, and integrated FPU; ideal for real-time control requirements
- In-package serial flash; see Section 1.4 for details
- User-accessible cores support execute-in-place (XIP) from flash
- Five "ISU" serial interface blocks which can be configured as I2C master. I2C slave, SPI master, SPI slave, or UART; I2C runs at up to 1MHz, SPI at up to 40MHz, and UARTs at up to 3Mbps
- Two I2S interfaces supporting slave and TDM slave modes
- Eight-channel, 12-bit, 2MS/s single-ended successive approximation ADC using internal 2.5V or external 1.8V reference
- 76 programmable GPIO pins with programmable drive strength (some multiplexed with other functions)
- 12 PWM outputs

- 24 external interrupt inputs
- Six hardware counter blocks which can count and measure pulses and perform quadrature decoding
- RTC can run from dedicated 32 kHz external input, from on-die 32 kHz oscillator, from on-die ring oscillator, or from main oscillator
- One-time programmable e-fuse block for storing chip-specific information
- Two additional, dedicated UARTs, one for each CM4F I/O subsystem
- Per-core watchdog timers
- Per-core general-purpose timers

1.2.2 Pluton Security Subsystem

- Provides security and secure power management for entire chip
- Dedicated ARM Cortex-M4F security processor with 128kB secured TCM and 64kB secured mask ROM bootloader
- Microsoft Azure Sphere Pluton security engine provides cryptographic engines and hardware root of trust
- Hardware random number generator with entropy monitoring system to ensure true random numbers
- Side-channel attack and tampering counter-measures
- Dedicated, secure one-time programmable e-fuse block for storing security-related configuration information
- Provides secure boot via ECDSA, hardware support for remote attestation and certificate-based security

1.2.3 Wi-Fi

- Dedicated high-performance N9 32-bit RISC core
- Dedicated one-time programmable e-fuse block for storing Wi-Fi specific calibration and configuration information
- IEEE 802.11 a/b/g/n compliant
- Supports 20MHz bandwidth in 2.4GHz band and 5GHz band
- Dual-band 1T1R mode
- Supports STBC, LDPC, explicit beamforming as the beamformee
- Greenfield, mixed mode, legacy modes support
- IEEE 802.11 d/e/h/i/k/r/w support
- Security support for WFA WPA/WPA2 personal, WPS2.0, WAPI
- Supports 802.11w protected managed frames
- QoS support of WFA WMM, WMM PS
- Integrated LNA, PA, and T/R switch
- Built-in RX diversity support
- Full TX/RX antenna diversity support via external DPDT switch
- Optional external LNA and PA support
- Multiple external support component configuration options for BoM flexibility

1.2.4 Power Management and Clock Sources

- Integrated high efficiency power management unit with single 3.3V power supply input

- Integrated under-voltage lockout, three low drop-out (LDO) regulators and a high efficiency buck converter
- Integrated comparator for supply brown-out detection with configurable threshold
- 26MHz crystal clock support with low power operation mode
- 32kHz crystal real-time clock with external battery-backup supply

1.2.5 Management Interfaces

- 'Recovery' UART for re-loading device firmware
- 'Service' UART for in-production and in-field firmware update and device management

1.2.6 Technology and Package

- Highly integrated 40nm RFCMOS technology
- System-in-package (SIP) serial flash
- 12mm x 12mm 164 pin DR-QFN package
- Designed to support 4-layer PCB construction based on widely supported PCB design rules
- RoHS compliant

1.3 MT3620 Block Diagram

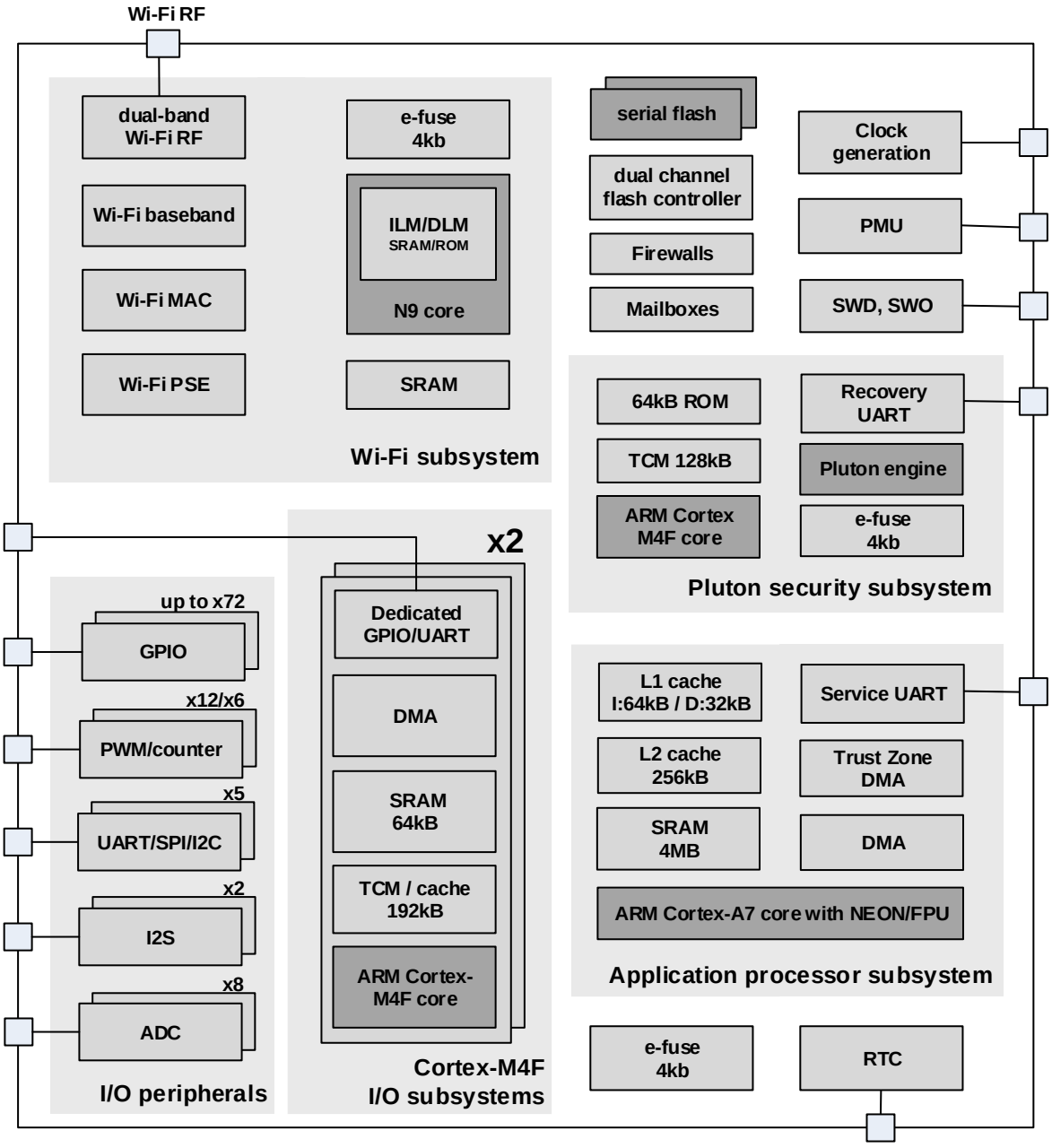


Figure 1. MT3620 Block Diagram

1.3.1 Block Diagram Acronyms

PSE	Wi-Fi packet switch engine	PMU	Power management unit	PWM	Pulse-width modulation
TCM	Tightly-coupled memory	RTC	Real-time clock	GPIO	General purpose input/output
ILM	Instruction local memory	DMA	Direct memory access	FPU	Floating point unit
DLM	Data local memory	I2C	Inter-IC communications	I2S	Inter-IC sound
ADC	Analog to digital converter	NEON	Arm's single instruction multiple data architecture	UART	Universal asynchronous receiver/transmitter

PSE	Wi-Fi packet switch engine	PMU	Power management unit	PWM	Pulse-width modulation

1.4 Ordering information

Part number	Total flash	Flash configuration
MT3620AN	16MB	2x 8MB dual channel quad SPI

2 Application Support

2.1 Application development

MT3620 was designed in close cooperation with Microsoft as part of the Microsoft Code-name 4x4 security system. Whilst the Cortex-A7 application processor must always run the Azure Sphere secure OS supplied by Microsoft, it is also available for running a custom user-mode application hosted by the secure OS. Microsoft provides a powerful development environment based on the gcc compiler which includes a Visual Studio extension, allowing this application to be developed in C. Visual Studio debugging, including features such as single-step execution, breakpoints, and watchpoints are supported using a SLIP interface to the CA7 via a dedicated Azure Sphere service UART.

In addition to the Cortex-A7 application processor subsystem, MT3620 includes two Cortex-M4F I/O subsystems. The two M4F I/O subsystems are primarily intended to support real-time I/O processing but can also be used for general purpose computation and control. The M4F cores may run any end-user-provided operating system, or run a 'bare metal app' with no operating system.

Debugging on the I/O subsystems is supported through a shared multi-core SWD channel with SWO support. There is also optional support for higher bandwidth trace via a 16-bit ARM TPIU interface. Each Cortex-M4F core also has a dedicated UART which can be used to support debugging if necessary.

Operation of MT3620 security features and Wi-Fi networking is isolated from, and runs independently of, end user applications. As such, security features and Wi-Fi are only accessible via defined APIs and are robust to programming errors in end-user applications regardless of whether these applications run on the CA7 or the user-accessible CM4F cores.

2.2 Hardware config & control

Microsoft-provided libraries support a variety of functions including hardware configuration, network communication, and use of the MT3620 peripherals. Please refer to the latest "Azure Sphere MT3620 Support Status" document from Microsoft for information about currently supported hardware configurations, network communications, and peripherals. Note that due to the secure nature of the Azure Sphere system, features not yet supported by Microsoft are not available by any other means.

2.3 RF testing support

MT3620 can enter a radio test mode that allows test lab personnel or automated test equipment to set low-level radio parameters and transmit and receive custom test signals and packets. This functionality is suitable for radio emissions compliance testing of an MT3620-based product.

The MT3620 radio test mode can also be used to support per-device production line Wi-Fi calibration and test. Production test RF equipment from test equipment suppliers such as LitePoint will include support for MT3620.

2.4 Manufacturing test support

MT3620 allows manufacturers to create custom manufacturing test applications using the same application development tools used to create end-user applications. These test applications support in-circuit functional testing during manufacturing. Microsoft will provide documentation and utilities to allow these tests to integrate with factory processes.

3 Radio Characteristics

3.1 Wi-Fi Radio Characteristics

3.1.1 Wi-Fi 2.4GHz Band RF Receiver Specifications

The specification in table below is measured at the antenna port, which includes the frond-end loss.

Table 1. 2.4GHz RF Receiver Specification

Parameter	Description		Performance			
		MIN	TYP		MAX	Unit
			Main	Aux		
Frequency range	Center channel frequency	2412			2484	MHz
RX sensitivity	DBPSF, 1 Mbps DSSS	-	-94.6	-97.1	-90.0	dBm
	DQPSF, 2 Mbps DSSS	-	-91.6	-94.1	-87.0	dBm
	DQPSF, 5.5 Mbps CCK	-	-89.6	-92.1	-85.0	dBm
	DQPSF, 11 Mbps CCK	-	-86.6	-89.1	-82.0	dBm
	BPSK rate 1/2, 6 Mbps OFDM	-	-91.6	-94.1	-87.0	dBm
	BPSK rate 3/4, 9 Mbps OFDM	-	-89.3	-91.8	-86.0	dBm
	QPSK rate 1/2, 12 Mbps OFDM	-	-88.5	-91.0	-84.0	dBm
	QPSK rate 3/4, 18 Mbps OFDM	-	-86.1	-88.6	-82.0	dBm
	16QAM rate 1/2, 24 Mbps OFDM	-	-82.8	-85.3	-81.0	dBm
	16QAM rate 3/4, 36 Mbps OFDM	-	-79.4	-81.9	-78.0	dBm
	64QAM rate 1/2, 48 Mbps OFDM	-	-75.2	-77.7	-73.0	dBm
	64QAM rate 3/4, 54 Mbps OFDM	-	-73.9	-76.4	-71.0	dBm
RX Sensitivity BW=20MHz Mixed mode 800ns Guard Interval Non-STBC	MCS 0, BPSK rate 1/2	-	-90.9	-93.4	-87.0	dBm
	MCS 1, QPSK rate 1/2	-	-87.7	-90.2	-86.0	dBm
	MCS 2, QPSK rate 3/4	-	-85.3	-87.8	-84.0	dBm
	MCS 3, 16QAM rate 1/2	-	-82.3	-84.8	-81.0	dBm
	MCS 4, 16QAM rate 3/4	-	-78.8	-81.3	-77.0	dBm
	MCS 5, 64QAM rate 2/3	-	-74.4	-76.9	-74.0	dBm
	MCS 6, 64QAM rate 3/4	-	-73.0	-75.5	-71.0	dBm
	MCS 7, 64QAM rate 5/6	-	-71.8	-74.3	-69.0	dBm
Maximum Receive Level	1 Mbps DSSS	-20	-10		-	dBm
	11 Mbps CCK	-20	-10		-	dBm
	6 Mbps OFDM	-20	-10		-	dBm
	54 Mbps OFDM	-20	-10		-	dBm
	HT20 MCS0	-20	-10		-	dBm
	HT20 MCS7	-20	-20		-	dBm
Receive Adjacent Channel Rejection	BPSK rate 1/2, 6 Mbps OFDM	16	34		-	dBm
	BPSK rate 3/4, 9 Mbps OFDM	15	31		-	dBm
	QPSK rate 1/2, 12 Mbps OFDM	13	30		-	dBm
	QPSK rate 3/4, 18 Mbps OFDM	11	27		-	dBm
	16QAM rate 1/2, 24 Mbps OFDM	8	25		-	dBm
	16QAM rate 3/4, 36 Mbps OFDM	4	23		-	dBm
	64QAM rate 1/2, 48 Mbps OFDM	0	22		-	dBm
	64QAM rate 3/4, 54 Mbps OFDM	-1	22		-	dBm
	MCS 0, BPSK rate 1/2	16	33		-	dBm
	MCS 1, QPSK rate 1/2	13	29		-	dBm
	MCS 2, QPSK rate 3/4	11	26		-	dBm
	MCS 3, 16QAM rate 1/2	8	24		-	dBm
	MCS 4, 16QAM rate 3/4	4	20		-	dBm

Parameter	Description		Performance			
		MIN	TYP		MAX	Unit
			Main	Aux		
	MCS 5, 64QAM rate 2/3	0	18		-	dBm
	MCS 6, 64QAM rate 3/4	-1	17		-	dBm
	MCS 7, 64QAM rate 5/6	-2	15		-	dBm
Receiver Residual PER	All rates, -50dBm input power	-	-		0.005	%

3.1.2 Wi-Fi 2.4GHz Band RF Transmitter Specifications

The specification in table below is measured at the antenna port, which includes the front-end loss.

Table 2. 2.4GHz RF Transmitter Specifications

Parameter	Description	Performance			
		MIN	TYP	MAX	Unit
Frequency range		2412	-	2484	MHz
Output power with spectral mask and EVM compliance	1 Mbps DSSS	-	16(1)	-	dBm
	11 Mbps CCK	-	16(1)	-	dBm
	6 Mbps OFDM	-	16(1)	-	dBm
	54 Mbps OFDM	-	16(1)	-	dBm
	HT20 MCS 0	-	16(1)	-	dBm
	HT20 MCS 7	-	16(1)	-	dBm
Output power with spectral mask and EVM compliance (at -40°C and 85°C)	1 Mbps DSSS	-	15(1)	-	dBm
	11 Mbps CCK	-	15(1)	-	dBm
	6 Mbps OFDM	-	15(1)	-	dBm
	54 Mbps OFDM	-	15(1)	-	dBm
	HT20 MCS 0	-	15(1)	-	dBm
	HT20 MCS 7	-	15(1)	-	dBm
TX EVM	1 Mbps DSSS	-	-	-10	dB
	11 Mbps CCK	-	-	-10	dB
	6 Mbps OFDM	-	-	-5	dB
	54 Mbps OFDM	-	-	-25	dB
	HT20, MCS 0	-	-	-5	dB
	HT20, MCS 7	-	-	-28	dB
Output power variation(2)	TSSI closed-loop control across all temperature range and channels and VSWR ≦ 1.5:1.	-1.5	-	1.5	dB
Carrier suppression		-	-	-30	dBc
Harmonic Output Power	2nd Harmonic	-	-45	-43	dBm/MHz
	3nd Harmonic	-	-45	-43	dBm/MHz

Note 1: Low power PA.

Note 2: VDD33 voltage is within ±5% of typical value.

The specification in table below is measured at the antenna port, which includes the front-end loss.

Table 3. 5GHz RF receiver specifications

Parameter	Description		Performance			
		MIN	TYP		MAX	Unit
			Main	Aux		
Frequency range	Center channel frequency	5180	-		5825	MHz
RX sensitivity	BPSK rate 1/2, 6 Mbps OFDM	-	-90.0	-91.5	-86.0	dBm
	BPSK rate 3/4, 9 Mbps OFDM	-	-87.7	-89.2	-85.0	dBm
	QPSK rate 1/2, 12 Mbps OFDM	-	-87.0	-88.5	-83.0	dBm
	QPSK rate 3/4, 18 Mbps OFDM	-	-84.5	-86.0	-81.0	dBm
	16QAM rate 1/2, 24 Mbps OFDM	-	-81.3	-82.8	-75.0	dBm
	16QAM rate 3/4, 36 Mbps OFDM	-	-78.0	-79.5	-72.0	dBm
	64QAM rate 1/2, 48 Mbps OFDM	-	-73.6	-75.1	-70.0	dBm
	64QAM rate 3/4, 54 Mbps OFDM	-	-72.2	-73.7	-68.0	dBm
RX Sensitivity BW=20MHz HT Mixed mode 800ns Guard Interval Non-STBC	MCS 0, BPSK rate 1/2	-	-89.3	-90.8	-86.0	dBm
	MCS 1, QPSK rate 1/2	-	-86.3	-87.8	-84.0	dBm
	MCS 2, QPSK rate 3/4	-	-83.8	-85.3	-82.0	dBm
	MCS 3, 16QAM rate 1/2	-	-80.8	-82.3	-76.0	dBm
	MCS 4, 16QAM rate 3/4	-	-77.3	-78.8	-74.0	dBm
	MCS 5, 64QAM rate 2/3	-	-72.8	-74.3	-72.0	dBm
	MCS 6, 64QAM rate 3/4	-	-71.4	-72.9	-70.0	dBm
	MCS 7, 64QAM rate 5/6	-	-70.2	-71.7	-66.0	dBm
Maximum Receive Level	6 Mbps OFDM	-30	-10		-	dBm
	54 Mbps OFDM	-30	-20		-	dBm
	MCS0	-30	-15		-	dBm
	MCS7	-30	-20		-	dBm
Receive Adjacent Channel Rejection	BPSK rate 1/2, 6 Mbps OFDM	16	24		-	dBm
	BPSK rate 3/4, 9 Mbps OFDM	15	23		-	dBm
	QPSK rate 1/2, 12 Mbps OFDM	13	21		-	dBm
	QPSK rate 3/4, 18 Mbps OFDM	11	19		-	dBm
	16QAM rate 1/2, 24 Mbps OFDM	8	15		-	dBm
	16QAM rate 3/4, 36 Mbps OFDM	4	10		-	dBm
	64QAM rate 1/2, 48 Mbps OFDM	0	5		-	dBm
	64QAM rate 3/4, 54 Mbps OFDM	-1	3		-	dBm
	MCS 0, BPSK rate 1/2	16	24		-	dBm
	MCS 1, QPSK rate 1/2	13	21		-	dBm
	MCS 2, QPSK rate 3/4	11	19		-	dBm
	MCS 3, 16QAM rate 1/2	8	16		-	dBm
	MCS 4, 16QAM rate 3/4	4	12		-	dBm
	MCS 5, 64QAM rate 2/3	0	7		-	dBm
	MCS 6, 64QAM rate 3/4	-1	5		-	dBm
	MCS 7, 64QAM rate 5/6	-2	3		-	dBm
Receiver Residual PER	All rates, -50dBm input power	-	-		0.005	%

3.1.3 Wi-Fi 5GHz Band RF Transmitter Specifications

The specification in table below is measured at the antenna port, which includes the frond-end loss.

Table 4. 5GHz RF Transmitter Specifications

Parameter	Description	Performance			
		MIN	TYP	MAX	Unit
Frequency range		5180	-	5825	MHz
Output power with spectral mask and EVM compliance	6 Mbps OFDM	-	14(1)	-	dBm
	54 Mbps OFDM	-	14(1)	-	dBm
	HT20, MCS 0	-	14(1)	-	dBm
	HT20, MCS 7	-	14(1)	-	dBm

Parameter	Description	Performance			
		MIN	TYP	MAX	Unit
Output power with spectral mask and EVM compliance (at -40°C and 85°C)	6 Mbps OFDM	-	13(1)	-	dBm
	54 Mbps OFDM	-	13(1)	-	dBm
	HT20 MCS 0	-	13(1)	-	dBm
	HT20 MCS 7	-	13(1)	-	dBm
TX EVM	6 Mbps OFDM	-	-	-5	dB
	54 Mbps OFDM	-	-	-25	dB
	HT20, MCS 0	-	-	-5	dB
	HT20, MCS 7	-	-	-28	dB
Output power variation(2)	TSSI closed-loop control across all temperature range and channels and VSWR ≦1.5:1.	-1.5	-	1.5	dB
Carrier suppression		-	-	-30	dBc
Harmonic Output Power	2nd Harmonic	-	-45	-43	dBm/MHz
	3nd Harmonic	-	-45	-43	dBm/MHz

Note 1: Low power PA

Note2: VDD33 voltage is within ±5% of typical value.

3.1.4 Wi-Fi RF Receiver Blocking Specifications

The specification in table below is measured at the antenna port, which includes the front-end loss.

Table 5 RF Receiver Blocking Specifications

Parameter	Description	Performance			
		MIN	TYP	MAX	Unit
Receiver In-band Blocking(1) CW and BT interferers	2.4 GHz CW and BT interfering signal @ ±20MHz offset	-47	-	-	dBm
	2.4 GHz CW and BT interfering signal @ ±25MHz offset	-40	-	-	dBm
	5 GHz CW interfering signal @ ±20MHz offset	-35	-	-	dBm
Receiver Out-band Blocking(1) CW interferer	25 ≤ f < 2300 MHz	-28	-	-	dBm
	2300 ≤ f < 2395 MHz	-40	-	-	dBm
	2483.5 < f ≤ 2583.5 MHz	-45	-	-	dBm
Receiver Out-band Blocking(1) CDMA, GSM, DCS and PCS interferers(2)	CDMA UL: 824 – 849 MHz	-20	-	-	dBm
	CDMA DL: 869 – 894 MHz	-10	-	-	dBm
	GSM UL: 880 – 915 MHz	-10	-	-	dBm
	GSM DL: 925 – 960 MHz	-10	-	-	dBm
	DCS UL: 1710 – 1785 MHz	-13	-	-	dBm
	DCS DL: 1805 – 1880 MHz	-20	-	-	dBm
	PCS UL: 1850 – 1910 MHz	-20	-	-	dBm
	PCS DL: 1930 – 1990 MHz	-20	-	-	dBm
Receiver Out-band Blocking(1) WIFI interferers	5G receiver only, interfering signal: 2400 < f ≤ 2483.5 MHz	-20	-	-	dBm
	2G receiver only, interfering signal: 5125 < f ≤ 5850 MHz	-20	-	-	dBm

Note 1: The desired signal's strength is 3 dB above the Maximum RX sensitivity. **PER ≤ 10%.**

Note 2: Except harmonic mixing..

3.2 Antenna Diversity

MT3620 can support two modes of antenna diversity.

- RX diversity
- It uses the WF0_RXA_AUX_IN and WF0_RXG_AUX_IN as the RX port for RX diversity function. No external antenna select pins are required.
- TX/RX diversity

It needs an additional DPDT and two control pins (ANT_SEL) to implement this feature.

MT3620 can support hardware based antenna selection. It measures the RX power on default antenna, and then another antenna when receiving the packet preamble. Before starting receiving payload, it selects the suitable antenna based on power consumption measurement data.

4 Electrical Characteristics

4.1 Absolute Maximum Rating

Table 6. Absolute maximum rating

Symbol	Parameters	Maximum rating	Unit
VDD33	3.3V Supply Voltage	-0.3 to 3.63	V
T_{STG}	Storage Temperature	-40 to +125	°C
VESD	ESD protection (HBM)	2000	V

4.2 Recommended Operating Range

Table 7. Recommended Operating Range

Symbol	Rating	MIN	Typical	MAX	Unit
VDD33	3.3V supply	2.97	3.3	3.63	V
AVDD_3V3_RTC	RTC supply when using internal ring oscillator	2.5	3.3	3.63	V
	RTC supply when using crystal oscillator	2.0	3.3	3.63	V
$T_{AMBIENT}$	Ambient Temperature	-40	-	85	°C

4.3 DC Characteristics

Table 8. DC Characteristics

Symbol	Parameter	Conditions	MIN	MAX	Unit
V_{IL}	Input Low Voltage	LVTTL	-0.28	0.8	V
V_{IH}	Input High Voltage		2.0	3.63	V
V_{OL}	Output Low Voltage	$\|I_{OL}\|$ = 4~16 mA	-0.28	0.4	V
V_{OH}	Output High Voltage	$\|I_{OH}\|$ = 4~16 mA	2.4	VDD33+0.33	V
R_{PU}	Input Pull-Up Resistance	PU=high, PD=low	40	190	KΩ
R_{PD}	Input Pull-Down Resistance	PU=low, PD=high	40	190	KΩ

4.4 Crystal Oscillator

The table below lists the requirement for the main crystal .

Table 9. Crystal Oscillator Requirement

Parameter	Value
Frequency	26MHz.
Frequency stability	±10 ppm @ 25°C
Aging	±3 ppm/year

4.5 Current consumption

Table 10. Current consumption

*** All data preliminary ****

Power mode	Description	Details		Typical current consumption	Hardware wake-up latency
		Subsystem	Power state		
RTC mode	Only RTC domain is on. Memory is not retained, requires a cold boot to resume.	Pluton CM4 subsystem	Off	0.01mA or 0.02mA (*1)	24ms (crystal and PLL lock, PMU time
		CA7 subsystem	Off		
		CM4F I/O subsystems	Off		
		Wi-Fi subsystem	Off		
		Buses/peripherals	Off		
Worst-case power consumption, no Wi-Fi	All subsystems apart from Wi-Fi running at full speed	Pluton CM4 subsystem	On	220mA Worst case 380mA (*2)	N/A, 650us WiFi subsystem resume latency
		CA7 subsystem	On		
		IO 0/1 CM4 subsystems	On		
		Wi-Fi subsystem	Light sleep		
		Buses/peripherals (*3)	On		
Worst-case power consumption with Wi-Fi (*2)	All subsystems running at full speed, Wi-Fi very active	Pluton CM4 subsystem	On	520mA (*4) Worst case 750mA (*2)	N/A
		CA7 subsystem	On		
		IO 0/1 CM4 subsystems	On		
		Wi-Fi subsystem	On		
		Buses/peripherals (*3)	On		
		RF (A or G Band)	On		
		Flash (*5)	On		

Note *1: 0.01mA/0.02mA with/without external 3.3v source PMIC control switch respectively.

Note *2: The current values are measured under typical case (TT silicon and 25C/1.15V) and the TDP (maximum thermal design power) includes simulation worst case condition (TT/125C/1.15V/MC99, MC99 is PTPX power simulation library).

Note *3: It depends on how busy the peripherals are and how they are configured.

Note *4: This data is based on 100% Wi-Fi transmission on the 5GHz band at 14dBm.

Note *5: Depends on I/O loading and flash power consumption.

4.6 PMU Characteristics

Table 11. PMU Electrical Characteristics

PARAMETER	CONDITIONS	PERFORMANCE			
		MIN	TYPICAL	MAX	UNIT
General					
UVLO power-on threshold voltage		2.65	2.7	2.75	V
UVLO power-off threshold voltage		2.45	2.5	2.55	V
UVLO hysteresis		-	200	-	mV
Switching regulator					
Input voltage		2.97	3.3	3.63	V
Output voltage	Default voltage setting in the programmable range[1]	1.55	1.6	1.9	V
Output current		-	-	800	mA
Quiescent current	<1mA load current	-	150	-	uA
Line regulation	3V to 3.6V input voltage range @ no load	-	-	1	%
Load regulation	200mA to 600mA load current	-	-	0.05	mV/mA
Efficiency	400mA load current	-	85	-	%
Over-current shutdown	Threshold	0.96	1.6	4	A
Digital LDO					
Input voltage		1.55	1.6	1.9	V
Output voltage		0.86	1.15	1.3	V
Output current		-	-	420	mA
Quiescent current		-	40	50	uA
Analog LDO (ALDO)					
Input voltage		2.97	3.3	3.63	V
Output voltage		2.3	2.5	2.7	V
Output current		-	-	50	mA
Quiescent current		-	-	50	uA
PMU deep sleep mode					
Input voltage		2.97	3.3	3.63	V

PARAMETER	CONDITIONS	PERFORMANCE			
		MIN	TYPICAL	MAX	UNIT
Output voltage	CLDO output voltage ALDO is off		0.85 0		V
Output current		-	-	10	mA
Quiescent current		-	-	30	uA

4.7 ADC Characteristics

This section specifies the electrical characteristics of the ADC.

Table 12. ADC Specification

Symbol	Parameter	Min	Typical	Max	Unit
N	Resolution	-	12	-	bit
FC	Clock Rate	-	2	-	MHz
FS	Sampling Rate @ N-Bit (1)	-	2	-	MSPS
TS	Sample period	-	0.5	-	µS
VPP	Input Swing (4)	-	-	1.8	V
VIN	Input voltage (4)	0	-	1.8	
SC	Sampling capacitance	-	4	-	pF
RIN	Input Impedance: Unselected channel Selected channel	 400M -	 - 10K	 - -	Ohm
	Dither waveform type	-	Sawtooth	-	
	RMS noise added at input (3)	0.2	0.3	0.4	LSB
	Dither step size (programmable)	0	4	4	LSB
Navg	Number of samples averaged in hardware (programmable) (5)	1	32	64	
Tdither	Dither period (level, programmable) (6)	1	16	16	TS (7)
	Dither magnitude	0	64	64	LSB
DNL	Differential nonlinearity without dithering and averaging	-	± 1	± 2	LSB
INL	Integral nonlinearity without dithering and averaging	-	± 2	± 4	LSB
DNLdither+ average	Differential nonlinearity with dithering and averaging	-	± 0.5	± 1	LSB
INLdither+ average	Integral nonlinearity with dithering and averaging	-	-	± 2	LSB
OE	Offset error	-	-	± 10	mV
FSE	Full swing error	-	-	± 50	mV
SNR	Signal-to-noise ratio (2)	60	63	66	dB
	Current consumption	-	-	400	µA
	Power-down current	-	-	1	µA

Note1: Given that FS=2MHz
Note2: At 1K Hz Input Frequency

Note3: Programmable by changing comparator tail current
Note4: 1.77V when dithering is on.
Note5: Programmable number 1,2,4,8,16,32,64.
Note6: Programmable number 1,2,4,8,16. The number of averaging should be equal or larger than the number of dithering level.
Note 7: TS = time of sampling period, i.e. 0.5us.

4.8 I2S PLL Characteristics

The section describes the I2S PLL (XPLL) electrical characteristics.

Table 13. I2S PLL Specification

Symbol	Parameter	Min	Typical	Max	Unit
F_{in}	Input Clock Frequency	0.1	-	120	MHz
BW	PLL Bandwidth	-	2	-	MHz
F_{out}	Ouput Clock Frequency (VDD=3.3±10%)	500	-	1500	MHz
	Ouput Clock Frequency (VDD=2.5±10%)	500	-	1000	MHz
N	Feedback Divide Ratio	1	-	128	
J_{LT}	Output Clock Long Term Jitter (Delay 10us)	-	20	-	RMS ps
J_P	Output Clock Period Jitter	-	50	-	P-P ps
J_{PH}	Output Clock Phase Jitter	-	20	-	RMS ps
DVDD	Digital Power Supply	1.035	1.15	1.265	V
AVDD	Analog Power Supply	2.25	2.5	2.75	V
I	Current Consumption	-	-	3	mA
I_{off}	Power Down Current	-	-	1	uA
T_{settle}	PLL settling time	-	-	20	us

4.9 PLL1/PLL2 Characteristics

PLL1 and PLL2 are used in a cascaded mode to generate the 960MHz clock for WiFi. This section describes the PLL1 and PLL2 electrical characteristics.

Table 14. PLL1 Specification

Symbol	Parameter	Min	Typical	Max	Unit
F_{in}	Input Clock Frequency	20	-	52	MHz

Symbol	Parameter	Min	Typical	Max	Unit
F_{out}	Output Clock Frequency	640	-	832	MHz
DVDD	Digital Power Supply	-	1.15	-	V
AVDD	Analog Power Supply	-	3.3	-	V
T_{settle}	PLL settling time	-	-	50	us

Table 15. PLL2 Specification

Symbol	Parameter	Min	Typical	Max	Unit
F_{in}	Input Clock Frequency	20	-	32	MHz
F_{out}	Output Clock Frequency	-	960	-	MHz
DVDD	Digital Power Supply	-	1.15	-	V
AVDD	Analog Power Supply	-	3.3	-	V
T_{settle}	PLL settling time	-	-	300	us

4.10 Thermal Characteristics

Θ_{JC} assumes that all the heat is dissipated through the top of the package, while Ψ_{Jt} assumes that the heat is dissipated through the top, sides, and the bottom of the package. Thus it's suggested to use Ψ_{Jt} to estimate the junction temperature.

Table 16. Thermal Characteristics

Symbol	Description	Performance	
		Typical	Unit
T_J	Maximum Junction Temperature (Plastic Package)	125	°C
Θ_{JA}	Junction to ambient temperature thermal resistance[1]	40	°C/W
Θ_{JC}	Junction to case temperature thermal resistance	17.07	°C/W
Ψ_{Jt}	Junction to the package thermal resistance[2]	12.56	°C/W

Note:

[1] JEDEC 51-9 system FR4 PCB size: 101.5mm x 114.3mm

[2] 10.4mm x 10.4mm BGA package

4.11 UART Electrical Specifications

Table 17. UART Electrical Specifications

SYMBOL	PARAMETER	TEST CONDITIONS	PERFORMANCE			Unit
			MIN	TYP	MAX	
TX_{BR}	Supported TX Baud Rate	-	-	-	3(*1)	Mbps
RX_{BR}	Supported RX Baud Rate	-	-	-	3(*1)	Mbps
TX_{error}	UART Tx Baud Rate Error Rate	-	-	-	0.25	%
RX_{error}	Acceptable Error Rate on Rx Baud Rate	-	-	-	3	%

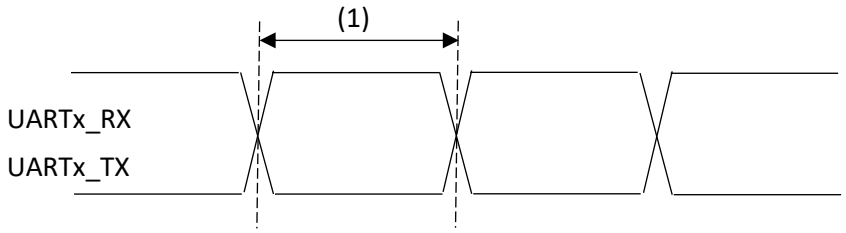


Figure 2. UART timing diagram

4.12 SPI Master Electrical Specifications

Table 18. SPI Master Electrical Specifications

SYMBOL	PARAMETER	CONDITIONS	PERFORMANCE			Unit
			MIN	TYP	MAX	
fSPI	Serial Clock Cycle Time	-	T_{cycle}			ns
tSCK_rising	SCK rising	-	-	-	-	ns
tSCK_falling	SCK falling	-	-	-	-	ns
tSCKL	SCK Low Pulse	-	½ *T_{cycle}	-	-	ns
tSCKH	SCK High Pulse	-	½ *T_{cycle}	-	-	ns
tSDO_OD	SCK Falling Edge to SDO Delay Time	-	-	-	¼*T_{cycle}	ns
tSDI_setup	SDI to SCK Rising Setup Time	-	¼*T_{cycle}	-	-	ns
tSDI_hold	SCK Rising to SDI Hold Time	-	0	-	-	ns
tCSB_setup	CSB Falling to SCK Falling Setup Time	-	34	-	-	ns
tCSB_hold	SCK Rising to CSB Rising Hold Time	-	9	-	-	ns

T_{cycle} is 25ns for which maximum frequency is 40MHz.

SPI Master (Mode0)

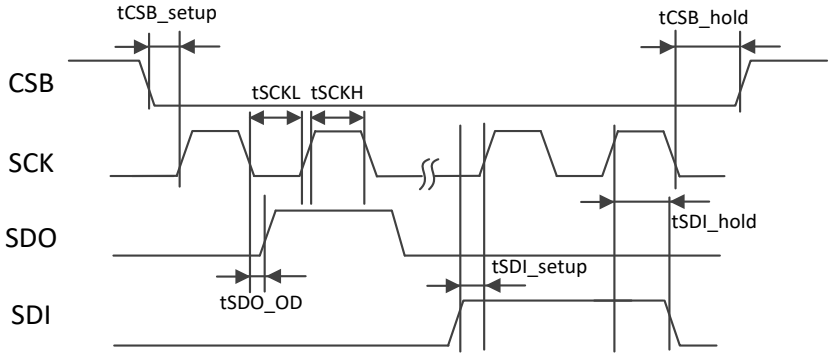


Figure 3. SPI Master timing diagram

4.13 SPI Slave Electrical Specifications

Table 19. SPI Slave Electrical Specifications

SYMBOL	PARAMETER	CONDITIONS	PERFORMANCE			Unit
			MIN	TYP	MAX	
fSPI	Serial Clock Cycle Time	-	T_{cycle}	-	-	ns
tSDO_OD	SCK Falling Edge to SDO Delay Time	-	-	-	¼*T_{cycle}	ns
tSDI_setup	SDI to SCK Rising Setup Time	-	4	-		ns
tSDI_hold	SCK Rising to SDI Hold Time	-	0	-		ns

T_{cycle} is 25ns for which maximum frequency is 40MHz.

SPI Slave (Mode0)

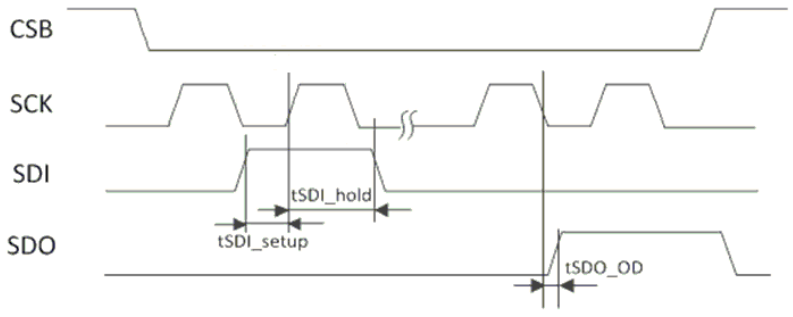


Figure 4. SPI Salve timing diagram

4.14 I2S Electrical Specifications

Table 20. I2S (Slave mode) Electrical Specifications

SYMBOL	PARAMETER	TEST CONDITIONS	PERFORMANCE			Unit
			MIN	TYP	MAX	
t_{MCLKY}	MCLK Output Frequency (MCLK Cycle Time)	-	-	-	12.288	MHz
t_{MCLKDS}	Clock Pulse Width Low	-	45	-	55	%
	Clock Pulse Width High	-	45	-	55	%
t_{sW}	I2SWS→I2SCK Set Up Time	-	8	-	-	ns
t_{hW}	I2SCK→I2SWS Hold Time	-	0	-	-	ns
t_{dCD}	I2SCK↓→I2SDO Delay Time	-	-	-	32	ns
t_{sD}	I2SDI→I2SCK↑Setup Time	-	8	-	-	ns
t_{hD}	I2SCK↑→I2SDI Hold Time	-	0	-	-	ns
t_r	Rise Time (Including MCLK, TX)	-	-	-	8	ns
t_f	Fall Time (Including MCLK, TX)	-	-	-	8	ns

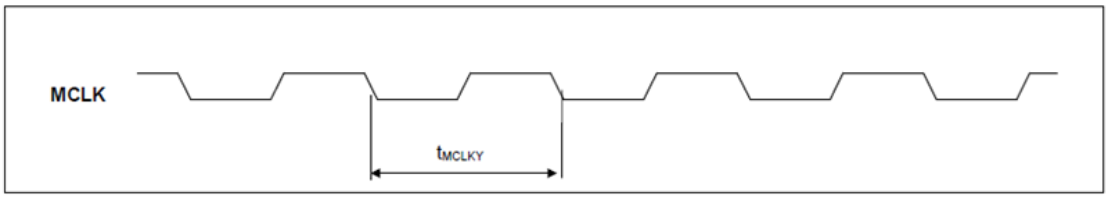


Figure 5. I2S MCLK timing diagram

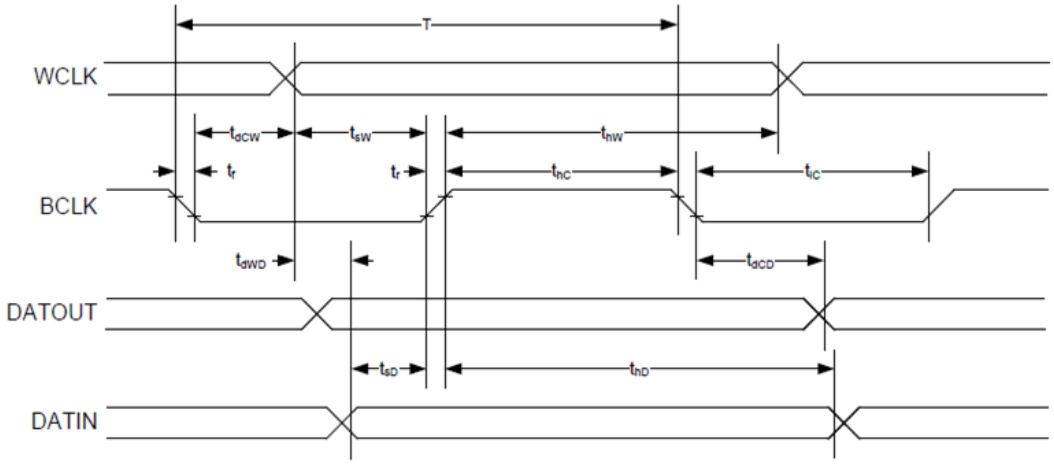


Figure 6. I2S timing diagram

4.15 I2C Electrical Specifications

Table 21. I2C Electrical Specifications

SYMBOL	PARAMETER	TEST CONDITION	PERFORMANCE			Unit
			MIN	TYP	MAX	
Standard Mode						
f_{SCL}	SCL Clock Frequency	-	0	-	100	KHz
$t_{HD:STA}$	Hold Time(Repeated) START Condition.	After This Period, The First Clock Pulse is Generated	4.0	-	-	uS
t_{LOW}	Low Period of SCL Clock	-	4.7	-	-	uS
t_{HIGH}	HIGH Period of SCL Clock	-	4.0	-	-	uS
$t_{SU:STA}$	Set-up Time for a Repeated START Condition	-	4.7	-	-	uS
$t_{HD:DAT}$	Data hold time	I^2C-bus device	0	-	-	uS
$t_{SU:DAT}$	Data Set-up Time	-	250	-	-	nS
t_r	Rise Time of Both SDA and SCL Signals	-	-	-	1000	nS
t_f	Fall Time of Both SDA and SCL Signals	-	-	-	300	nS
$t_{SU:STO}$	Set-up Time for STOP Condition	-	4.0	-	-	uS
t_{BUF}	Bus free time between a STOP and START		4.7		-	uS
C_b	Capacitive Load for Each Bus Line	-	-	-	400	pF
Fast Mode						
f_{SCL}	SCL Clock Frequency	-	0	-	400	KHz
$t_{HD:STA}$	Hold Time(Repeated) START Condition.	After This Period, The First Clock Pulse is Generated	0.6	-	-	uS
t_{LOW}	Low Period of SCL Clock	-	1.3	-	-	uS
t_{HIGH}	HIGH Period of SCL Clock	-	0.6	-	-	uS
$t_{SU:STA}$	Set-up Time for a Repeated START Condition	-	0.6	-	-	uS
$t_{HD:DAT}$	Data hold time	I^2C-bus device	0	-	-	uS
$t_{SU:DAT}$	Data Set-up Time	-	100	-	-	nS
t_r	Rise Time of Both SDA and SCL Signals	-	20	-	300	nS
t_f	Fall Time of Both SDA and SCL Signals	-	20 × (V_{DD} / 5.5V)	-	300	nS
$t_{SU:STO}$	Set-up Time for STOP Condition	-	0.6	-	-	uS
t_{BUF}	Bus free time between a STOP and START		1.3			uS

C_b	Capacitive Load for Each Bus Line	-	-	-	60	pF
Fast Mode Plus						
f_{SCL}	SCL Clock Frequency	-	0	-	1000	KHz
$t_{HD:STA}$	Hold Time(Repeated) START Condition.	After This Period, The First Clock Pulse is Generated	0.26	-	-	uS
t_{LOW}	Low Period of SCL Clock	-	0.5	-	-	uS
t_{HIGH}	HIGH Period of SCL Clock	-	0.26	-	-	uS
$t_{SU:STA}$	Set-up Time for a Repeated START Condition	-	0.26	-	-	uS
$t_{HD:DAT}$	Data hold time	I^2C-bus device	0	-	-	uS
$t_{SU:DAT}$	Data Set-up Time	-	50	-	-	nS
t_r	Rise Time of Both SDA and SCL Signals	-	-	-	120	nS
t_f	Fall Time of Both SDA and SCL Signals	-	20 × (V_{DD} / 5.5V)	-	120	nS
$t_{SU:STO}$	Set-up Time for STOP Condition	-	0.26	-	-	uS
t_{BUF}	Bus free time between a STOP and START		0.5	-	-	uS
C_b	Capacitive Load for Each Bus Line	-	-	-	60	pF

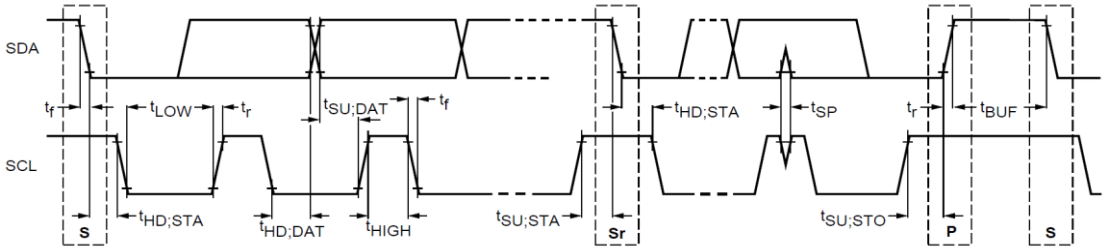


Figure 7. I2C F/S-mode timing diagram

5 Pin and Package Specification

5.1 Pin Layout

MT3620 uses DR QFN package of 164 pins with 12mm x12mm dimension.

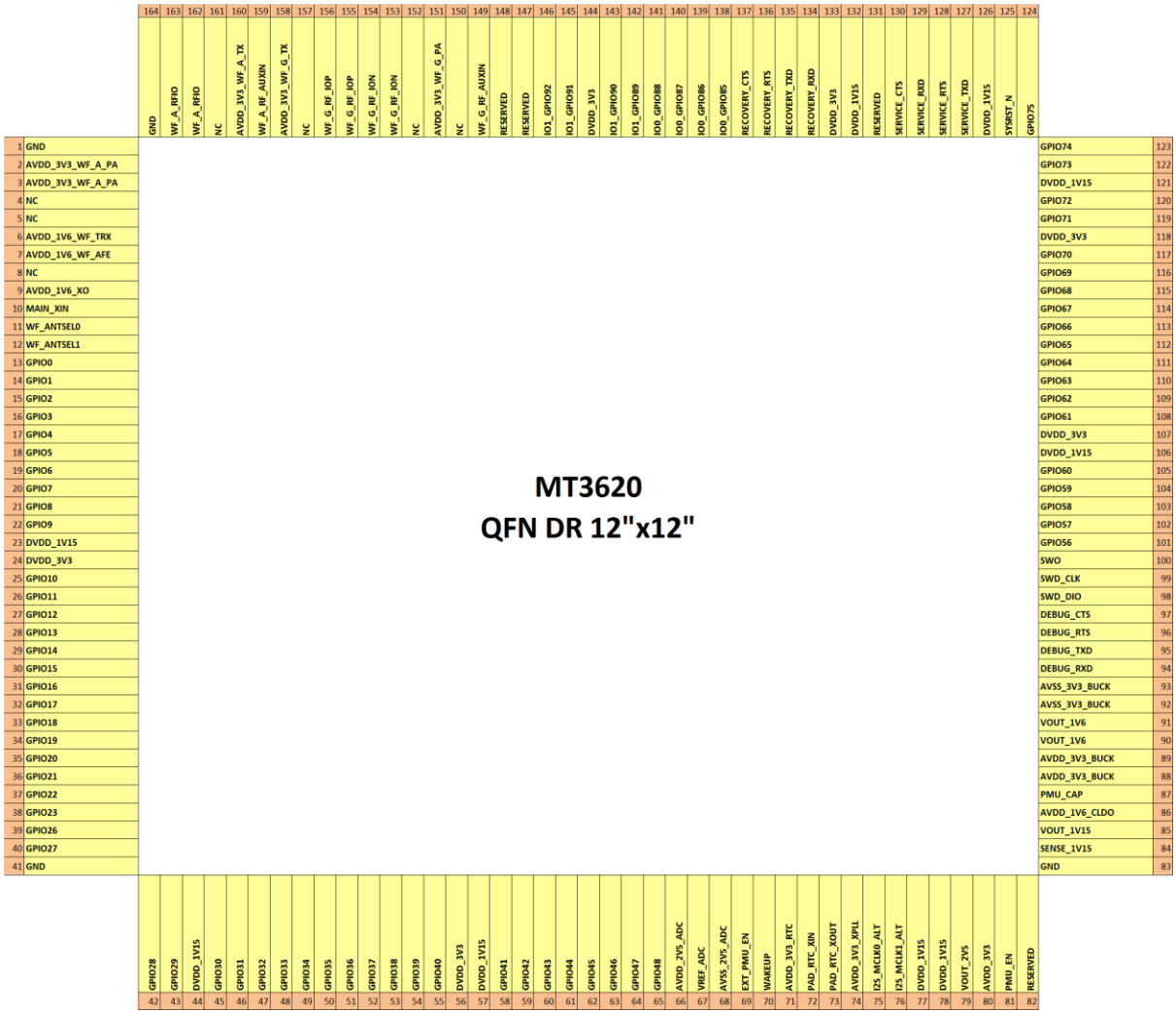


Figure 8. Package pin layout

5.2 Pin Description

This section describes the MT3620 pin functionality. There are totally 165 pins for MT3620 including power and ground pins and the large central EPAD. Note that the pin number column reflects the package pin number.

For the 'Type' column, P = power, I = input, OL = output low, OH = output high, A = analog, D = digital, RF = radio frequency. The 'PU/PD' column shows if there is a default internal pull-up or pull-down resistor at chip reset. The 'I/O' column indicates if a pin is an input or output at chip reset, and in the latter case whether the pin is driven high or low.

Pins named 'RESERVED' should not be connected. Pins named 'TEST' much be connected in the manner described. Pins named 'NC' are not connected inside the chip and may be left unconnected on the PCB..

Table 22. Pin Descriptions

Pin #	Pin name	Major Functions	Type	Pin description	PU/PD	I/O	Supply domain
Reset, clock, RTC							
125	SYSRST_N		DI	System reset, active low. When held in reset the chip is not in a power saving mode and the PMU is active (unless PMU_EN is held low).	PU	I	DVDD_3V3
148	RESERVED		DI	no connection necessary, external pull-down is optional	PD	I	DVDD_3V3
10	MAIN_XIN		AI	Main crystal oscillator input	NA	I	AVDD_1V6_XO
70	WAKEUP		DI	External wakeup from RTC mode (deepest sleep mode)	NA	I	AVDD_3V3_RTC
69	EXT_PMU_EN		DO	External power supply enable output	NA	OH	AVDD_3V3_RTC
72	RTC_XIN		AI	Realtime clock crystal oscillator input. If not using an external RTC crystal then do not connect this pin.	NA	I	AVDD_3V3_RTC
73	RTC_XOUT		AO	Realtime clock crystal oscillator output. If not using an external RTC crystal then do not connect this pin.	NA	O	AVDD_3V3_RTC
GPIO							

Pin #	Pin name	Major Functions	Type	Pin description	PU/PD	I/O	Supply domain
13	GPIO0	GPIO0/PWM0	DIO	Interrupt-capable GPIO multiplexed with PWM output	NA*	I	DVDD_3V3
14	GPIO1	GPIO1/PWM1	DIO	Interrupt-capable GPIO multiplexed with PWM output	NA*	I	DVDD_3V3
15	GPIO2	GPIO2/PWM2	DIO	Interrupt-capable GPIO multiplexed with PWM output	NA*	I	DVDD_3V3
16	GPIO3	GPIO3/PWM3	DIO	Interrupt-capable GPIO multiplexed with PWM output	NA*	I	DVDD_3V3
17	GPIO4	GPIO4/PWM4	DIO	Interrupt-capable GPIO multiplexed with PWM output	NA*	I	DVDD_3V3
18	GPIO5	GPIO5/PWM5	DIO	Interrupt-capable GPIO multiplexed with PWM output	NA*	I	DVDD_3V3
19	GPIO6	GPIO6/PWM6	DIO	Interrupt-capable GPIO multiplexed with PWM output	NA*	I	DVDD_3V3
20	GPIO7	GPIO7/PWM7	DIO	Interrupt-capable GPIO multiplexed with PWM output	NA*	I	DVDD_3V3
21	GPIO8	GPIO8/PWM8	DIO	Interrupt-capable GPIO multiplexed with PWM output	NA*	I	DVDD_3V3
22	GPIO9	GPIO9/PWM9	DIO	Interrupt-capable GPIO multiplexed with PWM output	NA*	I	DVDD_3V3
25	GPIO10	GPIO10/PWM10	DIO	Interrupt-capable GPIO multiplexed with PWM output	NA*	I	DVDD_3V3
26	GPIO11	GPIO11/PWM11	DIO	Interrupt-capable GPIO multiplexed with PWM output	NA*	I	DVDD_3V3
27	GPIO12		DIO	Interrupt-capable GPIO	NA*	I	DVDD_3V3
28	GPIO13		DIO	Interrupt-capable GPIO	NA*	I	DVDD_3V3
29	GPIO14		DIO	Interrupt-capable GPIO	NA*	I	DVDD_3V3
30	GPIO15		DIO	Interrupt-capable GPIO	NA*	I	DVDD_3V3
31	GPIO16		DIO	Interrupt-capable GPIO	NA*	I	DVDD_3V3
32	GPIO17		DIO	Interrupt-capable GPIO	NA*	I	DVDD_3V3
33	GPIO18		DIO	Interrupt-capable GPIO	NA*	I	DVDD_3V3
34	GPIO19		DIO	Interrupt-capable GPIO	NA*	I	DVDD_3V3
35	GPIO20		DIO	Interrupt-capable GPIO	NA*	I	DVDD_3V3
36	GPIO21		DIO	Interrupt-capable GPIO	NA*	I	DVDD_3V3

Pin #	Pin name	Major Functions	Type	Pin description	PU/PD	I/O	Supply domain
37	GPIO22		DIO	Interrupt-capable GPIO	NA*	I	DVDD_3V3
38	GPIO23		DIO	Interrupt-capable GPIO	NA*	I	DVDD_3V3
I2C, SPI, and UART interface							
39	GPIO26	GPIO26/SCLK0/TXD0	DIO	GPIO multiplexed with ISU 0 functions	NA	I	DVDD_3V3
40	GPIO27	GPIO27/MOSI0/RTS0/SCL0	DIO	GPIO multiplexed with ISU 0 functions	NA	I	DVDD_3V3
42	GPIO28	GPIO28/MISO0/RXD0/SDA0	DIO	GPIO multiplexed with ISU 0 functions	NA	I	DVDD_3V3
43	GPIO29	GPIO29/CSA0/CTS0	DIO	GPIO multiplexed with ISU 0 functions	NA	I	DVDD_3V3
45	GPIO30	GPIO30/CSB0	DIO	GPIO multiplexed with ISU 0 functions	NA	I	DVDD_3V3
46	GPIO31	GPIO31/SCLK1/TXD1	DIO	GPIO multiplexed with ISU 1 functions	NA	I	DVDD_3V3
47	GPIO32	GPIO32/MOSI1/RTS1/SCL1	DIO	GPIO multiplexed with ISU 1 functions	NA	I	DVDD_3V3
48	GPIO33	GPIO33/MISO1/RXD1/SDA1	DIO	GPIO multiplexed with ISU 1 functions	NA	I	DVDD_3V3
49	GPIO34	GPIO34/CSA1/CTS1	DIO	GPIO multiplexed with ISU 1 functions	NA	I	DVDD_3V3
50	GPIO35	GPIO35/CSB1	DIO	GPIO multiplexed with ISU 1 functions	NA	I	DVDD_3V3
51	GPIO36	GPIO36/SCLK2/TXD2	DIO	GPIO multiplexed with ISU 2 functions	NA	I	DVDD_3V3
52	GPIO37	GPIO37/MOSI2/RTS2/SCL2	DIO	GPIO multiplexed with ISU 2 functions	NA	I	DVDD_3V3
53	GPIO38	GPIO38/MISO2/RXD2/SDA2	DIO	GPIO multiplexed with ISU 2 functions	NA	I	DVDD_3V3
54	GPIO39	GPIO39/CSA2/CTS2	DIO	GPIO multiplexed with ISU 2 functions	NA	I	DVDD_3V3
55	GPIO40	GPIO40/CSB2	DIO	GPIO multiplexed with ISU 2 functions	NA	I	DVDD_3V3
113	GPIO66	GPIO66/SCLK3/TXD3	DIO	GPIO multiplexed with ISU 3 functions	NA	I	DVDD_3V3
114	GPIO67	GPIO67/MOSI3/RTS3/SCL3	DIO	GPIO multiplexed with ISU 3 functions	NA	I	DVDD_3V3

Pin #	Pin name	Major Functions	Type	Pin description	PU/PD	I/O	Supply domain
115	GPIO68	GPIO68/MISO3/RXD3/SDA3	DIO	GPIO multiplexed with ISU 3 functions	NA	I	DVDD_3V3
116	GPIO69	GPIO69/CSA3/CTS3	DIO	GPIO multiplexed with ISU 3 functions	NA	I	DVDD_3V3
117	GPIO70	GPIO70/CSB3	DIO	GPIO multiplexed with ISU 3 functions	NA	I	DVDD_3V3
119	GPIO71	GPIO71/SCLK4/TXD4	DIO	GPIO multiplexed with ISU 4 functions	NA	I	DVDD_3V3
120	GPIO72	GPIO72/MOSI4/RTS4/SCL4	DIO	GPIO multiplexed with ISU 4 functions	NA	I	DVDD_3V3
122	GPIO73	GPIO73/MISO4/RXD4/SDA4	DIO	GPIO multiplexed with ISU 4 functions	NA	I	DVDD_3V3
123	GPIO74	GPIO74/CSA4/CTS4	DIO	GPIO multiplexed with ISU 4 functions	NA	I	DVDD_3V3
124	GPIO75	GPIO75/CSB4	DIO	GPIO multiplexed with ISU 4 functions	NA	I	DVDD_3V3
ADC							
58	GPIO41	GPIO41/ADC0	ADIO	GPIO multiplexed with ADC input	NA	I	AVDD_2V5_ADC
59	GPIO42	GPIO42/ADC1	ADIO	GPIO multiplexed with ADC input	NA	I	AVDD_2V5_ADC
60	GPIO43	GPIO43/ADC2	ADIO	GPIO multiplexed with ADC input	NA	I	AVDD_2V5_ADC
61	GPIO44	GPIO44/ADC3	ADIO	GPIO multiplexed with ADC input	NA	I	AVDD_2V5_ADC
62	GPIO45	GPIO45/ADC4	ADIO	GPIO multiplexed with ADC input	NA	I	AVDD_2V5_ADC
63	GPIO46	GPIO46/ADC5	ADIO	GPIO multiplexed with ADC input	NA	I	AVDD_2V5_ADC
64	GPIO47	GPIO47/ADC6	ADIO	GPIO multiplexed with ADC input	NA	I	AVDD_2V5_ADC
65	GPIO48	GPIO48/ADC7	ADIO	GPIO multiplexed with ADC input	NA	I	AVDD_2V5_ADC
I2S interface							
101	GPIO56	GPIO56/TX0	DIO	GPIO multiplexed with I2S 0	NA	I	DVDD_3V3
102	GPIO57	GPIO57/MCLK0	DIO	GPIO multiplexed with I2S 0	NA	I	DVDD_3V3
103	GPIO58	GPIO58/FS0	DIO	GPIO multiplexed with I2S 0	NA	I	DVDD_3V3

Pin #	Pin name	Major Functions	Type	Pin description	PU/PD	I/O	Supply domain
104	GPIO59	GPIO59/RX0	DIO	GPIO multiplexed with I2S 0	NA	I	DVDD_3V3
105	GPIO60	GPIO60/BCLK0	DIO	GPIO multiplexed with I2S 0	NA	I	DVDD_3V3
108	GPIO61	GPIO61/TX1	DIO	GPIO multiplexed with I2S 1	NA	I	DVDD_3V3
109	GPIO62	GPIO62/MCLK1	DIO	GPIO multiplexed with I2S 1	NA	I	DVDD_3V3
110	GPIO63	GPIO63/FS1	DIO	GPIO multiplexed with I2S 1	NA	I	DVDD_3V3
111	GPIO64	GPIO64/RX1	DIO	GPIO multiplexed with I2S 1	NA	I	DVDD_3V3
112	GPIO65	GPIO65/BCLK1	DIO	GPIO multiplexed with I2S 1	NA	I	DVDD_3V3
Management and debug interfaces							
98	SWD_DIO		DIO	ARM SWD for Cortex CM4F debug	PU	I	DVDD_3V3
99	SWD_CLK		DI	ARM SWD for Cortex CM4F debug	PD	I	DVDD_3V3
100	SWO		DO	ARM SWO for Cortex CM4F debug	NA	OL	DVDD_3V3
94	DEBUG_RXD		DI	Reserved for Codename 4x4 debug	PU	I	DVDD_3V3
95	DEBUG_TXD		DO	Reserved for Codename 4x4 debug	PD	OH	DVDD_3V3
96	DEBUG_RTS		DO	Reserved for Codename 4x4 debug	PD	OH	DVDD_3V3
97	DEBUG_CTS		DI	Reserved for Codename 4x4 debug	PU	I	DVDD_3V3
127	SERVICE_TXD		DO	Codename 4x4 service port	NA	OH	DVDD_3V3
128	SERVICE_RTS		DO	Codename 4x4 service port	NA	OH	DVDD_3V3
129	SERVICE_RXD		DI	Codename 4x4 service port	NA	I	DVDD_3V3
130	SERVICE_CTS		DI	Codename 4x4 service port	NA	I	DVDD_3V3
131	RESERVED				NA	OL	DVDD_3V3
134	RECOVERY_RXD		DI	Codename 4x4 recovery port	PU	I	DVDD_3V3
135	RECOVERY_TXD		DO	Codename 4x4 recovery port	PU	OH	DVDD_3V3

Pin #	Pin name	Major Functions	Type	Pin description	PU/PD	I/O	Supply domain
136	RECOVERY_RTS		DO	Codename 4x4 recovery port	PD	OH	DVDD_3V3
137	RECOVERY_CTS		DI	Codename 4x4 recovery port	PU	I	DVDD_3V3
138	IO0_GPIO85	IO0_GPIO85/IO0_RXD	DI	Dedicated GPIO multiplexed with UART for I/O CM4F 0	PU	I	DVDD_3V3
139	IO0_GPIO86	IO0_GPIO86/IO0_TXD	DO	Dedicated GPIO multiplexed with UART for I/O CM4F 0	PD	OH	DVDD_3V3
140	IO0_GPIO87	IO0_GPIO87/IO0_RTS	DO	Dedicated GPIO multiplexed with UART for I/O CM4F 0	PU	OH	DVDD_3V3
141	IO0_GPIO88	IO0_GPIO88/IO0_CTS	DI	Dedicated GPIO multiplexed with UART for I/O CM4F 0	PU	I	DVDD_3V3
142	IO1_GPIO89	IO1_GPIO89/IO1_RXD	DI	Dedicated GPIO multiplexed with UART for I/O CM4F 1	PU	I	DVDD_3V3
143	IO1_GPIO90	IO1_GPIO90/IO1_TXD	DO	Dedicated GPIO multiplexed with UART for I/O CM4F 1	PD	OH	DVDD_3V3
145	IO1_GPIO91	IO1_GPIO91/IO1_RTS	DO	Dedicated GPIO multiplexed with UART for I/O CM4F 1	PD	OH	DVDD_3V3
146	IO1_GPIO92	IO1_GPIO92/IO1_CTS	DI	Dedicated GPIO multiplexed with UART for I/O CM4F 1	PU	I	DVDD_3V3
147	RESERVED				NA	OL	DVDD_3V3
Wi-Fi							
11	WF_ANTSEL0		DO	Wi-Fi antenna select for external DPDT switch	NA	OL	DVDD_3V3
12	WF_ANTSEL1		DO	Wi-Fi antenna select for external DPDT switch	NA	OL	DVDD_3V3
162,163	WF_A_RFIO		RF	5GHz Wi-Fi antenna port (unbalanced). If not used connect to ground to avoid leakage current.	NA	I/O	AVDD_3V3_WF_A
155,156	WF_G_RF_IOP		RF	2.4GHz Wi-Fi antenna port (differential). If not used connect to ground to avoid leakage current.	NA	I/O	AVDD_3V3_WF_G
153,154	WF_G_RF_ION		RF	2.4GHz Wi-Fi antenna port (differential). If not used connect to ground to avoid leakage current.	NA	I/O	AVDD_3V3_WF_G
159	WF_A_RF_AUXIN		RF	5GHz Wi-Fi receive diversity port. If not used connect to ground to avoid leakage current.	NA	I	AVDD_3V3_WF_A
149	WF_G_RF_AUXIN		RF	2.4GHz Wi-Fi receive diversity port. If not used connect to ground to avoid leakage current.	NA	I	AVDD_3V3_WF_G
PMU							

Pin #	Pin name	Major Functions	Type	Pin description	PU/PD	I/O	Supply domain
81	PMU_EN		DI	Internal PMU override. If driven low, MT3620 is turned off and in a very low power state, equivalent to RTC mode power consumption. Only the PMU quiescent current will be drawn. When released, the PMU will start up.	NA	I	NA
82	RESERVED				NA	OL	NA
90,91	VOUT_1V6		PO	Output from internal 1.6V buck converter	NA	O	NA
88,89	AVDD_3V3_BUCK		PI	3.3V power rail for internal 1.6V buck DC-DC converter	NA	I	NA
92,93	AVSS_3V3_BUCK		P	Ground for internal 1.6V buck converter	NA	NA	NA
80	AVDD_3V3		PI	3.3V power rail	NA	I	NA
87	PMU_CAP		A	Connect a capacitor between this pin and AVDD_3V3_BUCK to maintain PMU stability.	NA	I/O	NA
86	AVDD_1V6_CLDO		PI	1.6V power rail for the internal 1.15V core LDO	NA	I	NA
84	SENSE_1V15		AI	Sense input to stabilise the 1.15V power supply	NA	I/O	NA
85	VOUT_1V15		PO	Output from internal 1.15V LDO	NA	O	NA
79	VOUT_2V5		PO	Output from internal 2.5V LDO	NA	O	NA
Miscellaneous							
75	I2S_MCLK0_ALT		AO	Analog alternative to MCLK0	NA	O	NA
76	I2S_MCLK1_ALT		AO	Analog alternative to MCLK1	NA	O	NA
Power & ground							
23	DVDD_1V15		PI	1.15V power rail	NA	NA	NA
44	DVDD_1V15		PI	1.15V power rail	NA	NA	NA
57	DVDD_1V15		PI	1.15V power rail	NA	NA	NA
77	DVDD_1V15		PI	1.15V power rail	NA	NA	NA
78	DVDD_1V15		PI	1.15V power rail	NA	NA	NA

Pin #	Pin name	Major Functions	Type	Pin description	PU/PD	I/O	Supply domain
106	DVDD_1V15		PI	1.15V power rail	NA	NA	NA
121	DVDD_1V15		PI	1.15V power rail	NA	NA	NA
126	DVDD_1V15		PI	1.15V power rail	NA	NA	NA
132	DVDD_1V15		PI	1.15V power rail	NA	NA	NA
24	DVDD_3V3		PI	3.3V power rail	NA	NA	NA
56	DVDD_3V3		PI	3.3V power rail	NA	NA	NA
107,118	DVDD_3V3		PI	3.3V power rail	NA	NA	NA
133,144	DVDD_3V3		PI	3.3V power rail	NA	NA	NA
66	AVDD_2V5_ADC		PI	2.5V power rail for ADC	NA	NA	NA
67	VREF_ADC		AI	Reference voltage input for ADC	NA	NA	AVDD_2V5_ADC
68	AVSS_2V5_ADC		P	Ground for ADC	NA	NA	NA
2,3	AVDD_3V3_WF_A_PA		PI	3.3V power rail for 5GHz Wi-Fi power amplifier	NA	NA	NA
151	AVDD_3V3_WF_G_PA		PI	3.3V power rail for 2.4GHz Wi-Fi power amplifier	NA	NA	NA
160	AVDD_3V3_WF_A_TX		PI	3.3V power rail for 5GHz Wi-Fi transmit	NA	NA	NA
158	AVDD_3V3_WF_G_TX		PI	3.3V power rail for 2.4GHz Wi-Fi transmit	NA	NA	NA
6	AVDD_1V6_WF_TRX		PI	1.6V power rail for Wi-Fi transmit/receive	NA	NA	NA
7	AVDD_1V6_WF_AFE		PI	1.6V power rail for Wi-Fi analog front end	NA	NA	NA
9	AVDD_1V6_XO		PI	1.6V power rail for main crystal oscillator	NA	NA	NA
74	AVDD_3V3_XPLL		PI	3.3V power rail for internal I2S phase-locked loop	NA	NA	NA
71	AVDD_3V3_RTC		PI	Power rail for real-time clock	NA	NA	NA

Pin #	Pin name	Major Functions	Type	Pin description	PU/PD	I/O	Supply domain
1,41,83,164,165	GND		P	Ground	NA	NA	NA
4,5,8,150,152,157,161	NC				NA	NA	NA

* GPIO0-23 have configurable defaults for internal pull-up / pull-down resistors. These may be configured using e-fuses and become active about 27.6ms after power on (based on a 26MHz crystal). These defaults persist a chip reset.

5.3 Pin Multiplexing

The pin multiplexing can be controlled via the configuration register from 0x3001_0020 to 0x3001_004Ch in CA7 configuration register space (PINMUX_AON section). Each pin's hardware power-on default function will be the pin multiplexing of CR value "0000". For the IO pin multiplexing feature, MT3620 provides a programmable flexibility for users to define the state of the IO when the chip enters sleep mode.

The driving strength of all pins is programmable: 4mA, 8mA, 12mA, and 16mA. The default setting for all pins are 4mA. The slew rate, the driving strength, and the pull up/down of IOs can be individually configured via control registers.

Note: the 24 dedicate GPIO and the 25 signals of five I2C/SPI/UART interface sets are using the GPIO with additional 0.15mA low driving strength IO which is meets low speed rise/fall time requirement.

Table 23. Pin Multiplexing

IO name (CR Address)	CR Value Default *	Name	Dir	Default dir	Default PU/PD	Description
GPIO0 (0x3001_0020[3:0])	0000 *	GPIO[0]	I/O	I	PD	GPIO 0
	0001	PWM[0]	O			PWM 0
	0101	EINT[0]	I			External interrupt
	0110	GPIO[0]	I/O			GPIO 0
	0111	ANTSEL2	O			Antenna select 2
GPIO1 (0x3001_0020[7:4])	0000 *	GPIO[1]	I/O	I	PD	GPIO 1
	0001	PWM[1]	O			PWM 1
	0011	ICAP_TRIG_EXT	I			WIFI capture mode trigger signal
	0101	EINT[1]	I			External interrupt
	0110	GPIO[1]	I/O			GPIO 1
	0111	ANTSEL3	O			Antenna select 3
GPIO2 (0x3001_0020[11:8])	0000 *	GPIO[2]	I/O	I	PD	GPIO 2
	0001	PWM[2]	O			PWM 2
	0101	EINT[2]	I			External interrupt
	0110	GPIO[2]	I/O			GPIO 2
	0111	ANTSEL4	O			Antenna select 4
GPIO3	0000 *	GPIO[3]	I/O	I	PD	GPIO 3

IO name (CR Address)	CR Value Default *	Name	Dir	Default dir	Default PU/PD	Description
(0x3001_0020[15:12])	0001	PWM[3]	O			PWM 3
	0100	WF_LED_B	I/O			WIFI action LED indication signal
	0101	EINT[3]	I			External interrupt
	0110	GPIO[3]	I/O			GPIO 3
	0111	ANTSEL5	O			Antenna select 5
GPIO4 (0x3001_0020[19:16])	0000 *	GPIO[4]	I/O	I	PD	GPIO 4
	0001	PWM[4]	O			PWM 4
	0010	MCU_JTCK	I			N9 JTAG debugger
	0101	EINT[4]	I			External interrupt
	0110	GPIO[4]	I/O			GPIO 4
	0111	ANTSEL6	O			Antenna select 6
GPIO5 (0x3001_0020[23:20])	0000 *	GPIO[5]	I/O	I	PD	GPIO 5
	0001	PWM[5]	O			PWM 5
	0010	MCU_JTMS	I			N9 JTAG debugger
	0100	WF_LED_B	I/O			WIFI action LED indication signal
	0101	EINT[5]	I			External interrupt
	0110	GPIO[5]	I/O			GPIO 5
	0111	ANTSEL7	O			Antenna select 7
GPIO6 (0x3001_0020[27:24])	0000 *	GPIO[6]	I/O	I	PD	GPIO 6
	0001	PWM[6]	O			PWM 6
	0010	MCU_JTDI	I			N9 JTAG debugger
	0101	EINT[6]	I			External interrupt
	0110	GPIO[6]	I/O			GPIO 6
GPIO7 (0x3001_0020[31:28])	0000 *	GPIO[7]	I/O	I	PD	GPIO 7
	0001	PWM[7]	O			PWM 7
	0010	MCU_JTRST_B	I			N9 JTAG debugger
	0101	EINT[7]	I			External interrupt
	0110	GPIO[7]	I/O			GPIO 7
GPIO8 (0x3001_0024[3:0])	0000 *	GPIO[8]	I/O	I	PD	GPIO 8
	0001	PWM[8]	O			PWM 8
	0010	MCU_DBGIN	I			N9 JTAG debugger

IO name (CR Address)	CR Value Default *	Name	Dir	Default dir	Default PU/PD	Description
	0011	ICAP_TRIG_EXT	I			WIFI capture mode trigger signal
	0101	EINT[8]	I			External interrupt
	0110	GPIO[8]	I/O			GPIO 8
GPIO9 (0x3001_0024[7:4])	0000 *	GPIO[9]	I/O	I	PD	GPIO 9
	0001	PWM[9]	O			PWM 9
	0011	ICAP_TRIG_EXT	I			WIFI capture mode trigger signal
	0100	TDATA[12]	O			TPIU trace port
	0101	EINT[9]	I			External interrupt
	0110	GPIO[9]	I/O			GPIO 9
GPIO10 (0x3001_0024[11:8])	0000 *	GPIO[10]	I/O	I	PD	GPIO 10
	0001	PWM[10]	O			PWM 10
	0010	MCU_DBGACKN	O			N9 JTAG debugger
	0101	EINT[10]	I			External interrupt
	0110	GPIO[10]	I/O			GPIO 10
GPIO11 (0x3001_0024[15:12])	0000 *	GPIO[11]	I/O	I	PD	GPIO 11
	0001	PWM[11]	O			PWM 11
	0010	MCU_JTDO	O			N9 JTAG debugger
	0100	WF_LED_B	I/O			WIFI action LED indication signal
	0101	EINT[11]	I			External interrupt
	0110	GPIO[11]	I/O			GPIO 11
GPIO12 (0x3001_0024[19:16])	0000 *	GPIO[12]	I/O	I	PD	GPIO 12
	0001	TCLK	O			TPIU trace port
	0010	PLUTON_TCLK	O			PLUTON TPIU trace port
	0011	IO0_TCLK	O			IO0 TPIU trace port
	0100	IO1_TCLK	O			IO1 TPIU trace port
	0101	EINT[12]	I			External interrupt
	0110	GPIO[12]	I/O			GPIO 12
GPIO13 (0x3001_0024[23:20])	0000 *	GPIO[13]	I/O	I	PD	GPIO 13
	0001	TDATA[0]	O			TPIU trace port
	0010	PLUTON_TDATA [0]	O			PLUTON TPIU trace port

IO name (CR Address)	CR Value Default *	Name	Dir	Default dir	Default PU/PD	Description
	0011	IO0_TDATA[0]	O			IO0 TPIU trace port
	0100	IO1_TDATA[0]	O			IO1 TPIU trace port
	0101	EINT[13]	I			External interrupt
	0110	GPIO[13]	I/O			GPIO 13
GPIO14 (0x3001_0024[27:24])	0000 *	GPIO[14]	I/O	I	PD	GPIO 14
	0001	TDATA[1]	O			TPIU trace port
	0010	PLUTON_TDATA [1]	O			PLUTON TPIU trace port
	0011	IO0_TDATA[1]	O			IO0 TPIU trace port
	0100	IO1_TDATA[1]	O			IO1 TPIU trace port
	0101	EINT[14]	I			External interrupt
	0110	GPIO[14]	I/O			GPIO 14
GPIO15 (0x3001_0024[31:28])	0000 *	GPIO[15]	I/O	I	PD	GPIO 15
	0001	TDATA[2]	O			TPIU trace port
	0010	PLUTON_TDATA [2]	O			PLUTON TPIU trace port
	0011	IO0_TDATA[2]	O			IO0 TPIU trace port
	0100	IO1_TDATA[2]	O			IO1 TPIU trace port
	0101	EINT[15]	I			External interrupt
	0110	GPIO[15]	I/O			GPIO 15
GPIO16 (0x3001_0028[3:0])	0000 *	GPIO[16]	I/O	I	PD	GPIO 16
	0001	TDATA[3]	O			TPIU trace port
	0010	PLUTON_TDATA [3]	O			PLUTON TPIU trace port
	0011	IO0_TDATA[3]	O			IO0 TPIU trace port
	0100	IO1_TDATA[3]	O			IO1 TPIU trace port
	0101	EINT[16]	I			External interrupt
	0110	GPIO[16]	I/O			GPIO 16
GPIO17 (0x3001_0028[7:4])	0000 *	GPIO[17]	I/O	I	PD	GPIO 17
	0001	TCTL	O			TPIU trace port
	0101	EINT[17]	I			External interrupt

IO name (CR Address)	CR Value Default *	Name	Dir	Default dir	Default PU/PD	Description
	0110	GPIO[17]	I/O			GPIO 17
GPIO18 (0x3001_0028[11:8])	0000 *	GPIO[18]	I/O	I	PD	GPIO 18
	0100	TDATA[13]	O			TPIU trace port
	0101	EINT[18]	I			External interrupt
	0110	GPIO[18]	I/O			GPIO 18
GPIO19 (0x3001_0028[15:12])	0000 *	GPIO[19]	I/O	I	PD	GPIO 19
	0010	CA7_NTRST	I			CA7 Jtag
	0101	EINT[19]	I			External interrupt
	0110	GPIO[19]	I/O			GPIO 19
GPIO20 (0x3001_0028[19:16])	0000 *	GPIO[20]	I/O	I	PD	GPIO 20
	0001	SWO_IO0	O			SWO for IO0 CM4
	0100	TDATA[14]	O			TPIU trace port
	0101	EINT[20]	I			External interrupt
	0110	GPIO[20]	I/O			GPIO 20
GPIO21 (0x3001_0028[23:20])	0000 *	GPIO[21]	I/O	I	PD	GPIO 21
	0001	SWO_IO1	O			SWO for IO1 CM4
	0100	TDATA[15]	O			TPIU trace port
	0101	EINT[21]	I			External interrupt
	0110	GPIO[21]	I/O			GPIO 21
GPIO22 (0x3001_0028[27:24])	0000 *	GPIO[22]	I/O	I	PD	GPIO 22
	0010	CA7_TDI	I			CA7 Jtag
	0101	EINT[22]	I			External interrupt
	0110	GPIO[22]	I/O			GPIO 22
GPIO23 (0x3001_0028[31:28])	0000 *	GPIO[23]	I/O	I	PD	GPIO 23
	0010	CA7_TDO	O			CA7 Jtag
	0100	WF_LED_B	I/O			WIFI action LED indication signal
	0101	EINT[23]	I			External interrupt
	0110	GPIO[23]	I/O			GPIO 23
WF_ANTSEL0 (0x3001_002C[3:0])	0000 *	ANTSEL0	O	O	NA	Antenna select 0
	0010	MCU_DBGACKN	O			N9 JTAG debugger
	0100	TDATA[14]	O			TPIU trace port

IO name (CR Address)	CR Value Default *	Name	Dir	Default dir	Default PU/PD	Description
	0110	GPIO[24]	I/O			GPIO 24
WF_ANTSEL1 (0x3001_002C[7:4])	0000 *	ANTSEL1	O	O	NA	Antenna select 1
	0010	MCU_JTDO	O			N9 JTAG debugger
	0100	TDATA[15]	O			TPIU trace port
	0110	GPIO[25]	I/O			GPIO 25
GPIO26 (0x3001_002C[11:8])	0000	SPI0_SCK	O	I (A1)	NA	SPI master 0
	0001	UART0_TX	O			UART 0
	0100	SPI0_SCK_S	I			SPI slave 0
	0110 *	GPIO[26]	I/O			GPIO 26
GPIO27 (0x3001_002C[15:12])	0000	SPI0_MOSI	O	1 (A1)	NA	SPI master 0
	0001	UART0_RTS	O			UART 0
	0010	I2C0_CLK	I/O			I2C 0
	0100	SPI0_MOSI_S	I			SPI slave 0
	0110 *	GPIO[27]	I/O			GPIO 27
GPIO28 (0x3001_002C[19:16])	0000	SPI0_MISO	I	I	NA	SPI master 0
	0001	UART0_RX	I			UART 0
	0010	I2C0_DATA	I/O			I2C 0
	0100	SPI0_MISO_S	O			SPI slave 0
	0110 *	GPIO[28]	I/O			GPIO 28
GPIO29 (0x3001_002C[23:20])	0000	SPI0_CSA	O	I (A1)	NA	SPI master 0
	0001	UART0_CTS	I			UART 0
	0100	SPI0_CS_S	I			SPI slave 0
	0110 *	GPIO[29]	I/O			GPIO 29
GPIO30 (0x3001_002C[27:24])	0000	SPI0_CSB	O	I (A1)	NA	SPI master 0
	0110 *	GPIO[30]	I/O			GPIO 30
GPIO31 (0x3001_002C[31:28])	0000	SPI1_SCK	O	I (A1)	NA	SPI master 1
	0001	UART1_TX	O			UART 1
	0100	SPI1_SCK_S	I			SPI slave 1
	0110 *	GPIO[31]	I/O			GPIO 31
	0111	WF_GPIO0	I/O			WIFI GPIO 0
GPIO32	0000	SPI1_MOSI	O	I	NA	SPI master 1

IO name (CR Address)	CR Value Default *	Name	Dir	Default dir	Default PU/PD	Description
(0x3001_0030[3:0])	0001	UART1_RTS	O	(A1)		UART 1
	0010	I2C1_CLK	I/O			I2C 1
	0100	SPI1_MOSI_S	I			SPI slave 1
	0110 *	GPIO[32]	I/O			GPIO 32
	0111	WF_GPIO1	I/O			WIFI GPIO 1
GPIO33 (0x3001_0030[7:4])	0000	SPI1_MISO	I	I	NA	SPI master 1
	0001	UART1_RX	I			UART 1
	0010	I2C1_DATA	I/O			I2C 1
	0100	SPI1_MISO_S	O			SPI slave 1
	0110 *	GPIO[33]	I/O			GPIO 33
	0111	WF_GPIO2	I/O			WIFI GPIO 2
GPIO34 (0x3001_0030[11:8])	0000	SPI1_CSA	O	I (A1)	NA	SPI master 1
	0001	UART1_CTS	I			UART 1
	0100	SPI1_CS_S	I			SPI slave 1
	0110 *	GPIO[34]	I/O			GPIO 34
	0111	WF_GPIO3	I/O			WIFI GPIO 3
GPIO35 (0x3001_0030[15:12])	0000	SPI1_CSB	O	I (A1)	NA	SPI master 1
	0110 *	GPIO[35]	I/O			GPIO 35
	0111	WF_GPIO4	I/O			WIFI GPIO 4
GPIO36 (0x3001_0030[19:16])	0000	SPI2_SCK	O	I (A1)	NA	SPI master 2
	0001	UART2_TX	O			UART 2
	0100	SPI2_SCK_S	I			SPI slave 2
	0110 *	GPIO[36]	I/O			GPIO 36
	0111	WF_GPIO5	I/O			WIFI GPIO 5
GPIO37 (0x3001_0030[23:20])	0000	SPI2_MOSI	O	I (A1)	NA	SPI master 2
	0001	UART2_RTS	O			UART 2
	0010	I2C2_CLK	I/O			I2C 2
	0100	SPI2_MOSI_S	I			SPI slave 2
	0110 *	GPIO[37]	I/O			GPIO 37
GPIO38 (0x3001_0030[27:24])	0000	SPI2_MISO	I	I	NA	SPI master 2
	0001	UART2_RX	I			UART 2

IO name (CR Address)	CR Value Default *	Name	Dir	Default dir	Default PU/PD	Description
	0010	I2C2_DATA	I/O			I2C 2
	0100	SPI2_MISO_S	O			SPI slave 2
	0110 *	GPIO[38]	I/O			GPIO 38
GPIO39 (0x3001_0030[31:28])	0000	SPI2_CSA	O	I (A1)	NA	SPI master 2
	0001	UART2_CTS	I			UART 2
	0100	SPI2_CS_S	I			SPI slave 2
	0110 *	GPIO[39]	I/O			GPIO 39
GPIO40 (0x3001_0034[3:0])	0000	SPI2_CSB	O	I (A1)	NA	SPI master 2
	0110 *	GPIO[40]	I/O			GPIO 40
GPIO41 (0x3001_0034[7:4])	0000 *	ADC0	I	I	NA	ADC 0
	0110	GPIO[41]	I/O			GPIO 41
GPIO42 (0x3001_0034[11:8])	0000 *	ADC1	I	I	NA	ADC 1
	0110	GPIO[42]	I/O			GPIO 42
GPIO43 (0x3001_0034[15:12])	0000 *	ADC2	I	I	NA	ADC 2
	0110	GPIO[43]	I/O			GPIO 43
GPIO44 (0x3001_0034[19:16])	0000 *	ADC3	I	I	NA	ADC 3
	0110	GPIO[44]	I/O			GPIO 44
GPIO45 (0x3001_0034[23:20])	0000 *	ADC4	I	I	NA	ADC 4
	0110	GPIO[45]	I/O			GPIO 45
GPIO46 (0x3001_0034[27:24])	0000 *	ADC5	I	I	NA	ADC 5
	0110	GPIO[46]	I/O			GPIO 46
GPIO47 (0x3001_0034[31:28])	0000 *	ADC6	I	I	NA	ADC 6
	0110	GPIO[47]	I/O			GPIO 47

IO name (CR Address)	CR Value Default *	Name	Dir	Default dir	Default PU/PD	Description
GPIO48 (0x3001_0038[3:0])	0000 *	ADC7	I	I	NA	ADC 7
	0110	GPIO[48]	I/O			GPIO 48
DEBUG_RXD (0x3001_0038[7:4])	0000	UART_RX_CA7	I	I	PU	CA7 debug UART
	0110 *	GPIO[49]	I/O			GPIO 49
DEBUG_TXD (0x3001_0038[11:8])	0000	UART_TX _CA7	O	I (A1)	PD	CA7 debug UART
	0110 *	GPIO[50]	I/O			GPIO 50
DEBUG_RTS (0x3001_0038[15:12])	0000	UART_RTS_CA7	O	I (A1)	PD	CA7 debug UART
	0110 *	GPIO[51]	I/O			GPIO 51
DEBUG_CTS (0x3001_0038[19:16])	0000	UART_CTS_CA7	I	I	PU	CA7 debug UART
	0110 *	GPIO[52]	I/O			GPIO 52
SWD_DIO (0x3001_0038[23:20])	0000	SWD_DIO	I/O	I	PU	SWD debugger
	0100	WF_LED_B	I/O			WIFI action LED indication signal
	0110	GPIO[53]	I/O			GPIO 53
SWD_CLK (0x3001_0038[27:24])	0000	SWD_CLK (I)	I	I	PD	SWD debugger
	0011	ICAP_TRIG_EXT	I			WIFI capture mode trigger signal
	0110	GPIO[54]	I/O			GPIO 54
SWO (0x3001_0038[31:28])	0000	SWO_PLUTON	O	O	NA	PLUTON SWO output
	0001	SWO_IO0	O			IO0 SWO output
	0010	SWO_IO1	O			IO1 SWO output
	0011	ICAP_TRIG_EXT	I			WIFI capture mode trigger signal
	0100	WF_LED_B	I/O			WIFI action LED indication signal
	0110	GPIO[55]	I/O			GPIO 55
GPIO56 (0x3001_003C[3:0])	0000	I2S0_TX	O	I (A1)	NA	I2S 0
	0110 *	GPIO[56]	I/O			GPIO 56

IO name (CR Address)	CR Value Default *	Name	Dir	Default dir	Default PU/PD	Description
	0111	WF_GPIO0	I/O			WIFI GPIO 0
GPIO57 (0x3001_003C[7:4])	0000	I2S0_MCLK	O	I (A1)	NA	I2S 0
	0110 *	GPIO[57]	I/O			GPIO 57
	0111	WF_GPIO1	I/O			WIFI GPIO 1
GPIO58 (0x3001_003C[11:8])	000	I2S0_FS	I	I	NA	I2S 0
	0110 *	GPIO[58]	I/O			GPIO 58
	0111	WF_GPIO2	I/O			WIFI GPIO 2
GPIO59 (0x3001_003C[15:12])	0000	I2S0_RX	I	I	NA	I2S 0
	0110 *	GPIO[59]	I/O			GPIO 59
	0111	WF_GPIO3	I/O			WIFI GPIO 3
GPIO60 (0x3001_003C[19:16])	0000	I2S0_BCLK	I	I	NA	I2S 0
	0110 *	GPIO[60]	I/O			GPIO 60
	0111	WF_GPIO4	I/O			WIFI GPIO 4
GPIO61 (0x3001_003C[23:20])	0000	I2S1_TX	O	I (A1)	NA	I2S 1
	0110 *	GPIO[61]	I/O			GPIO 61
	0111	WF_GPIO5	I/O			WIFI GPIO 5
GPIO62 (0x3001_003C[27:24])	0000	I2S1_MCLK	O	I (A1)	NA	I2S 1
	0110 *	GPIO[62]	I/O			GPIO 62
GPIO63 (0x3001_003C[31:28])	0000	I2S1_FS	I	I	NA	I2S 1
	0110 *	GPIO[63]	I/O			GPIO 63
GPIO64 (0x3001_0040[3:0])	0000	I2S1_RX	I	I	NA	I2S 1
	0110 *	GPIO[64]	I/O			GPIO 64
GPIO65 (0x3001_0040[7:4])	0000	I2S1_BCLK	I	I	NA	I2S 1
	0110 *	GPIO[65]	I/O			GPIO 65

IO name (CR Address)	CR Value Default *	Name	Dir	Default dir	Default PU/PD	Description
GPIO66 (0x3001_0040[11:8])	0000	SPI3_SCK	O	I (A1)	NA	SPI master 3
	0001	UART3_TX	O			UART 3
	0100	SPI3_SCK_S	I			SPI slave 3
	0110 *	GPIO[66]	I/O			GPIO 66
GPIO67 (0x3001_0040[15:12])	0000	SPI3_MOSI	O	I (A1)	NA	SPI master 3
	0001	UART3_RTS	O			UART 3
	0010	I2C3_CLK	I/O			I2C 3
	0100	SPI3_MOSI_S	I			SPI slave 3
	0110 *	GPIO[67]	I/O			GPIO 67
GPIO68 (0x3001_0040[19:16])	0000	SPI3_MISO	I	I	NA	SPI master 3
	0001	UART3_RX	I			UART 3
	0010	I2C3_DATA	I/O			I2C 3
	0100	SPI3_MISO_S	O			SPI slave 3
	0110 *	GPIO[68]	I/O			GPIO 68
GPIO69 (0x3001_0040[23:20])	0000	SPI3_CSA	O	I (A1)	NA	SPI master 3
	0001	UART3_CTS	I			UART 3
	0100	SPI3_CS_S	I			SPI slave 3
	0110 *	GPIO[69]	I/O			GPIO 69
GPIO70 (0x3001_0040[27:24])	0000	SPI3_CSB	O	I (A1)	NA	SPI master 3
	0110 *	GPIO[70]	I/O			GPIO 70
GPIO71 (0x3001_0040[31:28])	0000	SPI4_SCK	O	I (A1)	NA	SPI master 4
	0001	UART4_TX	O			UART 4
	0100	SPI4_SCK_S	I			SPI slave 4
	0110 *	GPIO[71]	I/O			GPIO 71
GPIO72 (0x3001_0044[3:0])	0000	SPI4_MOSI	O	I (A1)	NA	SPI master 4
	0001	UART4_RTS	O			UART 4
	0010	I2C4_CLK	I/O			I2C 4
	0100	SPI4_MOSI_S	I			SPI slave 4
	0110 *	GPIO[72]	I/O			GPIO 72
GPIO73	0000	SPI4_MISO	I	I	NA	SPI master 4

IO name (CR Address)	CR Value Default *	Name	Dir	Default dir	Default PU/PD	Description
(0x3001_0044[7:4])	0001	UART4_RX	I			UART 4
	0010	I2C4_DATA	I/O			I2C 4
	0100	SPI4_MISO_S	O			SPI slave 4
	0110 *	GPIO[73]	I/O			GPIO 73
GPIO74 (0x3001_0044[11:8])	0000	SPI4_CSA	O	I (A1)	NA	SPI master 4
	0001	UART4_CTS	I			UART 4
	0100	SPI4_CS_S	I			SPI slave 4
	0110 *	GPIO[74]	I/O			GPIO 74
GPIO75 (0x3001_0044[15:12])	0000	SPI4_CSB	O	I (A1)	NA	SPI master 4
	0110 *	GPIO[75]	I/O			GPIO 75
IO0_GPIO85 (0x3001_0048[23:20])	0000	UART_RX_IO0	I	I	PU	IO0 CM4 debug UART
	0001	TDATA[4]	O			TPIU trace port
	0110 *	GPIO[85]	I/O			GPIO 85
IO0_GPIO86 (0x3001_0048[27:24])	0000	UART_TX _IO0	O	I (A1)	PD	IO0 CM4 debug UART
	0001	TDATA[5]	O			TPIU trace port
	0110 *	GPIO[86]	I/O			GPIO 86
IO0_GPIO87 (0x3001_0048[31:28])	0000	UART_RTS_IO0	O	I (A1)	PU	IO0 CM4 debug UART
	0001	TDATA[6]	O			TPIU trace port
	0110 *	GPIO[87]	I/O			GPIO 87
IO0_GPIO88 (0x3001_004C[3:0])	0000	UART_CTS_IO0	I	I	PU	IO0 CM4 debug UART
	0001	TDATA[7]	O			TPIU trace port
	0110 *	GPIO[88]	I/O			GPIO 88
IO1_GPIO89 (0x3001_004C[7:4])	0000	UART_RX_IO1	I	I	PU	IO1 CM4 debug UART
	0001	TDATA[8]	O			TPIU trace port
	0110 *	GPIO[89]	I/O			GPIO 89
IO1_GPIO90 (0x3001_004C[11:8])	0000	UART_TX _IO1	O	I (A1)	PD	IO1 CM4 debug UART
	0001	TDATA[9]	O			TPIU trace port
	0110 *	GPIO[90]	I/O			GPIO 90
IO1_GPIO91 (0x3001_004C[15:12])	0000	UART_RTS_IO1	O	I (A1)	PD	IO1 CM4 debug UART
	0001	TDATA[10]	O			TPIU trace port

IO name (CR Address)	CR Value Default *	Name	Dir	Default dir	Default PU/PD	Description
	0110 *	GPIO[91]	I/O			GPIO 91
IO1_GPIO92 (0x3001_004C[19:16])	0000	UART_CTS_IO1	I	I	PU	IO1 CM4 debug UART
	0001	TDATA[11]	O			TPIU trace port
	0100	WF_LED_B	I/O			WIFI action LED indication signal
	0110 *	GPIO[92]	I/O			GPIO 92

5.4 Bootstrap

This section describes the MT3620 bootstrap function. During power up the chip will detect various configuration options and operating modes based on the state of several 'bootstrapping pins'. These pins are not dedicated for this strapping purpose, they are shared with other chip functions. After chip reset, this configuration information is stored in a register which determines the device configuration and operating mode.

The following pins are used for bootstrap:

- DEBUG_TXD
- DEBUG_RTSIO0_TXD
- IO0_RTS
- IO1_TXD
- RECOVERY_TXD
- RECOVERY_RTS

MT3620 system design should follow the following guidelines:

- The bootstrapping pins shall not be used as input functions because an external signal might affect the values sensed at boot.
- These pins shall not be used with an open-drain function because the pull-up resistor would affect the values sensed at boot.
- These pins may default to being outputs before being configured by firmware. This doesn't affect the bootstrapping function but the user should make sure that any boot-time outputs do not conflict with external signals to which these pins are connected.
- Strapping pins should be pulled low or high with a 4.7kΩ resistor.

Each of DEBUG_TXD, IO1_TXD and RECOVERY_RTS must always be pulled low. The other strapping pins should be wired according to the information in Table 24 – Table 25.

Table 24. Bootstrap Option – Flash Recovery Mode

Flash recovery mode	Strapping Pin Name DEBUG_RTS	Description
Normal mode	Pull-down(1)	ROM code jumps to XIP flash to initial standard boot.
Recovery mode	Pull-up	ROM code does not jump to XIP flash but will wait for UART commands on the RECOVERY UART.

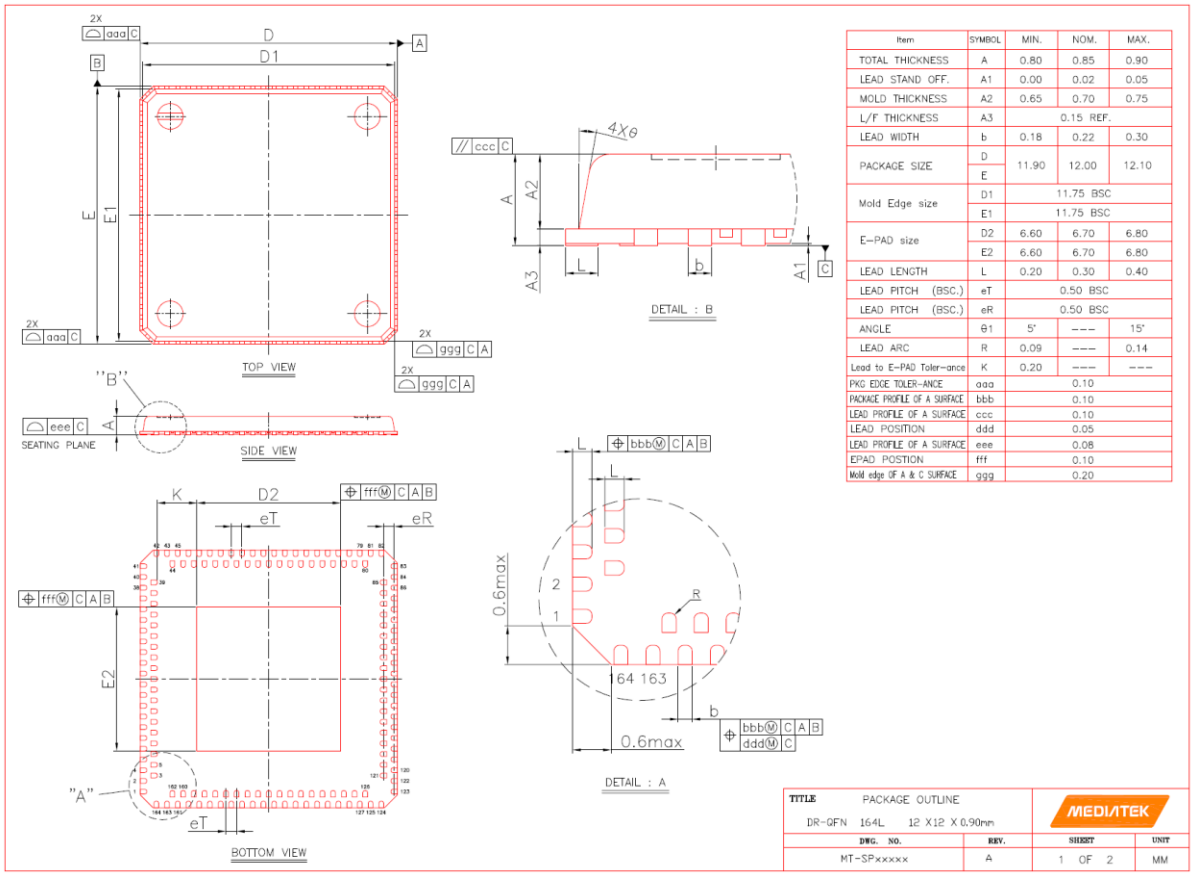
Note: No external pull-down resistor is required because internal pull-down is active during power up.

Table 25. Bootstrap Option – 32kHz Clock Option

32kHz clock option	Strapping Pin Name RECOVERY_TXD	Description
Internal 32kHz clock	Pull-down	32kHz clock sourced from 26MHz clock (default)
External 32kHz clock	Pull-up	32kHz clock sourced from external pin

5.5 Package Information

MT3620 is DR-QFN 12mmx12mm package and the package diagram is shown below.



Item	SYMBOL	MIN.	NOM.	MAX.
TOTAL THICKNESS	A	0.80	0.85	0.90
LEAD STAND OFF.	A1	0.00	0.02	0.05
MOLD THICKNESS	A2	0.65	0.70	0.75
L/F THICKNESS	A3		0.15 REF.	
LEAD WIDTH	b	0.18	0.22	0.30
PACKAGE SIZE	D	11.90	12.00	12.10
	E			
Mold Edge size	D1		11.75 BSC	
	E1		11.75 BSC	
E-PAD size	D2	6.60	6.70	6.80
	E2	6.60	6.70	6.80
LEAD LENGTH	L	0.20	0.30	0.40
LEAD PITCH (BSC.)	eT		0.50 BSC	
LEAD PITCH (BSC.)	eR		0.50 BSC	
ANGLE	θ1	5°	---	15°
LEAD ARC	R	0.09	---	0.14
Lead to E-PAD Toler-ance	K	0.20	---	---
PKG EDGE TOLER-ANCE	aaa		0.10	
PACKAGE PROFILE OF A SURFACE	bbb		0.10	
LEAD PROFILE OF A SURFACE	ccc		0.10	
LEAD POSITION	ddd		0.05	
LEAD PROFILE OF A SURFACE	eee		0.08	
EPAD POSTION	fff		0.10	
Mold edge OF A & C SURFACE	ggg		0.20	

Figure 9. Package outline drawing

5.6 Top Mark

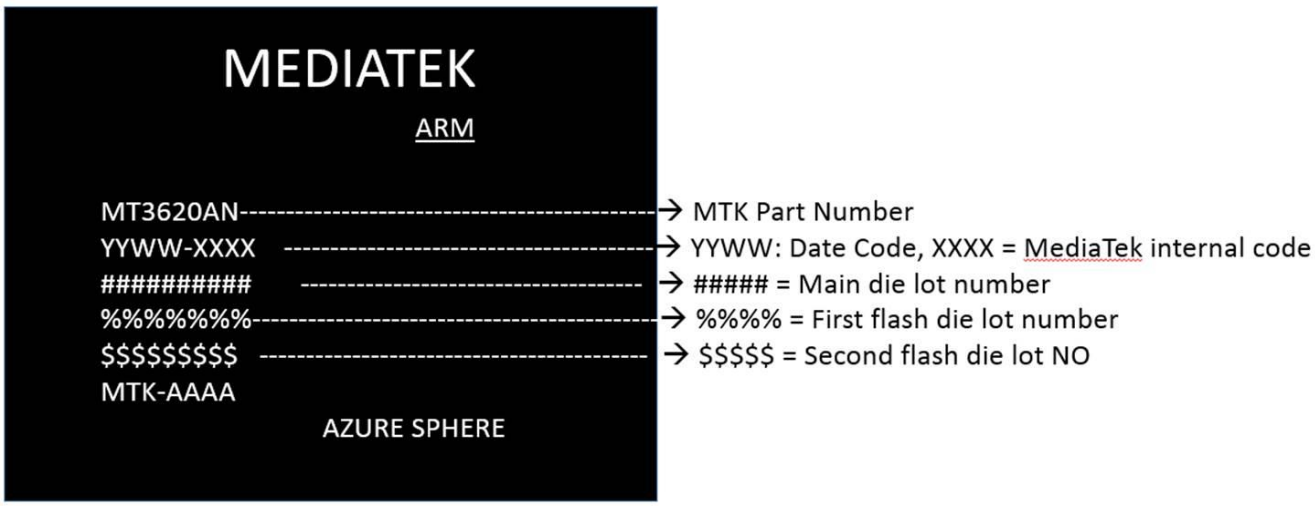


Figure 10. Top Mark

6 General

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