Effects of Substrate Surface Preparation on Chemical Vapor Deposition Growth of 4H-SiC Epitaxial Layers

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The effects of chemical mechanical polish (CMP) and pre-growth oxidation and etching of vicinal 4H-SiC substrates on the quality of epitaxial films have been investigated. Samples with and without a collodial silica CMP and oxidation/etch treatment were studied with optical microscopy, cross section transmission electron microscopy (TEM) and atomic force microscopy (AFM) before and after chemical vapor deposition. Evidence of polishing damage was evident prior to growth in all samples without CMP treatment. Oxidation and etching appeared to generate defects by preferential etching of bulk defects such as dislocations and low angle grain boundaries. Evidence of the polishing damage remained after chemical vapor deposition (CVD) growth on the samples without CMP and the defect density was worse for the oxidized samples compared to the unoxidized ones. The unoxidized CMP wafer had the lowest defect density and rms roughness of the samples studied.

Key words: Chemical mechanical polishing, silicon carbide, atomic force microscopy, surface morphology

INTRODUCTION

Silicon carbide (SiC) is a wide bandgap semiconductor being developed for high temperature, high power and high frequency electronic applications. It is also an important substrate for growth of group III nitrides because of its close lattice match and high thermal conductivity. SiC wafers up to 75 mm diameter are currently available and 100 mm diameter wafers have been demonstrated.[1,2] However, due to it's mechanical hardness and resistance to chemical action, SiC is much more difficult to polish than conventional semiconductors such as silicon and gallium arsenide. Standard surface preparation techniques use a diamond paste based mechanical polish to produce a near specular surface that is free of damage to the naked eye. Studies of SiC surfaces have, however, revealed that the surface of commercial wafers is often covered with very fine scratch marks and that a subsurface damage layer extending tens of nanometers from the surface is present.[3,4]

Several techniques have been used to remove the sub-surface damage layer in SiC wafers. Hydrogen etching removes the polishing damage but often leaves a stepped surface that might not be appropriate for all devices.[5,6] Wet oxidation and etching has been used to prepare SiC surfaces for metallization[7–9] and for epitaxial growth.[10] Chemical mechanical polishing (CMP) has been used for some time to prepare damage free surfaces for silicon and gallium arsenide and is under development for SiC.[11,12] CMP is believed to be under development by several wafer suppliers but their processes are proprietary. Zhou et al.[11] have demonstrated a collodial silica based CMP for SiC and achieved removal of the subsurface damage layer present in as-received wafers. Their atomic force microscopy studies demonstrated that scratch-free surfaces could be produced with CMP. Mitchel et al.[12] used a similar process and achieved scratch and damage free surfaces on vicinal 4H-SiC wafers. However, there have been no studies of epitaxial growth of SiC on CMP prepared wafers reported to date that the authors are aware of. We report here such a study of the effects of CMP and oxidation followed by etching on the quality of chemical vapor deposition (CVD) grown SiC. Samples with and without CMP and with

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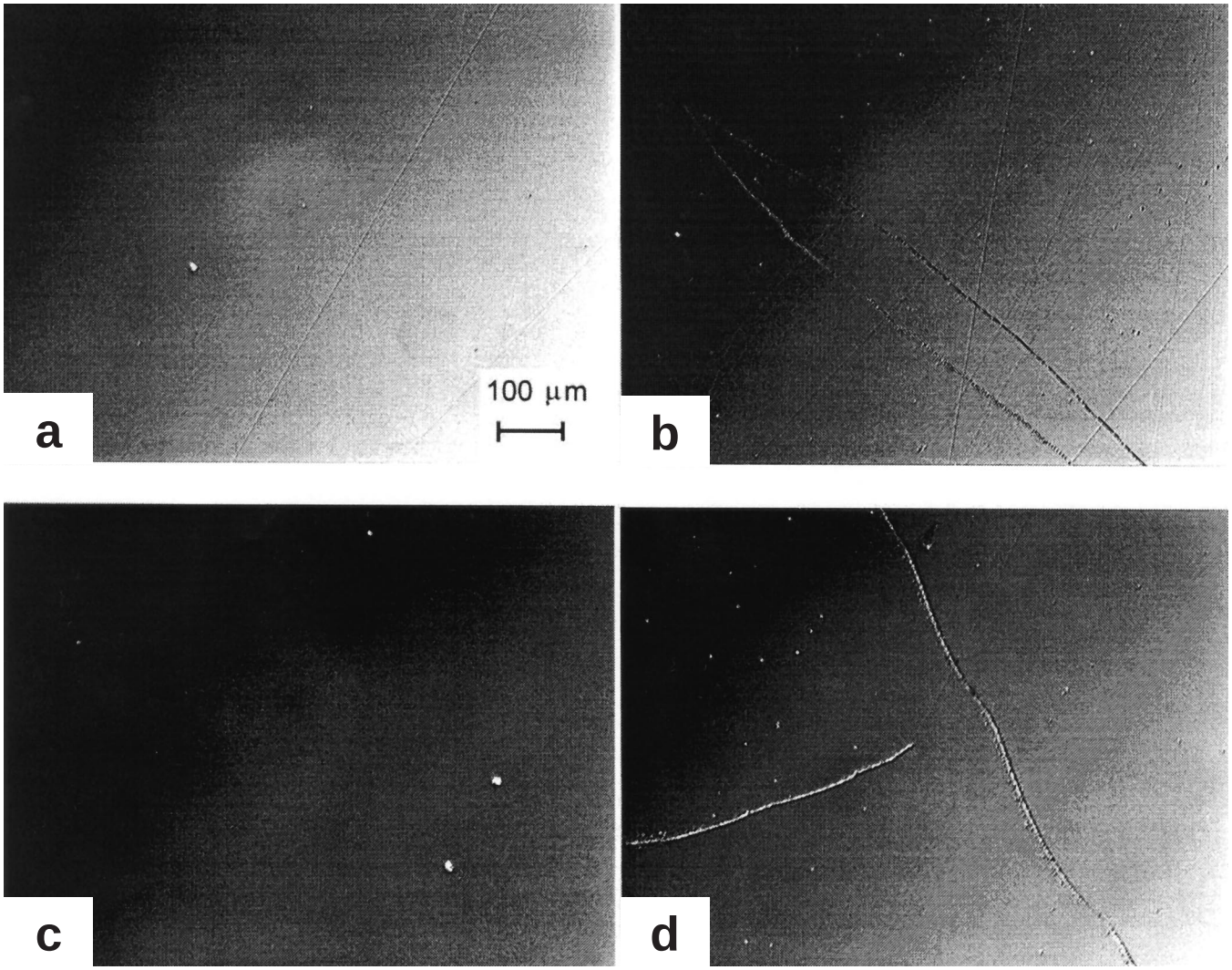

Fig. 1. Nomarski differential interference contrast (NDIC) microscopy images of 4H-SiC substrates. (a) As-received wafer; (b) as-received wafer after wet oxidation and HF etch; (c) sample after CMP; and (d) samples after CMP and oxidation/etch treatment.

and without an oxidation/etch treatment were compared after CVD growth. Based on an AFM study of the surfaces after growth collodial silica based CMP was found to provide the best substrates for growth.

EXPERIMENTAL DETAILS

Substrate Polishing and Oxidation/Etch

The wafers used in this study were standard commercial n-type, 1 3/8 inch diameter, 8° off axis 4H-SiC substrates. One wafer was given CMP treatment and the other was left in the as-received condition for control purposes. The CMP process used in this study is similar to that of Zhou et al.[11] A Strasbaugh model R6DE-DC-4 polisher was used with Rodel regular politex polishing pads and full strength Logitech SF1 collodial silica polishing solution. The wafer was polished for one hour under 2000 gm pressure at a speed of 200 rpm. Unlike Zhou et al. there was no intentional heating of the wafer during polishing. Typical removal rates for unheated polishing were found to be approximately 150 Å/h but this rate was found to have a significant error and to depend on a number of parameters including the age of the polishing pad and the pH of the polishing solution. The wafer was rinsed in DI water immediately after polishing to prevent matter from sticking to the surface. Full wafers were polished because our experience with CMP has shown that the sharp edges of partial wafers tend to cut the polishing pads and chip the wafers. This often results in increased damage to the wafer during the CMP process. We were therefore not able to compare as-received and CMP on the same wafer. The as-received control wafer was chosen to be as similar as possible to the CMP wafer, it was from the same vendor and thus had identical surface treatment but it should be noted that the wafers studied were not from the same boule.

The control wafer and the CMP wafer were first cut in half. One half from each wafer was then treated by wet oxidation. Prior to oxidation the two halves were given a standard RCA clean and a dilute HF etch and then annealed together in wet O_2 at 1150°C for 4 h. After the sacrificial oxidation step the wafers were etched in a dilute HF solution to remove the oxide

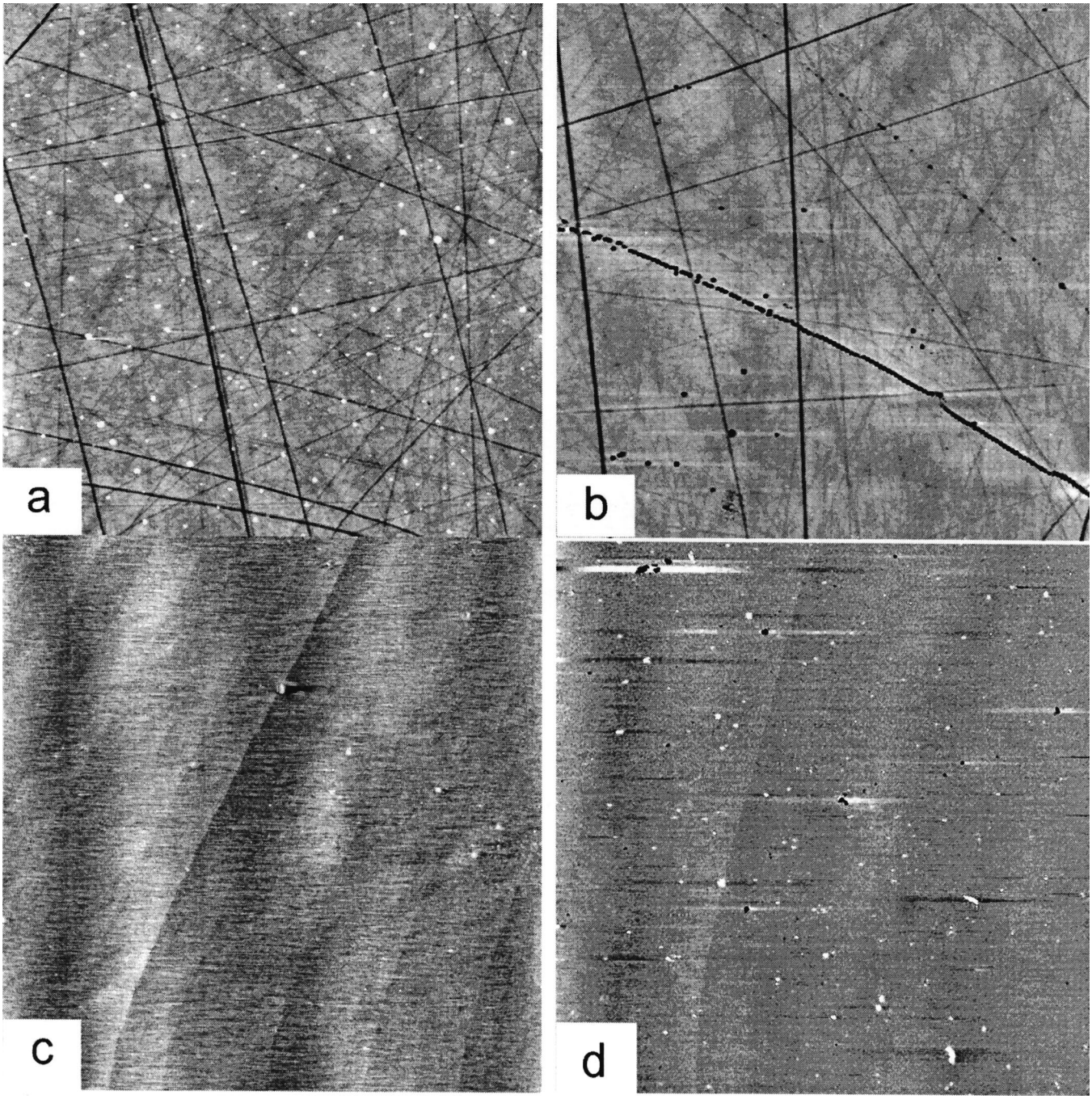

Fig. 2. 50 × 50 μm atomic force microscopy images of SiC substrates after various surface treatments. (a) as-received; (b) oxidation/etch treatment; (c) CMP; and (d) CMP and oxidation/etch treatment.

layer and thus leave an ultraclean SiC surface for subsequent CVD growth.

CVD Growth

Epitaxial growth was performed in a horizontal, cold-wall, atmospheric pressure CVD system using a standard dual-precursor CVD growth technique with a growth temperature of 1580°C.[13] There was no intentional HCl or H_2 etching of the sample prior to initiation of the growth. The RF generator is switched on with H_2 carrier gas and propane precursor gas flow. At 1490°C silane precursor gas flow is added which then begins the growth of the SiC epitaxial layer. The substrate is heated under carbon-rich conditions so that any free Si will not adsorb to the surface but rather form SiC. The epitaxial layer thickness was approximately 2 μm and the conductivity was n-type with a net doping density, as determined by capacitance-voltage techniques using an Hg-probe, of approximately 1×10^{16} cm^{-3}.

RESULTS

Figure 1 shows Nomarski differential interference contrast (NDIC) microscopy images prior to epitaxial

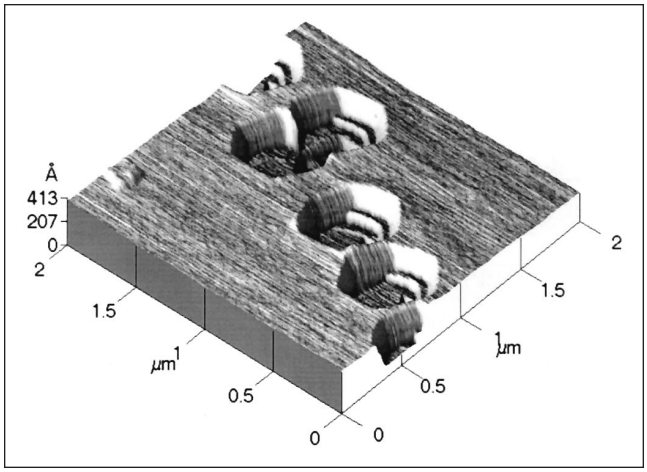

Fig. 3. High resolution AFM image of pits in the oxidized/etched sample from Fig. 2.

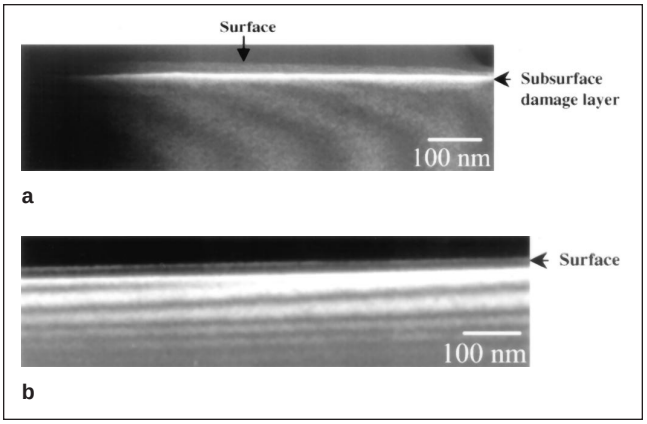

Fig. 4. Cross section TEM micrographs of 4H-SiC growth samples prior to CVD. (a) as-received sample. The bright line just below the top surface is the subsurface damage layer. (b) CMP sample which does not show the damage layer.

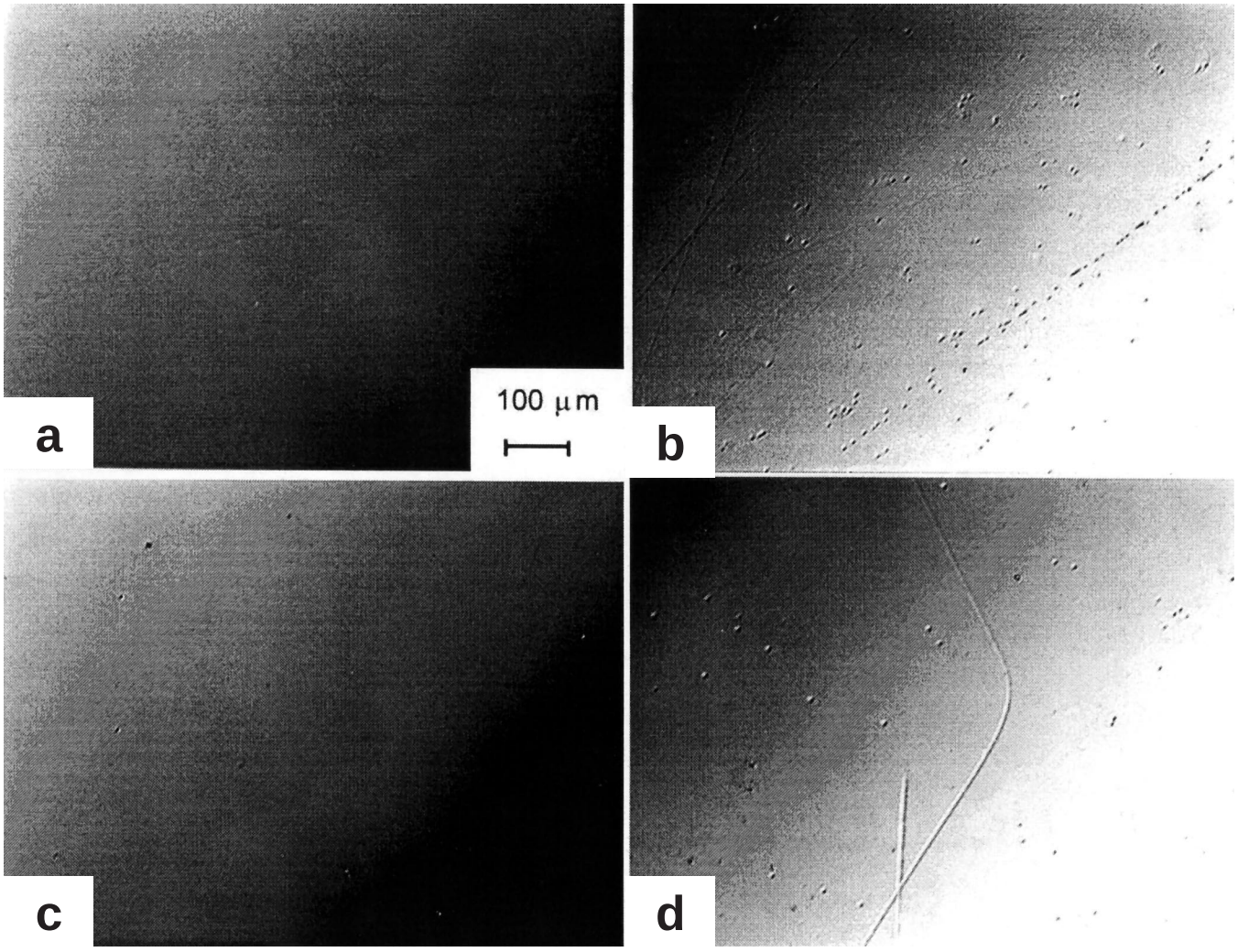

Fig. 5. NDIC images of SiC wafers with various surface treatments after CVD growth. (a) as-received sample; (b) oxidized/etched sample; (c) CMP sample; and (d) CMP and oxidized/etched sample.

growth for the as-received (sample A), the as-received/oxidized/etched (sample B), the CMP only (sample C) and the CMP/oxidized/etched (sample D) samples. Very faint cross hatched scratch marks are visible in both samples A and B but not in the CMP samples. Other than this, the micrographs of the unoxidized samples are, in general, featureless. However, a high density of pits and irregular line defects were ob-

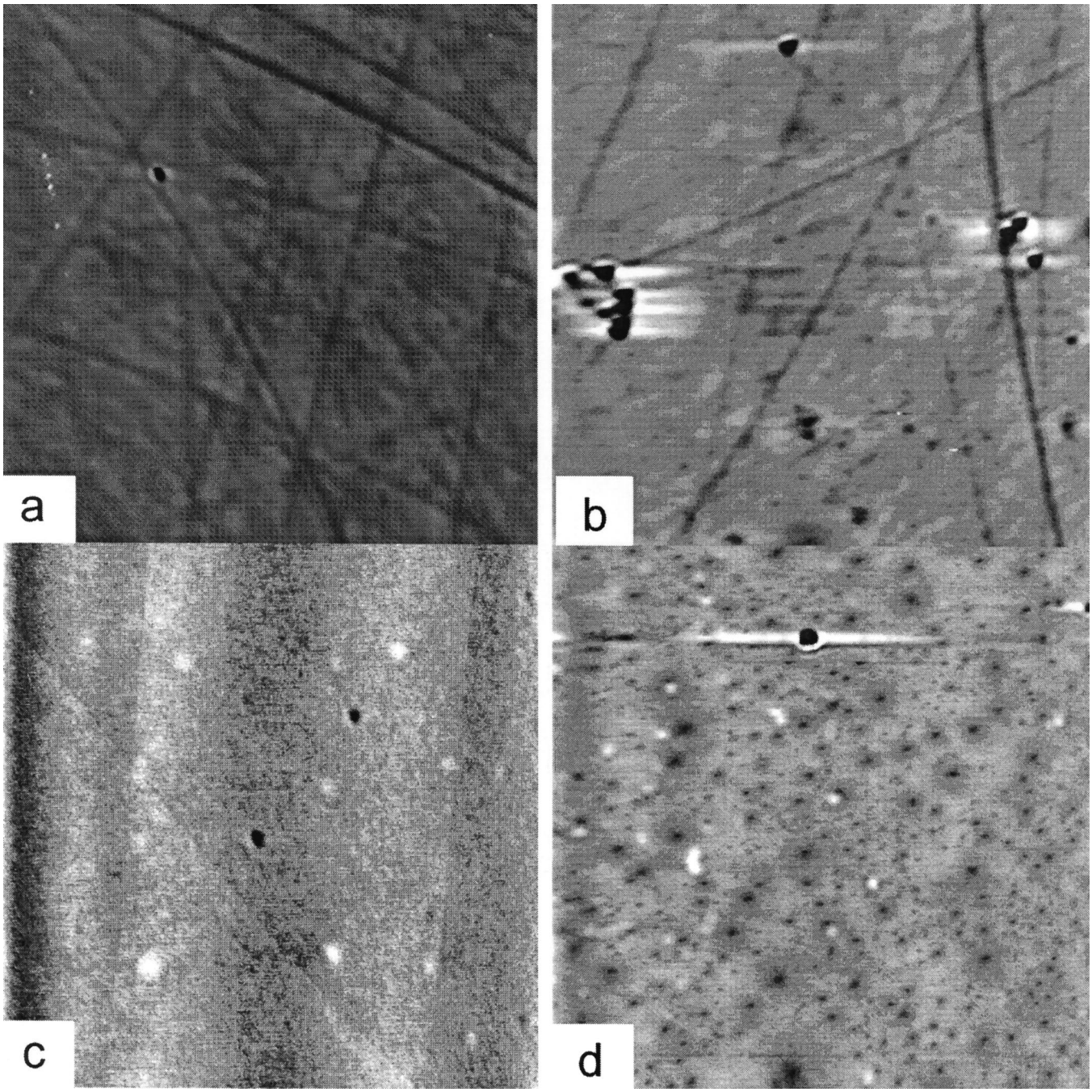

Fig. 6. 50 × 50 μm AFM images of SiC samples after CVD growth. (a) as-received sample; (b) oxidized etched sample; (c) CMP sample; and (d) CMP and oxidized/etched sample. The white dots on c and d are unidentified at this time but similar features can be seen on the images in Fig. 2 as well. They might be contamination created immediately after the termination of the polishing processes.

served in both oxidized/etched samples. These line defects are distinguishable from the polishing induced damage in that the latter are very straight. These features are more clearly visible in the AFM results for the four substrates shown in Fig. 2. The scratch marks are clearly visible in samples A and B and are not present samples C and D. One of the irregular line defects is seen in Fig. 2b. The defect is composed of a dense line of regular hexagonal pits. Many isolated pits in this sample had similar structure. Figure 3 is a higher resolution image of these pits. The pits are very regular and have clearly defined bottoms, which indicates that they are not related to micropipes. Features that resemble these line and isolated defects, but on a much larger scale and less regular, have been reported in a study of molten KOH etched SiC. Ha et al.[14] attribute the linear arrays of dislocation pits to either slip bands or low angle grain boundaries, both of which were present in their samples. We have also seen isolated pits and linear arrays of pits in sample D, but their shape is not as regular. We believe that the isolated

Table I. Atomic Force Microscopy Measurement of Linear RMS Roughness of the CVD Grown 4H-SiC Films

Sample	Treatment	10 × 10 μm	50 × 50 μm
A	As-received	3.52 Å	5.68 Å
B	Oxidized and etched	2.85 Å	7.43 Å
C	CMP	1.06 Å	1.86 Å
D	CMP/oxidized/etched	1.09 Å	2.64 Å

pits in the oxidized samples are due to preferential oxidation at dislocations and that, in agreement with Ha et al, the irregular linear arrays of defects are due to etching of dislocations located at low angle grain boundaries or slip bands. The parallel lines visible in the AFM images of the CMP samples, Fig. 2c and d, are step edges due to the miscut of the wafer. The presence of step edges is an indication of the high quality of the polish. Cross-section-transmission electron microscopy (TEM) micrographs from pieces of samples A and C are shown in Fig. 4. A buried subsurface damage layer is visible in the as-received sample located several tens of nanometers below the surface. This is the bright band marked in the figure. Such subsurface damage in as-received SiC substrates has been reported elsewhere.[3,11] Similar to the results of Zhou et al.[11] we were unable to detect the subsurface damage layer in the TEM micrographs after CMP, shown in Fig. 4b. The broad parallel bands in Fig. 4b are interference fringes and are not related to the damage layer in fig. 4a. Fringes are also visible in Fig. 4a but are less intense. We have observed subsurface layers like this in several as-received SiC wafers but have never seen it in any of the several off-axis SiC wafers with CMP that we have studied to date.

Simultaneous CVD epitaxial layer growth as described in the previous section was performed on the two substrates without oxidation and on the two oxidized/etched substrates. NDIC micrographs of the epitaxial layers are shown in Fig. 5. These micrographs are very similar to those taken before growth. While not readily visible in reproduced images, polishing scratches were still visible in the samples A and B. The defect density in samples A and C was very low as seen in the figure but high in the other two samples. The irregular line defects were still visible after growth but were more diffuse. The density of isolated defects in both samples B and D is similar to that for the isolated pits prior to growth and we feel comfortable in attributing the bulk of the isolated defects in these two samples to the pits produced by the oxidation/etch process. TEM characterization of sample A after growth failed to detect any remnant of the subsurface damage layer seen in Fig. 4a. In fact we were unable to detect the interface by TEM in any of these homoepitaxial samples. This suggests that the in-situ preparation procedures and/or the early stages of growth etch away enough of the substrate to either remove the subsurface damage layer or the growth temperature of approximately 1580°C was sufficient to anneal out the damage. The benefits of CMP are best seen in the AFM images of Fig. 6. The polishing scratches are still visible in both samples A and B but not in the two CMP treated samples. To obtain a more accurate comparison RMS roughness measurements of 50 μm and 10 μm AFM line scans were made. Large pits were deliberately avoided. The averages of several such measurements made within the same image are given in Table I. The 10 μm results are all good, indicating the absence of large scratches at this resolution but as can be seen in the 50 × 50 μm images the CMP samples are clearly superior. Even at 50 μm the RMS roughness was less than 2 Å, while that for the as-received sample was over 5 Å.

CONCLUSIONS

Comparisons of surface and subsurface damage and defects in CVD 4H-SiC epitaxial layers grown on substrates with different surface treatments have been made. Epitaxial layers grown on chemical mechanical polished material was superior to both as-received wafers and oxidized as well as etched wafers. Wet oxidation and etching were effective in removing subsurface damage but produced pits and irregular line defects in the epitaxial layers which is believed to be due to the preferential etching of dislocations at low angle grain boundaries. Oxidation and etch treatments did not remove mechanical polishing induced scratches which were revealed in epitaxial layers grown on substrates without CMP treatment. We therefore conclude that CMP treatment of SiC substrates without a sacrificial oxidation and etching step results in the best substrate surface for subsequent layer growth as determined by the surface morphology and roughness of the grown epitaxial layers investigated in this study.

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REFERENCES

1. D. Hobgood, M. Brady, W. Brixius, G. Fechko, R. Glass, D. Henshall, J. Jenny, R. Leonard, D. Malta, St. G. Müller, V. Tsvetko, and C.H. Carter, Jr., *Mater. Sci. Forum* 338-342, 3 (2000).
2. D.W. Snyder, V.D. Heydemann, W.J. Everson, and D.L. Barrett, *Mater. Sci. Forum* 338-342, 9 (2000).
3. W. Qian, M. Skowronski, G. Augustine, R.C. Glass, H.McD. Hobgood, and R.H. Hopkins, *J. Electrochem. Soc.* 142, 4290 (1995).
4. J.A. Powell and D.J. Larkin, *phys. stat. sol. (b)* 202, 529 (1997).
5. C. Hallin, A.S. Bakin, F. Owman, P. Mårtensson, O. Kordina, and E. Janzén, *Inst. Phys. Conf. Ser.* 141, 613 (1996).
6. V. Ramachandran, M.F. Brady, A.R. Smith, R.M. Feenstra, and D.W. Greve, *J. Electron. Mater.* 27, 308 (1998).
7. T. Teraji, S. Hara, H. Okuski, and K. Kajimura, *Inst. Phys. Conf. Ser.* 142, 593 (1996).
8. S. Liu, K. Reinhart, C. Severt, and J. Scofield, *Inst. Phys. Conf. Ser.* 142, 589 (1996).
9. T. Jang, L.M. Porter, G.W.M. Rutsch, and B. Odekirk, *Appl.*

Phys. Lett. 75, 3956 (1999).
10. U. Starke. Ch. Bram, P.-R. Steiner, W. Hartner, L. Hammer, K. Heinz, and K. Müller, *Appl. Surf. Sci.* 89, 175 (1995).
11. L. Zhou, V. Audurier, P. Pirouz, and J.A. Powell, *J. Electrochem. Soc.* 144, L161 (1997).
12. W.C. Mitchel, J. Brown, D. Buchanan, R. Bertke, K. Mahalingham, F.D. Orazio, Jr., P. Pirouz, H.-J. R. Tseng, U.B. Ramabadran, and B. Roughani, *Mater. Sci. Forum* 338-342, 841 (2000).
13. G. Melnychuk, S.E. Saddow, M. Mynbaeva, S. Rendakova, and V. Dmitriev, *Proc. Mater. Res. Soc.* (in press)
14. S. Ha, N.T. Nuhfer, M. DeGraef, G.S. Rohrer, and M. Skowronski, *Mater. Sci. Forum* 338-342, 477 (2000).