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Advances in AFM for the electrical characterization of semiconductors

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Abstract

Atomic force microscopy (AFM) is a key tool for nanotechnology research and finds its principal application in the determination of surface topography. However, the use of the AFM tip as a probe of electrical properties allows enormous insights into material functionality at the nanoscale. Hence, a burgeoning suite of techniques has been developed to allow the determination of properties such as resistivity, surface potential and capacitance simultaneously with topographic information. This has required the development of new instrumentation, of novel probes and of advanced sample preparation techniques. In order to understand and quantify the results of AFM-based electrical measurements, it has proved important to consider the interplay of topographic and electrical information, and the role of surface states in determining a material's electrical response at the nanoscale. Despite these challenges, AFM-based techniques provide unique insights into the electrical characteristics of ever-shrinking semiconductor devices and also allow us to probe the electrical properties of defects and self-assembled nanostructures.

(Some figures in this article are in colour only in the electronic version)

This article was invited by Professor C J Humphreys.

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List of acronyms

1D	one dimensional	C-V	capacitance-voltage
2D	two dimensional	CVD	chemical vapour deposition
3DAP	three-dimensional atom probe	DT	direct tunnelling
AFM	atomic force microscopy	ECAFM	enhanced conductive atomic force microscopy
C-AFM	conductive atomic force microscopy	EFM	electrical force microscopy
		EJ	electrical junction

ELOG	epitaxial layer overgrowth
ESD	electrostatic discharge
FEM	finite element modelling
FIB	focused ion beam
FNT	Fowler–Nordheim tunnelling
GB	grain boundary
IC	intermittent contact
ISO	International Organization for Standardization
I – V	current–voltage
KPFM	Kelvin probe force microscopy
LED	light emitting diode
LPE	liquid phase epitaxy
MJ	metallurgical junction
MOS	metal–oxide–semiconductor
MOVPE	metal–organic vapour phase epitaxy
NF EBIC	near-field electron beam induced current imaging
nid	non-intentionally doped
QD	quantum dot
QW	quantum well
SCM	scanning capacitance microscopy
SCS	scanning capacitance spectroscopy
SDSRM	scanning differential spreading resistance microscopy
SIMS	secondary ion mass spectrometry
SNR	signal-to-noise ratio
SOI	silicon-on-insulator
SPM	scanning probe microscopy
SRP	spreading resistance profiling
SSRM	scanning spreading resistance microscopy
SSRS	scanning spreading resistance spectroscopy
STM	scanning tunnelling microscopy
SVM	scanning voltage microscopy
TD	threading dislocation
TEM	transmission electron microscopy
TUNA	tunnelling atomic force microscopy
UHV	ultra-high vacuum
VLS	vapour–liquid–solid

1. Introduction

1.1. Probing semiconductors at the nanoscale

The invention of scanning probe microscopy (SPM) has provided scientists with unprecedented access to the nanoscale structure of materials and is seen by many as the starting point of the nanoscience and nanotechnology revolution [1]. In particular, atomic force microscopy (AFM) has proved enormously adaptable, and is now used to assess not only the topography of nanostructured samples but also a diverse range of other properties: mechanical, electrical and magnetic. Simultaneous with the development of techniques to explore the ‘nanoworld’, the apparently inexorable shrinkage of silicon electronics has pushed critical device dimensions down to the nanometre level and researchers have discovered a plethora of techniques for the formation of nanoscale structures. Hence, the semiconductor industry and semiconductor

research and development programmes now place stringent demands on techniques to measure the electrical properties of semiconductor nanostructures and devices; demands that the AFM is well-placed to meet [2].

This report focuses on the most common AFM-based techniques which are used to characterize the electrical properties of semiconductor structures. The principles of each technique are described, introducing the reader to the basic physics that allows electrical-property-dependent contrast to be observed in an SPM image, and the instrumentation which is required in order to practically achieve this. Armed with such a toolkit, the review then describes the application of AFM-based electrical characterization techniques, not only to the most common applications of dopant density assessment and the study of conventional semiconductor devices but also to the assessment of defects in semiconductors and of self-assembled nanostructures.

Given the simplicity of the AFM principle—not dissimilar to that of an old-fashioned record player—it is astounding just how much can be achieved by scanning a very small tip very close to a semiconductor surface. However, throughout our discussions of the various applications of SPM to semiconductor characterization, a number of challenges are encountered. As the demands of the scientific community become ever more stringent in terms of resolution, calibration accuracy, elimination of artefacts and application to diverse problems, AFM-based techniques will have to develop still further. The range of available AFM techniques is continually broadening, and it seems we remain far from the limits of scientists’ imaginations in terms of the uses to which our ‘very small tip’ can be put. Hence in the last sections of this review, some of the recent attempts to overcome common disadvantages of AFM-based techniques are discussed, along with the latest developments in SPM characterization of electronic materials and devices.

1.2. The atomic force microscope

Since its invention by Binnig *et al* [3] as an extension of the scanning tunnelling microscope (STM), the atomic force microscope (AFM) has achieved immense popularity as a tool for the examination of semiconductor materials. Briefly leaving aside its application in electrical characterization, it is an ideal tool for nanoscale morphological assessment. Sub-Ångstrom vertical resolution and ~ 5 nm lateral resolution may be routinely achieved in an ambient environment, without any requirement for sample conductivity or sophisticated surface preparation. This combination of high resolution and easy implementation [4] along with the stringent requirements of the semiconductor industry in terms of surface roughness and defect density [5] have made AFM an attractive option for ‘in-line’ semiconductor process evaluation [6], in addition to the technique’s broad appeal in the research environment. With the development of low cost systems, the AFM is becoming increasingly ubiquitous. Here, we introduce the basic principles which underlie the technique, to provide the necessary background for our later discussion of AFM-based electrical characterization.

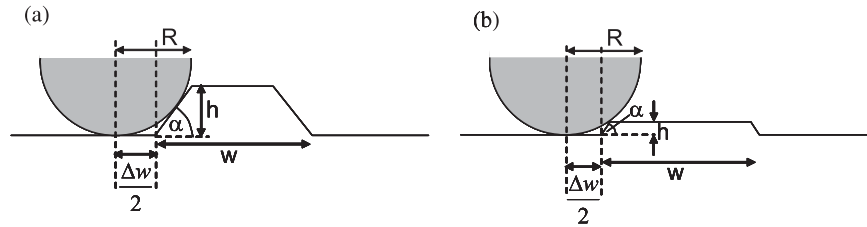


Figure 1. Schematic of the interaction of a hemispherical tip with a flat-topped nanoscale island for (a) $h > R(1 - \cos \alpha)$ and (b) $h < R(1 - \cos \alpha)$.

1.2.1. Basic principles. In AFM, an ultrasharp tip mounted on a very small cantilever (typically a few $100\ \mu\text{m}$ long and a few tens of micrometres wide) is positioned very close to the sample surface. The ability to position this probe with extremely high precision is key to the success of scanning probe techniques and is usually achieved using piezo-electric actuators [7]. In the simplest mode of operation, the probe is scanned over the surface and the deflection of the cantilever is measured, most commonly by monitoring the deviation of a laser beam reflected from the cantilever using a 4-sector photodetector. The deflection of the cantilever is, to a good approximation, directly proportional to the force on the cantilever. Although some of the earliest measurements were taken in this way [8], with the deflection of the cantilever varying as it was scanned over the sample, from the technique's inception [3], feedback circuits have been used to control the voltage applied to the relevant piezo-element, and hence to maintain a constant cantilever deflection. This allows the user to control the force acting on the sample, maintaining a low value even for significant changes in sample height, and thus preventing damage to both tip and sample. The piezo-elements must be carefully calibrated in order that the voltages applied to maintain the cantilever deflection setpoint may be accurately converted into changes in the height of the sample surface. This is usually achieved using lithographically or holographically defined calibration grids.

Contact mode, where the AFM tip is in constant contact with the sample and its deflection is measured and maintained, is one of the two most popular AFM operation modes. The other is intermittent contact (IC) mode, often referred to as tapping mode. In this case a small piezo-electric element is used to vibrate the cantilever at, or close to, its resonant frequency. As the tip is brought towards the sample, the interaction between the tip and the sample leads to a force gradient which modifies the cantilever resonant frequency, so that for a fixed drive frequency, the cantilever's amplitude of vibration decreases [9]. Additionally, for typical IC mode conditions, the tip makes contact with the surface at the bottom of each oscillation, resulting in a damping of the cantilever oscillation amplitude. (Further details of the tip-sample interaction are beyond the scope of this review, but the reader is referred to Burnham *et al* [10] for more information.) Overall, under typical imaging conditions, the amplitude of vibration is dependent on the tip-sample distance, and hence with appropriate calibration may be used to measure changes in the sample height. In this case the feedback circuit is employed to maintain a constant cantilever vibration amplitude rather

than a constant cantilever deflection. The major advantage of this approach over contact mode is that since the probe only contacts the sample briefly, at the bottom of its downward swing, lateral (friction) forces between tip and sample are minimized, reducing the likelihood of soft samples being damaged. In fact, semiconductor samples are generally rather hard, and this is less of a concern, but the reduced lateral forces also reduce tip wear, and IC mode is popular for all material types for this reason.

1.2.2. Topographic resolution. For most commercial AFM systems, the achievable vertical resolution is limited only by the resolution of the vertical scanner movement which is usually significantly sub-Ångström. In practical terms, acoustic, mechanical or electrical noise means that the resolution does not achieve this ultimate limit. However, the lateral resolution is determined entirely by the radius of the apex of the probe used. The measured topography is often rather inaccurately described as a convolution of the real surface and the tip shape. To describe the tip-sample interaction more correctly, operations from mathematical morphology should be used: dilation describes the image formation process, and its dual operation, erosion, can then be used to try to recover the 'true' surface from the image [11]. However, further details of the mathematics need not concern us here. Instead, as a simple example, we consider a schematic (figure 1) of a hemispherical tip, traversing a surface on which there is a flat-topped island of width w , height h and sidewall angle α . As shown, it is not just the apex of the tip that touches the island, but also the sides. In this simple case, it may be shown using basic trigonometry that the measured width is larger than the real width by an amount Δw :

$$\frac{\Delta w}{2} = \begin{cases} \sqrt{h(2R-h)} - h \cot \alpha & \text{for } h < R(1 - \cos \alpha), \\ R \tan(\alpha/2) & \text{for } h \geq R(1 - \cos \alpha). \end{cases}$$

Whilst the specifics of this example are not significant, it is important to note that the error in the width measurement depends not only on the shape of the tip but also on the shape of the object being imaged. This means that for an unknown tip shape imaging an unknown object, the process of recovering the 'true' shape of the object from the image is in no way straightforward. Whilst routines using the tools of mathematical morphology have been developed which attempt to do this [11], it is not possible for such methods to provide a perfect reconstruction of the true surface.

One should remember that the shape of the tip may also affect the measured data in the vertical direction. For a closely

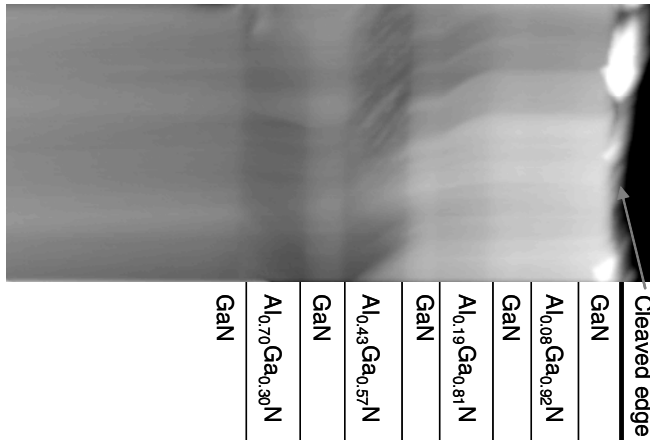


Figure 2. AFM image of a cleaved $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ multi-layer, illustrating that topographic imaging of cleaved samples may provide information about sub-surface layers.

packed array of nanostructures, the finite size of the tip may make it impossible for it to penetrate to the bottom of the gaps between the structures, resulting in an underestimate of the nanostructure height. For deep trenches, even for tips with sharp apexes, the slope of the tip sides away from the apex will often prevent the tip from accurately measuring the trench sidewall angle, and may also impede it from reaching the bottom of the trench.

1.2.3. Typical applications. Despite these well-known limitations, AFM is extremely widely used in semiconductor research. In the fabrication of silicon-based integrated circuits, AFM has found application at many stages of the process, from the analysis of boules of Czochralski-grown bulk silicon [12], to the investigation of surface polishing [13] and etching [14], the development of new etch resists [15], and the assessment of oxidation [16] and metallization [17] processes. Outside of the device fabrication sphere, AFM is used to explore the growth of epitaxial layers [18], including self-assembled quantum dots [19], to characterize and quantify defect structures [20] and in many other surface characterization applications. Whilst AFM is intrinsically a surface characterization technique, it may also be used to investigate sub-surface structures—most commonly by cleaving a semiconductor wafer and analysing the cleaved surface.

An example of a topographic image of a cleaved semiconductor multi-layer is shown in figure 2. The sample consists of $\text{Al}_{1-x}\text{Ga}_x\text{N}$ layers of varying composition (x) separated by GaN spacers [21], which may be observed in the AFM image as shallow troughs (ca 0.5–2 nm deep), whose depth depends on the Al-content of the layer. The existence of topographic changes associated with strained epitaxial layers is due to a partial relaxation of the epitaxial growth strain in the layers; in this case the strain is tensile, causing inward bowing of the surface. The imaging of cleaved multi-layers is a key technique in electrical characterization of semiconductors, since it is widely used to provide access to sub-surface layers with varying electrical characteristics in test samples and device structures.

2. AFM-based electrical characterization techniques

Before reviewing some of the applications of AFM-based methodologies to the electrical characterization of semiconductors, we first outline the basic physics underlying the most commonly used techniques.

2.1. Electrical force microscopy

In topographic imaging, the main forces on the AFM tip are due to the van der Waal's interaction between the tip and the sample and, for small tip-sample separations, electrostatic repulsion between the electron clouds of the tip and sample atoms. Additionally, for imaging in air, a fluid layer may form on the surface and capillary forces play a role. The key insight which led to the development of electrical force microscopy (EFM) and various related techniques is the possibility of using the AFM tip to measure other local forces. Initially, the additional forces measured were magnetic [22]. In early magnetic force microscopy measurements an iron cantilever briefly magnetized by exposure to a strong magnetic field was employed. The cantilever (and sample) properties were chosen so that the force gradient due to magnetic forces would considerably outweigh the influence of the van der Waal's interaction [23]. The surface was imaged in IC mode, resulting in a map of the magnetic domains in the sample. In this case no topographic image was simultaneously recorded. These advances in magnetic imaging influenced and inspired the development of what was originally called localized charge force microscopy [24], based on the principle that if a local charge is present at the surface the Coulomb interaction between the charge and its image charge on the tip will contribute to the force gradient experienced by the cantilever. In order to separate out the topographic and electrostatic effects, a range of instrumentation configurations have been developed, which allow topographic and electrostatic images to be recorded simultaneously. Here we briefly review some common configurations.

In a basic IC mode scan, the amplitude of vibration is largely dominated by the damping effect of the contact between tip and sample. Hence, for an appropriate amplitude setpoint, the topographic data are generally assumed to be largely independent of the local electrostatic forces. (Some recent studies have questioned the accuracy of this assumption [25].) Following the recording of a topographic line scan, the tip is lifted above the surface to a fixed height. As the cantilever makes a second pass over the surface (known as the lift scan), the cantilever follows the height profile recorded in the previous scan (but with an additional constant offset), so that the tip-sample distance, and hence the van der Waal's interactions, should be kept constant. During this second scan, variations in the force gradient should be due to Coulomb interactions between the tip and any local charges [26]. Since the resonant frequency of vibration of the cantilever varies as

$$\omega = \omega_0 \sqrt{1 - \frac{1}{\kappa} \frac{dF}{dz}},$$

where dF/dz is the force gradient, this allows the local electrostatic forces to be monitored by (for a constant cantilever

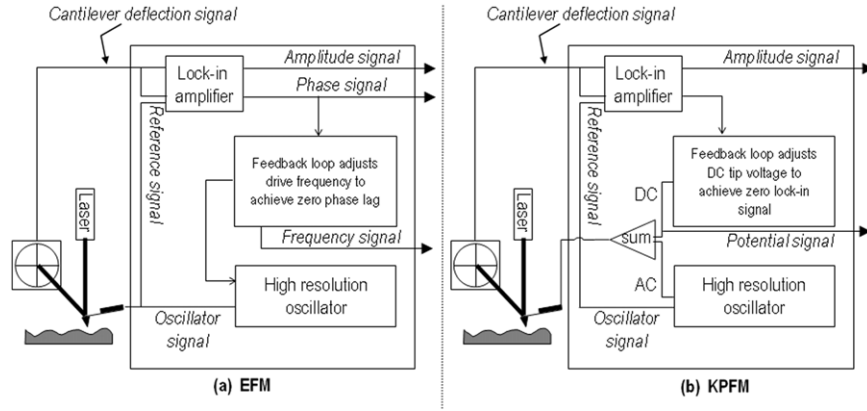


Figure 3. Schematic drawings of potential instrumental configurations for (a) EFM and (b) KPFM, illustrating the differences between them.

drive frequency) observing changes in either the amplitude or phase of the cantilever vibration. Alternatively, a feedback loop may be used to adjust the drive frequency to maintain a phase lag of zero, thus allowing the variation in the resonant frequency to be recorded. This provides a qualitative image of the local surface charge variation.

Extending this basic approach to achieve a more quantitative image involves further consideration of the force gradient acting on the tip. The tip and sample may be modelled (very simply) as a parallel plate capacitor. The energy stored in such a capacitor:

$$U = \frac{1}{2} C (\Delta V)^2,$$

where C is the local capacitance between the AFM tip and the sample and ΔV is the voltage difference between them. The resulting force on the tip, F , may then be written, in terms of the tip-sample separation, z :

$$F = -\frac{dU}{dz} = -\frac{1}{2} \frac{dC}{dz} (\Delta V)^2.$$

In quantitative variants of EFM, the potential difference applied to the tip has both a dc and an ac component. Hence ΔV may be written:

$$\Delta V = \Delta V_{dc} + V_{ac} \sin(\omega t)$$

giving a force on the tip as follows:

$$F = -\frac{1}{2} \frac{dC}{dz} \left(\Delta V_{dc}^2 + \frac{1}{2} V_{ac}^2 \right) - \frac{dC}{dz} \Delta V_{dc} V_{ac} \sin(\omega t) + \frac{1}{4} \frac{dC}{dz} V_{ac}^2 \cos(2\omega t).$$

There are three terms in this summation: a dc term (F_{dc}), an ac term with frequency ω (F_{ω}) and a second ac term with frequency 2ω ($F_{2\omega}$). F_{dc} leads to a cantilever deflection, rather than a cantilever oscillation, and can be difficult to detect [26]. However, either of the two ac terms may be used in measuring local surface charge or surface potential.

In one common variant, Kelvin probe force microscopy (KPFM—sometimes referred to as surface potential microscopy or scanning Kelvin probe microscopy), the applied

ac bias is at, or close to, the resonant frequency of the cantilever. Given that the cantilever's response at its resonant frequency is significantly stronger than its response at the second harmonic, the cantilever amplitude of vibration, A , is, to a first approximation, directly proportional to the amplitude of F_{ω} :

$$A \propto \frac{dC}{dz} \Delta V_{dc} V_{ac}.$$

KPFM data is recorded during the lift scan, with no mechanical vibration applied to the cantilever. The ac bias tends to vibrate the cantilever unless ΔV_{dc} is zero, in which case the surface potential and the applied tip potential must be equal. A is monitored, and a feedback circuit adjusts the applied dc bias to try and maintain $A = 0$. Hence, the surface potential may be monitored. Figure 3 shows schematics of the instrumentation used for EFM and for this KPFM implementation, to allow comparisons to be drawn.

Other, more sophisticated approaches eliminate the effects of the tip-sample capacitance by judicious selection of the applied dc and ac biases so that both F_{ω} and $F_{2\omega}$ may be simultaneously monitored [27]. In this case the capacitance gradient may be eliminated as follows:

$$|\Delta V_{dc}| = \frac{1}{4} V_{ac} \left| \frac{F_{\omega}}{F_{2\omega}} \right|.$$

In fact, a variety of instrumentation configurations are currently applied under the heading of EFM, extended EFM, KPFM or surface potential microscopy [26]. In all cases the basic principle remains the measurement of the force gradient due to local charges or potentials, as distinct from the force gradient due to the van der Waal's and interatomic repulsions.

2.2. Scanning capacitance microscopy

The earliest scanning capacitance microscopes were not AFM-based devices. Instead, they had more in common with stylus profilometry systems [28]. Later, scanning capacitance microscopy (SCM) based on STM [29] was implemented, and both types of microscope influenced the development of the AFM-based [30] scanning capacitance microscope. In this technique, a metal-coated tip is scanned over an oxidized

semiconductor surface in contact mode, employing the usual feedback circuit to maintain a fairly constant cantilever deflection [31]. The metal-coated tip and the oxidized semiconductor together form a metal-oxide-semiconductor (MOS) capacitor (as illustrated in figure 4). The capacitance of such a structure depends on the applied voltage: for an n-type semiconductor, when a positive bias is applied to the tip, carriers will accumulate at the semiconductor/oxide interface. In this case, the measured capacitance (the accumulation capacitance) depends solely on the properties of the oxide layer. If a negative bias is applied to the tip, carriers will be repelled from the semiconductor–oxide interface, creating a depletion layer which acts as an additional dielectric layer in series with the oxide layer, decreasing the capacitance of the system. As the applied bias slowly becomes more negative, a minority carrier inversion layer is generated at the semiconductor surface and hence the capacitance returns to its original, higher value. However, if the bias is changed quickly, there is no time for an inversion layer to develop, and the capacitance will continue to drop until the breakdown field is reached. (This is referred to as deep depletion [32].) These regimes are illustrated in figure 5(a). Capacitance–voltage (C – V) curves for p-type dopants are the mirror image of that shown in figure 5, since a positive bias will repel holes.

In SCM, a kilohertz frequency ac bias is applied to the tip to induce capacitance changes. Hence, inversion is avoided,

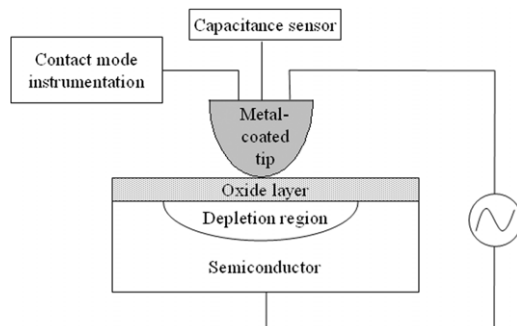


Figure 4. Simple schematic of a generic SCM illustrating the formation of a nanoscale MOS capacitor, consisting of the metal-coated tip, semiconductor oxide layer and semiconductor sample. The extent of the depletion region depends on the applied bias.

as there is too little time for minority carrier diffusion to occur, and the system operates in the deep depletion regime. The form of the C – V curve is also dependent on the carrier concentration in the sample, as illustrated schematically in figure 5(b). Material with fewer carriers depletes more easily, resulting in increases in the difference in capacitance (ΔC) between the accumulation and deep depletion regimes, and in the slope in the depletion regime. Capacitance changes are measured using an ultra-high frequency capacitance sensor. In one common SCM mode, an ac bias voltage of fixed amplitude is applied to the tip, resulting in a corresponding change in capacitance, which may be detected using a lock-in amplifier. As the tip moves from a region with a high carrier density to one with a lower carrier density, the output from the lock-in amplifier increases due to the steeper slope of the C – V curve. This output is commonly described as the dC/dV amplitude signal. It is also possible to detect whether the slope of the curve is positive or negative, hence distinguishing between n- and p-type material. The sign of the slope is given by the dC/dV phase signal [31].

The above approach is sometimes described as open-loop SCM imaging. In the alternative mode (closed-loop imaging) a feedback circuit is employed to adjust the applied ac bias in order to maintain a constant capacitance. The magnitude of the required ac bias is then used as a measure of the carrier density. A higher ac bias is required to deplete regions with higher carrier concentration sufficiently to achieve the desired capacitance change. Hence, in closed-loop mode the output signal increases with increasing carrier concentration, whereas for open-loop imaging the relevant output (the dC/dV amplitude) decreases with increasing carrier concentration.

Note that throughout this section, we have referred to the SCM as being sensitive to carrier concentrations rather than dopant concentrations. Where all the dopants are ionized, the two will be equivalent. However, for deep dopant levels, or dopants which form electrically inactive complexes with impurities, this is not the case. This might be seen as either an advantage or a disadvantage of the technique, depending on whether one's goal is electrical or compositional profiling.

2.2.1. Scanning capacitance spectroscopy. Scanning capacitance spectroscopy (SCS, also known as dC/dV

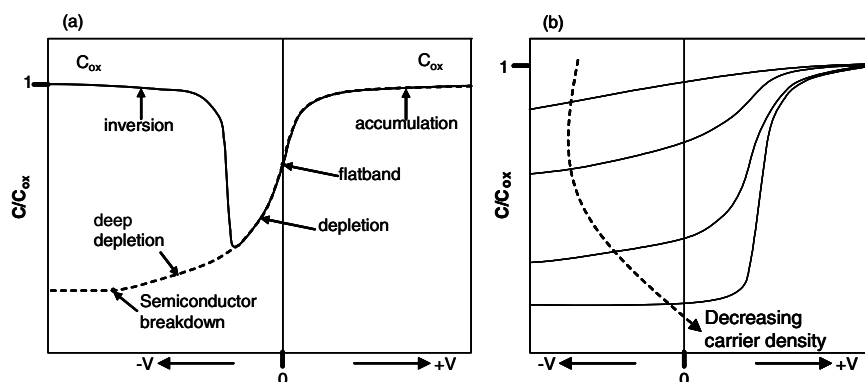


Figure 5. (a) Schematic C – V curves for an n-type semiconductor for low-frequency bias changes (solid line—*inversion*) and high frequency bias changes (dashed line—*deep depletion*). C_{ox} is the capacitance of the oxide layer at the semiconductor surface. (b) Schematic C – V curves for n-type semiconductors with different carrier densities for high frequency bias changes.

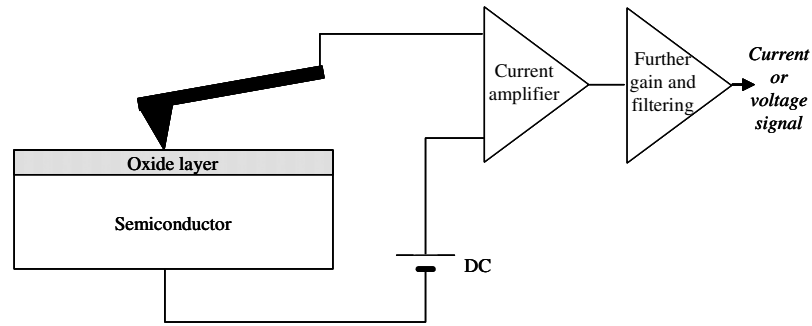


Figure 6. Schematic of a generic configuration for measurements involving tip-sample current flow. The nature of the amplifiers and the output signal depends on the particular technique used, which may be C-AFM, TUNA or SSRM.

spectroscopy) extends the SCM technique by ramping the dc bias applied to the sample at each pixel, so that a dC/dV versus V curve may be recorded [33,34]. An integration of these data yields capacitance voltage curves.

2.3. Techniques involving tip-sample current flow

Perhaps the simplest approach to measurement of electrical properties by AFM is to apply a bias to a conductive tip, and measure the resulting tip-sample current. This general approach, which is illustrated schematically in figure 6, is applied in two different techniques, which we address under the headings conductive AFM (C-AFM, section 2.3.1) and scanning spreading resistance microscopy (SSRM, section 2.3.2). Whilst conceptually rather similar, they were inspired by different pre-existing instruments, the first by the combination of AFM with scanning tunnelling microscopy and the second by the scaling down of spreading resistance profiling (SRP) to the nanometre regime.

2.3.1. Conductive AFM. An early combination of the AFM and STM arose out of a desire to interpret STM images of oxidized metal surfaces taken in air [35]. By using a biased, metal-coated cantilever to simultaneously measure the local topography, the applied force and the local current, conclusions could be drawn about the forces required to penetrate the oxide layer sufficiently to achieve stable carrier tunnelling. It was soon realized, however, that this technique had broader application to the separate measurement of topography and current in situations—such as on partially oxidized semiconductor surfaces—where the tunnelling current is not necessarily a good indicator of the surface morphology [36]. These early data were often referred to as scanning force tunnelling microscopy measurements [36], although in some cases (for example for measurements on oxide-free gold surfaces [35]) the tip-sample current flow mechanism was not actually tunnelling. However, the use of this technique became widespread for the characterization of SiO_2 gate oxide films, as discussed in more detail in section 3.3, following the early forays of Murrell *et al* [37]. In this case, the observed current is due to tunnelling through the oxide layer [37], and this technique is sometimes known as tunnelling AFM or TUNA. Instrumentally, the distinction is sometimes made between C-AFM, which employs a linear

current amplifier, with a range 2 pA–1 μA , and TUNA which has a lower noise floor (ca 40 fA) and employs a more sensitive linear current amplifier, with a range from 50 fA to 120 pA [38], although this is not generally maintained in the literature, where the two terms are used somewhat interchangeably.

2.3.2. Scanning spreading resistance microscopy. SSRM was developed from the more mature technology of SRP as a means of measuring carrier concentrations in semiconductors, principally silicon, on a sub-100 nm scale [39]. For imaging of silicon, in particular, a key difference between SSRM and TUNA is that in SSRM imaging, relatively high forces are applied (typically 15–20 μN) to penetrate any oxide layer which covers the silicon surface [40], whereas in TUNA the aim is to measure the properties of the oxide layer via the measurement of the tunnelling current through it. Since in SSRM the probe must withstand high forces to penetrate the oxide layer, doped-diamond-coated probes are often used instead of the metal-coated probes typically used in other techniques, since the metal coating is quickly damaged by imaging under these conditions.

In SSRM, if one assumes that the sample may be treated as a semi-infinite uniformly doped slab of resistivity ρ , and that it makes an Ohmic contact with a non-penetrating circular probe of radius a , then the measured resistance, R , will be dominated by the spreading resistance [41], so that

$$R = \frac{\rho}{4a}.$$

However, in reality the contact resistance between the probe and the sample may be substantial, and is dependent on the probe shape, the surface state concentration and energy distribution and the force acting on the probe. The resulting barrier resistance may be dependent on the doping density in the sample and hence on the resistivity, hence one may write [41]

$$R = \frac{\rho}{4a} + R_{\text{barrier}}(\rho).$$

This contribution of the barrier resistance results in non-linearities in the relationship between R and ρ , which has implications for the quantification of SSRM data as discussed in section 3.1.2.2.

In addition to the differences in physics between TUNA and SSRM, there is also usually a significant difference

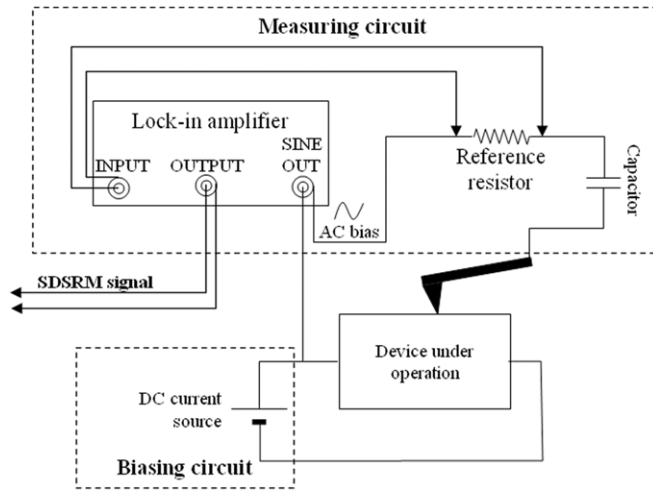


Figure 7. Schematic illustration of SDSRM instrumentation. A dc bias is applied to the device under test to simulate normal operating conditions, whereas an ac bias is used in the measurement circuit. A lock-in amplifier may be used to measure the ac current, and the output of the lock-in amplifier is then fed into the data acquisition system [43].

in instrumentation between the two: instead of the linear current amplifier employed in TUNA, SSRM employs a logarithmic amplifier with a current range of seven orders of magnitude from 10 pA up to 0.1 mA. In the context of device characterization, this enables it to measure resistance from both high- and low-doped semiconducting regions and from metallized sections without the higher currents damaging the amplifier or being recorded inaccurately.

2.3.2.1. Scanning differential spreading resistance microscopy. Scanning differential spreading resistance microscopy (SDSRM) is a recent development of the SSRM technique, which aims to provide an analogue for SSRM which may be successfully applied to actively biased devices [42]. In this case, a dc voltage is used to bias the device, whilst an ac voltage is applied between the conductive AFM tip and the cross-section of interest. A capacitor is connected in series with the tip in the measuring circuit to screen the dc bias. In order that the ac bias does not significantly perturb the operating device, a fairly low measurement bias is used (0.1–0.3 V ac) [42], and the resulting current is typically less than 1 μ A [43]. This current, which is measured using a lock-in amplifier system, is believed to have negligible effect on the device operation. Hence, using similar assumptions to those for SSRM, the changes in device resistivity under different operating conditions may be evaluated. A schematic of the SDSRM setup is shown in figure 7. It should be noted here that both SCM and KPFM can also be used to study operating devices without the addition of significant extra instrumentation, and that such studies are discussed further in section 3.2.2.

2.4. Scanning voltage microscopy

Whilst various approaches may be adapted or applied to the characterization of operating devices, the less widely known technique of scanning voltage microscopy (SVM)

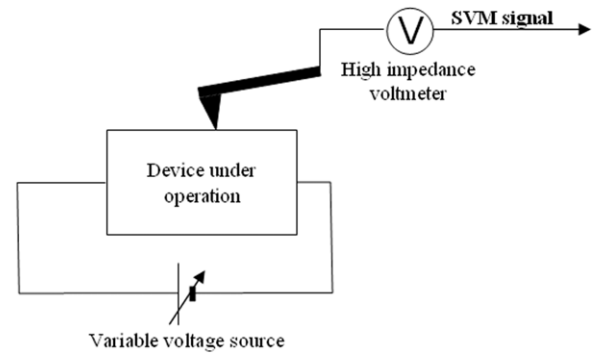


Figure 8. Schematic of the basic setup for SVM operation [44].

is unusual, in that data can only be taken from biased devices [43]. In this technique, which was originally referred to as nanopotentiometry [44], the conductive AFM tip is scanned in contact mode over the sample and is connected to a high impedance voltmeter, as illustrated schematically in figure 8. As with SSRM, it is necessary to apply a sufficiently high force to penetrate any native oxide layer on the semiconductor surface. As long as the carrier concentration under bias is not significantly different to the equilibrium carrier concentration, the voltage measured by the voltmeter is equal to the difference between the electrostatic potential under bias, and the built in electrostatic potential at equilibrium [45]. Hence for an unbiased device, no signal is observed [43]. The use of a high impedance probe is necessary, so that current flow through the tip is negligible, and the probe thus does not influence the device performance. That this may be achieved has been demonstrated by measuring device I – V (current–voltage) curves before, during and after SVM measurement to show that the device characteristics are unaffected [46].

Whilst SVM is undoubtedly an interesting technique, its application is not currently widespread. This may in part be due to the difficulty of preparing samples with very flat surfaces with minimal damage to prevent leakage current flow, which are also still electrically intact devices [46]. Additionally, the technique is inherently rather slow, since a steady state in both the sample and the measurement circuit must be reached at each point sampled before an accurate measurement can be obtained. The scan rate is then limited by the ratio of the desired pixel density to the slowest time required to reach steady state [43]. This time may be as long as 1 s, which for 2D imaging applications could be prohibitive.

2.5. Conductive AFM probes

The majority of the techniques described above require the use of a conductive probe connected to an external source. In the following discussion of such probes, we use ‘tip’ to refer to that part of the probe which interacts directly with the sample surface, whilst ‘cantilever’ designates the beam which deflects or oscillates during measurement, ‘chip’ the body on which the cantilever is mounted and ‘probe’ the entire assembly.

2.5.1. Probe selection. The simplest and cheapest options are silicon probes which have been coated in a layer of metal—usually a noble metal such as gold or platinum, to prevent tip

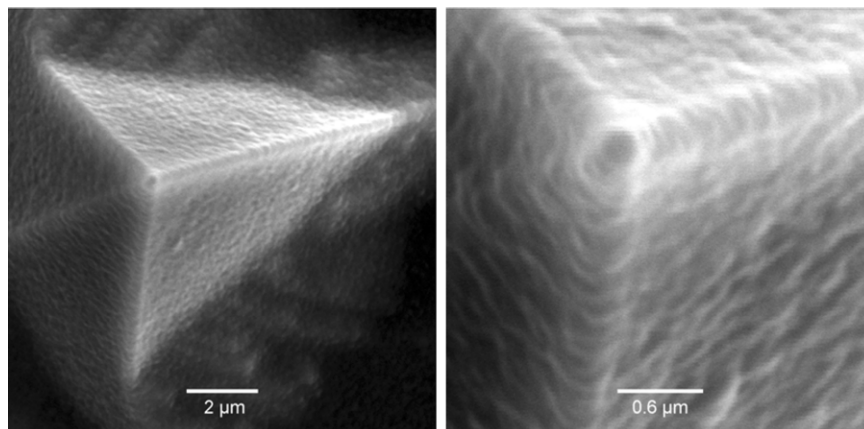


Figure 9. SEM images of a commercial doped-diamond coated silicon tip, showing the rough surface of the pyramidal tip, which results from the nanocrystalline nature of the doped-diamond film.

oxidation from affecting the measurement [47]. Such probes are used extensively for EFM, KPFM and SCM. However, in all cases the influence of stray capacitance (i.e. the capacitance between the cantilever and chip and the sample which exists in addition to the capacitance between the tip apex and the sample) may affect the accuracy of measurements. In addition, for SCM measurements, which are made in contact mode, the lateral forces experienced by the tip as it scans repeatedly across the sample can result in wear and de-adherence of the metal film [48]. Hence, alternative coating materials such as tungsten [49] and TiN [47] are being examined. An alternative approach is the fabrication of all metal tips (or all metal probes) so that wear of the tip does not result in a loss of conductivity, but merely a change in probe shape. Trenkler *et al* [50] advocate the use of Si cantilevers with all-metal pyramidal tips for SCM, whilst Bussmann and Williams [48] have prepared all-metal probes from fine platinum wire. These latter probes are sufficiently robust for repeated imaging at the micrometre scale and may also be used to achieve excellent spatial resolution in SCM. However—in common with all the novel solutions mentioned above—these probes are not yet commercially available.

Another option, in terms of avoiding tip wear in SCM, is to employ doped-diamond probes, which are widely used in SSRM. These fall into two categories: Si probes which are coated with a thin film of chemical vapour deposition (CVD) diamond or probes with all-diamond pyramidal tips. (The former are widely commercially available, although at greater cost than the metal-coated tips.) Malave *et al* [51] investigated the application of diamond cantilevers with integrated diamond tips to SCM and found that whilst Si-doped layers with dopant concentrations in the range 10^{15} – 10^{20} cm $^{-3}$, could be distinguished, the variation in contrast to doping concentration reversed at around 10^{17} cm $^{-3}$. Yabuhara *et al* [52] achieved more reliable results using diamond-coated Si probes, but still observed non-idealities in the C – V characteristics. However, since contrast reversal is also a problem in SCM when metal-coated probes are employed, and is generally related to surface preparation (see section 3.1.2.1.3), these issues may not prohibit the use of diamond tips.

The use of diamond-based probes for SSRM is well established, since, for measurements on silicon, a very

hard tip is needed to penetrate the surface oxide and allow measurement [53]. (This is not the case for all SSRM experiments; InP may be successfully imaged using metallic probes [50].) Both diamond-coated and all-diamond probes for AFM applications were initially developed by Niedermann *et al* [53]. Their initial diamond-coated probes exhibited a microstructure which persists in today's commercial probes (see figure 9); the diamond coating consists of many nanocrystallites 30–50 nm in diameter. The resulting rough probe surface was later found to cause problems when imaging samples which exhibited significant topography [54]. However, for smooth surfaces, it could lead to good resolution, since the apex of the tip may consist of the corner of a single nanocrystal providing a sharp point contact [54]. The all-diamond probes, on the other hand, were found to be rather stiff, and also often had low reflectivity [55] making optical monitoring of the cantilever deflection difficult. To overcome these problems, Hantschel *et al* [55] combined highly doped-diamond tips with silicon cantilevers. The resulting probes achieved a very broad dynamic range (approximately 5×10^{14} – 5×10^{20} cm $^{-3}$ for doping in n- and p-type silicon) [55], and an excellent spatial resolution [56] of around 5 nm. Similarly, efforts have been made to integrate all-diamond tips with metallic cantilevers [57, 58]. All-diamond tips represent a very promising solution for routine and accurate SSRM measurements, but are not yet widely commercially available.

2.5.2. Further developments in probe design and manufacture.

Various novel concepts have been applied to attempt to achieve improved performance of SPM probes for electrical characterization. Carbon nanotubes may be attached to the end of silicon tips and used to achieve considerably increased resolution in topographic measurements [59]. Similar tips may also be used in EFM and related IC mode techniques [60, 61], but additional development has been required to make nanotubes a robust and effective solution for contact-mode electrical characterization techniques. Wilson and MacPherson [62] have found that a bundle of carbon nanotubes may be attached to a silicon tip by exploiting van der Waal's forces, and then sputter-coated with metal to form a nanowire. These nanowires are then shortened to give a sharp

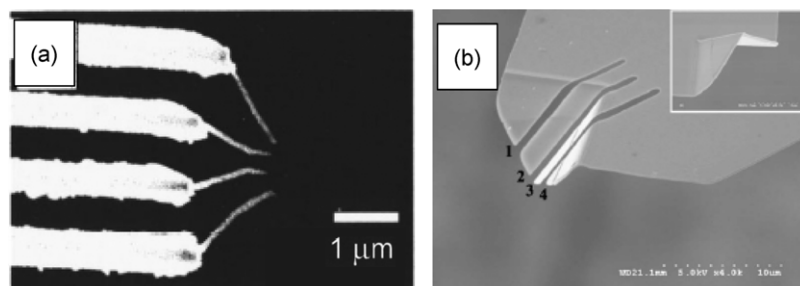


Figure 10. Design strategies for multi-probe measurements: (a) SEM image showing four closely spaced cantilevers with additional amorphous carbon nanotips. (Reprinted with permission from [65]. Copyright 2000, American Institute of Physics.) (b) SEM image of a single cantilever with three slits cut by FIB to form four probes. (Reprinted with permission from [67]. Copyright 2005, American Institute of Physics.)

robust tip, with guaranteed conductivity (whereas if a single nanotube is used it may have either semiconducting or metallic characteristics).

Attempts have also been made to reduce the problems of stray capacitances from the cantilever and chip in SCM and EFM measurements. Using either standard photo-lithography [63] or focused ion beam (FIB) nano-modification [64], researchers have attempted to reduce the conductive area of the cantilever and chip significantly: to a single metal strap connecting the tip apex to the outside world. However, these probes are prototypes and this approach has yet to be demonstrated to significantly improve the resolution of either SCM or EFM.

2.5.3. Multiple-probe techniques. Before leaving the topic of probes, it is worth highlighting the development of new probe concepts which may allow an additional measurement technique to be applied at the nanoscale. Four-point probe measurements have long been applied to the electrical characterization of bulk materials and thin films. However, in order to characterize material inhomogeneities at the micro or nanoscale the four probes must be very finely spaced. A variety of strategies has been employed to try to achieve this goal: Boggild *et al* [65] have fabricated very closely spaced cantilevers and then used a scanning electron microscope to grow additional amorphous carbon tips on each cantilever with a resulting end spacing of ca 350 nm. However, whilst they have demonstrated the efficacy of a four-point probe system based on finely spaced cantilevers [66], they have not yet produced similar data for the probe with the additional amorphous carbon nanotips.

An alternative approach, demonstrated by Ju *et al* [67] involved using a FIB to cut three slits in a gold-coated cantilever, and then etching the gold film to provide three well-separated conductive pathways. Whilst the electrode spacing achieved in this way was not as fine as that achieved by Boggild *et al* [65], it was demonstrated that the resulting probe could be used for both imaging and four-point electrical measurements. Imaging using multiple cantilever systems may prove difficult and is likely to damage the probe.

The above examples, which are illustrated in figure 10, epitomize the challenges inherent in the development of multi-electrode AFM probes. Before nanoscale four-point probe experiments become widespread, a robust, cost-effective

solution which provides reproducible results at a fine-enough scale to genuinely distinguish changes in conductivity around features of interest, such as defects, must be developed.

2.6. Topography-related artefacts

Whilst other artefacts, which are specific to certain techniques or applications, are discussed in context in later sections, the role of sample geometry is of such general relevance that it merits a separate discussion. The fact that the finite tip size has a profound effect on topographic imaging in AFM is universally acknowledged. However, the influence of topography on data taken in electrical imaging modes is equally pervasive, but this issue is frequently ignored [68].

Topographic artefacts (also described as geometric artefacts or distortions) have been most widely discussed in the context of EFM and KPFM. These electrical measurements are, as described in section 2.1, carried out during a lift scan, in which the tip-sample distance is assumed to be constant. Even ignoring any errors in this supposition, the tip-sample capacitance gradient is dependent on the surface topography; for instance it will be larger when the tip is located over a depression in the surface, since the proportion of the tip-surface area close to the surface is increased [69] (see figure 11). Efimov and Cohen [68] investigated the effect of such changes by performing KPFM on a gold film on a silicon surface. Since gold is highly conductive, they assumed this sample could be considered to be an equipotential surface, on which little or no contrast should be seen in KPFM. However, their KPFM images mirrored the sample topography (i.e. dips in the topography corresponded to bright features in the KPFM image, as shown in figure 12). They suggested a computational route to identify and remove such artefacts, whilst others have suggested the exploitation of transient phenomena [70] such as charge decay or the exploitation of the second harmonic signal in KPFM [69] as artefact reduction strategies. However, the difficulties of designing a sample in which the surface potential is absolutely known not to vary with the local topography make the assessment of all such strategies complex [69]. In addition to these considerations arising from the finite tip size, in techniques which employ a lift scan line for electrical measurements it is necessary to ensure that the topographic scan line on which the lift scan is based represents an accurate tracking of the surface and that no significant scanner or sample drift occurs (since such drift might result in the topography

underlying the lift scan line being different to that which was recorded during the topography scan).

Similar considerations apply to those electrical measurement techniques based on contact mode. The tip-sample contact area is profoundly influenced by local topography and clearly affects the capacitance measured in SCM, and the current which flows in SSRM and related techniques. For techniques in which a current must flow, the magnitude of the tip-sample contact force also influences the contact resistance, so every effort must be made to ensure optimal surface tracking with a constant tip deflection in order to avoid topography-related artefacts. A degree of scepticism is needed when features in an electrical mode scan correlate directly with features in the local topography, and where the question at hand concerns whether particular topographic features (for example grain boundaries) are associated with changes in the electrical properties, extra care must be taken in data analysis.

In SCM it should also be noted that the broad-scale sample topography far from the tip apex may alter the distance between the cantilever or the chip and the sample and thus alter

the stray capacitance, leading to artefacts in the image [71]. However, this effect is less easy to identify by comparison of the topography and SCM images.

3. Application of AFM-based electrical characterization techniques to semiconductors

3.1. Dopant profiling

Many of the techniques currently employed for the electrical characterization of semiconductors were originally developed with the aim of achieving high-resolution two-dimensional dopant profiling, in order to accurately calibrate simulations of semiconductor processing schemes [72] to improve their accuracy and aid in the design and development of nanoscale devices. Whilst SCM, SSRM and related techniques are actually sensitive to the location of *carriers* in the sample, not to the location of *dopants*, they have nonetheless been widely applied to this important technological problem. The earliest samples for dopant profiling by SCM were imaged in plan-view and consisted of broad stripes (of e.g. 8 μm in width [73]) of doped and undoped material. However, most later profiling studies have been performed in a cross-sectional geometry. Methods for the preparation of cross-sectioned samples are thus initially addressed in this section, and are followed by an account of attempts to develop electrical AFM characterization techniques for quantitative dopant profiling.

3.1.1. Cross-section sample preparation. In section 1.2.3, the possibility of cleaving samples and imaging them in cross-section to reveal sub-surface layers was discussed. This simple approach to the preparation of sample cross-sections is applied to the study of many compound semiconductors by SSRM, including InP [74], GaAs [75], SiC [76] and ZnO [77]. It has also been applied to the study of GaN heteroepitaxial layers grown on sapphire for both SSRM [21] and SCM [78] studies, but the different crystallographic orientation of layer and substrate makes it difficult to form a flat cleaved GaN surface, and large topographic steps are often present, resulting in artefacts in the electrical measurement as the tip-sample contact area changes [78]. For the SSRM profiling of Si-based staircases and devices, the samples are often polished [79]

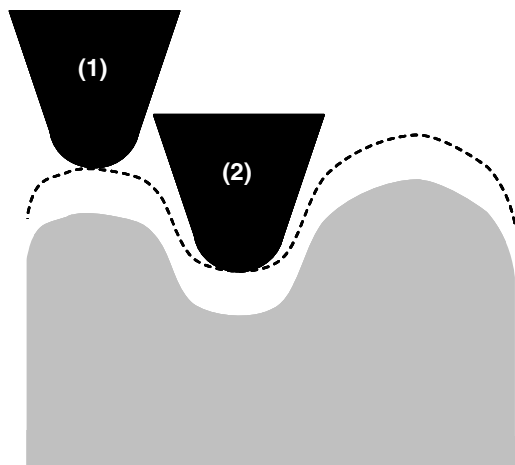


Figure 11. Schematic of the positions of a tip during a lift scan, in which it follows the dotted line which defines a constant distance above the surface. At position (2) the proportion of the tip-surface area in close proximity to the surface is greater than at position (1), increasing the tip-sample capacitance gradient.

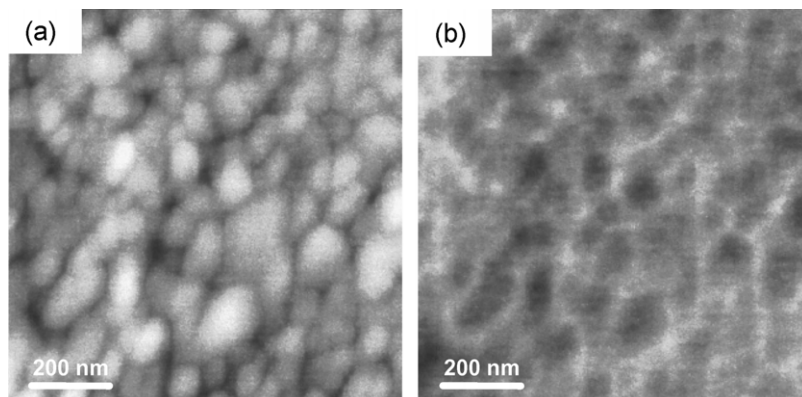


Figure 12. Simultaneously acquired (a) topographic and (b) KPFM measurements of a gold film on a silicon surface. The gold film is assumed to be an equipotential surface, but nonetheless the KPFM data show features which mirror the topography, due to the changes in the tip-sample interaction area. (Reprinted with permission from [68]. Copyright 2000, American Vacuum Society.)

following cleaving to ensure a flat surface and to help locate specific sites. Smearing of the top layer of material can be a problem in this technique, and it may be worthwhile to reduce the applied load during the final stages of polishing to prevent this [80].

Unfortunately, these straightforward sample preparation methods are sometimes found to be lacking in the context of SCM, where usual operation requires a layer of oxide between sample and tip to form a MOS capacitor. For Si samples, the native oxide formed on cleaved surfaces is too thin to prevent tunnelling current flow at the biases used during SCM measurement [81]. Hence, on cleaved samples it may be necessary to deliberately grow an oxide layer. Unfortunately, the usual temperature for thermal oxidation of Si—900 °C—is high enough to cause dopant diffusion, altering the structure under examination [82]. Huang *et al* [82] developed an alternative preparation route in which silicon dioxide was sputtered onto the cross-section surface. The sample was annealed at 500 °C in an H₂ ambient for 30 min in order to make the oxide less porous and reduce the surface state density. Later studies suggested that it was difficult to control the oxide thickness grown in this way [83]. Additionally, for device studies, preparation of site-specific samples by cleaving proved awkward.

Hence, as with SSRM, Si cross-sections for SCM are often prepared by polishing. The polishing process is similar to that used in the preparation of transmission electron microscopy samples, but in the final stage a colloidal silica solution is used which contains a hydroxide that reacts with the silicon surface during polishing and forms a thin oxide layer [83]. Initially, studies were performed exploiting this insulating layer, with no further processing carried out. However, this approach was found to have several disadvantages, including low signal-to-noise ratios (SNRs), non-uniform oxide properties along the cross-section, and unacceptably high densities of trap states in the oxide (which lead to a stretching of the transition region between accumulation and inversion in the *C*–*V* curves) [84]. Hence, various steps have been taken to improve the oxide quality, including heating under UV irradiation [84], and etching with HF and regrowth of the oxide using H₂SO₄:H₂O₂ [85]. Goghero *et al* [86] assessed the reliability of these dry and wet oxide growth techniques, and concluded that dry oxidation gives more reproducible data, but that over many scans tip changes may dominate SCM results rather than any effects of the oxide growth route.

The preparation of cross-sectional samples of other materials for SCM has been less thoroughly studied, and generally cleaving followed by native oxide growth is relied upon [87]. It should be noted that given the roughness of cleaved GaN/sapphire cross-sections mentioned above, polishing of these samples has been attempted, but resulted in a loss of almost all SCM signal, which is attributed to the formation of a non-semiconducting damaged layer [78]. The transfer of relevant sample preparation techniques from the well-studied Si system is thus not necessarily straightforward.

SCM and SSRM are by far the most common carrier profiling techniques. However, KPFM is also occasionally used in this way. Lack of a suitable cross-sectional sample

preparation technique has considerably hampered efforts to perform ultra-high vacuum KPFM on Si test samples [88], but some progress has been made for measurements of Si structures in air using samples polished as if for SCM and then etched with 1% HF just prior to imaging to provide a passive, oxide-free surface [89].

3.1.1.1. Bevelled samples. In order to improve the lateral resolution of macroscopic carrier profiling techniques such as SRP, it is possible to use polishing to produce bevelled samples—i.e. samples in which the cross-section is cut through at a very shallow angle to the layers of interest, considerably increasing the distance over which each layer intersects the surface, and hence effectively providing magnification. The same approach has been taken to improve the resolution of both SCM [90] and SSRM [91] in imaging staircase samples, and magnifications of up to 50 times have been achieved in SCM. However, as we see in section 3.1.2.4.1, phenomena such as carrier spilling complicate data interpretation from bevelled samples significantly [91].

3.1.1.2. Sample preparation using the focused ion beam microscope (FIB). Polishing and cleaving have both been used for site-specific sample preparation but, with the continuing miniaturization of devices, in order to find (for instance) specific failed devices and assess them by SPM, a more precise technique may be required. Hence, Rodriguez *et al* [92] have assessed the effectiveness of preparing samples for SCM by FIB. Their initial studies do not involve site-specific samples, but simply the FIB-based polishing of test samples. SCM imaging is not possible directly after FIB polishing—only noise is seen—but a second step involving a plasma etch has been shown to remove most if not all of the damage caused by the FIB, allowing SCM imaging to be successfully performed.

3.1.2. Si as a test system for dopant profiling. Given the technical importance of silicon and the drive towards miniaturization of Si-based devices, techniques for carrier profiling at the nanoscale have been extensively tested for this material. Hence, our discussion of the current capabilities of AFM-based techniques in carrier profiling centres on Si test samples. Our initial discussions focus on samples which do not include p–n junctions, with delineation of the metallurgical and electrical junction positions being discussed separately (section 3.1.2.4).

3.1.2.1. SCM dopant profiling.

3.1.2.1.1. Calibration and quantification. The aim of many SCM studies on doped Si has been to convert an SCM signal profile into an accurate dopant profile. For samples consisting of flat layers of doped material the resulting dopant concentrations can then be compared with secondary ion mass spectrometry (SIMS) data, in order to assess their accuracy. For Si, as long as the dopant density only varies gently over a length scale of a few Debye lengths (13 nm for a dopant concentration of 10¹⁷ cm^{−3} and 0.4 nm for a concentration

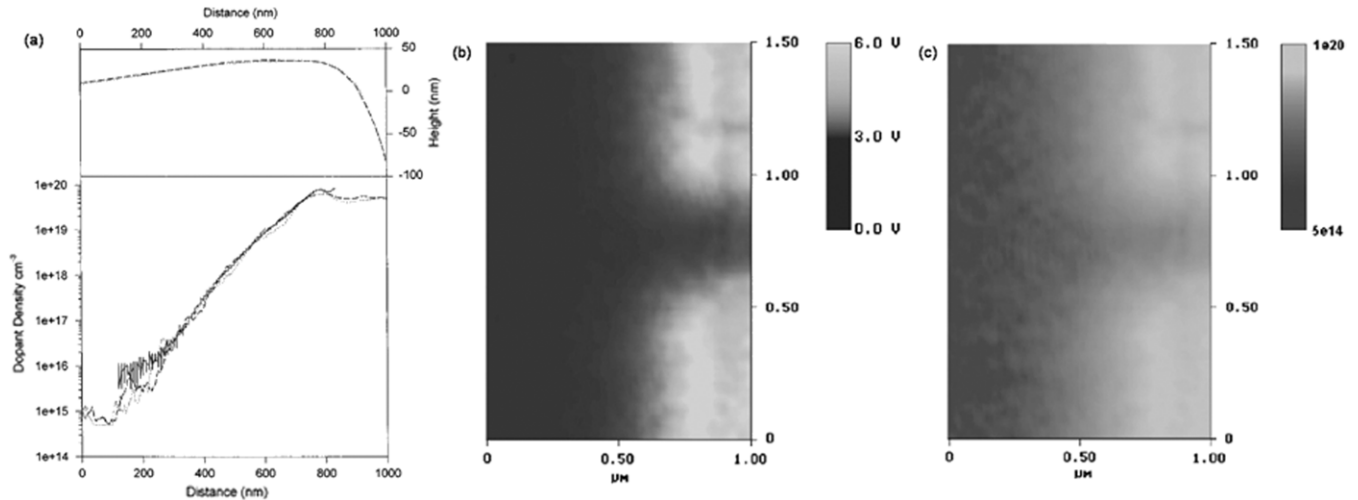


Figure 13. (a) Top: topography data from SCM measurement. Bottom: Comparison of inverted SCM data for a line scan perpendicular to the sample surface with an appropriate vertical SIMS profile, (b) Raw SCM 2D image and (c) SCM data following conversion to dopant concentrations using inversion algorithm with parameters used in (a). (Reused with permission from [72]. Copyright 1998, AVS The Science and Technology Society.)

of 10^{20} cm^{-3}), the carrier density is a reasonable measure of the activated dopant density [93]. Huang *et al* [93] made one of the first comparisons between dopant densities extracted from SCM and SIMS data. They took closed-loop SCM measurements on boron-implanted p-type Si in cross-section. In the closed-loop mode, the action of the feedback circuit should maintain a constant depletion depth in the semiconductor (see section 2.2). If the conditions are optimized to keep this depletion depth small, compared with the tip size and surface oxide thickness, Huang *et al* [93] showed that a quasi-one-dimensional (1D) model may be used to extract a dopant profile from the SCM trace, within the assumption that the dopant density and the carrier density are locally similar. To calibrate the model, the dopant density at (at least) one point in the SCM trace must be known. Additional input parameters to the model include the tip size, and the thickness and dielectric constant of the surface oxide, which are not necessarily well known in an experimental situation. Given these uncertainties, application of the model becomes somewhat an exercise in fitting the SCM data to the SIMS trace by manipulation of the free parameters. Even with this manipulation, only poor fits were obtained at dopant concentrations lower than $\sim 10^{17} \text{ cm}^{-3}$, perhaps because the Debye length becomes large in comparison with the tip size and the quasi-1D model breaks down. Kopanski *et al* [94] developed a slightly more sophisticated model of SCM, achieving a numerical solution of a nonlinear Poisson's equation in three dimensions. However, they encountered many of the problems described above, requiring the same input parameters, which are difficult to measure, and noted again the need for experimental determination of calibration factors which relate the SCM data to the model output.

Despite these problems, Huang *et al* [95] went on to develop an inversion routine based initially on their quasi-1D model which would allow the automatic extraction of dopant concentrations from SCM traces. Based on the dopant concentration at the single known data point, and on the other

input parameters, including the applied bias, a capacitance change is calculated using the quasi-1D model. Since in closed-loop mode, the capacitance change is kept constant by the feedback loop during the scan, at every other point in the SCM trace an iterative routine may be used to search for the dopant density which would give that capacitance change at the ac bias recorded for that point. Hence, the recorded biases from the closed-loop measurement may be converted into dopant concentrations. McMurray *et al* [96] went on to improve the accuracy of the 1D model and to extend it to 2D, and to develop a faster version of the inversion algorithm. Unfortunately, none of these developments really overcame the original issues with the broad range of unknown input parameters.

These difficulties can be somewhat overcome by using a combination of SIMS and SCM to achieve one of the main original aims of many SCM researchers. It is difficult to calibrate semiconductor process simulators just using normal SIMS, since the aim is to produce a 2D or 3D map of the dopant locations, and SIMS can only provide a 1D profile, given its extremely limited lateral resolution. Techniques such as NanoSIMS which seek to surmount this are not widely available. However, a 1D SIMS profile from an appropriate section of a device can be used to calibrate the SCM data in some detail. Once parameter fitting has achieved a good match between the SIMS profile and a relevant inverted 1D SCM profile, those parameters may be used to convert a 2D SCM image into a 2D dopant concentration map which can then be compared with a process simulation for the device under examination. Figure 13 shows the results achieved by McMurray *et al* [72] by applying this approach to an n-type gate-like structure.

An alternative routine for the conversion of SCM datasets to dopant concentrations has been developed by Marchiando *et al* [97], who suggested that finite element modelling (FEM) could provide a more accurate simulation of the tip-sample interaction than simplified analytical solutions. However, since FEM is slow, they developed a pre-calculated database

of C - V curves, for dopant concentrations ranging from 10^{17} to 10^{20} cm^{-3} , and oxide thicknesses ranging from 5 to 20 nm. This database could then be used to extract dopant concentrations from any dataset, within the assumption of a known tip radius (10 nm). However, the database was calculated for uniform doping, and later studies demonstrated that for dopant profiles with realistic dopant concentration gradients this leads to significant errors in both dopant profile peak magnitude and position [98]. Indeed, the issue of carrier spilling (i.e. carrier diffusion leading to a carrier concentration profile which does not match the dopant concentration profile) at sharp gradients in dopant concentration is an issue which has thus far been poorly addressed in attempts to convert 2D SCM images into dopant profiles [31].

3.1.2.1.2. Errors and reproducibility. If the inversion routines developed by Huang *et al* [95] and Marchiando *et al* [97] are to be of practical use, they need to reproducibly produce accurate dopant concentrations. In fact, a number of sources of error currently preclude this. In particular, the inversion algorithm developed by Huang *et al* [95] is extremely sensitive to noise in the original SCM data. Zavylov *et al* [99] assessed the main noise sources and divided them into two categories: noise arising from the capacitance sensor, and noise arising from the sample surface. Sensor noise can be quite easily dealt with by filtering the data appropriately after imaging is complete. Surface noise arises from local fluctuations in the oxide thickness, local contamination, and a varying density of interface states and charge traps. The most problematic noise source is the tip-induced local charging of traps in the oxide, which varies with time. It should be possible to reduce all these surface effects through improved surface preparation.

These issues of sample surface quality were highlighted by Malberti *et al* [100] as causes of non-reproducibility in SCM dopant density measurement. They also identified humidity, tip-induced oxide growth and irreproducible compensation of stray capacitance as being important issues. However, the most intractable problems limiting reproducibility were suggested to relate to the tip, rather than the surface. During scanning, change in the tip shape, wear of the metallic tip coating, and contamination of the tip by impurities can all occur. These factors may mean that even within a single image the same doping level does not give rise to the same SCM signal, resulting in discrepancies between model and simulated data.

A practical demonstration of these difficulties with reproducibility occurred when Duhayon and colleagues at several different institutions performed a 'round-robin' study, in which the same samples were assessed by SCM in different laboratories [88]. Despite valiant efforts by all the laboratories to prepare good quality surface oxide layers, there was significant variation between the experimental datasets achieved, as may be seen in figure 14, which illustrates the differences in the SCM signal versus resistivity calibration curves achieved by different labs, despite the fact that all the SCM signals have been normalized to 1 for the highest resistivity region of the sample. Figure 14 also shows that the recorded data deviate from theoretical predictions.

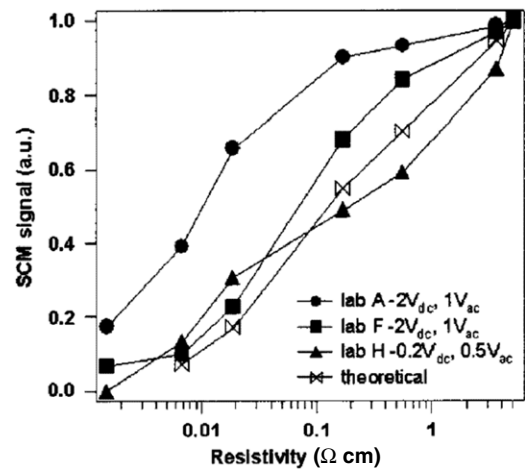


Figure 14. SCM signal versus resistivity calibration curves for the same p-type Si calibration sample measured by different labs. The SCM data are normalized to 1 for the highest resistivity region of the sample, but nonetheless show distinct differences. The dc biases used by each lab to achieve a monotonic relationship between SCM data and dopant concentration also varied and are indicated in the key. (Reprinted with permission from [88]. Copyright 2004, American Vacuum Society.)

Additionally, all the laboratories reported that an applied dc bias was required, in addition to the usual ac bias, in order to achieve a monotonic relationship between SCM data and dopant concentration. However, the required dc bias varied between laboratories; these biases are indicated in the key to figure 14. This issue of non-monotonic SCM versus dopant density characteristics under some biasing conditions is often described as contrast reversal and is discussed below.

3.1.2.1.3. Contrast reversal in SCM. An example of the contrast reversal problem can be seen in figure 15, which shows data recorded by Stephenson *et al* [101]. In their experiments, when an n-type dopant staircase (the structure of which is illustrated by the SIMS data in figure 15(a)) was imaged without an applied dc bias (figure 15(b)), the resulting open-loop SCM signal did not show a monotonic increase, for decreasing dopant concentrations. Instead, for dopant concentrations lower than 10^{17} cm^{-3} , the SCM signal decreased as the doping level decreased. By applying a dc bias of -6 V , Stephenson *et al* [101] were able to prevent this contrast reversal (figure 15(c)). However, they noted that this particular dc bias was not generally applicable to achieving monotonic signal variations; the required dc bias was dependent on the sample preparation route, the size of the tip and the environmental humidity levels. Furthermore, the dc bias required to achieve monotonic trends in imaging of p-type staircases was typically rather different to that needed for n-type material, making it impossible to simultaneously achieve a monotonic response for both dopant types in a single image.

The observed contrast reversal was attributed to the existence of trapped charges in the oxide layer of the sample [101]. Numerical simulations indicated that contrast reversal, whilst not usually expected at a dc bias of 0 V , would be seen

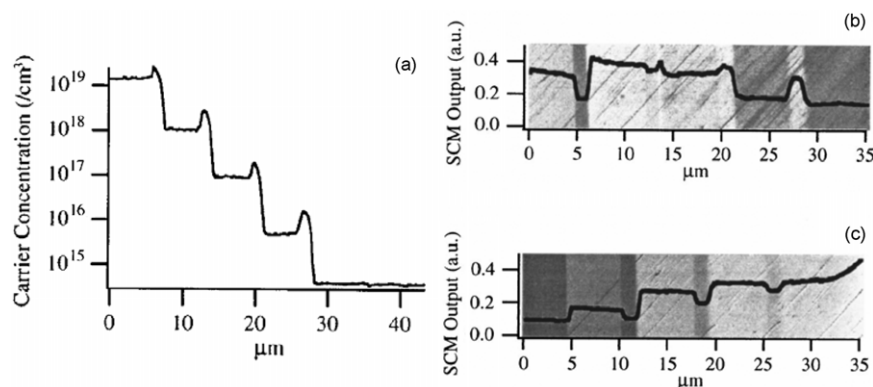


Figure 15. Measurements performed on an n-type dopant staircase in Si. (a) SIMS data, (b) SCM data, 6 V ac, 0 V dc and (c) SCM data, 6 V ac, -6 V dc. (Reprinted with permission from [101]. Copyright 1998, American Institute of Physics.)

at other dc biases. The existence of trapped charge in the oxide layer alters the effective dc operating voltage, shifting the operating condition to regions of the dC/dV versus V curve where contrast reversal is inevitable. An externally applied dc bias may be used to mitigate against this effect. Goghero *et al* [102] used a variety of sample preparation methods to prepare samples with varying densities of surface states, and showed that this shifted the dC/dV versus V curve, leading to contrast reversal as Stephenson *et al* [101] predicted.

Whilst the application of a dc bias can overcome the observed non-monotonic signal variation, the sample-, environment- and tip-dependence of the appropriate dc bias makes it difficult to apply this approach to unknown samples, in which it may not be clear whether contrast reversal is occurring. Additionally, a continuously applied dc bias may lead to image quality degradation due to damage to the native oxide migration of contaminant species towards the imaging area, or voltage-enhanced tip wear [103]. Hence, these problems with contrast reversal once again illustrate the importance of the development of reproducible sample preparation methods which reliably minimize the density of trapped charge in the oxide layer.

3.1.2.2. SSRM dopant profiling. The general approach to dopant profiling in SSRM has been based on the macroscopic technique from which it is largely derived: SRP. The usual practice in SRP is to record a calibration curve based on several homogeneous samples of known dopant concentration, and then to use the calibration curve in the assessment of samples with unknown dopant density. Initial efforts to use SSRM for dopant profiling followed this approach closely [39]. However, performing multiple measurements on different samples to generate a calibration curve is time consuming, and also risks changes to the tip shape or conductivity between measurements. Clarysse *et al* [104] developed an epitaxially grown staircase structure consisting of layers of B-doped Si with dopant concentrations from 10¹⁵ to 10²⁰ cm⁻³ on a lightly doped substrate. The layers were each 4–5 μm thick. This allowed a calibration curve to be constructed from a single SSRM scan, and direct comparison of the SSRM data with SIMS and SRP data.

With either separate calibration samples (typical data from which are illustrated in figure 16) [39] or a single

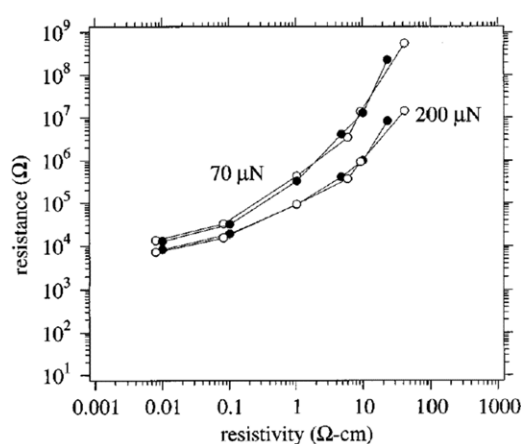


Figure 16. Typical resistance versus resistivity calibration curve for SSRM of a n-type (open circles) and p-type (closed circles) Si. The curves deviate from linearity for both high and low resistivity material. (Reprinted with permission from [39]. Copyright 1996, American Vacuum Society.)

staircase calibration sample [104], the relationship between the measured resistance and the known sample resistivity deviates from the ideal linear relationship. For highly doped Si (i.e. material with a low resistivity), materials of differing resistivity exhibit indistinguishable SSRM resistance, since the resistance of the diamond tip, or the tip-sample contact, dominates the measured value. For Si with a low doping level (i.e. material with a high resistivity) the measured resistance increases more steeply than expected with resistivity, possibly due to the formation of a non-Ohmic contact between tip and sample. The nature of the tip-sample contact at different points on a sample can be investigated using scanning spreading resistance spectroscopy (SSRS), which involves taking a current-voltage or resistance-voltage curve at each point in the image. These curves can then be used to assess the nature of the tip-sample contact and how it depends on the sample doping level [105].

Despite these deviations from the ideal resistance-resistivity relationship, the construction of experimental calibration curves provides a straightforward method for the characterization of unknown samples, whose measured resistance may be converted into a resistivity based on the calibration curve using linear interpolation as necessary. It

has been suggested that this simple approach can provide dopant profiles which are accurate to within about 20–30% for samples of practical interest [105]. However, to achieve greater accuracy, particularly for samples which contain significant variation in resistivity, it is necessary to consider the paths which the current will follow through a non-uniformly doped sample. If we consider a measurement taken on a high-resistivity region close to a boundary with a region of much lower resistivity, then we would expect that much of the current flowing from the tip might follow a path through the lower resistivity material, and this would reduce the measured resistance. In fact, the resistance value measured at any particular point is not exclusively determined by the carrier concentration at that point, but by the entire surrounding carrier profile.

This issue was explored in some depth by de Wolf *et al* [41], who used finite element simulations to assess the current paths in inhomogeneous samples, and the effect of the inhomogeneity on the measured resistance. They suggested that the actual resistance measured in SSRM should be computed thus:

$$R = CF(a, \rho) \frac{\rho}{4a} + R_{\text{barrier}}(\rho),$$

where $CF(a, \rho)$ is a correction factor, which depends on the dopant profile shape and the probe radius. They developed a method to parametrize 1D dopant profiles, and hence a look-up table was constructed which gave correction factors for a broad range of their selected dopant profile parameters and tip sizes. However, the extension of the parametrization scheme, and thereafter the database, to 2D dopant profiles is a daunting task and this approach has not been pursued. Since in practical measurements neither the tip size nor the barrier resistance (which will depend on the density of surface states [106], and hence the sample preparation method) are well known, the accurate determination of dopant densities from such a database would be challenging even if all the necessary analytical and computational challenges were overcome. Hence, the use of experimental calibration curves remains widespread in the application of SSRM, although the shortcomings of this method, particularly in samples with steep dopant gradients, should be considered when it is applied.

3.1.2.3. A comparison of key techniques. In the above section, SCM and SSRM dopant profiling have been discussed in some detail. KPFM has also occasionally been applied to this problem, but (as mentioned in section 3.1.1) problems with sample preparation initially made recording data in air challenging [88]. More recently [89], some success has been achieved with KPFM, but the dopant profiles produced were less accurate than those achieved on the same samples using SCM.

Whilst SSRM and SCM have both been used to greater effect than KPFM, cross-sectional surface preparation also has an enormous influence on the data recorded using these techniques. The influence of surface states due to imperfect surface preparation influences both techniques most strongly for low doping concentrations [88]. Additionally,

the application of both techniques to dopant (rather than carrier) concentration profiling is marred by carrier spilling, particularly when steep dopant concentration gradients exist. This problem has been assessed mathematically for the SSRM case (de Wolf *et al* 1998 [41]) but, for dopant profiles without p–n junctions, this has been less thoroughly addressed for SCM. This is surprising in the context of the extensive modelling and data inversion efforts which have been carried out in the SCM field. For both SCM and SSRM, the available models require the input of unknown parameters such as the size of the tip or the density of surface states, and hence the approach used widely in SSRM of comparing unknown samples with calibration curves is perhaps advisable for both techniques. As a caveat to this recommendation, the possibility of tip change between the measurement of a calibration curve and the measurement of an unknown sample should always be kept in mind. Lastly, experience and anecdotal evidence suggest that SSRM is more difficult to operate and useful images can be more quickly and reliably achieved using SCM. This may be born out by the relatively higher number of publications addressing dopant profiling in both standard samples and device structures using SCM.

3.1.2.4. p–n junction delineation. In considering the application of AFM-based techniques to the delineation of the position of p–n junctions in semiconductor materials, we must first clarify the definition of the p–n junction. First, we may consider the *metallurgical* junction (MJ), which is located where the chemical donor and acceptor densities are equal. Delineation of the MJ is linked to attempts to find a dopant concentration profile for the semiconductor across the junction. On the other hand, the *electrical* junction (EJ) is located where the concentrations of electrons and holes are equal. Delineation of the electrical junction is connected, strictly, with *carrier* rather than *dopant* profiling. Within this context, we must remember that techniques such as SCM and SSRM provide a direct measure of carrier rather than dopant densities. However, with SCM in particular, efforts have been made to elucidate both carrier and dopant profiles in the vicinity of p–n junctions.

In SCM, the position of the p–n junction is most easily seen in the dC/dV phase data, since the n-type and p-type material will exhibit opposite slopes of the C – V curve, and hence will give signals out of phase with one another by 180° . However, SCM phase imaging of p–n junction structures revealed that the position of the junction depended on the dc bias applied to the tip [107]. This effect may be explained if we consider the effect of a biased tip on the carrier distribution in the semiconductor. If the tip is in contact with the p–n junction's depletion region, and a negative bias is applied to it, then holes will be attracted towards the tip from the nearby p-type material. This will deform the carrier distribution inside the depletion region and shift the position of the EJ towards the n-type side. (Similarly, a positive tip bias will result in a shift of the EJ towards the p-type side [108].) If we also consider the possibility that surface charge traps may lead to an effective dc offset even when no dc bias is applied to the tip, then the reliable delineation of the EJ position from a single SCM phase image becomes problematic.

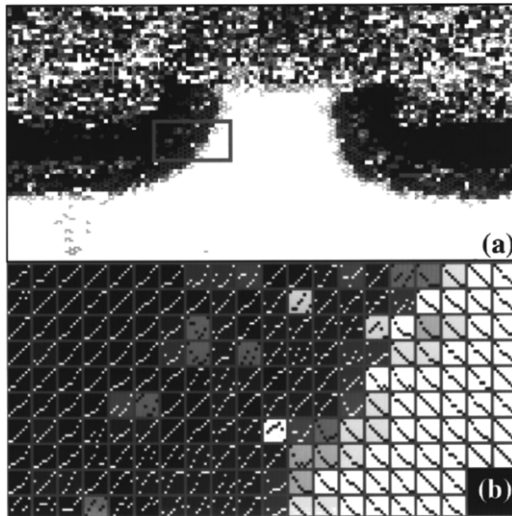


Figure 17. Illustration of SCS methods for p-n junction visualization. In (a) the pixel colour is given by the voltage value at the lowest point on the $C-V$ curve (p-type gives white and n-type black). (b) illustrates the relevant $C-V$ curves, pixel by pixel, for the box highlighted in (a). (Reprinted with permission from [107]. Copyright 1998, American Institute of Physics.)

To overcome these problems, Edwards *et al* [107] explored the application of SCS to p-n junction delineation. They suggested that when the SCM tip was over the EJ, the $C-V$ curve should exhibit a minimum, whilst away from the junction, the curve should not exhibit a minimum, but should be similar to the curves shown in figure 5(b), with the sign of the gradient being dependent on the carrier type. When the tip is within one minority carrier diffusion length of the junction, the majority carriers from either side of the junction are able to travel to the inversion region beneath the tip. Hence, electrons and holes accumulate in turn beneath the tip as the tip bias sweeps from negative to positive, giving a curve similar to a low-frequency $C-V$ curve (such as the curve in figure 5(a) which displays both accumulation and inversion). Edwards *et al* [107] demonstrated this effect by taking SCS images of p-n junctions, with a $C-V$ curve taken every 15 nm. At the junction position the curve demonstrated a clear minimum, and the junction position could be identified within ± 30 nm. An example of the images resulting from this approach is shown in figure 17. Modelling of the carrier densities under the tip at the p-n junction by O'Malley *et al* [109] confirmed the qualitative picture presented by Edwards *et al* [107] and also suggested that whilst no single dc bias would provide optimal imaging for a possible structures, imaging at mid-gap would give the best approximation to the junction position.

However, this approach using SCS only gives information on the position of the EJ, not the MJ. For symmetric step junctions (i.e. with an abrupt change from p- to n-type doping and with equal amounts of each type of dopant) the EJ and MJ position should be identical if the probe voltage does not perturb the junction position, and using an appropriate dc bias, the SCM data can provide information on the MJ position [110]. However, for asymmetric junctions (with higher doping levels on one side of the junction than the other) and for implanted junctions (where for an n-type implant into a p-type

substrate, the p-doping level is constant and the n-doping level varies smoothly, not in a step-like fashion), the MJ and the EJ do not coincide. Zavylov *et al* [111] examined highly asymmetric n+-p implanted samples, where the separation between the MJ and EJ is greater than the tip radius. In the n-type material away from the depletion region, the inversion routines developed by McMurray *et al* [96] for samples with only one dopant type may be applied to calculate an n-type dopant profile from the carrier profile. These routines fail to produce accurate data within the depletion region where the assumed relationships between carrier and dopant density no longer apply. However, if the MJ is far from the EJ and the doping density of the p-type substrate is known, then the MJ may be identified as being the point where the dopant density of the n-type implant (extracted from the SCM data) drops to the doping level of the p-type substrate. Whilst this approach produces credible data for some highly asymmetric junctions, attempts to apply the same methodology to shallow junctions produces dopant profiles which deviate significantly from control measurements taken by SIMS [111]. Additionally, this approach is only viable for highly asymmetric junctions and cannot be considered generally applicable.

In section 3.1.2.1.3, we noted that to avoid contrast reversal in SCM imaging an appropriate dc bias should be applied, and that this dc bias would not be the same for n- and p-type material. Hence, dopant profiling of samples containing p-n junctions is fraught with problems due to the influence of surface states. Additionally, both theoretical [112] and experimental [113] studies have suggested that high densities of surface states can increase the apparent width of the depletion region and decrease the peak dC/dV amplitude observed. These issues once again highlight the importance of reproducible surface preparation. Another source of poor reproducibility in SCM junction measurements is the amount of light incident on the sample from the laser which is used to monitor the tip height. If the laser wavelength is greater than the bandgap of the semiconductor under examination, light will be absorbed and extra carriers will be generated [114]. This will affect measurement of the junction more than the rest of the sample, since in the depletion region the carrier density is low, and proportionally the extra carriers will thus have a bigger impact. The photo-generated carriers tend to broaden the measured depletion region width and to decrease the peak dC/dV amplitude observed [113]. Hence, Yang *et al* [113] have suggested a mode of SCM measurement in which the laser is used during topography measurement but is switched off using SCM data collection.

For SSRM, as for SCM, the junction position (seen in the SSRM case as a peak in the resistance profile) has been seen to vary with applied bias used during imaging [115]. This has led to the suggestion [115] that SSRS should be used for junction imaging, just as SCS was used in the SCM case. Overall, less effort has been expended on junction imaging by SSRM, but (rather recently) Eyben *et al* [116] have achieved some encouraging results using full-diamond tips, suggesting that it may be possible to identify the junction position to within about 1 nm. However, this work does not consider possibility of bias induced junction shifts. Other sources of error noted

by Eyben *et al* [116] include surface roughness and smearing of the material due to the high forces used in SSRM of silicon. Additionally, photo-perturbation of the carrier density may be relevant in SSRM as it is in SCM, and certainly laser light and other light sources have been shown to influence those few p–n junction measurements which have been performed by KPFM [117].

Overall, the difficulties of interpreting data from p–n junction samples mean that extracting absolute values for either carrier or dopant densities remains challenging. Nonetheless, comparison of junction samples for which the cross-sections are prepared in the same way and imaged under similar conditions may provide insights into how different device processing or annealing schedules affect the dopant distribution, and this approach has been applied reasonably successfully in both SCM [118] and SSRM [116] studies.

3.1.2.4.1. p–n junction samples measured in on-bevel configuration. Samples polished to form a shallow bevel are used extensively in SRP to provide magnification, and it is thus perhaps natural that they have been widely investigated for use with SSRM. Many of these studies also address SCM. When a p–n junction is imaged in on-bevel configuration in SRP, carrier spilling is known to effect the junction position, leading to differences between the junction position determined by SIMS and that determined by SRP. Two contributions to the carrier spilling effect have been identified [119]: (a) the zero-field carrier spilling which results from carrier redistribution following the removal of material during the bevelling process and (b) the pressure-induced carrier spilling which occurs in SRP when high pressures are applied to the surface by the probe, leading to a phase-change to beta-tin phase silicon under the probe [120]. Whilst it was initially assumed [121] that this understanding of carrier spilling could be extended to SCM and SSRM, this was not borne out by later studies. In SCM studies, we should not see pressure-induced carrier spilling, since the forces involved are fairly small. Surprisingly, when comparing the junction position measured by SCM and that measured by SRP, similar values have often been found [120]. Clarysse *et al* [120] suggested that surface states lead to additional carrier spilling, and showed that SCM on bevelled samples was particularly sensitive to the surface preparation method used and hence to the density of surface states. However, their simulations of SSRM measurements of on-bevel junctions suggested that surface states also needed to be taken into account in order to fully reproduce SSRM results. Whilst on-bevel junction measurements have a significant advantage in that, following demagnification, any bias induced EJ shift becomes negligible [119], the complexities of quantifying the carrier spilling effect in the bevel geometry may mean that simple cross-sectional measurements are still more accurate.

3.1.3. Carrier profiling in compound semiconductors. Since much of the physics of the tip–sample interaction described above for dopant or carrier profiling in silicon is equally applicable to other semiconductors, we do not attempt an exhaustive review of the current research in this area of compound semiconductors, but merely highlight key

similarities and differences which arise when comparing these materials to Si. For example, in studies of 6H–SiC by SCM [122], the finite element method has been used to produce a database of C – V curves which can then be employed in the conversion of SCM data to dopant profiles, following the approach suggested by Marchiando *et al* [97] for Si. As with Si, the curve database only addresses uniformly doped samples, and this may account for the deviation of the SCM dopant profile from the SIMS profile in regions where the dopant concentration varies steeply. Other SCM studies of SiC, however, have highlighted issues which are yet to arise in studies of Si. SiC samples are usually doped by implantation, and damage can arise from this process as the accelerated ions collide with atoms in the target material and displace them from their original lattice sites. Annealing is required after implantation to reduce the damage. In studies of SiC samples implanted with Si (which does not produce a doping effect) Giannazzo *et al* [123] showed that in SCM imaging contrast is observed in the implanted regions, despite the lack of doping variation, and attribute this to the formation of damage-related deep states in the SiC bandgap, which are known to affect macroscopic C – V measurements. Hence, care should be taken in analysing implanted and annealed samples with SCM, since residual damage may alter the SCM signal.

SiC has also been assessed using SSRM (4H–SiC in this case), and for p-type material the measured resistance correlates well with the dopant distribution [124]. However, for n-type material a higher resistance is observed than for p-type material with the same doping concentration, despite the fact that the n-type dopant has a lower ionization energy, and the electron mobility is about 10 times higher than the hole mobility in this material. Osterman *et al* [124] suggest that this is due to the use of a p-type doped diamond tip, and the formation of a p–n junction between tip and sample. However, in other compound semiconductors (such as GaAs and InP) [125] the tip–sample interaction has been successfully modelled by treating the tip as metallic, rather than semiconducting, suggesting that further exploration of the nature of the tip–sample contact in SiC is required. Osterman *et al* [124] have, however, highlighted one interesting issue which does not appear to have been assessed in other materials systems: the possibility that, due to the flow of currents during SSRM measurement, localized resistive heating may increase the fraction of ionized dopants. They conclude that for SiC, this effect is only significant for highly doped materials, imaged at high biases. For other materials, this question has yet to be properly investigated.

For SSRM imaging of GaAs [125] and InP [126], higher tip–sample biases must be applied than are usually used for Si (1–5 V as opposed to ~ 100 mV). Additionally, the measured resistance is dependent on the polarity of the applied bias. Both these phenomena may be accounted for by considering the tip–sample contact, which forms a nanoscale Schottky diode, due to the pinning of the Fermi level at the middle of the bandgap by surface states [127]. Current transport across the Schottky barrier was modelled in detail by Lu *et al* [125] who showed that the contact barrier-lowering mechanisms under forward bias and the current transport mechanisms under reverse bias

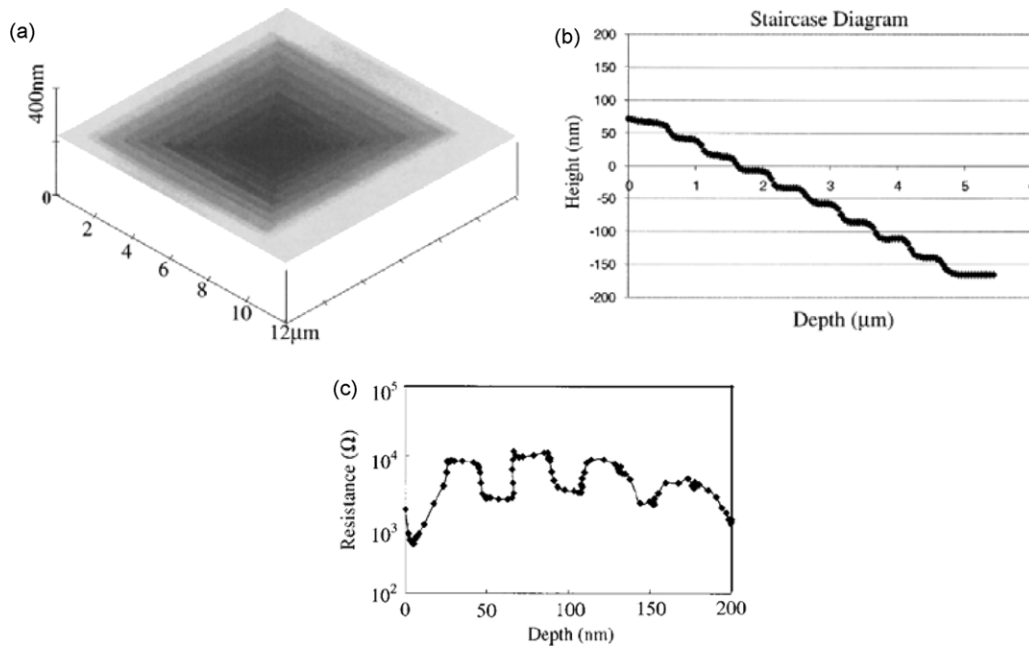


Figure 18. Example of three-dimensional carrier profiling of InP: (a) a stepped pit in the surface of an InP sample, produced by successive scans with a diamond-coated probe. (b) A depth profile of the stepped pit, illustrating control of the depth at which each successive scan is taken. (c) An SSRM depth profile. The top surface of the sample corresponds to the left-hand side of the profile. (Reprinted with permission from [128]. Copyright 2002, American Institute of Physics.)

depended on the doping level in the material, resulting in a complex relationship between measured resistance and doping levels, and necessitating the use of calibration samples for data interpretation.

SSRM imaging of InP also differs from Si in the magnitude of the contact forces used. Whilst measurements on Si require contact forces of around 15–20 μN in order to penetrate the surface oxide layer, forces at least an order of magnitude lower are required to achieve good results on InP, allowing the use of metallic or metal-coated probes rather than diamond-coated probes [126]. Even with these lower contact forces, the InP surface is easily damaged. Xu *et al* [128] exploited this damage by imaging InP samples in plan-view rather than cross-section using diamond-coated tips. With each scan, they removed a layer of material, by scratching it away from the surface, so that the next scan was taken at a greater depth into the sample. Then, using the SSRM data taken at different depths, they were able to build up a three-dimensional picture of the sample's resistivity. In addition to the possibility of 3D imaging, this technique provides good resolution in the near-surface region which can be difficult to image in cross-section. The process is illustrated in figure 18. Imaging of samples whose doping did not change with depth, indicated that 10 or more scans could be taken without significant deviation from the expected profile. However, after 20 scans the deviation became significant. Nonetheless, this is an imaginative approach to three-dimensional carrier profiling, although sadly it only seems applicable to rather soft materials like InP.

Following the development of GaN light emitters, there has been significant activity in the application of AFM-based electrical techniques to these materials. Systematic studies of dopant profiling have only recently begun, however, and are mainly focused on SCM. Recent studies have employed

calibration structures for quantification, and have taken the unusual step of growing the calibration structure directly onto the surface of the unknown sample under investigation and then imaging the resulting sample in cross-section, allowing simultaneous imaging of the calibration stack and the unknown regions [129]. This has been necessary due to two specific issues: (a) the observation that if the tip is retracted from and re-engaged with the surface of the same GaN sample following imaging, the SCM signal amplitude in the subsequent image can differ significantly from that in the previous image, necessitating simultaneous imaging of calibration structure and unknown sample, and (b) the difficulties of achieving a low-noise SCM signal following polishing of GaN samples [78], so that the technique of sandwiching two samples together, and then polishing them to achieve a level cross-section prior to imaging both simultaneously is not easily applicable here.

Studies on the nitrides have also highlighted another issue pertinent to the imaging of compound semiconductors: the possibility of imaging samples or devices where not only the doping concentration but also the composition may change. Fraser *et al* [21] have shown that for samples containing $\text{Al}_x\text{Ga}_{1-x}\text{N}$ layers with varying Al contents and doping levels, the measured resistance in SSRM appears to correlate with the Al content, rather than the doping concentration. However, the quantification of either doping levels or compositions in samples where neither is precisely known is an extremely complex problem and thus far such data may only be interpreted qualitatively.

3.2. Assessment of electronic and optoelectronic devices

3.2.1. Device characterization. A wide variety of semiconductor devices have been characterized using

electrical SPM techniques. Many of the challenges involved in device imaging are similar to those encountered in the basic profiling studies described above, although unfortunately not all authors take these issues into account, which may lead to over-confident interpretation of data. Nonetheless, careful application of the SCM and SSRM techniques in particular has lead to some interesting insights on device structures.

In preparing samples of complete devices, adaptations to the usual sample preparation techniques may be required. Since these devices may contain layers of metals, oxides, silicides or other materials, in addition to the semiconductor, care must be taken that differential polishing or etching rates do not lead to unacceptably large topographic steps. For example, in studies of silicon-on-insulator (SOI) transistors, the final chemo-mechanical polishing step with colloidal silica solution often used on silicon samples may lead to differential polishing of the semiconducting and buried oxide layer. Hence, Alvarez *et al* [130] recommended simple mechanical polishing in this case. Additionally, they used FIB milling to open up trenches at the end of the devices of interest, which were then filled with tungsten as a means of making electrical contact to the device [130].

The varying materials found within complete devices may also lead to difficulties in data interpretation when imaging with SCM, since this technique does not return a signal for either insulating or metallic regions, making it difficult to distinguish between them [131]. Semiconductors with very high or very low doping levels may also present a problem. The logarithmic current amplifiers used in SSRM allow resistances to be recorded from semiconductors with a wide range of dopant concentrations and for metallic regions, but in this case the large forces applied may lead to the smearing of metallic regions across the sample, broadening their apparent width [132].

Given the complexities of achieving accurate absolute quantification of individual samples, one sensible approach to understanding devices using AFM-based techniques is to make comparisons between samples prepared in the same way, under the same imaging conditions and using the same tips, to look for differences in the resulting data. Bowallius *et al* [133] took this approach a step further in their studies of InP buried heterostructure lasers. The fabrication of such devices involves overgrowth of a lithographically formed mesa structure, and the result is that p–n junctions are grown on facets with different crystallographic orientations, which may have different rates of dopant incorporation. Single SCM images of a device contain information about all orientations of junction within the device, allowing straightforward comparisons to be made, with no concerns about changes in the state of the tip. Using this approach, Bowallius *et al* [133] were able to show that lasers grown by liquid phase epitaxy (LPE) showed more dependence of the dopant concentration on facet orientation than those grown by metal–organic vapour phase epitaxy (MOVPE).

The most frequently applied method to achieve more quantitative assessment of devices is the use of calibration curves based on well-known samples. In their round-robin study Duhayon *et al* [88] assessed the reproducibility of this approach, and found that two separate laboratories achieved

similar results in quantifying the dopant concentration in a bipolar junction transistor by SSRM. However, as devices of smaller and smaller dimension are studied, quantification using calibration standards becomes more difficult. Eyben *et al* [134] found that for 90 nm CMOS technology a comparison of dopant densities found by process simulation software and those found by SSRM reveals that the data from two methods diverge when the dopant profiles vary sharply. This may be because use of larger-scale calibration structures in quantification fails to take into account the available current paths through the locally varying carrier environment. More encouragingly, the same study showed that, if full diamond tips are used, the dimensions indicated by the SSRM data usually agree with those from the process simulator to within ± 3 nm.

Whilst, by using calibration structures and by making comparisons, some effective basic characterization of devices may be performed, another increasingly attractive opportunity is the imaging of actively biased devices, to provide insight into their operation, and by extension, to the imaging of failed devices, to understand why they no longer operate properly. These two applications are discussed in more detail below.

3.2.2. Imaging devices in operation. In order to image actively biased devices, it is necessary to use the correct instrumentation configuration. Often for SCM and SSRM, the sample is connected to a broad area contact and dc or ac biases between tip and sample are applied via this contact. However, for device operation, the usual connections to the device must be maintained, and tip–sample potential differences should thus be applied by biasing the tip, not the sample. This requires modification of some commercial systems [135]. Additionally, changes to the sample preparation method may be necessary. It is important to ensure that leakage currents via surface conduction paths do not significantly alter the device operation, and the surface preparation must thus be optimized to ensure that the device characteristics are substantially unchanged in the cross-sectioned sample [135, 136].

Due to the difficulty of forming a cross-section on a real device at the point of interest, and maintaining appropriate electrical connections to that device, many initial device studies were performed on specially fabricated test devices [135, 136]. Early SCM studies performed on actively biased devices used specially designed MOSFET structures to allow visualization of the changes in carrier concentration involved in the formation of a conducting channel between source and drain with increasing gate bias [137]. Quite recently, however, Kimura *et al* [138] have been able to prepare cross-sections of real, commercially relevant devices which could be actively biased during imaging. Their strategy was an extension of that employed by Alvarez *et al* [130] for SSRM of devices: they made electrical contact to the device of interest by etching contact holes by FIB and depositing tungsten vias into these holes using FIB-CVD, which could then be connected to tungsten bond pads. As with the test devices, channel formation could be visualized, as illustrated in figure 19. Good agreement was seen between the voltage at which the channel appears to penetrate from source to drain in the SCM images, and the turn-on voltage of the device observed in the

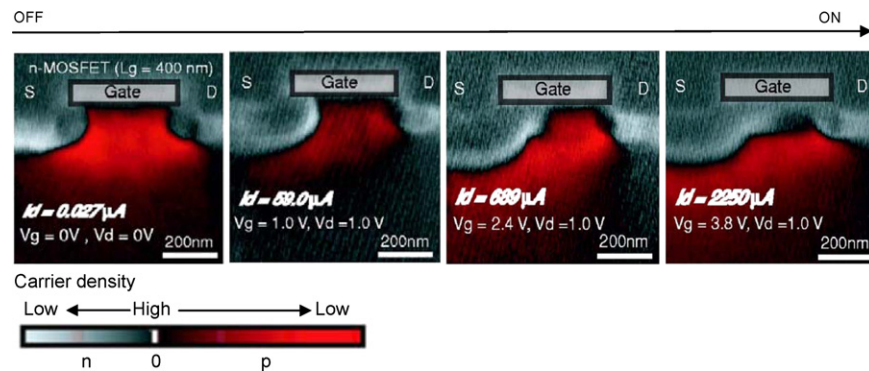


Figure 19. Visualization of channel formation in an actively biased, cross-sectioned n-MOSFET. S—source, D—drain, I_d —drain current, V_d —drain voltage, V_g —gate voltage. As the gate voltage increases the n-channel extends across the region below the gate, so that for $V_g = 3.8$ V, $V_d = 1.0$ V, the device switches on and a greatly increased drain current flows. (Reused with permission from [138] Copyright 2006, AVS The Science and Technology Society.)

macroscopic device characteristic. However, as with other MOSFET studies by SCM, data interpretation is currently largely qualitative.

Similar qualitative analysis of operating MOSFETs has been performed by SVM [44]. The SVM technique has been more extensively developed, however, for studies of InP-based devices. Initially, a simple biased p–n junction was examined as a proof-of-concept and good agreement was obtained between the variation of the observed depletion width of junction with applied bias and the results of semi-classical theoretical calculations [139]. Thereafter, quantification of internal potential distributions in real InP-based laser diode structures proved more challenging due to uncertainties in the tip-sample contact potential and the surface potentials of differently doped semiconductor regions [140]. However, useful insights into device operation have been achieved. For example, lateral current spreading in ridge lasers has been quantified, with the results being in good agreement with theoretical predictions [43].

The signal in SVM is dependent on both the local electrostatic potential and the local carrier density. To help separate out these two effects when imaging operating devices SDSRM may be used to extract information on carrier densities. Whilst application of this technique is in its infancy, it has been successfully used to visualize carrier accumulation in the active (quantum well) region of an InP laser diode, and also carrier escape from that region [43]. The observed effects agree qualitatively with theoretical expectations, but further study is needed before these data can be used to fully quantify changes within such devices. Both SVM and SDSRM have only been applied extensively to InP-based samples, and may not be easily applicable to other materials systems. For instance, Zavylov *et al* [136] suggest that the large forces required to penetrate the surface oxide in SVM of Si-based samples may lead to surface damage and the evolution of increased leakage currents during imaging (although Trenkler *et al* [44] did not observe this effect in their studies of Si-based MOSFETs). The issue does not arise in imaging of InP-based samples where much lower forces may be applied.

3.2.3. Failure and reliability analysis. In order to analyse failed devices, both cross-sectional and plan-view measurements may be taken, usually by SCM. Cross-sectional samples are prepared using established methods, but—where completed devices are to be analysed—plan-view samples require the removal of non-semiconducting layers. For silicon-based devices, metallic and dielectric layers are etched away using HF and polysilicon lines may be peeled off using adhesive tape [141]. Most analyses performed in both plan-view and cross-section to date have involved comparisons between working and failed devices either in terms of the spatial extent of a dopant implant [142] or the dopant density in an implanted area [141]. Such qualitative comparisons can be quite informative, and can help identify problems within the device processing procedure without the necessity of complex quantification procedures [141]. Many analyses simply compare one failed and one working device. However, more thorough studies use images of multiple working devices taken under identical conditions to establish a normal range for the parameters of interest, so that it is clear when the processing of a failed device has stepped outside the usual tolerances [141]. In addition to processing-related failures, damage caused to a MOSFET by electrostatic discharge (ESD) has also been examined by SCM [143]. The area where the ESD damage occurred was first identified by scanning electron microscopy (SEM), and a cross-section taken at the appropriate point. The spatial extent of the n-type implant in the damaged region was shown to be much greater in the damaged region than in the rest of the device.

Although Nakakura *et al* [135] have briefly commented on analysing actively biased failed devices by SCM, to provide a deeper insight into failure mechanisms (suggesting that carrier concentrations in electrically damaged devices may be seen to change with applied bias, but the nature of the observed changes differ from those in working devices), this approach has not thus far been extensively applied. The effectiveness of SVM in analysing actively biased, failed InP-based lasers has, however, been demonstrated by Ban *et al* [144] who identified a current leakage path which occurs only at high voltages in such structures and which prevents successful high power operation. This example suggests that SPM-based techniques

may become a useful tool for identifying mechanisms of device failure, and hence aid in improved device design to avoid such faults.

In this section, we have considered failures within the semiconducting parts of the device. However, SPM can also be used to analyse degradation and breakdown of the dielectric films which are an integral part of many devices. These issues are considered separately—in section 3.3.3.

3.3. Assessment of dielectric films on semiconductor substrates

In MOSFETs, in addition to nanoscale doping control, the reliability and long-term stability of the gate oxide is of paramount importance, since oxide degradation or breakdown leads to device failure [145]. Scanning probe microscopy provides a means to assess this oxide at the nanoscale, and the development of this technique is also relevant to other devices which utilize dielectric films grown on semiconductor surfaces, from random access memory cells [146] to potential spintronic devices [147].

3.3.1. Assessment of thickness and thickness homogeneity. Sub-nanometre variations in oxide thickness can severely impact the threshold voltage of MOS devices and lead to locally raised stress. As devices shrink, gate oxides become ever thinner, increasing the severity of this problem. Hence, methods for the measurement of oxide thickness at a local level by scanning probe microscopy are being developed. Whilst SCM data is sensitive to oxide thickness [148], and some effort has recently been made to quantify thicknesses using this technique [149], this area has been most extensively explored using C-AFM and TUNA.

For oxide thicknesses in excess of about 5 nm, current flow through the oxide occurs by Fowler–Nordheim tunnelling (FNT) [150]—electrons tunnel from conduction band of the semiconductor into that of the oxide through part of the potential barrier at the semiconductor–oxide interface. Olbrich *et al* [145] recorded current–voltage (I – V) curves using TUNA for oxides of varying thickness and, as shown in figure 20, fitted these experimental curves to the FNT equation with the effective area of the tip and the oxide thickness as free parameters. The fitted values for the oxide thickness agreed well with those measured by ellipsometry and x-ray reflectometry. They also produced current maps of the boundary between the gate oxide and the field oxide of a MOS device, and showed that an increased current flowed in the topographic groove which is observed between the two regions. By measuring I – V curves at various points across the boundary, they were able to extract values for the oxide thickness changes at the groove, although these were not confirmed by any other technique. Nonetheless, this study illustrates the potential of TUNA in identifying thickness inhomogeneities in MOS structures.

However, the thinnest oxide layers measured by Olbrich *et al* [145] were ca 3 nm thick. Studies of thinner layers by Ando *et al* [151] revealed significant deviations of the I – V curves from the FNT equation predictions. These deviations

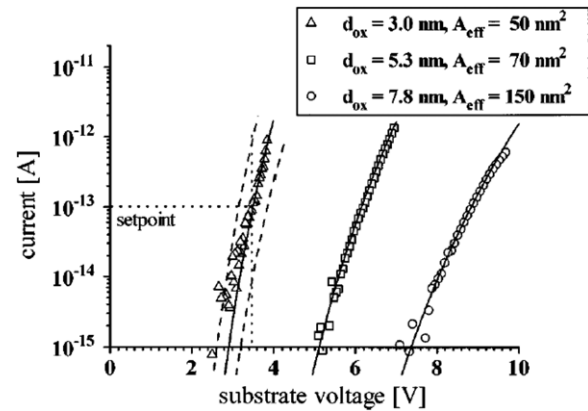


Figure 20. TUNA current–voltage data for SiO₂ films whose thickness was measured by ellipsometry to be 3.0 (○) 5.3 (□) and 7.7 (△) nm. The solid lines represent the FNT current fits to the data, and the corresponding fit parameters are displayed in the key. (Reprinted with permission from [145]. Copyright 1998, American Institute of Physics.)

arise because, for oxide layers thinner than 3 nm, current transport is not by FNT, but rather by direct tunnelling (DT) [150], in which electrons from the conduction band of the semiconductor are transferred across the oxide directly (i.e. without any change in energy) into the conduction band of the metal electrode. However, before a measurement of an oxide of unknown thickness is taken, one cannot know which tunnelling mechanism will dominate, particularly if the oxide may be between 3 and 5 nm thick, which is the range over which the transition between the two mechanisms occurs [150].

Hence, Frammelsberger *et al* [152] developed a semi-analytical tunnelling equation which could effectively simulate the tunnelling current through MOS structures for either tunnelling regime. Based on a wide-ranging survey of available literature data, they extracted a parameter set for this equation which allowed good fits to be achieved to all of the datasets surveyed, with the resulting oxide thicknesses being very similar to the expected values. Using this tunnelling equation, they achieved reasonable agreement with optical measurements for thicknesses down to 1.5 nm, although the deviation between the electrical and optical thickness increased with decreasing optical thickness [153]. Whether these deviations represent a genuine failing of the model or whether the optical and electrical methods actually measure different parameters is unclear. The structural thickness and the effective electrical thickness are not necessarily identical [146].

Despite the progress that has recently been made in this area, concerns remain about whether the achievable accuracy of the technique is affected by the impact the TUNA measurement has on the oxide film. For normal operating voltages, charge may be deposited on the oxide surface by contact electrification or corona discharge [154]. This surface charge creates an electric field which can lead to migration of charged contaminants from the tip. The applied field may also lead to the creation of charge traps [154]. Additionally, changes to the topography of the oxide film [153] have been observed which cannot be solely attributed to the repulsion

of the tip by the deposited surface charges, and must thus involve structural changes to the oxide film itself or to the underlying semiconductor [154]. These effects certainly limit the usefulness of TUNA in assessing oxide–semiconductor interface states [154], and their possible impact on thickness measurements has yet to be fully assessed. Another possible source of inaccuracy is, as with SCM of dopant structures, the influence of the laser used to monitor the cantilever height on the carrier density; reducing the stray light irradiating the sample has been shown to shift the I – V curves for TUNA measurements on silicon [155].

3.3.2. Leakage currents and their relationship to microstructure. Thickness fluctuations represent only one of the possible causes of current leakage through gate oxides. For electrically stressed oxides, charge trapping at the oxide/silicon interface may lead to weak spots at which leakage currents are enhanced [156]. Using TUNA, such weak spots may be identified as regions of higher current flow in current maps, and I – V curves may be taken at these points. Polspoel *et al* [157] showed that whilst I – V curves taken far from the weak spots exhibit smooth FNT characteristics, on the weak spots the curves exhibit multiple jumps, which could be due to the random population and depopulation of charge traps as current flows by trap-assisted tunnelling. Care must be taken in interpreting data concerning charge traps from TUNA, however, since the fields applied during the measurement could be responsible for trap creation, rather than the film growth method or electrical stressing procedure carried out prior to measurement [154].

For potential high- κ gate dielectric materials, such as HfO_2 [158] and PrO_2 [159], which are being intensively studied since they may allow leakage currents to be considerably reduced in future, ultra-thin gate oxide layers [159], other concerns arise. These materials may crystallize during device processing [158], leading to increased leakage currents via grains of a crystalline phase with a lower dielectric constant, or via grain boundaries [160]. C-AFM is being used to explore the spatial variation of leakage currents in these materials, but cannot provide a direct insight into the microstructural changes responsible. Another technique, such as transmission electron microscopy (TEM), must be used to identify potential microstructural features which may relate to the electrical weak spots [160]. Ideally, perhaps, one would take a TEM cross-section through a weak spot identified by C-AFM, to identify precisely the microstructure which causes the current leakage. This is practically difficult, however, and has not yet been achieved.

3.3.3. Breakdown. Following continued electrical stressing, current flow through weak spots in gate dielectrics may increase to the point where the dielectric breaks down entirely and can no longer be considered an insulator. Breakdown, as observed in macroscopic testing, is known to be a localized phenomenon and can thus be studied by C-AFM or TUNA [161]. (In fact, the earliest C-AFM experiments on gate dielectrics, before the advent of the high sensitivity current amplifiers used in TUNA, involved such high current densities

that all data was considered to relate to breakdown rather than leakage [162].) The sample may be stressed via the AFM tip, using either constant voltages or voltage ramps and then larger areas surrounding the stressed area imaged to provide insight into the effects of stressing [161]. Alternatively, the sample may be stressed macroscopically, and then the gate electrodes removed, allowing imaging of the stressed device by C-AFM [163].

The first of these two approaches is particularly powerful in that it allows the dynamics of the breakdown event at individual breakdown sites to be assessed, with current versus time curves taken under constant stress revealing jumps between conduction states, which might not be observed in a macroscopic measurement where events from many breakdown sites would be superimposed [164]. However, since electrical stresses may have to be applied via the AFM tip for extended time periods (perhaps several hundred minutes), issues of scanner related or thermal drift, and hence change in the stressing position must be considered [165]. Oohira and Ando [165] monitored the cantilever position during extended C-AFM stressing of a film at a single point, and showed that displacements of the cantilever position in the plane of the film may occur. They suggested that monitoring of cantilever torsional deflection, and feedback to maintain a fixed value, might be used to prevent this drift. This system has not yet been implemented, and the possibility that the tip position may change during stressing may cast doubts upon some of the results obtained using C-AFM. For example, Porti *et al* [166] suggested that the spots over which high currents flow after breakdown are larger than the area stressed by the tip, and that this suggests lateral propagation of the breakdown event. However, if the tip has moved during scanning, this could explain the increased size of the breakdown spot, without any lateral propagation.

Analysis of breakdown presents specific instrumental challenges, since prior to breakdown only very small currents flow, which it is desirable to detect and image, but after breakdown much larger currents flow. Many commercial C-AFM or TUNA setups have current limiters to prevent damage to the detection electronics, and even where these limiters are absent, the currents flowing during breakdown events are often so high that they saturate the detectors, preventing detailed analysis of the current flow mechanism [167]. The logarithmic amplifiers commonly used in SSRM may be more suitable for measurement of these high currents, but have insufficient sensitivity to the small tunnelling currents which flow prior to breakdown. Blasco *et al* [168] have developed a technique which they describe as ‘enhanced CAFM’ (ECAFM) in which the standard hardware used to bias the tip–sample system and to measure the resulting currents have been replaced with source monitor units (SMUs) which provide a variable and autoselectable measurement range, helping to overcome this problem and also providing an easy means of performing constant-current stressing, in addition to the constant-voltage stressing or ramped-voltage stressing usually used in C-AFM breakdown studies [169].

As with measurement of the oxide thickness, topographic changes to the sample surface are observed following

breakdown experiments. Where measurements are taken in air, the sample should be negatively biased relative to the tip, since this prevents anodic oxidation of the sample surface (i.e. the growth of further oxide). However, topographic changes are nonetheless seen. Zhang and Mitani [170] performed C-AFM measurements in vacuum to avoid anodic oxidation issues, and observed topographic changes which they attributed to electromigration of silicon. Porti *et al* [171], in contrast, suggest that some of the apparent topographic changes actually relate to forces on the tip from breakdown-induced negative charges trapped in the oxide layer. They have attempted to use KPFM and SCM to measure the amount of trapped charge. The estimates from the two techniques differ by more than an order of magnitude, leaving the exact nature of the topographic or other changes occurring during tip-induced breakdown still in question. However, this study illustrates a recent trend [172] to address questions relating to breakdown (and other device failure issues) with multiple AFM-based techniques.

3.4. Characterization and analysis of defects in semiconductors

Many semiconductors, silicon in particular, are astoundingly perfect, with very low densities of extended defects such as dislocations. However, some of the more recently developed materials such as GaN and ZnO may contain rather higher defect densities which may significantly impact their electrical properties. Here, we discuss the application of AFM-based techniques to characterize the electrical influence of point and extended defects.

3.4.1. Point defects: dissolved contamination Whilst AFM-based techniques have yet to be extensively developed for the examination of point defects such as vacancies, they can be used to study substitutional impurities in semiconductors, where such impurities act as dopants. This is an obvious extension of the dopant profiling technique described in section 3.1, with the main difference being that it may be unclear which element is acting as a dopant. As an example, GaN grown on sapphire often exhibits unintentional n-type conductivity, and depth-dependent Hall probe measurements have shown that much of this conductivity is localized in a layer adjacent to the GaN–sapphire interface [173]. Figure 21 shows a cross-sectional SCM dC/dV amplitude image of a GaN/sapphire epilayer, the first $\sim 5\ \mu\text{m}$ of which has not been intentionally doped. On top of this non-intentionally doped (nid) material, a staircase structure consisting of Si-doped GaN layers with varying, known dopant concentration separated by nid spacers has been grown. This staircase structure can be used to approximately calibrate the carrier concentration in the unintended conductive region which is observed as a grey band of varying thickness adjacent to the GaN–sapphire interface. A similar sample was studied by SIMS, which revealed an oxygen-contaminated layer in the GaN adjacent to the interface, of similar thickness to that observed by SCM [174]. The density of oxygen in the sample was also similar to the carrier concentration estimated from SCM [174]. Since oxygen is known to act as an n-type dopant in GaN,

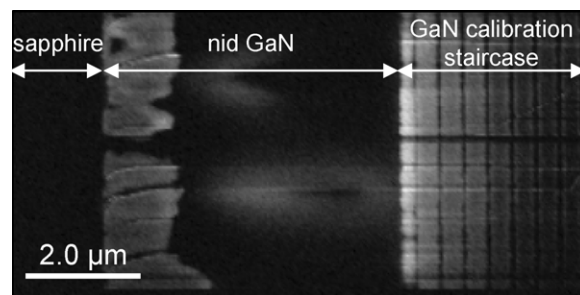


Figure 21. SCM dC/dV amplitude image of a GaN epilayer grown on sapphire. An unintentionally doped conductive region is seen adjacent to the GaN–sapphire interface.

this oxygen contamination was thus identified as the source of the unintended conductivity. Oxygen contamination may arise from diffusion out of the sapphire substrate or from contaminants in the reactants used to grow the epilayer.

3.4.2. Extended defects.

3.4.2.1. Dislocations. GaN light emitting diodes (LEDs) are largely grown on heteroepitaxial substrates giving rise to a high density ($\sim 10^8\text{--}10^{10}\text{ cm}^{-2}$) of threading dislocations (TDs). The charge state of these TDs is of interest since it may affect the mechanism of recombination of carriers in the active region of the LED, whilst the conductivity of the TD will affect leakage through the diodes. Given these and other device-related concerns, most AFM-based electrical characterization of dislocations relates to growth-related TDs in GaN, although recently some efforts to study deformation-related defects in other materials, such as ZnO have been made [175].

Attempts to study the impact of TDs on the electrical properties of GaN have been made using SCM [176], C-AFM [177] and KPFM [178]. In all cases, it is necessary to demonstrate that any features observed in the SPM-based electrical measurements are related to TDs, and preferably to identify which type of TDs (edge, screw or mixed) are related to the observed feature. Without imaging the TDs directly in SPM, it is possible to correlate the density of TDs of different types as observed in TEM with the density of electrical features observed in the SPM measurement, and hence identify which TD type may give rise to the electrical feature [179]. For samples grown by epitaxial layer overgrowth (ELOG) the TD density varies significantly and systematically across the surface. Moore *et al* [180] showed, using images such as those in figure 22, that the density of current leakage spots through ELOG GaN was much higher in the regions where a high TD density is expected from the known growth mechanism, and hence linked current leakage in *a*-plane GaN with TD locations. Alternatively, Hsu *et al* [181] have noted that current leakage can occur at the top of growth hillocks. If these hillocks have a spiral structure, this implies the presence of a screw or mixed TD at their centre, which could act as a leakage path. (However, Oliver *et al* [18] have shown that hillocks in GaN-based materials may consist of either a spiral structure or stacks of concentric islands, with only the spirals being related to TDs. The topographic resolution achieved

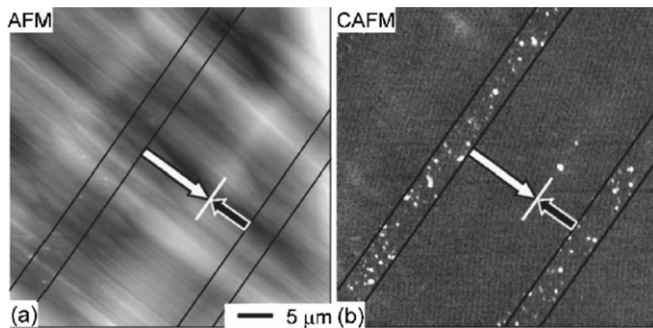


Figure 22. (a) Topography and (b) C-AFM data for an a-plane GaN epitaxial film grown by ELOG. The ‘window’ regions (between the closely spaced black parallel lines), and the coalescence boundary (indicated by the shorter white line) are known to have a higher TD density than surrounding regions and also exhibit an increased density of leakage current spots. (Reprinted with permission from [180]. Copyright 2007, American Institute of Physics.)

during C-AFM measurements may not always be sufficient to differentiate between the two.) Another indirect route used to relate electrical features to TDs is the measurement of the characteristic length scale of the electrical image from the power spectral density function and comparison of this with the dislocation density, since as the dislocation density decreases the dislocation spacing increases, presumably increasing the separation between electrical features [178].

Despite the ingenuity of these approaches, it may be preferable to be able to image the TD positions simultaneously with the electrical data. Since screw and mixed TDs give rise to step edge terminations, and all TDs give rise to small surface pits, due to their line tensions, such direct structural imaging is possible with a sufficiently sharp tip [20]. Hansen *et al* [176], for example, correlated areas of decreased SCM signal with the locations of surface pits relating to TDs. There is one possible pitfall relating to this approach which is particularly relevant to the characterization of LED structures where the TDs may open up into large (100–300 nm diameter) ‘V-pits’. In C-AFM imaging of such V-pits, Cao *et al* [182] observed current flow only around the edges of the pits, an observation which they were unable to account for. At the pit edges an increased contact area may be formed between the sloping pit wall and the tip sidewall, but as the tip moves to the centre of the pit, this contact area may decrease again if the tip fails to penetrate the bottom of the pit. Hence the features observed by Cao *et al* [182] may be a topographic artefact. Other researchers, however, have demonstrated a correlation between TDs and increased current flow even when the TD pits were too small to be imaged directly, and might thus be expected to decrease the tip–sample contact area [179].

Thus, despite the difficulties of relating the electrical and structural characterization of the samples, the weight of evidence from SPM and other techniques is that TDs do locally affect the electrical properties of GaN. The cause of this effect is difficult to elucidate from SPM alone, since the precise electronic structure of the TD core remains unclear, and depends on what impurities are present [178]. Additionally, the dislocations may act as an impurity getter so that a volume of material around the TD core has a reduced

concentration of intended or unintended dopants, and this affects the local electronic properties [177]. Since the size of the tip is greater than the size of the TD core, the SPM will sample the material in the core and its surroundings simultaneously, complicating data interpretation further [178]. Lastly, impurity concentrations are certainly dependent on the growth method, potentially leading to differing results between different samples. Hence, future studies should involve the correlation of the SPM data with other techniques such as TEM, looking at the same material (and preferably the same actual defect) to help clarify some of these issues. The combination of different SPM techniques to study the same region of material has already proved fruitful [177], and we advocate here an extension of this approach.

3.4.2.2. Inversion domains. In addition to dislocations, GaN may also contain inversion domains—i.e. regions in which the crystal polarity is inverted compared with the majority of the epilayer. Jones *et al* [183] prepared a reference sample by masking half of a sapphire wafer during AlN buffer growth, and then overgrowing with GaN, so that the GaN grown directly on sapphire was N-polar, whereas the GaN grown on the AlN buffer was Ga-polar. They confirmed these polarity differences by etching with hot H_3PO_4 which removes N-polar material much faster than Ga-polar material. They then showed a significant surface potential difference between the two polarities in KPFM measurements, independent of the surface topography. Having thus demonstrated the efficacy of KPFM in surface polarity determination, they were able to identify small hexagonal inversion domains in other MBE-grown GaN films. This approach is illustrated in figure 23. Bozek [184] extended this approach by preparing bevelled samples, so that the position on the bevel surface corresponded to different depths through the GaN film, and showed that the density of inversion domains was higher closer to the GaN–sapphire interface than at the surface.

3.4.2.3. Grain boundaries. Polycrystalline semiconductors are exploited in devices such as solar cells. In these devices carriers must cross grain boundaries (GBs) during operation, providing an incentive for exploration of the electrical properties of GBs on the nanoscale. Often the polycrystalline thin films under examination exhibit rather rough topography [185] (particularly in comparison with the carefully polished surfaces used in Si device studies). Whilst the topographic features may provide a simple indication of the position of grains and GBs, significant care must be taken in interpreting electrical data from such films, in order to demonstrate that observed contrast in electrical images is genuinely related to the film’s properties and not a consequence of changes in tip–sample interaction area. For SCM investigations of polycrystalline CdTe, Visoly-Fisher *et al* [185] showed that the observed contrast between the grain boundaries and the grains could be reversed by changing the applied dc bias, hence ruling out topographic artefacts in their experiments. However, they found that KPFM was rather more sensitive to the local topography.

Where comparisons between two samples with similar topography can be made, some confidence may be placed

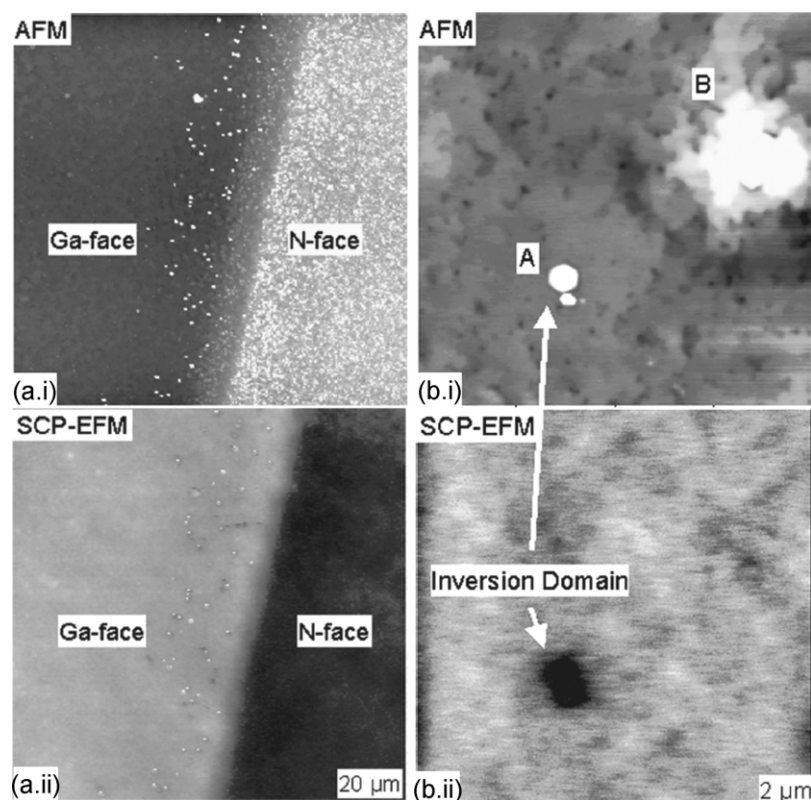


Figure 23. Simultaneous AFM ((a.i) and (b.i)) and EFM ((a.ii) and (b.ii)) images of ((a.i) and (a.ii)) a GaN sample deliberately grown to contain both Ga-polar and N-polar material and ((b.i) and (b.ii)) a sample grown by MBE with unintentional inversion domains. Comparison of the data in (a) and (b) allows identification of an inversion domain in (b). (Reprinted with permission from [183]. Copyright 2001, American Institute of Physics.)

in SPM electrical data if the electrical data differs strikingly between the two samples [186]. Moutinho *et al* [187] compared C-AFM data from as-grown CdTe/CdS solar cells, and samples which had been etched with bromine and methanol. Whilst the sample topography was largely unchanged, the current at the GBs was increased significantly by the etching process (see figure 24). Alternatively, if a network of electrical features is seen, some of which coincide with obvious topographic features and others of which do not, researchers may infer that all the electrical features relate to genuine changes in electrical properties at the grain boundaries [188]. (In this case, however, it remains possible that the electrical features which do relate to topographic changes are topographic artefacts and/or that the electrical features which do not relate to topographic changes are not actually grain boundaries.)

The imaging of telluride-based solar cells in contact mode is also challenging due to the softness of the material, which may be damaged unless the applied contact forces are reduced to the 10^{-7} N range [187]. Moutinho *et al* [187] additionally observed a decrease in the observed current if the same area is imaged multiple times in C-AFM, which they attributed to the growth of oxide during current imaging. However, no major topographic changes were associated with this change in current flow, casting doubt on this explanation.

As with other devices, the laser used to monitor the AFM cantilever height may give rise to extra current flow in a solar cell. However, in this case this photocurrent is actually very relevant to solar cell operation, and hence comparison of the

different currents with and without the laser illumination may prove interesting. Azulay *et al* [189] have recently attempted to examine the photocurrent by comparing the current during two passes of the C-AFM tip. During the second pass the laser was switched off and the tip height was defined by the topography recorded in the first pass in order to try and maintain a constant contact force. Examination of the photocurrent through the grain boundaries under broad-spectrum illumination (rather than just red laser light) may also be of interest in the future.

Despite the difficulties of understanding the influence of the topography on the electrical data, various studies have illustrated that GBs do have different electrical properties to the surrounding grains. However, a more taxing problem is to use the SPM data to understand the electrical structure of the GB, rather than just identify it as qualitatively different. Leendertz *et al* [190] have used finite element modelling to examine whether KPFM is capable of distinguishing between different possible grain boundary electronic structures. Whilst these different electronic structures would give rise to different shapes of the potential dip at the grain boundary, the tip samples the area around the grain boundary simultaneously with the boundary [191], blurring out the dip and making it difficult to distinguish the necessary details. The model does not yet include effects of topography, which may make the interactions between the sample and the tip sidewalls even stronger, further distorting the electrical signal. Hence, to use KPFM for these detailed electrical studies sharper tips or flatter surfaces

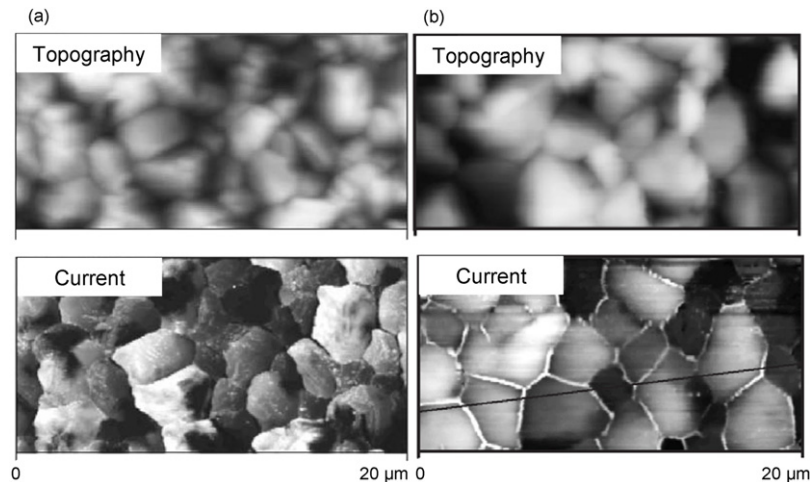


Figure 24. Topography and current images of a polycrystalline CdTe/CdS solar cell (a) before and (b) after etching with bromine and methanol. The topography is similar in both cases but the current at the grain boundaries is greatly increased after etching. (Reprinted from [187]. Copyright (2006), with permission from Elsevier.)

may be required. The authors also suggest that KPFM under illumination could be used to provide extra mechanistic data.

3.5. Characterization of nanostructures

3.5.1. Quantum wells. Cross-sectional imaging of quantum wells (QWs) has provided a useful testing ground to assess the resolution of electrical SPM techniques. Whilst for narrow dopant profiles, carrier diffusion broadens the feature, the potential barriers which bound QWs ensure that the area of increased carrier density associated with them is rather sharply defined, making them ideal test structures. Douheret *et al* [192] used QWs of varying width to estimate a resolution of 15 nm or better for SSRM and a resolution of 30–60 nm for SCM. For KPFM, Usanami *et al* [193] illustrated that it was possible to identify structures of width 40 nm in air, whilst (in a study separate to their SSRM work) Douheret *et al* [194] imaged 5 nm structures successfully in ultra-high vacuum (UHV). As figure 25 illustrates, the finite width of the tip means that whilst such small structures may be identified, their width is often broadened in the SPM image. Schwarzmann *et al* [195] developed a routine to restore the ‘true’ surface potential image from the KPFM data, for improved width measurement of QWs. However, the model does assume a known shape and size for the tip, which is unlikely to be accurate unless tips are individually qualified.

To achieve improved spatial resolution it is possible to use beveled samples. Given the confinement of carriers in the QW, carrier spilling in beveled samples is less problematic in this case than it is for the measurement of ultranarrow dopant profiles [196]. However, Ferguson *et al* [197] identified bevel surface roughness as leading to inaccuracies in quantum well width measurement, and additionally noted that if the QW is corrugated rather than flat, the bevel may cut it in several places leading to multiple stripes in the SPM image. Nonetheless, measurements on beveled samples have allowed Giannazzo *et al* [198] to move beyond the use of QWs as a test system; their studies combined SCM and SSRM studies of Si/Si_{0.75}Ge_{0.25}/Si studies to extract the drift mobility for carriers in quantum

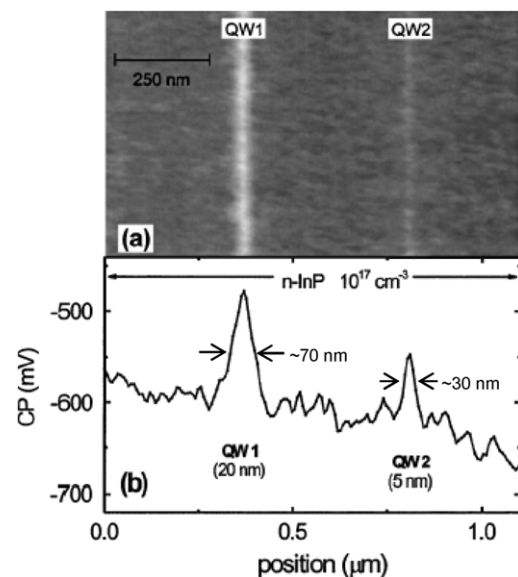


Figure 25. (a) UHV KPFM image of an InGaAs/InP QW sample showing QWs of width 20 nm (QW1) and 5 nm (QW2). (b) Typical line scan of the variation in surface potential with position across the QW structure. The observed feature widths are greater than the true feature widths, due to the finite tip size. (Reprinted with permission from [194]. Copyright 2004, American Institute of Physics.)

wells down to 1 nm in width. Calibration samples were used to quantify the SPM data, so that carrier concentrations could be extracted from the SCM images and resistivities from the SSRM images. Combining the two datasets, drift mobility was calculated, and shown to decrease with decreasing QW width.

Most studies in the SiGe/Si system or in conventional III–Vs have not considered possible non-uniformities within the plane of the well. In GaN-based materials, however, QW inhomogeneity is relied upon to achieve carrier localization and thus prevent carrier diffusion to TDs. The microstructural nature of the localization sites is a matter of significant controversy [199]. Zhou *et al* [200] attempted to identify the localization sites by using SCM to examine an InGaN

QW with a thin GaN cap from the top surface. Clear variations in carrier density were identified, which did not relate to any GaN topographic surface feature. Modelling of the carrier densities in QWs with different compositions and thicknesses, and comparison with SCS data, suggested that such variations might be attributed to local compositional variations. However, the models related to separate, uniform wells, rather than to the actual electronic effects of non-uniformity. No other microstructural characterization of the studied QW was provided to confirm the compositional variation. Nonetheless, this study does indicate the potential of SCM in studying sub-surface nanostructures in a non-destructive manner.

3.5.2. Epitaxial quantum dots.

3.5.2.1. Surface quantum dots. Epitaxial quantum dots (QDs) have primarily been studied in plan-view without a semiconducting cap. Transport studies by C-AFM on III–V QDs reveal differences in the current between the QD and the wetting layer (WL), which are attributed to differences in the surface states, and hence the tip–sample Schottky barrier [201]. These effects dominate measurements both in air [201] and in UHV [202]. Similarly, surface effects dominate KPFM studies, as expected, but interpreting observed potential differences in terms of the dot properties is difficult for small nanostructures since the sample topography strongly influences the local electrostatics. Ono and Takahashi showed using finite element modelling that for a small region of reduced surface potential, the measured change in surface potential was very strongly dependent on the lateral extent of the region [203]. Tevaarwerk *et al* [70] performed similar studies for a more realistic tip–QD geometry, and showed that for features whose size is of the order of or smaller than the radius of influence of the tip apex (which they define as the radius of the area of sample responsible for 50% of the electrostatic force gradient), realistic values for surface properties could only be extracted from KPFM data by using detailed modelling (which, as usual, requires one to know the tip shape).

The interactions between the tip and nanostructure shape have made it difficult to extract detailed information concerning QDs from electrical SPM data. However, Xue *et al* [204] in C-AFM studies of SiGe QDs were able to compare QDs of similar size and shape grown at different temperatures and note a difference in C-AFM current distribution between them, as illustrated by the height and current profiles in figure 26. They attributed this to a difference in the Ge content and Ge distribution in the QDs, and were able to partially confirm their hypothesis using selective etching experiments. Although these experiments were performed in air, it was later shown that the resulting oxide coating on the uncapped dots largely affects the magnitude of the measured current, not the shape of the current distribution [205], validating this approach and showing that some information on the structure of QDs may be extracted from non-destructive electrical SPM measurements.

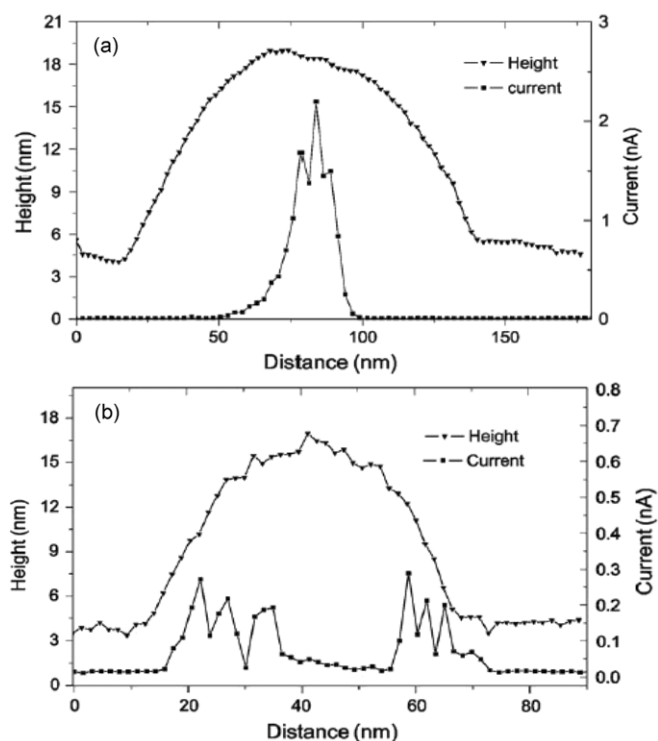


Figure 26. Topography and current profiles across SiGe QDs grown at (a) 550 °C and (b) 640 °C. Whilst the dot shapes are similar, the current profiles differ significantly and these differences can be related to differences in the Ge distribution within the dots. (Reprinted from [204]. Copyright (2005), with permission from Elsevier.)

3.5.2.2. Buried quantum dots. The work of Zhou *et al* [200] on capped InGaN quantum wells, indicates that SCM may be an appropriate technique for the non-destructive characterization of buried nanostructures, such as QDs. Thus far, few studies have attempted this, but Decossas *et al* [206] have imaged Ge domes capped with 15 nm of Si with SCM, and Smaali *et al* [207] have examined InAs QDs capped with InP by C-AFM, although in the latter case the cap does not entirely cover the QDs. The use of SPM-based techniques to image sub-surface nanostructures is in its infancy, but may blossom in the future, since it may allow the non-destructive identification of specific nanostructures with useful properties where no related topographic features are present.

3.5.3. Non-epitaxial nanostructures. In this section we discuss semiconductor nanostructures—nanocrystals (also referred to as quantum dots) and nanowires (or quantum wires)—which are formed by methods other than epitaxial growth at surfaces. Such structures are prepared by a wide range of methods, and the aims and requirements of electrical SPM studies to determine their properties vary wildly. Here, we simply highlight a few interesting examples.

3.5.3.1. Nanocrystals. Chalcogenide nanocrystals made by organometallic synthesis and dispersed on various substrates have been studied by EFM-based techniques. Whilst in order to achieve detailed quantification of the data extensive modelling of the tip–sample system would again be required (such as

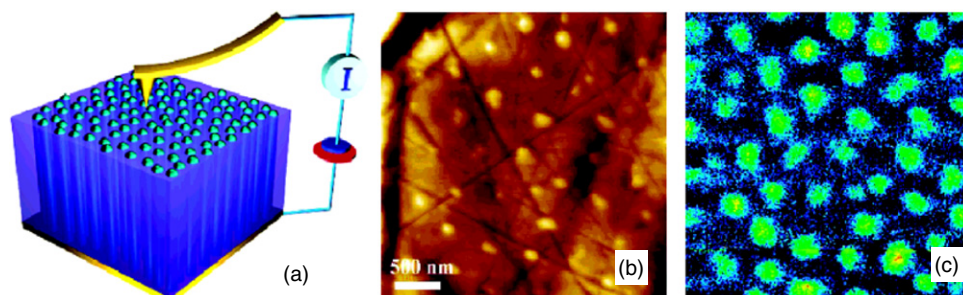


Figure 27. (a) Measurement geometry used by Erts *et al* [214] to perform longitudinal conductivity measurements on individual nanowires; (b) topographic and (c) current images taken in this geometry. (Reprinted with permission from [214]. Copyright (2006) American Chemical Society.)

the finite element modelling carried out by Melin *et al* [208]), useful information about the charge state of the nanocrystal is nonetheless available. For example, Krauss and Brus [209] showed that ~ 5 nm diameter CdSe nanocrystals may be either positively charged or neutral, and that by illuminating the structures above their bandgap, positive charges could be induced on additional nanocrystals. The time constant for the decay of the photo-induced charge was low enough that by taking EFM images of multiple nanocrystals at different times, the dynamics of the process could be understood [210]. In the original experiments [209], each nanocrystal was shown to store only one hole, showing the sensitivity of EFM-based techniques to very small charge variations.

3.5.3.2. Nanowires. Nanowires produced by a range of methods including vapour–liquid–solid (VLS) growth [211], and electrodeposition in anodic alumina templates [212] have been studied by C-AFM. Nanowire conductivity has been assessed in both transverse [213] and longitudinal [214] geometries. For transverse conductivity assessments, the nanowires are dispersed on a conductive substrate, and current through the nanowire cross-section and the substrate is measured. Liang *et al* [213] used this approach to confirm that nanowires coated in SiO_2 had been successfully insulated from the substrate, by comparing I – V curves from coated and uncoated structures.

For the assessment of longitudinal conductivity, one end of the nanowire must be attached to a macroscopic contact, whilst along the rest of its length the nanowire should only be contacted by the C-AFM tip. For nanowires grown on a conducting substrate, in a vertical geometry, this is easily achieved, with AFM imaging of the tops of the nanowires in the array allowing identification of individual structures. An example of this approach is shown in figure 27, illustrating the work of Erts *et al* [214] who studied the longitudinal conductivity of Ge nanowires in an anodic alumina template. Figure 27(a) shows the imaging geometry, whilst figures 27(b) and (c) show topographical and current data respectively. Protrusions in the topographic data correspond to increased currents in figure 27(c) where conduction through the nanowires is occurring. I – V curves may also be taken in this geometry, but naturally depend in part on the nature of the tip–nanowire contact.

Alternatively, nanowires may be distributed on an insulating substrate, and macroscopic metal contacts deposited

at random so that they intersect one end of some of the nanowires. Using this geometry, Zhou *et al* [215] measured the current through the nanowire as a function of the separation between the macroscopic electrode and the C-AFM tip. They were thus able to show that current flow was ballistic for tip–electrode separations of less than 200 nm. For larger separations, the motion of electrons was drift-dominated.

4. Concluding remarks: current trends and future directions

Currently, of the various electrical characterization applications of SPM which have been discussed, only dopant profiling can be thought of in any way as a routine procedure, and even in that case approaches to quantification vary between research groups and between materials systems. Characterization of dielectric layers using C-AFM or TUNA is also increasingly widespread, but many of the other studies that we have reviewed in section 3 involved experimental designs and analysis routes developed for one specific materials problem. With the ever-increasing variety of nanoscale semiconductor systems and additionally the increasingly imaginative uses to which scientists put the AFM probe, this proliferation of approaches is perhaps inevitable.

Nonetheless, throughout this review, several repeating motifs have arisen which must often be considered if we are to achieve accurate, reproducible and quantitative electrical data. The first of these is the influence of sample topography, which was highlighted specifically in section 2.6. Whilst for cross-sectional characterization of devices this topography may be minimized by optimized surface polishing procedures, these procedures may increase the density of trap states at the surface, influencing the electrical SPM data. For the study of defects and nanostructures the issue is more vexed, since in many experiments the only way to identify a feature of interest—such as a dislocation or a surface quantum dot—is from the topographic SPM data. However, the very existence of the topographic feature inevitably influences the measured electrical properties. Hence, in the future, we may hope to see further detailed modelling of the electrical properties of tip–sample systems including a realistic estimation of both the tip and nanostructure geometry. This wish, however, brings us directly to the second recurring major challenge which faces the field—the reliability of the currently available tips.

Our modelling and quantification efforts often require us to define the tip shape and electrical state, and these properties are difficult to gauge, particularly for tips which have already been used for multiple scans.

Topographic AFM is coming under increasing scrutiny from the International Organization for Standardization (ISO), in order to validate and standardize dimensional measurements [216]. Amongst other targets, they aim to standardize methods which attempt to restore the ‘true’ surface morphology from the raw topographic data, and to do this are developing standard samples for the determination of tip shape, using nanostructures of known dimensions [216]. This approach may be relevant to the determination of tip shapes for electrical SPM also, although in the case of metal coated tips, the loss or deformation of the metal coating during scanning may mean that tips require very frequent re-testing. The increasing use of all-metal [50] or all-diamond [55] tips may lead to more stable and predictable tip shapes.

The development of new applications also places increasing demands on the available probes. Zimmermann *et al* [143] have suggested that more robust high aspect ratio tips are required to allow SCM assessment of structures at the bottom of deep trenches. Meanwhile, Vandervorst *et al* [217] have proposed a new instrument concept—the Nanoprofiler—which places enormous demands on tip design. Whilst SSRM was originally conceived as a nanoscale analogue of SRP, conventional SRP uses two tips on a beveled surface and measures the current between them. If an SPM probe could be realized with two very closely spaced tips, connected to separate conducting channels, then this would be a true nanoscale analogue for SRP, and also provide data complementary to SSRM. It might also open the door to the implementation of other multi-probe techniques, such as the four-point probe, at the nanoscale—going beyond the multiple probe techniques detailed in section 2.5.3. Duriau *et al* [218] have realized cantilevers with integrated conducting lines, and also demonstrated that two separate conductive tips with sub-micrometre spacing can be produced on one cantilever using deep-UV lithography. However, the full ‘Nanoprofiler’ system has yet to be realized.

A further theme which has emerged from our discussions of SPM characterization of defects and nanostructures is the utility of combining electrical SPM techniques with structural characterization techniques such as TEM. With the increasing availability of FIB equipment, which allows site-specific sample preparation, one might hope not only to identify the general structural characteristics of a sample studied by electrical SPM but also to identify specific electrical features of interest, section these using the FIB and observe their structure using TEM or a three-dimensional atom probe (3DAP). FIB is already under investigation for site-specific sample preparation [92], and other opportunities to apply this flexible micro-machining technique are bound to arise.

Perhaps the ultimate in combining electron microscopy with SPM however, is the integration of an AFM into an electron microscope, so that the sample may be observed in the electron microscope whilst it is measured or manipulated by the AFM tip. One recent example of the combination of SEM

and AFM is found in the work of Troyon and Smaali [219] who have used an AFM tip coated with doped diamond to collect the current induced by the electron beam in an SEM. They term this technique, which is essentially a combination of SEM and C-AFM, near-field electron beam induced current imaging (NF EBIC), and show that it has a considerably better resolution than the standard EBIC technique in which the current is collected at a broad area contact.

Attempts have also been made to combine TEM with SPM. As early as 1991, Iwatsuki *et al* [220] developed a TEM specimen holder which allowed STM and reflection electron microscopy of the same area of a sample, and recently, interest in combined SPM-TEM systems has resurged. Such systems, which are now commercially available [221], are currently being used for the investigation of the changes occurring in the sample and/or tip during force–displacement measurements [221, 222], rather than to allow simultaneous SPM and TEM imaging, which has not yet (to our knowledge) been realized. In the future, it is possible that changes occurring to semiconductor samples during electrical or electromechanical manipulation may also be monitored in this way. Whilst this review has focused specifically on the *characterization* of semiconductors, rather than their *modification* using electrical SPM techniques, we have seen that (for example in studies of gate oxides using TUNA) such characterization may inadvertently alter the material structure, showing one possible motivation for combined SPM-TEM electrical studies.

With the availability of such rich opportunities to develop new probes or instruments and to combine microscopy techniques, it cannot be doubted that electrical scanning probe microscopy is poised to provide fascinating insights into the electrical properties of semiconductors at the nanoscale. This report has illustrated the utility of scanning probe techniques across an enormous breadth of the challenges currently faced in the semiconductor arena, from device failure analysis, to understanding the basic properties of nanoparticles. Certainly, application of SPM electrical techniques requires significant care both in practical and data interpretation terms. However, such efforts have been hugely beneficial and should reap further rewards in the future.

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