# 4x4 4-bit Comparator

Oday Ziq

Abstract—Gate Diffusion Input (GDI) technology offers an efficient alternative for low power VLSI applications, enabling circuits with significantly fewer transistors compared to traditional methods. This paper presents GDI cells applied to combinational circuits, including a novel low-power XOR design using only nMOS transistors. Performance metrics such as area, delay, and power dissipation are optimized and compared to standard CMOS logic. Additionally, an N×N bit magnitude/signed comparator using the 4-bit GDI technique is introduced, reducing the transistor count from 226 (CMOS) to 12 (GDI) and improving power efficiency and response time. Simulations using DSCH, Microwind 3.1 (120nm), and ELECTRIC TOOL EDA (4nm) demonstrate the GDI approach's robustness in modern electronic design.

## I. Introduction

In the rapidly advancing field of electronics, integrated circuit (IC) efficiency is crucial for modern digital systems. Power consumption has become a critical parameter in CMOS VLSI design with submicron technology scaling. Gate Diffusion Input (GDI) technology offers a promising solution, reducing transistor count and optimizing area, delay, and power consumption. This project explores the innovative application of the 4-bit GDI technique in designing a high-efficiency N×N bit magnitude or signed comparator. The design aims to overcome traditional CMOS comparator limitations by enhancing speed and reducing power consumption and silicon footprint.

### A. GDI overview

GDI approach makes use of a GDI cell as shown in fig.1 [9]. This cell resembles a CMOS inverter with some alterations. A GDI cell has four terminals – G (common gate of pMOS and nMOS transistors), N (input to the source and drain of the nMOS), P (outer diffusion node of pMOS transistor) and Out node which acts as a common diffusion node for both the transistors.

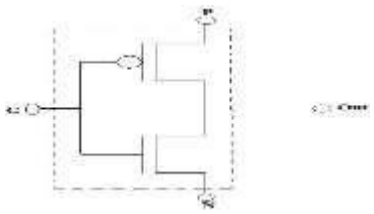

**Figure 1:** Basic GDI cell

Table I shows various functions and logical expressions that can be implemented using GDI cell . These functions may require 6-12 transistors with the use of CMOS technology but with GDI, implementations of these function is very simple and require only two transistors. This in turn reduces the area, delay and hence the power consumed by the circuitry.

With the help of GDI Multiple input gates can also be implemented. This can be done by combining several GDI cells.

**Table 1:** Basic GDI Functions

| N | P | G | Out | Function |
|---|---|---|---|---|
| „0“ | B | A | $AB$ | F1 |
| B | „1“ | A | $A+B$ | F2 |
| „1“ | B | A | $A+B$ | OR |
| B | „0“ | A | $AB$ | AND |
| C | B | A | $AB+AC$ | MUX |
| „0“ | „1“ | A | $A$ | NOT |
| | | | | |

### 1 Bit Magnitude Comparator

To realize 1 Bit magnitude comparator EXOR and AND mainly used. It consists of two inputs for allowing two single bit numbers and three outputs to generate less than, equal and greater than comparison outputs. Since XNOR produces output 1 for same bits of input, this property is used to find if the two bits are equal. An AND gate is used to check first bit is greater or lesser than the second. GDI cell based 1 Bit magnitude comparator is shown in fig. 10. The same principle can be further extended to n-bit comparator.

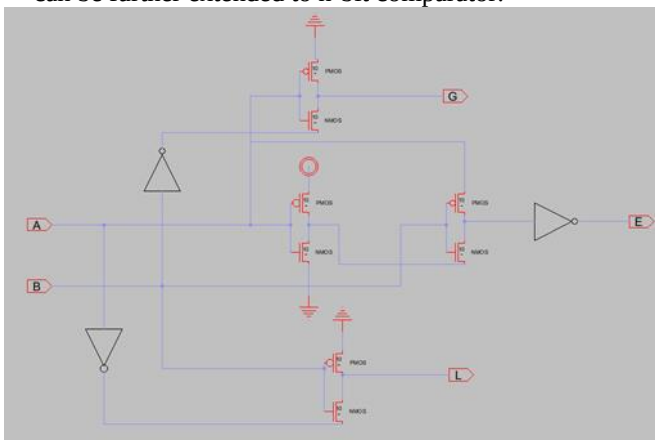


**Figure2: 1-bit comparator (sch)**

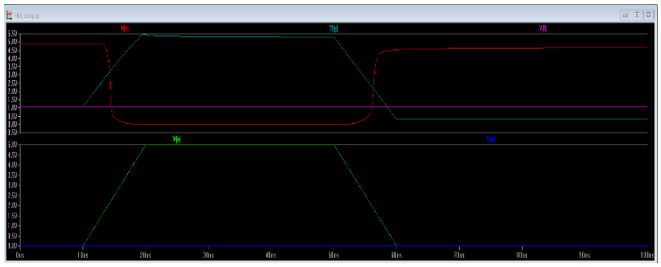

**Figure3: 1-bit comparator waveform**

The above 1-bit comparator was used to construct a 4-bit comparator by incorporating 4 1-bit comparators, along with 2 2-input AND gates, 2 3-input AND gates, 3 4-input AND gates, and 2 4-input OR gates. This design utilizes a total of 134 transistors, in comparison to 226 transistors used for the CMOS technique, as illustrated in the figure below.

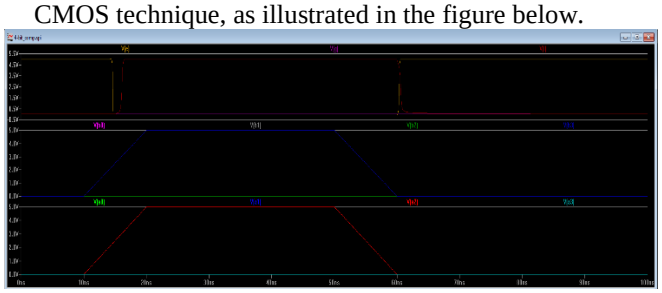

**Figure4: 4bit comparator waveform**

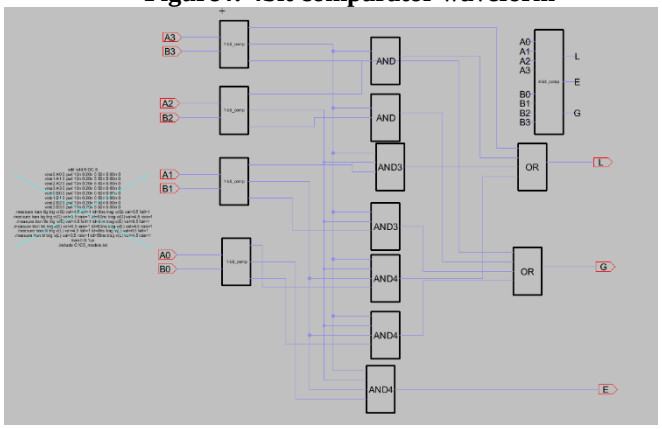


**Figure5: 4-bit comparator (sch)**

The below figures show us how the layout was designed for the 1 bit and 4 bit comparatos.

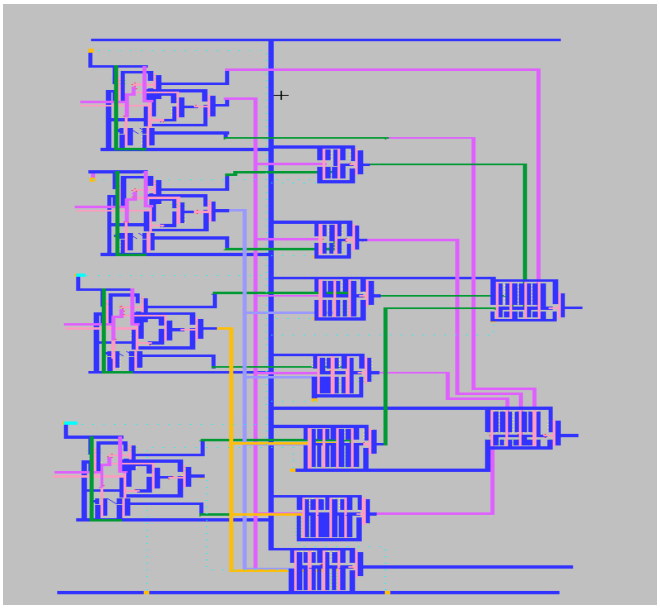

**Figure6: 4 bit comparator layout**

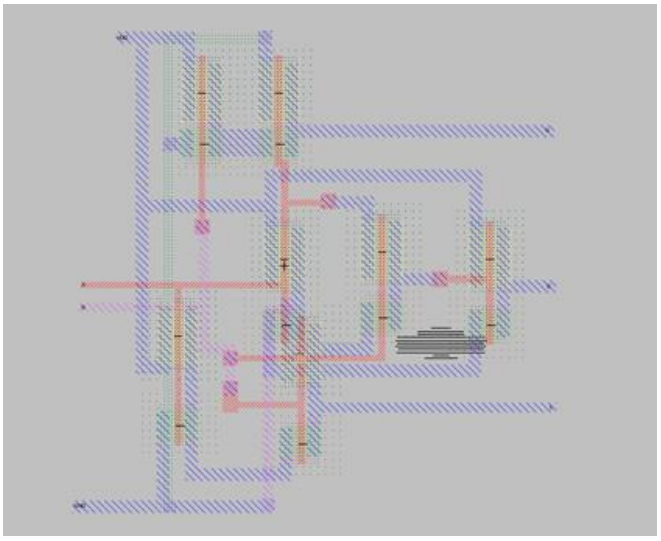

**Figure7: 1 bit comparator layout**

the below figures show us how the logic gates that was used was constructed using CMOS technique

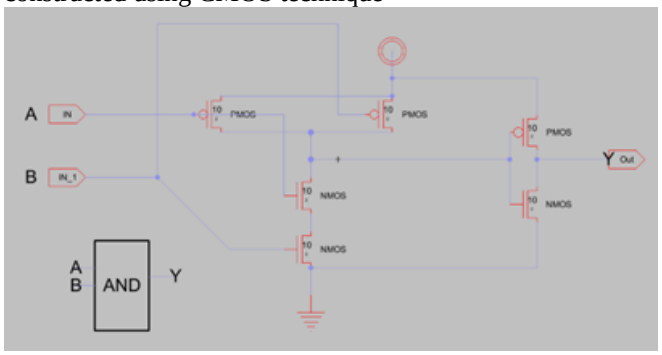


**Figure8: 2 input and gate (sch)**

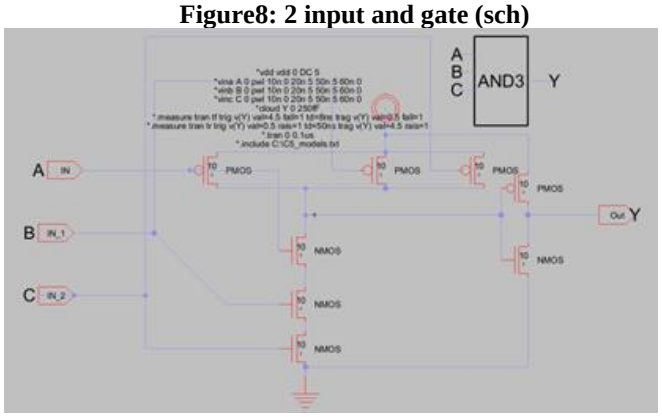


**Figure9: 3 input AND (sch)**

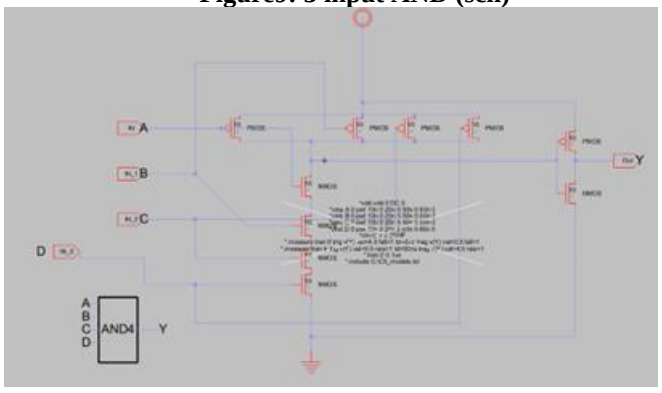


**Figure10: 4 input And gate (sch)**

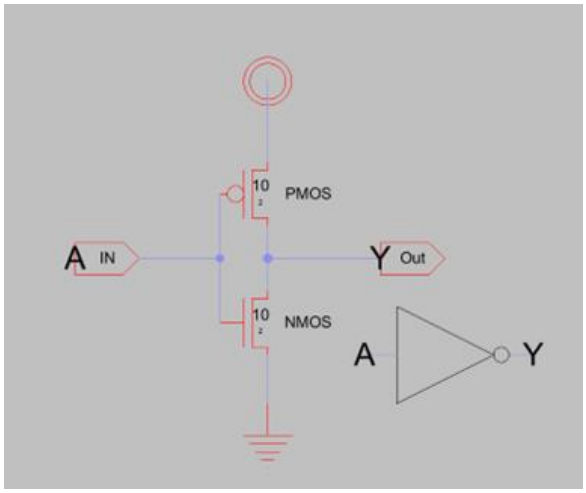


**Figure11: invertor (sch)**

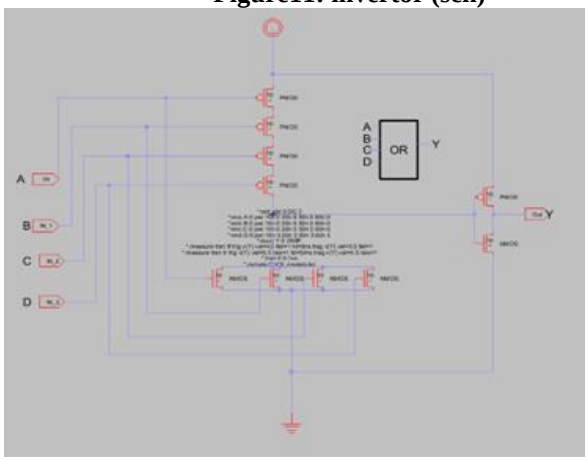


**Figure12: 4 input OR gat e(sch)**

*c. Comparison parameters GDI vs CMOS*

The delays for The delays for *g* g, *l* l, and *e* e were measured by analyzing the waveforms with various inputs:

a. Delay for *g* g: 20.2 ns

b. Delay for *l* l: 16.8 ns

c. Delay for *e* e: 15.5 ns

From these results, the worst-case delay is observed to be 20.2 ns for the g case, in comparison to 82 ns in the CMOS technique.

The power consumption can be calculated as VDD x IVDD = 5V x 58.8uA = 294 uW, in comparison to 316 uw in the CMOS technique.

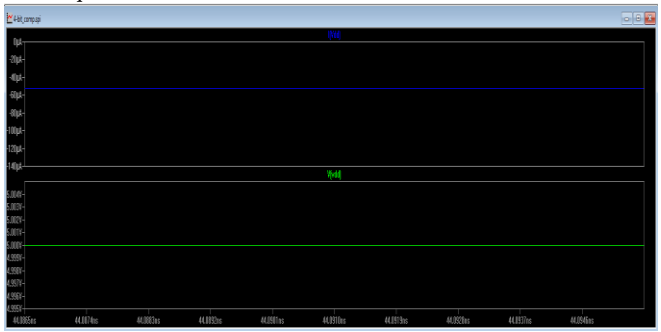

**Figure13: VDD and Ivdd values**

The Area of the layout for the 4-bit comparator can be calculated from the size in the Electric tool, size = 607 x 1180 = 716.3$nm^2$, in comparison to 1500$nm^2$ for the CMOS technique. As we can see from the results above, the design has better parameters than the CMOS technique overall.

## II. Conclusion

In this study, the efficiency of Gate Diffusion Input (GDI) technology was evaluated against traditional CMOS techniques for low power VLSI applications. The GDI-based 4-bit comparator uses 41% fewer transistors, reducing from 226 to 134 transistors, and occupies 52% less area, with a layout size of 716.3 nm² compared to 1500 nm² for CMOS. Power consumption is reduced by 7%, with GDI consuming 294 µW versus 316 µW for CMOS. The worst-case delay for the GDI comparator is 75% faster, at 20.2 ns compared to 82 ns for CMOS. These results highlight GDI's significant advantages in transistor efficiency, power consumption, speed, and area, making it a superior choice for modern digital circuit design.

## REFERENCES


[1] https://ietresearch.onlinelibrary.wiley.com/doi/10.1049/iet-cds.2018.5562

[2] Low-Power and Fast-Swing-Restoration GDI-Based Magnitude Comparator for High-Speed Applications" - This article discusses advanced GDI techniques that enhance speed and power efficiency in digital comparators.

[3] Gupta, V., Sharma, R. K. (2017). "A Comparative Study of 2-bit Magnitude Comparator Designs Using Conventional and GDI Techniques," in Proceedings of the International Conference on Microelectronics, Computing Communication Systems, pp. 305-314.

[4] Chen, L., Zhou, H. (2020). "Design and Analysis of High-Speed GDI-Based Digital Comparators," Microelectronics Journal, 103, 104763.

[5] Sharma, A., Gupta, M. (2019). "Low-Power and Area-Efficient GDI Magnitude Comparator," Journal of Semiconductor Technology and Science, 19(2), 227-235.

[6] Singh, P., Kumar, A. (2018). "Enhanced Performance of Digital Comparators Using GDI Technique," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 26(8), 1594-1601.

[7] "DESIGN OF 8-BIT COMPARATOR BASED GDI LOGIC USING FINFET TECHNOLOGY" - Explores the integration of GDI logic with FinFET technology for designing an 8-bit comparator.

[8] Rahman, F., Khan, Z. A. (2018). "Gate Diffusion Input (GDI) Technique for Power-Efficient Digital Logic Circuits: A Review," Journal of Low Power Electronics and Applications, 8(3), 28.

[9] Patel, J., Desai, A. (2021). "Innovative Approaches to Comparator Design Using GDI Techniques," IEEE Circuits and Systems Magazine, 21(2), 48-62.

[10] Mathur, S., Sharma, P. (2020). "Energy-Efficient and High-Speed Comparators in Nanoscale CMOS Technology Using GDI," Electronics Letters, 56(6), 278-280.