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# **example2**

**ipxact2systemverilog**

**Aug 28, 2025**



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## EXAMPLE2

Second demo example used for the testing of the ipxact2systemverilog tool.

**Base Address**

0x0

## 1.1 Registers

Address	Register Name	Description
0x00	<i>reg0</i>	read something useful for reg0
0x01	<i>reg1</i>	

## 1.2 reg0

**Name**

reg0

**Address**

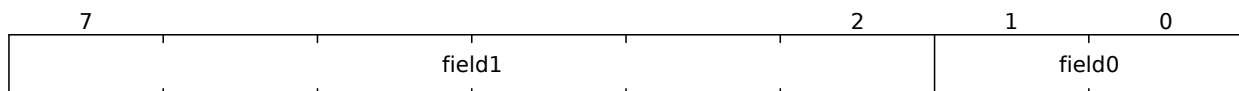
0x0

**Access**

read-only

**Description**

read something useful for reg0



Bits	Field name	Description
[7:2]	field1	read something useful for field1
[1:0]	field0	read something useful for field0

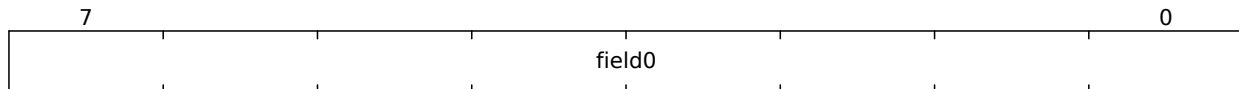
## 1.3 reg1

**Name**  
reg1

**Address**  
0x1

**Access**  
read-only

**Description**



Bits	Field name	Description
[7:0]	field0	read something useful for field0

### 1.3.1 field0

**Minimum**  
0x00

**Maximum**  
0x07