DFDV3100 – 2020/2021

Computer System Architectures and VHDL Programming

Universitetet i Sørøst-Norge

DFDV3100 – 2020/2021

(2nd part: Architectures)

Compulsory Coursework| Cache Cotrol FSM

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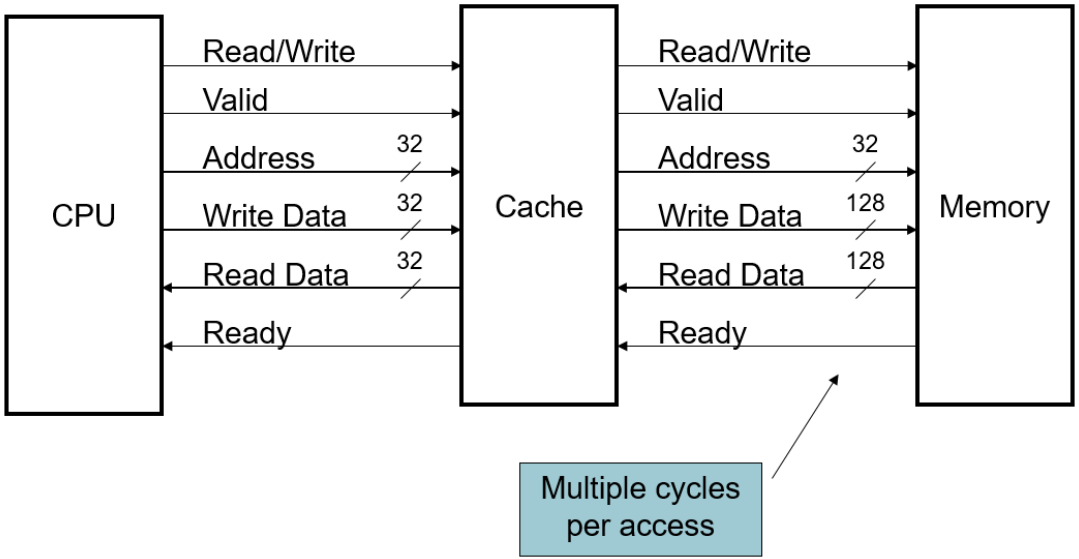
General Information

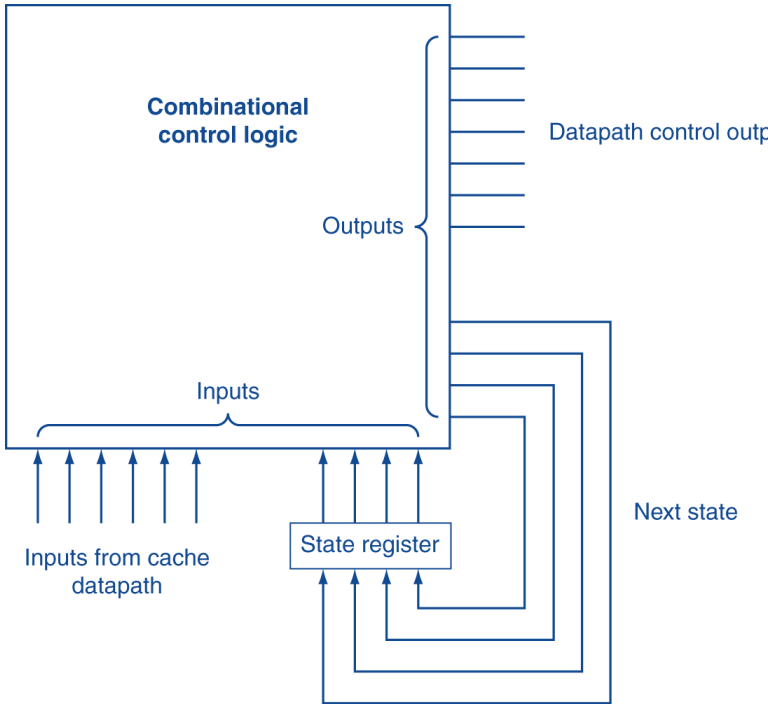
- **Work in Group of 2**
- **Timeframe: 4 weeks**
- **Resources: Lecture notes + Textbooks + Google +…**
- Delivery: Specification Document & Source Code
- How to hand in: Canvas
- Deadline: 20.11 (23:59)
- Criteria for approval: 60% workload

Signal Interface

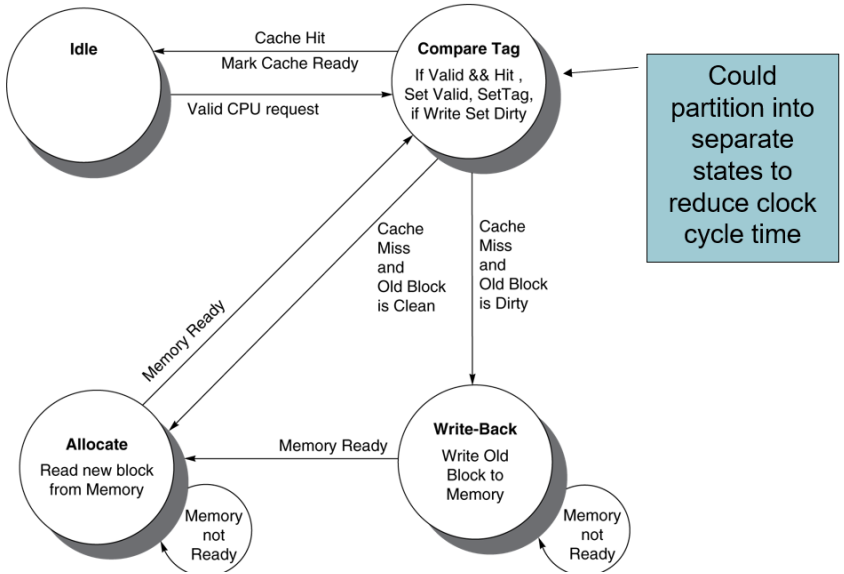


Finite State Machine (FSM)

- FSM for sequence control steps
- Set of States, transition on each clock edge
  - States are binary encoded
  - Current state stores in a register
  - Next state is a function of current states and input
  - Control Ouput



Cache Controller FSM



Tasks

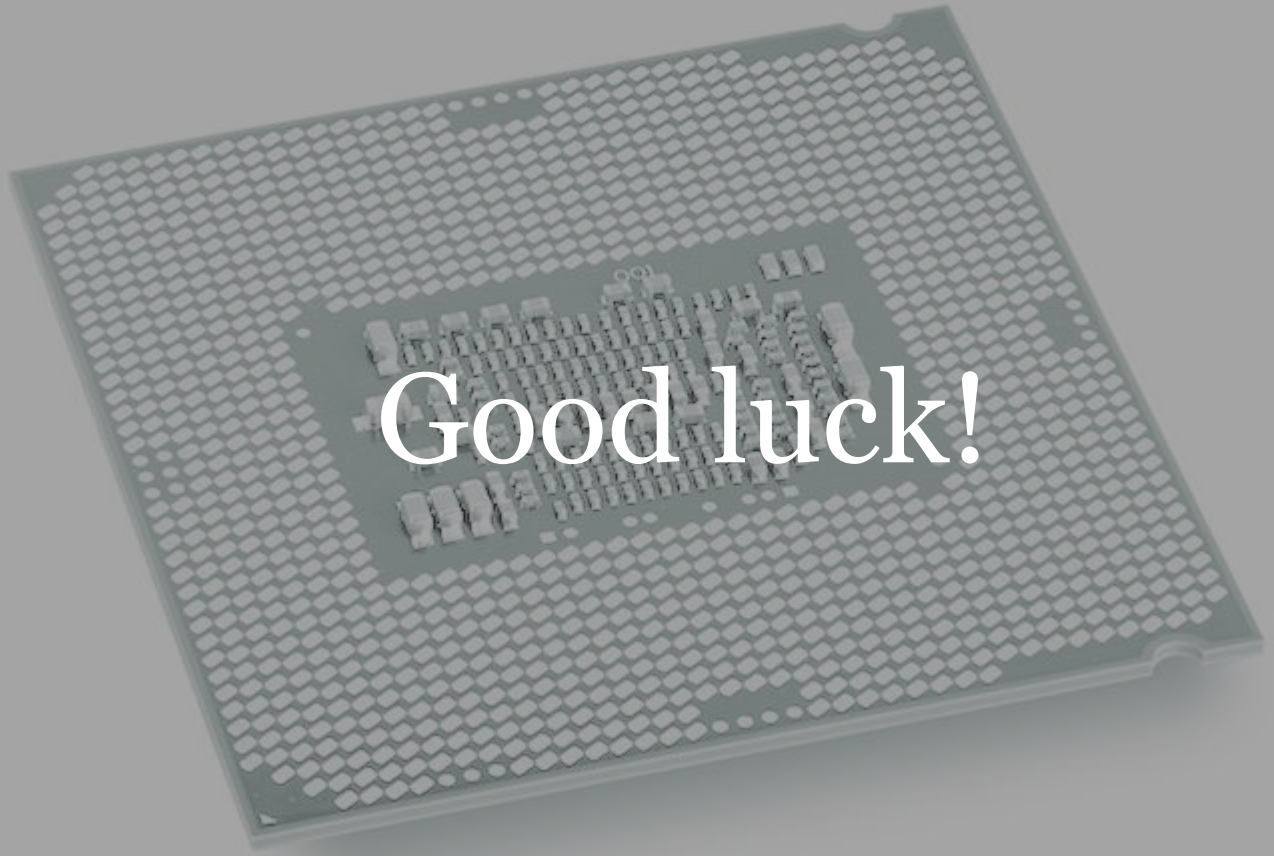
Task 01: Students read Chapter 5 in the book «Computer Organization and Design» to write detailed specifications on

- Number of bits and direction of each signal on Cache Controller FSM
- Conditions for the state transition on the FSM
- So on

Task 02: Develop VHDL Codes For Your Cache Controller

Task 03: Develop VHDL TestBench & Simulate Your Cache Controller

Task 04: Write Your Project Report



Good luck!