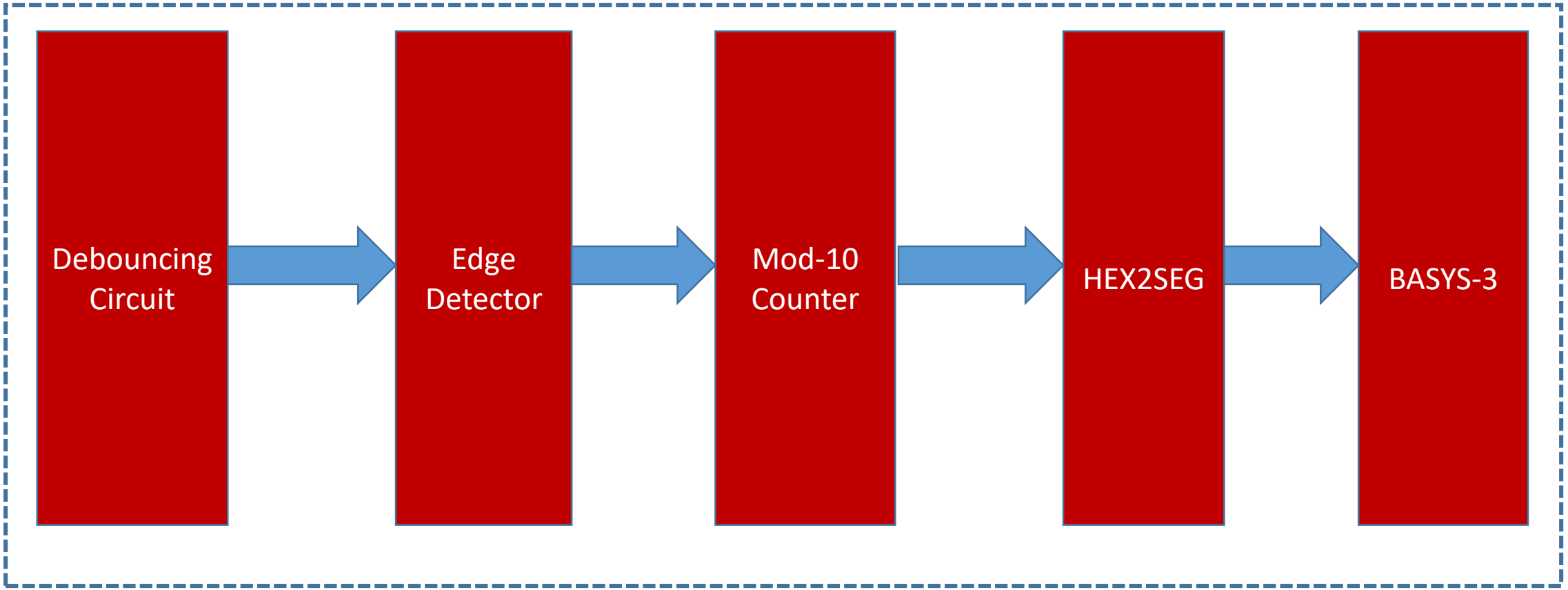
Course Project: Debouncing Test System

DDV3101 – Computer Architecture & VHDL Programming

Overall Project

In this project, students design the **de-bouncing** circuit and the **edge detector** circuit using the **finite state machines** (the reference designs are found in the textbook). These two circuits are combined with a **mod-M counter** and the **hex2seg circuits** to produce a queue generating system. Each time a user presses the push button (on BASYS-3), the counter increases its value a unit, and the current value of the counter is displayed on the seven leg segments on the BASYS-3 Board.

Overall Project



The block diagram of the queue generating system

Tasks

- **Task 01:** Develop and test the Debouncing circuit.
- **Task 02:** Develop and test the edge detector cicruit.
- **Task 03:** Integrate Debouncing and the edge detector circuits with the mod-M counter and Hex2Seg to produce the queue generating system
- **Task 04:** Create the XDC file and pin planning to test your system on BASYS-3
- **Task 05:** Write a short report for this project including the guideline of your design project
- **Task 06:** Deliver your project report together with your source codes

Deadline & Submission

- **Deadline**: Week 47 – 20/11/2020 Kl 23:59
- **Submission:** Canvas – Open for submission soon.