श्री गणेशाय नमः

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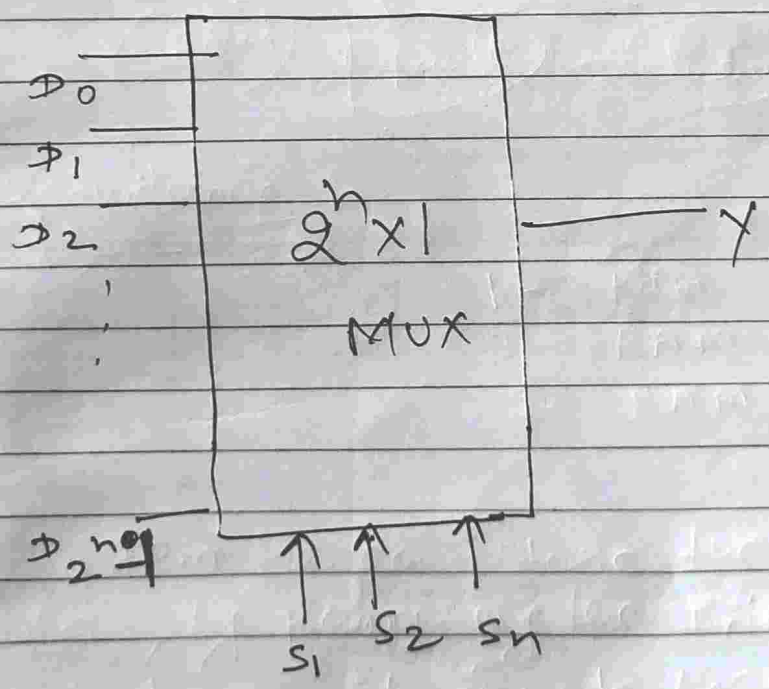
Multiplexer is a combinational logic circuit used to select only one input among several inputs based on selection lines.

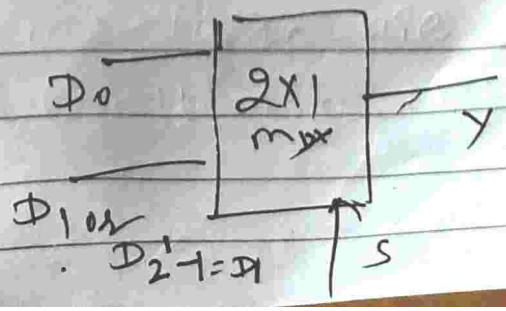
This can be act as digital switch

This is also called as data selector

For a multiplexer there can be 2^n inputs, n selection line (n is here selection line) & only one o/p.



example- 2x1 mux Design.



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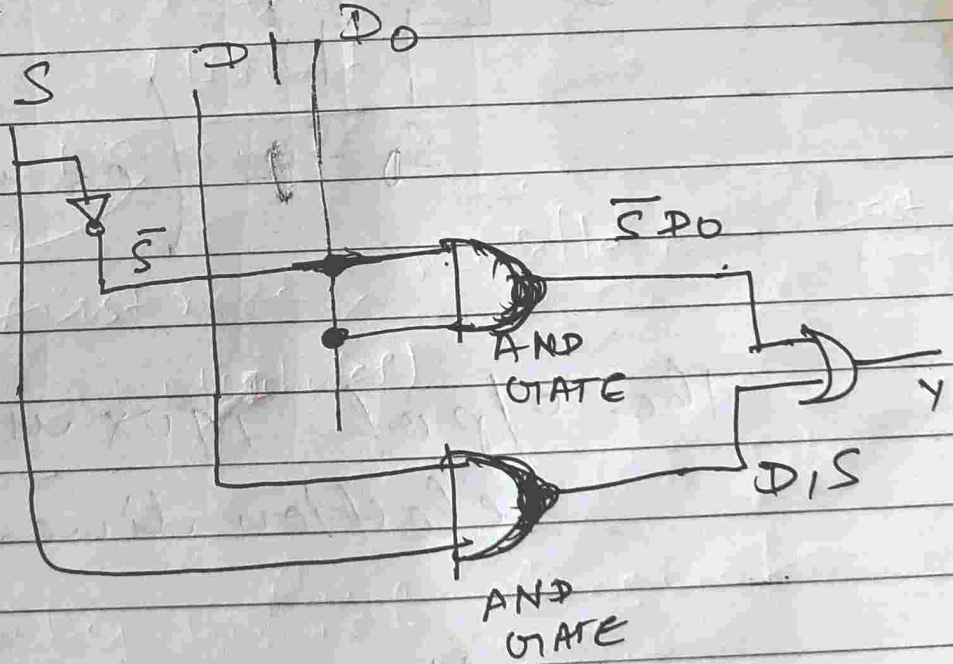
S	Y
0	D_0
1	D_1

Y output is depends upon selection input (S).

$S = 0 \Rightarrow \bar{S}$

$$Y = D_0 \bar{S} + D_1 S.$$



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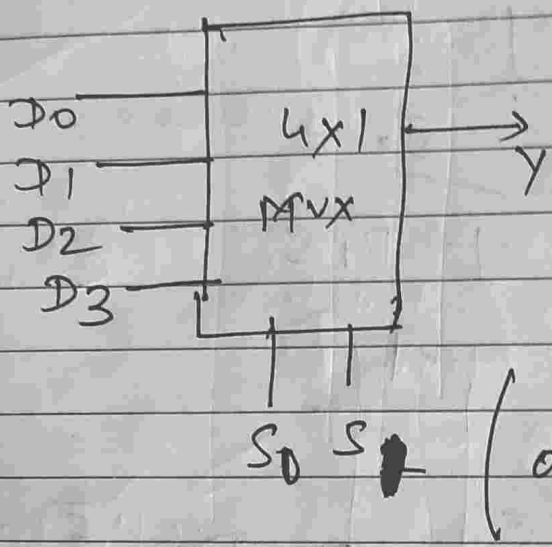
ex- 4×1 mux

$= 2^2 \times 1$ MUX

here $n = 2$

* ⇒ n = selection input (say S_0, S_1) and 4 input D_0, D_1, D_2, D_3



(or we can say S_1 and S_2)

The o/p of MUX is dependent upon selection lines (not inputs D_0 D_1 D_2 D_3)

Truth table →

S_0	S_1	Y
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

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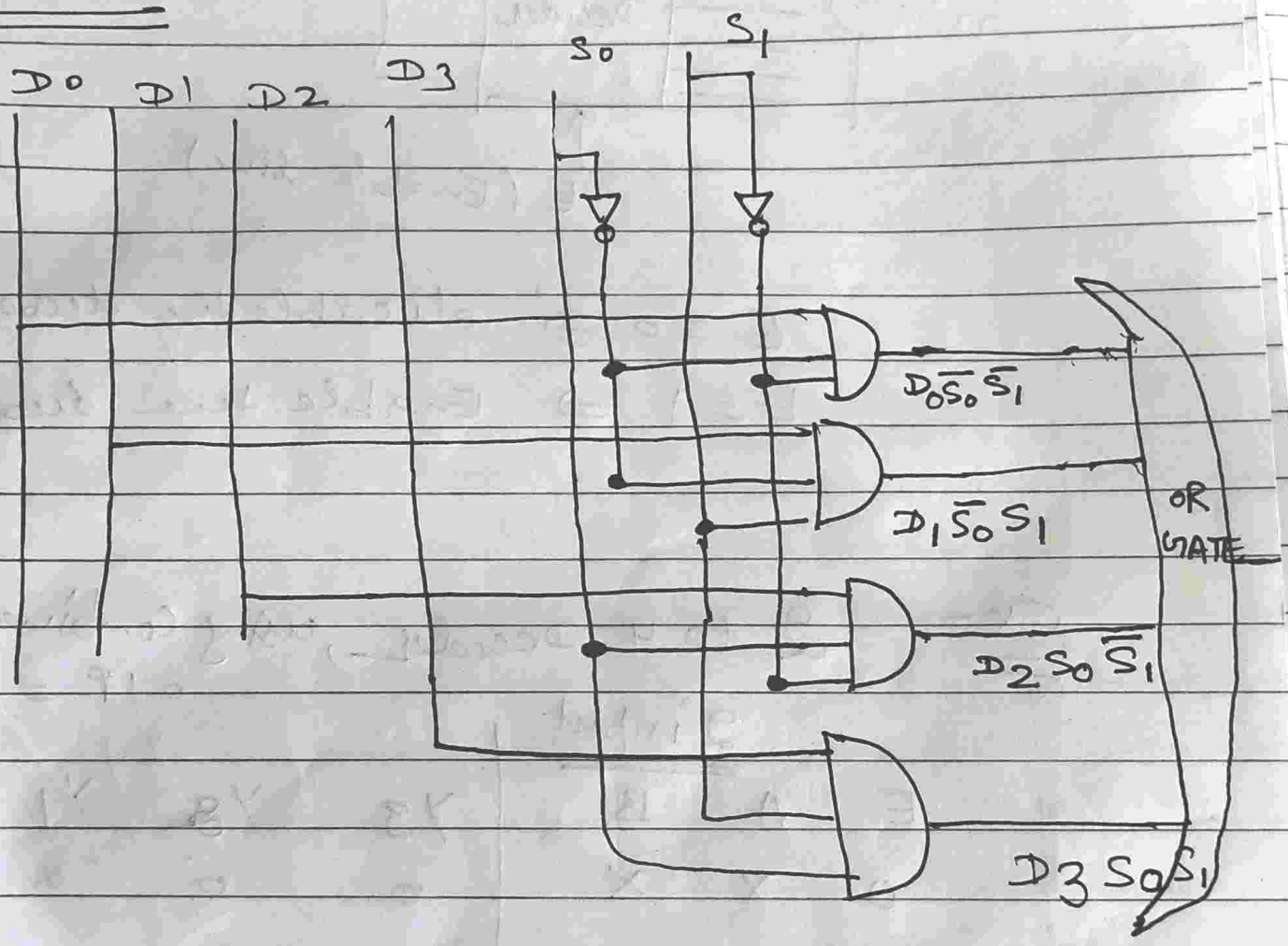
$$Y = D_0 \bar{S_0} \bar{S_1} + D_1 \bar{S_0} S_1 + D_2 S_0 \bar{S_1} + D_3 S_1 S_0$$

This is the expression for 4x1 mux

Logic Ckt:



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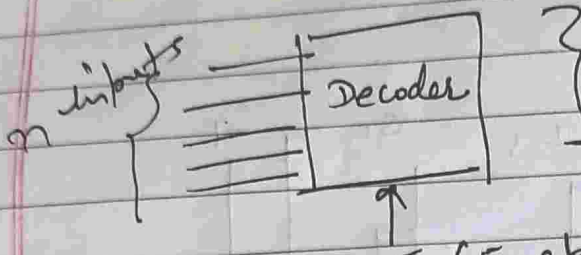
Decoders

Decoder is a multible-input, multiple-output logic circuit which decodes n inputs into 2^n possible o/ps.



E = 0 ⇒ disable the decoder
E = 1 ⇒ Enable the decoder

Ex- 2 to 4 Decoder, using combinational ckt.

o/p = $2^{2(\text{inputs})} = 4$

2 input						
E	A	B	Y_3	Y_2	Y_1	Y_0	
0	X	X	0	0	0	0	
1	0	0	0	0	0	1	→ Enable Y_0 line
1	0	1	0	0	1	0	
1	1	0	0	1	0	0	
1	1	1	1	0	0	0	

* at a time only one op line will enable as input is given
* o/p line will be enable only when E = 1

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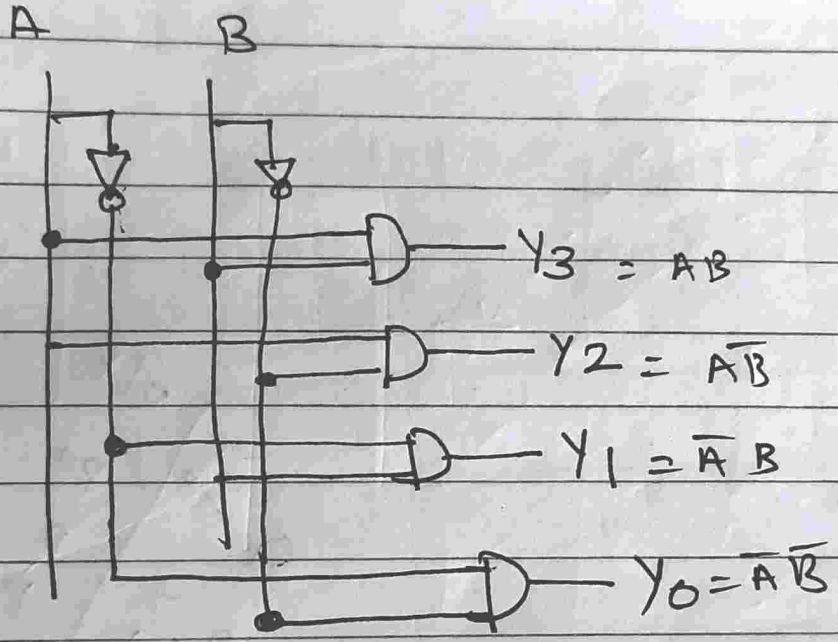
$Y_3 = AB$

$Y_2 = A\overline{B}$

$Y_1 = \overline{A}B$

$Y_0 = \overline{A}\,\overline{B}$



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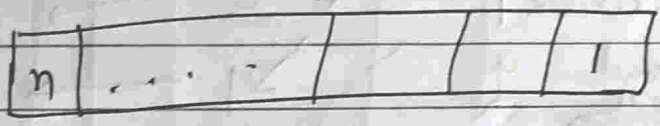
Register → it is the nearest Memory of a computer system.
(Memory nearest to CPU)

- Registers are made by using flip-flops. (ex- D-Flip flop)
- if a register having n bit size which basic meaning is that it use n flip flop.



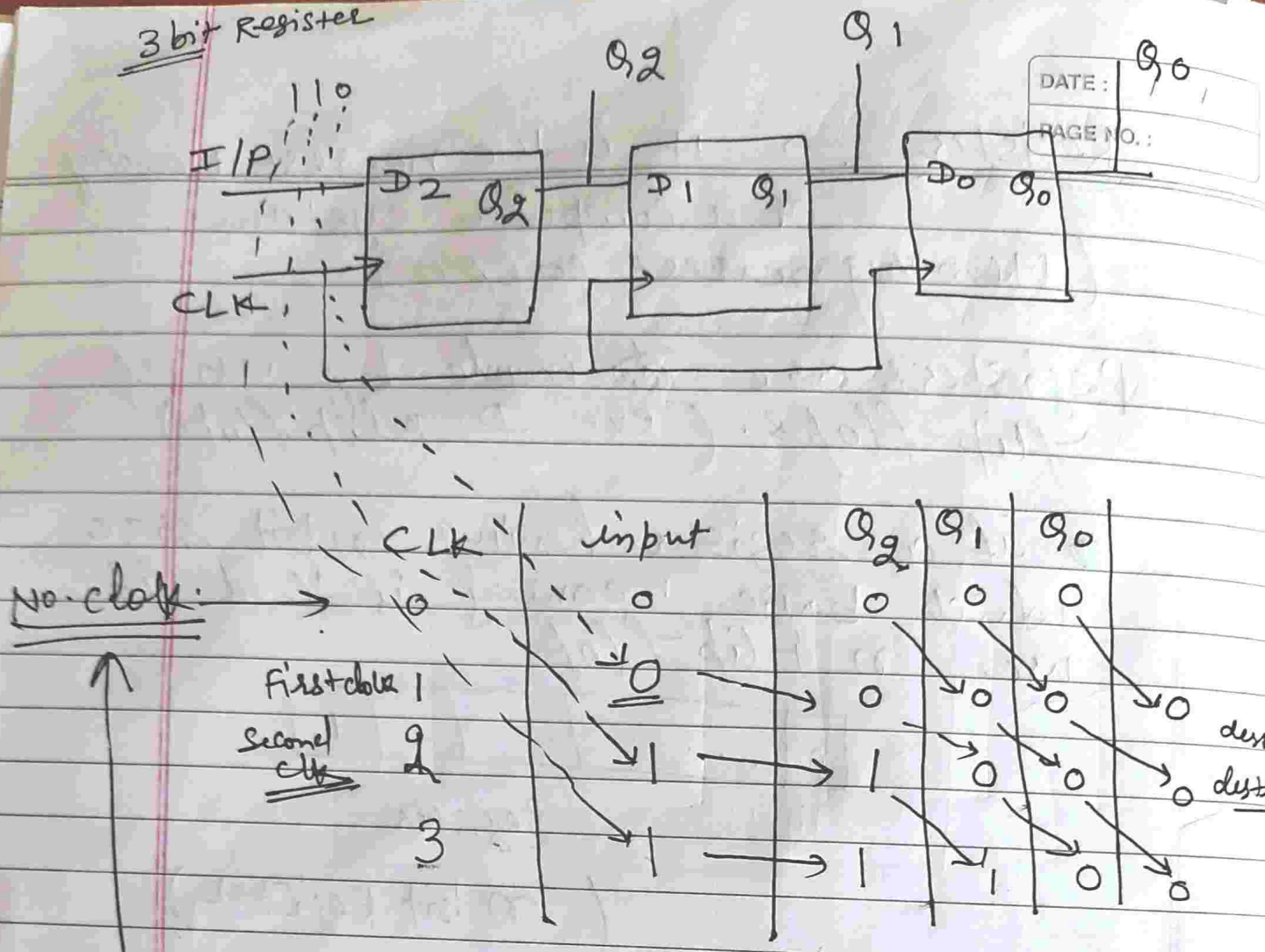
Register
(n bit Register)

These can be classified as.

→ serial in parallel out shift register
→ serial in serial out ,,

- To design the registers we use D Flip flop Because, the op of D Flip is the input that we provide to it.
Size of Register decides, the no. of Flip-flop required to design it.

3 bit Register



as the clock are applied all flip-flop Transfer their input to o/p.

* No. clock then Shift register Contain 000.

when apply the clock then the flip-flop come in working.

in D flip-flop, when we apply the clock then it gives the output, whatever input we apply

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* from the table we can see that the data is stored in register after 3 clock pulse

Total time taken to store 3 bits if clock puls are T sec.

sol:- 3 bit
3 clock pulse = 3T

, each clock = T sec = 3 sec

total time = N × T → number of bit
= 3 × T

if T = 3 sec ⇒

total time = 3 × 3 sec
= 9 sec

* In serial in, parallel out shift registers, we are giving input as serially and observing our output parallelly.

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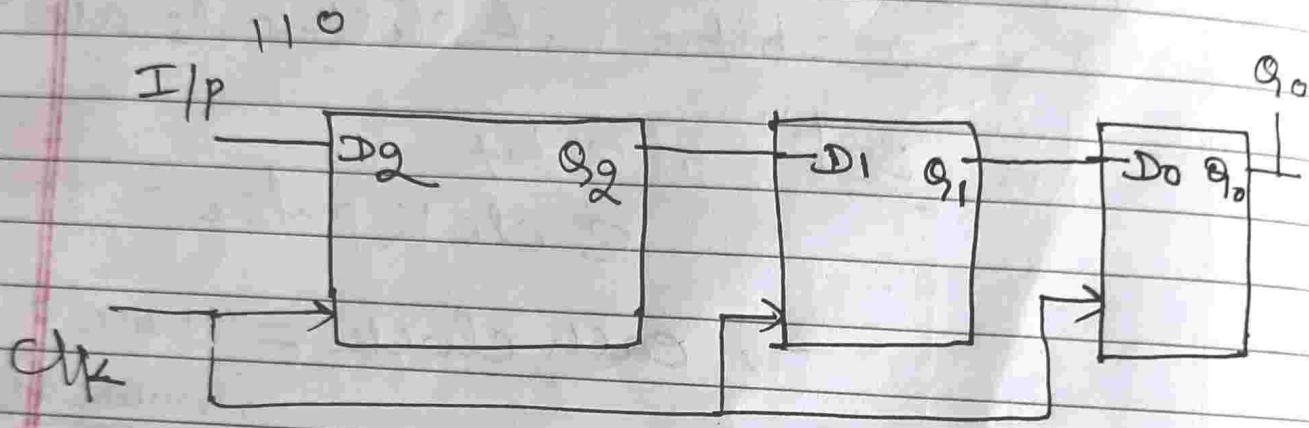
serial in serial out shift register

in this types of register we are giving input serially and we are observing o/p as serially.



clk	input	Q_2	Q_1	Q_0
0	0	0	0	0
1	0	0	0	0
2	1	1	0	0
3	1	1	1	0
4	0	0	1	1
5	0	0	0	1

destroy

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Time required in serial in serial out

(S-S)

$$\text{time} = [N + N-1]\,T$$

$$= [2N-1]\,T$$

here N → number of bits

T → clock duration

Q. How much time we required to get the serial in parall out data. (N = 3 bits) and T clock pulse = 2 ms.

$$\text{time} = NT$$

$$= 3 \times 2\ \text{ms} = 6\ \text{ms}$$

Q. How much time we required to get the serial in serial o/p. for register (data)

$$\text{time} = [N + N-1]\,T$$

$$= [2N-1]\,T = [2\times 3 - 1]\,T$$

$$= 5T$$

$$= 5 \times 2 = 10\ \text{sec.}$$