*מגיש: עודד יוסף, 203795851*

מרצה: ד"ר בנימין אברמוב

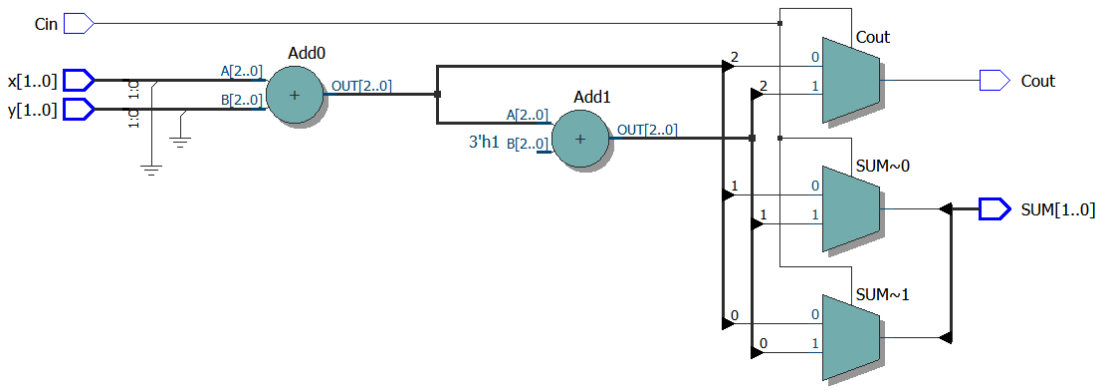
08/08/18

# עבודת הגשה 1 – Verilog

<u>מודל ראשון – הקוד במלואו:</u>

```
module Carry_Select_Adder(x,y,Cin,Cout,SUM);
parameter N=1;
input [N:0]x;
input [N:0]y;
input Cin;
output Cout;
output [N:0]SUM;

wire [N:0]s_zero;
wire [N:0]s_one;
wire cin_zero;
wire cin_one;
//adder//
assign {cin_zero,s_zero}=x+y+1'b0;
assign {cin_one,s_one}=x+y+1'b1;
//mux//
assign Cout = (Cin)?cin_one:cin_zero;
assign SUM = (Cin)?s_one:s_zero;
endmodule
```

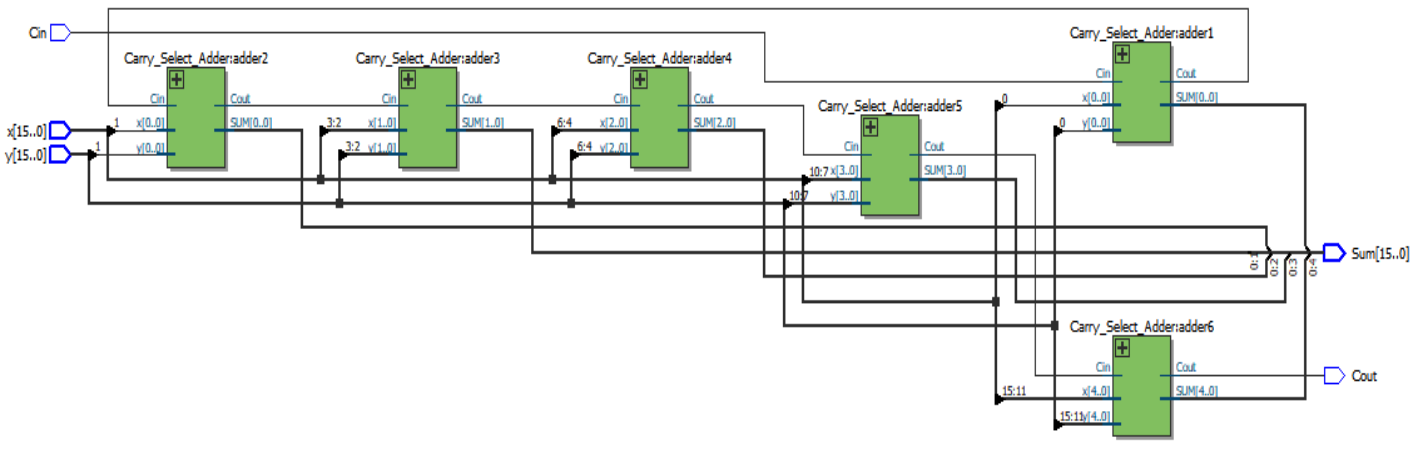
**<u>RTL View:</u>**



מודל שני-הקוד במלואו:

```
module Adder16Bit(x,y,Cin,Cout,Sum);
input Cin;
input [15:0]x;
input [15:0]y;
output [15:0]Sum;
output Cout;

wire carry1;
wire carry2;
wire carry3;
wire carry4;
wire carry5;      //5 different wires of carry's

defparam adder1.N=0;
Carry_Select_Adder adder1 (.x(x[0]),.y(y[0]),.Cin(Cin),.Cout(carry1),.SUM(Sum[0])); //LSB//

defparam adder2.N=0;
Carry_Select_Adder adder2 (.x(x[1]),.y(y[1]),.Cin(carry1),.Cout(carry2),.SUM(Sum[1]));

defparam adder3.N=1;
Carry_Select_Adder adder3 (.x(x[3:2]),.y(y[3:2]),.Cin(carry2),.Cout(carry3),.SUM(Sum[3:2]));

defparam adder4.N=2;
Carry_Select_Adder adder4 (.x(x[6:4]),.y(y[6:4]),.Cin(carry3),.Cout(carry4),.SUM(Sum[6:4]));

defparam adder5.N=3;
Carry_Select_Adder adder5
(.x(x[10:7]),.y(y[10:7]),.Cin(carry4),.Cout(carry5),.SUM(Sum[10:7]));

defparam adder6.N=4;
Carry_Select_Adder adder6
(.x(x[15:11]),.y(y[15:11]),.Cin(carry5),.Cout(Cout),.SUM(Sum[15:11]));  //MSB//

Endmodule
```

**RTL View:**



**Test bench – הקוד במלואו**

```
`timescale 1ns / 100 ps
module Adder16Bit_tb();
reg Cin;
reg [15:0]x;
reg [15:0]y;
wire [15:0]Sum;
wire Cout;

Adder16Bit UUT (.Cin(Cin),.x(x),.y(y),.Sum(Sum),.Cout(Cout));

initial
begin

x=16'b1001100101101100;
y=16'b1010101010101010;
Cin=1'b0;

#100;

x=16'b1101110100001100;
y=16'b1100111100100010;
Cin=1'b1;

#100;

x=16'b1111111100000000;
y=16'b0000000011111111;
Cin=1'b0;

#100;

$stop;
end
endmodule
```