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ORIGINAL ARTICLE

Increasing Efficiency and Power Factor for Power Supplies Using Parallel Flyback Converter

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Abstract
Increasing of ac/dc power supply, losses, and harmonic problems arise and power factor decrease due to the presence of the converter. Therefore, a fast, accurate and high-power supply performance became mandatory. In this paper, a new topology of dual flyback converters operated in parallel is introduced to increase the power factor, decrease the total current harmonic distortion and reduce the losses. The first flyback converter is utilized as dc/dc stage used to regulate the output voltage by adjusting the duty cycle. While the second flyback converter is utilized as ac/dc stage, it is also used for the power factor correction and reducing the harmonics. The second flyback converter generates the input current to be in phase with the input voltage by regulating the variable frequency and switching period keeping the switching on-time fixed. This topology improves the voltage regulation even if the input voltage is reduced by approximately 60%, small circuit size, improving power factor, reducing the total harmonic distortion, and increased efficiency. Finally, a small-scale prototype platform that has the ability to deal with universal input 80–260 V_{rms}, enhancing the supply performance, is carried out. The measurements have verified the theoretical analysis to check the effectiveness of the proposed system.

Keywords Flyback converter · Total harmonic distortion · Power factor correction

1 Introduction

A widespread using of renewable energy systems, smart devices, electric vehicles, electrical appliances, industrial applications and lighting systems, led to large-scale use of ac/dc power supply. Generally, this reduces the power factor (PF), increases the total harmonic distortion (THD), increases the losses, leads to overheating in transformers, existence a current in the neutral conductor, increases the possibility of occurring electrical resonances in the power system, and a distortion of the line voltage via the line impedance [1].

1.1 Related Works

Recently several circuits have been developed for the power factor correction (PFC). A high-PF LED driver is introduced in [2] by redesigning the converter parameters to increase the efficiency of the integrated buck-flyback converter. Flyback converter modeling of a cascade switching structure is proposed in [3] to achieve startup time in the deeply dimmed phase-cut LED driver. A stable power converter design for LED lamps using a converter current-controlled is introduced in [4]. Low dynamic resistance has been used to drive the current in the LED. Authors in [5] discussed the power quality mainly harmonics and the voltage sags which generated from the LED lamps converter. The harmonic distortion in this research was reduced by combining different types of LED lamps. Authors in [6, 7] introduced the same methodology for a PFC and increase the efficiency of a flyback converter which can deal with either utility power or PV power. This is performed by making the converter operate at a maximum power point tracking if it is low efficiency. Authors in [6] introduced a modified-SEPIC embedded-boost converter, which can deal with either utility power or PV power to serve as a high-brightness LED

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driver and battery charger. Also, the proposed converter can perform PFC for universal line input. Authors in [8–10] proposed a method to increase the dc/dc flyback converter efficiency by composing it with a resonant active-clamp circuit. This method limits the voltage stress and provides zero voltage switching turn-on and turn-off of the power switches. While, authors in [9, 10] used two series converters to double the power capacity, the proposed model consists of a low-pass filter, a diode rate and two flyback adapters that entangled operated with a 180° phase shift. Even though research in [11–13] introduced two flyback converter as in [9, 10] while they used a parallel connection of the two different output flyback converter, the two converters are classified into low power and high power flyback converters as a dc/dc converter and the input voltage range for both converters is low.

To sum up, there are two approaches for active PFC, a single flyback converter as introduced in [1–7] and a two-stage approach which normally consists of a boost converter as in [8–11]. The main disadvantage of the two-stage scheme is the high cost and lower efficiency. On the other side, single-stage approaches use the simplest flyback converter, which is not able to tightly regulate the output voltage.

1.2 Contribution

To integrate the advantages of both methods and avoid defects, this paper introduced a dual parallel flyback converter where the two converters work together at the same time to maintain the output voltage constant as well as improve PF and reduce THD. The main objective of converter-I is to control the output voltage against the waveform disturbance by change the switching on-time and off-time period while maintaining the switching period constant, the dynamic response of converter-I is very fast. On the other hand, converter-II controls the input current to be in the same phase angle of input voltage and makes the total harmonic distribution equal to zero thus the PF is unity. Converter-II controls the current using a variable frequency and variable switching period while maintaining the switching on-time fixed, the dynamic response of converter-II is slower than converter-I. This proposed topology is desired to regulate the output voltage even if the input voltage decreases by 60% and reduces product cost. Also, the circuit efficiency is increased by switching the active switch at zero crossing modes without an active clamp circuit and recycling the stored energy in the leakage inductance of the inductor. Besides, the near-unity PF and low THD are achieved. Finally, small-scale parallel flyback converters prototype with a universal input 80–260 V_{rms} and the output is 24 V, 10 A is built; the circuit response analysis for sudden load changes is tested. The circuit was tested on two types of loads, a matrix of LEDs and charging a set of batteries. The experimental results have verified the correctness and effectiveness of the theoretical analysis.

Finally, the main contribution of this paper is summarized in the following points.

- This paper introduced a new topology of a parallel flyback converter. The first converter used to regulate the output voltage. However, the second converter is used to improve the PF and reduce THD by generating the input current and input voltage with zero displacements.
- The introduced circuit is divided into two control categories. The first controller deals with converter-I derived by integrating two PWM converters while the second controller deals with converter-II derived by integrating a PWM converter and a half-bridge resonant converter.
- The controller in converter-I maintains the switching period constant but the switching on-time and off-time period are variables. While the controller in converter-II using variable frequency and variable switching period while switching on time is fixed. The dynamic response of the converter-I is faster than the converter-II.
- The introduced model increases operating efficiency by operating the two converters at discontinuous current mode, as well as recovering the energy stored in the leakage inductance of the coupled inductor.

1.3 Organization

The paper is organized into five sections. Section 2 introduces the system topology and control. Section 3 introduces a mathematical design of each element in the proposed circuit. Section 4 introduces the proposed system waveforms and flowchart. Finally, to ensure the proposed system capabilities, Sect. 5 illustrates a simulation and a prototype model result.

2 Proposed System Description

The parallel flyback converters consist of a diode, capacitor, and two flyback converters as shown in Fig. 1. Converter-I with a capacitor is regulated the output voltage. While converter-II is used to fulfill a PFC by making input current

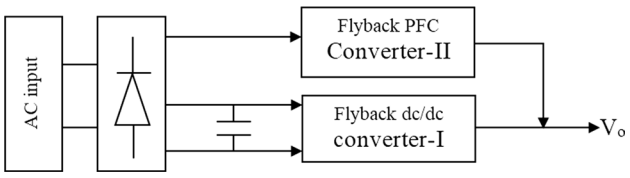


Fig. 1 A simplified parallel flyback converters scheme

in phase with the input voltage and regulating dc-output voltage.

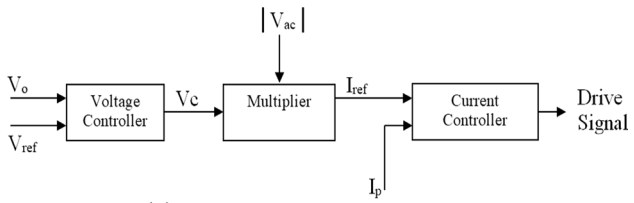
In the proposed approach, two separate control stages are introduced as in Fig. 2. The output voltage V_0 is an instantaneous voltage and the input voltage V_{ac} is the rms voltage.

3 Proposed Modeling Design

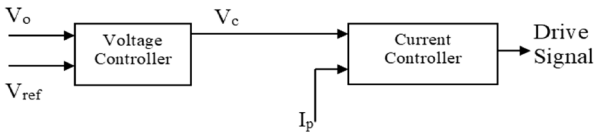
A parallel flyback converter is divided into two separate flyback converters and controls. The main task of converter-I is to achieve the load requirement and converter-II is to satisfy the supply requirement. Both converters are working in parallel to achieve high power capacity. In this section, construct a mathematical analysis of each converter with its control.

3.1 Flyback Converter-II PFC Design

The flyback converter is classified according to the current modes, continuous mode [14], discontinuous mode [15] and critical mode [16]. In continuous mode, stress and the losses are increased on the circuit elements, on the contrary in discontinuous mode; the system avoids these problems due to zero voltage crossing. In the critical mode, the current can be continuous or discontinuous by inserting a variable inductance in the circuit to control the continuity of the current. The converter in the three operation modes can be controlled by using, classic-PWM [17] or transition-PWM [18]. Classic-PWM based on fixed frequency mode, the main advantage of this type is a simple configuration, ease of control, and low current stress. But the output voltage is low and the PF value doesn't achieve the objective target. On the contrary, transition-PWM base on a variable frequency and switching period with maintain the switching on-time fixed. The main advantage of this type is high PF and output voltage.



(a) Flyback PFC converter-II control



(b) Flyback converter-I control

Fig. 2 Control block diagram of the flyback converter

To achieve the best performance and high-PF, this paper introduced two flyback converter connected in parallel. The first converter-I is a classic-PWM to control the output voltage. While converter-II as shown in Fig. 3 is a transition-PWM used to achieve PFC, it controls the input current to be in the same phase voltage sequence thus the PF is unity. In this paper, the controller is designed to operate at a discontinuous mode. The main objective of the analysis is to achieve high-PF and minimum THD, therefore the system controller always works at the best performance.

There are three assumptions are considered to deduce the mathematical model for the PFC based transition mode; the input voltage is pure sinewave, a fixed output error of the amplifier (V_{comp}), ideal coupling and unity PF of the transformer.

$$V_{in}(t) = \widehat{V_p}\sin(\theta) \tag{1}$$

$$I_p(t) = \widehat{I_p}\sin(\theta) \tag{2}$$

$$I_s(t) = n\widehat{I_p} \tag{3}$$

where: $V_{in}(t)$ is the rectified input voltage; $\widehat{V_p}$ is the peak input voltage; $I_p(t)$ is the rectified input current; $\widehat{I_p}$ is the peak primary current; $I_s(t)$ is the secondary current; n is the transformer's turns ratio; and θ is the phase angle "$\theta = 2\pi ft$" and f is the line frequency (50 Hz).

In a transition controller, the duty cycle and switch-on are variable while switch-off is constant [6]. Therefore; these periods must be calculated as a function in the voltage and current.

$$T_{on} = \frac{L_p I_p(t)}{V_{in}(t)} \tag{4}$$

$$T_{off} = \frac{L_s I_p(t)}{(V_{out} + V_f)} = \frac{L_p \widehat{I_p}|\sin(\theta)|}{n(V_{out} + V_f)} \tag{5}$$

$$V_R = n(V_{out} + V_f) \tag{6}$$

$$T = T_{on} + T_{off} = \frac{L_p \widehat{I_p}}{\widehat{V_p}}\left[1 + \frac{\widehat{V_p}}{V_R}|\sin\theta|\right] \tag{7}$$

$$f_s = \frac{1}{T} \tag{8}$$

$$D = \frac{T_{on}}{T} = \frac{1}{1 + \frac{\widehat{V_p}}{V_R}|\sin\theta|} \tag{9}$$

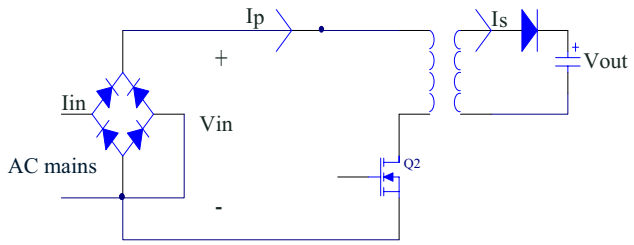


Fig. 3 Circuit diagram for a PFC flyback converter

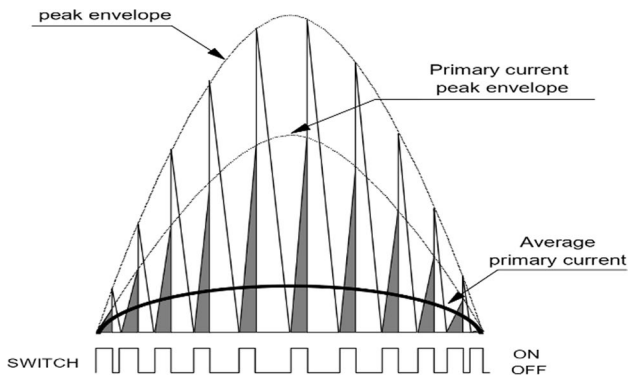


Fig. 4 High-PF current waveforms

$$K_v = \frac{\widehat{V_p}}{V_R} \tag{10}$$

where:T_{on} is the on-time of the power switch; L_p is the inductance of the transformer's primary winding; T_{off} is the off-time of the power switch; L_s is the inductance of the secondary winding; V_{out} is the output voltage of the converter (supposed to be a regulated dc value); V_f is the forward drop on the output diode; T is the switching period; V_R is the reflected voltage; f_s is the switching frequency; D is the duty cycle; K_v is the proportion of reflected voltage for the input voltage.

The relation between the primary current and the secondary current according to switching of the circuit is shown in Fig. 4. A triangular primary current shape is passing during the switching on.

According to Fig. 4 during each half-cycle, the height of these triangles varies with the instantaneous line voltage and their width is constant, but they are spaced out by a variable amount of switch-off period [19]. The supply current $I_{in}(t)$ can be computed as follows:

$$I_{in}(t) = \frac{D}{2} I_p(t) = \frac{\widehat{I_p}}{2} \frac{|\sin\theta|}{(1 + K_v|\sin\theta|)} \tag{11}$$

The average current value can be distinguished using a filter of the switching frequency [20]. To determine the distortion rate, the supply current wave must be drawn at different values of K_v as shown in Fig. 5. The current would be sinusoidal at $K_v = 0$, while when $K_v > 0$ the wave is distorted. The ideal case $K_v = 0$ is not realistic, it required the reflected voltage to tend to infinity and unity PF cannot be achieved unless boost converter is used.

Only half-wave and absolute value from $|\sin\theta|$ are considered. Therefore, the input power P_{in} can be calculated as follows:

$$P_{in} = \bar{V}_{in}(t)\bar{I}_{in}(t) = \frac{\widehat{V_p}\widehat{I_p}}{2} \frac{\overline{|\sin\theta|}^2}{(1 + K_v|\sin\theta|)} \tag{12}$$

Input power change according to the value of K_v. Therefore, for simplified we can assume the following function.

$$F^2(K_v) = \frac{\overline{|\sin\theta|}^2}{1 + K_v|\sin\theta|} = \frac{1}{\pi}\int_0^{\pi} \frac{|\sin\theta|^2}{1 + K_v|\sin\theta|} d\theta \tag{13}$$

Figure 6 represents a curve of the imposed function in Eq. 13. For simplification of the practical design, a curve fitting is applied to the curve in Fig. 6. The equation of curve fitting [21] can be representing as a function of variable x where $x \geq 0$ as shown in Eq. 14.

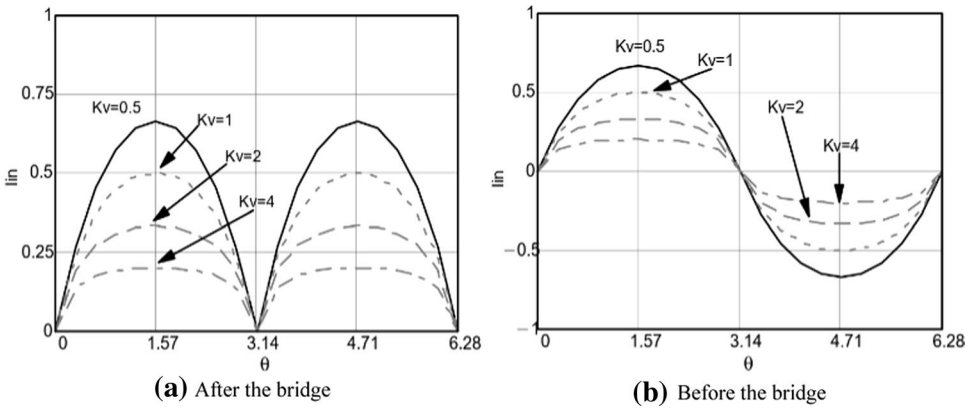


Fig. 5 Supply current at different values of K_v diagram

(a) After the bridge **(b)** Before the bridge

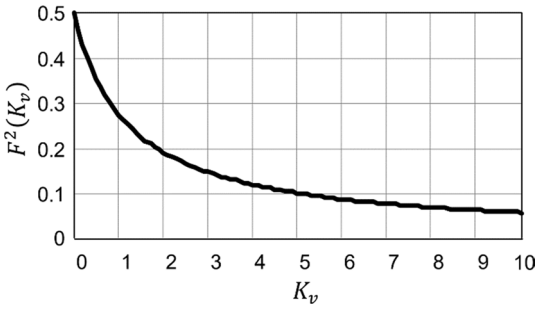


Fig. 6 Characteristic functions $F_2(K_v)$ diagram.

$$F^2(K_v) = \frac{0.5 + 1.4^{-3}x}{1 + 0.815x} \tag{14}$$

To calculate the primary side loss and to distinguish between ac and dc losses in the transformer, the primary *rms* current (I_{rmsp}) and the primary current (I_{dcp}) must be calculated as in Eqs. 15 and 16 respectively.

$$I_{rmsp} = \sqrt{\frac{D}{3}\,\overline{\hat{I}_p^{\,2}(\theta)}} = \hat{I}_p\sqrt{\frac{1}{3}\frac{\overline{|\sin\theta|^2}}{(1 + K_v|\sin\theta|)}} = \hat{I}_p\sqrt{\frac{F^2(K_v)}{3}} \tag{15}$$

$$I_{dcp} = \overline{I_{in}(t)} = \frac{1}{2}\hat{I}_p\,\frac{\overline{|\sin\theta|}}{1 + K_v|\sin\theta|} \tag{16}$$

For simplification, the function $F^1(K_v)$ is assumed and approximation best fitting rather than the exact expression as displayed in Eq. 17.

$$F^1(K_v) = \frac{\overline{|\sin\theta|}}{1 + K_v|\sin\theta|} = \frac{1}{\pi}\int_0^{\pi}\frac{|\sin\theta|}{1 + K_v|\sin\theta|}d\theta \cong \frac{0.637 + 4.6^{-3}x}{1 + 0.927x} \tag{17}$$

The output dc current ($I_o(t)$) of the converter, is an essential design data. $I_s(t)$ is the complementary triangle of $I_p(t)$ with a double line frequency during the switching cycle. $I_o(t)$,$\hat{I}_s$ and the total secondary rms current (I_{rmss}) can be deduced as follows:

$$I_o(t) = \frac{1}{2}I_s(t)(1 - D) = \hat{I}_s K_v\frac{|\sin\theta|^2}{1 + K_v|\sin\theta|} \tag{18}$$

$$\hat{I}_s = \frac{2I_{out}}{K_v F^2(K_v)} \tag{19}$$

$$I_{rmss} = \sqrt{\frac{(1 - D)}{3}\,\overline{\hat{I}_s^{\,2}(\theta)}} = \hat{I}_s\sqrt{\frac{K_v}{3}\frac{\overline{|\sin\theta|^3}}{1 + K_v|\sin\theta|}} = \hat{I}_p\sqrt{K_v\frac{F^3(K_v)}{3}} \tag{20}$$

$$F^3(K_v) = \frac{\overline{|\sin\theta|^3}}{1 + K_v|\sin\theta|} = \frac{1}{\pi}\int_0^{\pi}\frac{|\sin\theta|^3}{1 + K_v|\sin\theta|}d\theta \cong \frac{0.424 + 5.7^{-3}x}{1 + 0.826x} \tag{21}$$

The PF can be expressed in Eq. 22, and the first harmonic current can be deduced from Eq. 23. It is noticed that $I_{rms} \notin I_{rmsp}$ as in Eq. 15, while Eq. 22 I_{rms} refers to line frequency quantities. Therefore, I_{rms} is the *rms* value of $I_{in}(t)$ as in Eq. 24

$$PF = \frac{P_{in}}{S_{in}} = \frac{V_{rms}I^1_{rms}}{V_{rms}I_{rms}} = \frac{I^1_{rms}}{I_{rms}} \tag{22}$$

$$I^1_{rms} = \frac{P_{in}}{V_{rms}} = \sqrt{2}\frac{P_{in}}{\widehat{V_p}} \tag{23}$$

$$I_{rms} = \sqrt{\overline{I_{in}^2}} = \frac{1}{2}\hat{I}_p\sqrt{\frac{1}{\pi}\int_0^{\pi}\left[\frac{|\sin\theta|}{1 + K_v|\sin\theta|}\right]^2 d\theta} \tag{24}$$

where: V_{rms} is the effective line voltage; I^1_{rms} is the effective value of the first harmonic; and I_{rms} is the total rms current of the input waveform.

Figure 7 display the PF as a function in K_v. For practical use, PF can be approximated as in Eq. 25. Therefore, the best value of K_v which PF keeps quite close to 1 can be detected.

$$PF(K_v) \cong 1 - 8.1^{-3}K_v + 3.4^{-4}{K_v}^2 \tag{25}$$

3.2 Capacitor Design

The capacitor [22] is the input source to converter-I as shown in Fig. 3. To have a good performance, a slow control voltage is designed with a bandwidth lower than 100 Hz. The slow control leads to voltage distortion. Two components are found by analyzing the voltage waveform. The first one is high-frequency ripples and the second is low-frequency ripples (twice line frequency). Equivalent series resistance (R_{eq}) is responsible to eliminate the first component while

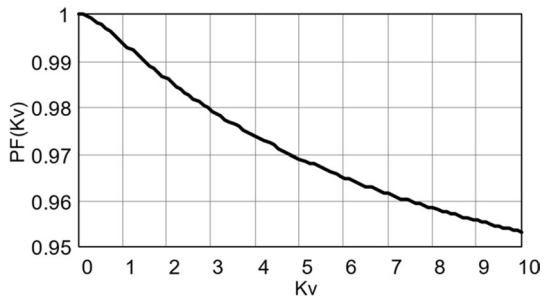


Fig. 7 Theoretical PF as a function of K_v.

the capacitor value is responsible to eliminate the second component. Therefore, a good design of the capacitor and R_{eq} must be established. Suitable value of the resistance can be computed from Eq. 26.

To design the capacitor, the second harmonic in $I_o(t)$ should be analyzed and defined as it is the more effective value. The peak value of the second harmonic in Eq. 27 is produced by applying Fourier analysis to Eq. 18. By simplified, Eq. 27 can be re-written in Eq. 29 form. Finally, the peak output voltage amplitude of the low-frequency is shown in Eq. 30

$$\Delta V_{hf} = \widehat{I}_s R_{eq} \tag{26}$$

$$I_o(\theta) = \frac{\widehat{I}_s K_v}{\pi} \int_0^{\pi} \frac{\sin^2\theta\cos 2\theta}{1 + K_v|\sin\theta|} d\theta \tag{27}$$

$$H^2(K_v) = \frac{1}{\pi}\left|\int_0^{\pi} \frac{\sin^2\theta\cos 2\theta}{1 + K_v|\sin\theta|}\right| d\theta \cong \frac{0.25 - 1.5^{-3}x}{1 + 1.047x} \tag{28}$$

$$I_o(\theta) = \widehat{I}_s K_v H^2(K_v) = 2I_{out}\frac{H^2(K_v)}{F^2(K_v)} \tag{29}$$

$$\Delta V_o = 2I_{o2}Z_{fl}C_o = \frac{1}{\pi}\frac{H^2(K_v)}{F^2(K_v)}\frac{I_{out}}{FLC_o} \tag{30}$$

where: ΔV_{hf} is the high-frequency peak to peak output ripple voltage.

3.3 Flyback Converter-I Regulator Design

Figure 8 shows the proposed PFC scheme. The output voltage is controlled through a capacitor and converter-I. While the circuit PF and THD are enhanced through flyback converter-II by making input current and voltage in phase also regulate the capacitor voltage. Inductor added to the flyback converter-I to smooth the input current.

The dc-link voltage "V_{dc}", flyback converter transformers ratio [23] "M", and current and voltage equations are shown as follows:

$$V_{dc} = \sqrt{2}V_s \tag{31}$$

$$M = \frac{V_o}{V_{dr}} \tag{32}$$

$$i_{dr} = i_{p1} + i_p \tag{33}$$

$$V_{Ldr} = L_{dr}\frac{di_{dr}}{dt} \tag{34}$$

$$V_{in} = V_{dr} - V_{Ldr} \tag{35}$$

where: V_o is the output voltage; V_{dr} is the rectified input voltage; i_{dr} is the rectified input current; i_{p1} is the flyback converter-I input current; i_p is the converter-II input current; V_{Ldr} is the input inductor voltages; V_{in} is the flyback converter-II input voltage; Q_1 and Q_2 are the MOSFET switch of both flyback converters "converters I and II" respectively; V_g is the gate voltage on the flyback transistor; D_o and D_{o1} are the output diode; and D_p is the control diode.

3.4 Transformer Design

Transformer design is one of the most complex processes in a flyback converter. Therefore, it is essential to determining the core size, and the air-gap length to achieve the desired

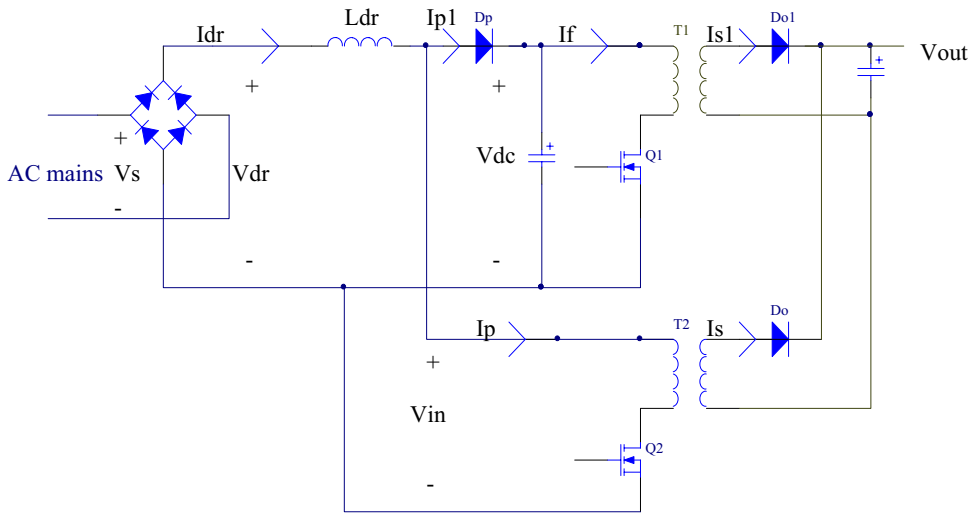


Fig. 8 A circuit diagram of a parallel flyback converter

inductance. The primary inductance and the minimum core area are estimated from the following equations.

$$L_p \le \frac{1}{2}\frac{F^2(K_{vmin})}{1+K_{vmin}}\frac{V_{PKmin}^2}{f_{swmin}.P_{inmax}} \tag{36}$$

$$A_{min} = \left[\frac{480.P_{in}}{f_{swmin}.(1+K_v).\sqrt{F^2(K_v)}}\right]^{1.585} . \left[J_H(K_v).f_{swmin} + J_E(K_v).f_{swmin}^2\right]^{0.66} \tag{37}$$

The area is a function in hysteresis losses $J_H(K_v)$ and the eddy current losses $J_E(K_v)$, whose best fit approximation are respectively [24]:

$$J_H(K_v) \approx \frac{1.87+1.26.K_v}{1+0.55.K_v}.10^{-5} \tag{38}$$

$$J_E(K_v) \approx \frac{1.88+1.06.K_v}{1+0.345.K_v}.10^{-10} \tag{39}$$

Figure 9, illustrates the required inductance and the core area at different values of K_v respectively.

4 Circuit Operation and Flow Chart

General theoretical waveforms of the parallel flyback converter for discontinuous-current mode are shown in Fig. 10. The operational sequences are as follows:

$T_0 > t > T_1$	Q_2 turn on; Q_1 is off; D_p turned off with a reverse bias; Converter-I feeds the load from V_{dc}; Converter-II feeds the load from source V_s; The current of flyback transformer does not flow simultaneously in both windings.
$T_1 > t > T_2$	Q_1 turns on; Q_2 is on; The load current from converter-I is I_f;
$T_2 > t > T_3$	Q_2 is turned off; Q_1 is on; D_p is turned to short-circuit; i_{p1} is decreased; i_{p1} is controlled by using L_{dr}.
$T_3 > t > T_4$	Q_1 turns off; Q_2 is off; D_p is turned off with a reverse bias; Flyback converter-I feed the load based on V_{dc}; The magnetization current of the two flyback transformers is discharging in the load.

The flowchart of the parallel flyback converter is displayed in Fig. 11.

5 Case Study

In this section, a practical circuit is simulated, designed and tested to verify the feasibility, accuracy, and speed of the proposed model. Power MOSFETs are used to control the input and output through varying the switching frequency, where the switching frequency up to 50 kHz. The circuit parameters are lists in Table 1. Also, from the transformer design Sect. 3.4, the transformer characteristics specification is shown in Table 2.

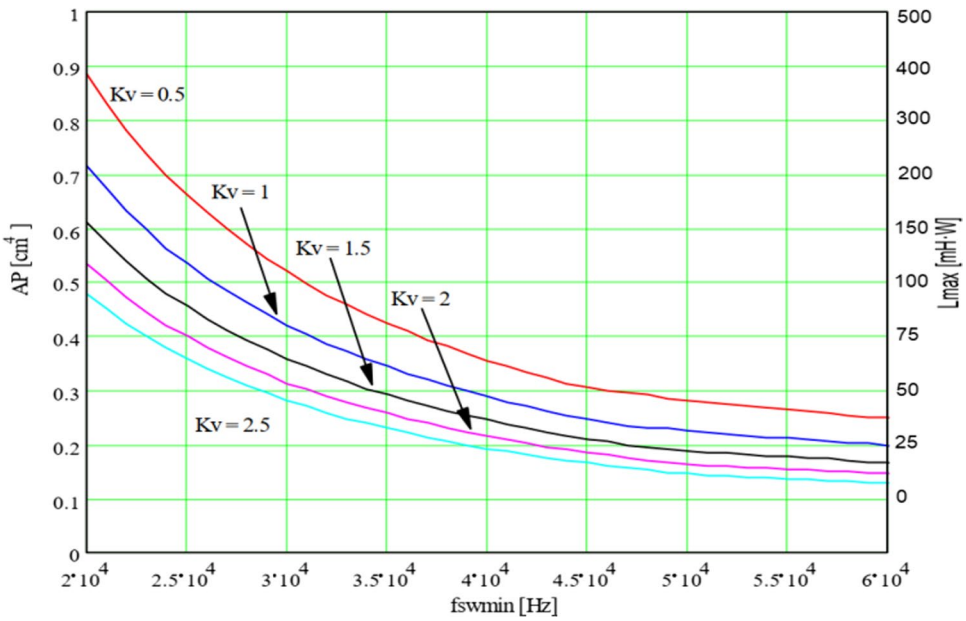


Fig. 9 Inductance and core area at different values of K_v

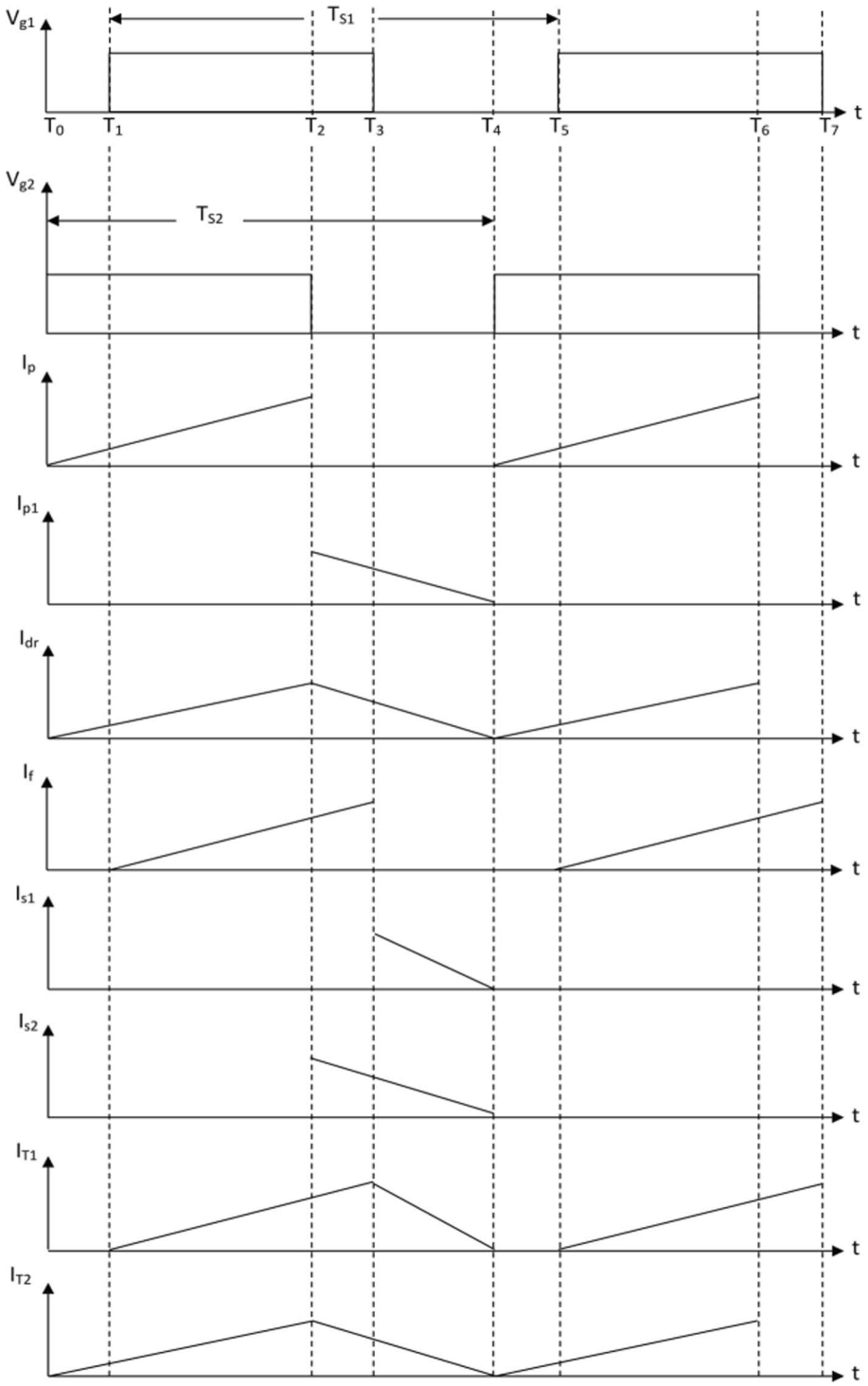


Fig. 10 Operational waveforms of the proposed topology

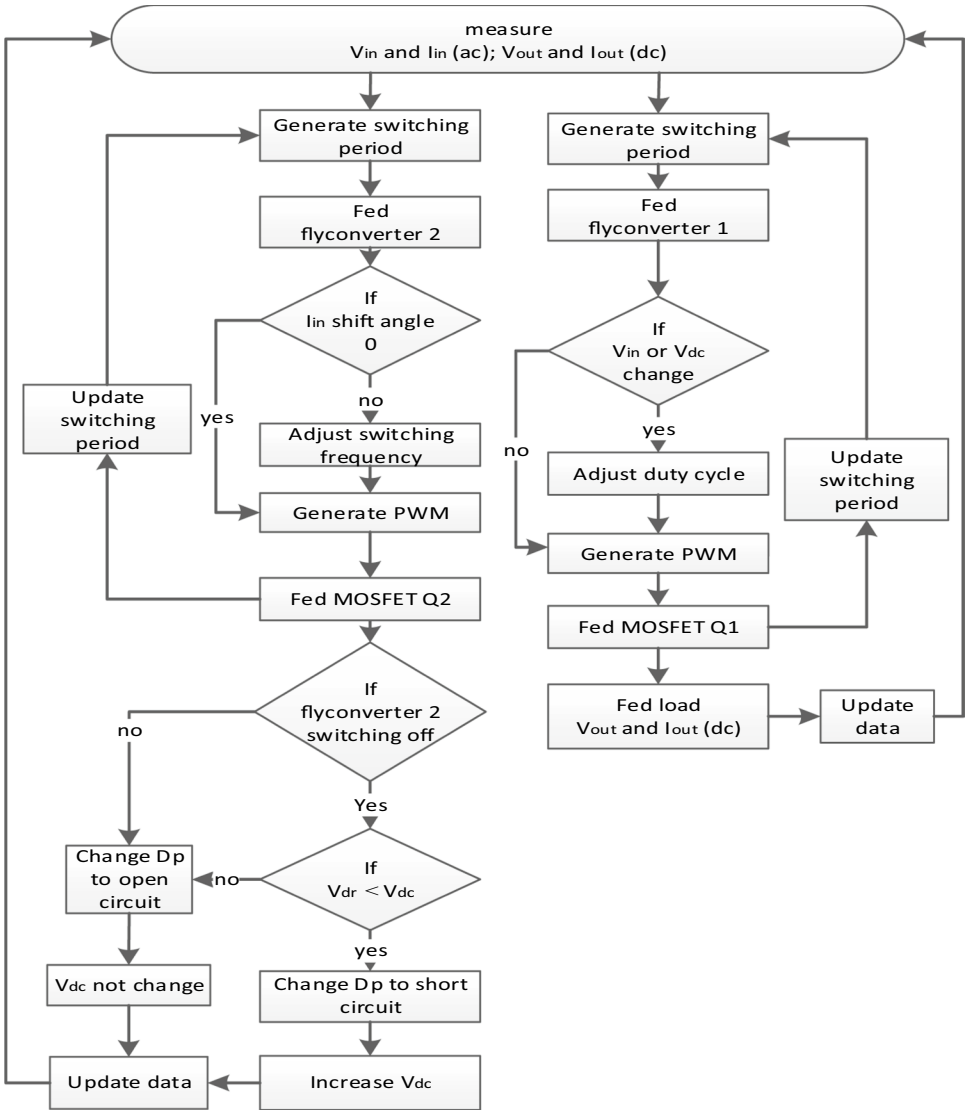


Fig. 11 Flowchart topology of a parallel flyback converter

5.1 Proposed Model Layout

The proposed model is simulated as shown in Fig. 12. The closed-loop control circuit that mainly consists of twelve loops is described as follows:

Loop 1: represents the power input loop; the input voltage is universal 80–220 V rms, 50 Hz.

Loop 2: represents the output power loop with output diode SF166; the output voltage is 24 V, 10 A. The output voltage is fed using flyback converter-I, which produce a nearly pure dc output wave due to the ability to remove high ripple; also, it can stabilize the output voltage even if the input voltage is reduced by 60% by control the duty cycle. Also, the output voltage is fed using flyback converter-II, which can deal with low ripple by the adjust switch frequency.

Loop 3: represents the Q2 MOSFET (30NG60) loop; where it is used for PFC.

Loop 4: represents the control diode (BY329); where it is used to support the capacitor voltage which connected by flyback converter-I.

Loop 5: represents the Q1 MOSFET (30NG60) loop; where it is used to control the output voltage.

Loop 6: represents an IC-controller (L6561); where it used to control Q2. To obtain the best PFC, L6561 is fed by voltage and current of the output as well as the input. It used to control the input current to be sinusoidal and in phase with the input voltage to achieve unity PF. The PF and THD are depending on the switching frequency of L6561, the range of switching frequency between 10 and 50 kHz. When switching frequency increased the PF and THD are enhancing while the circuit losses increased. Therefore, the control allocates optimal switching frequency which achieves minimum losses and bests the PF and THD.

Loop 7: represents an IC-controller (UC3842); where it used to control Q1 using complementary square-wave

Table 1 Circuit parameters

Input data	Input inductance	15 µH
	Main capacitor	100 µF
Flyback converter-I	Primary inductance	660 µH
	Secondary inductance	10 µH
	Output capacitors	2 mf
	Low-pass inductance	15 µH
	Low-pass capacitors	4 nF
Flyback converter-II	Primary inductance	500 µH
	Secondary inductance	32 µH
	Output capacitors	14 mF
	Low-pass inductance	15 µH
	Low-pass capacitors	25 nF

Table 2 Transformer specification

Minimum core area	0.68 cm^2
Air gap	1 mm
Primary turns	90 (split into two halves)
Primary inductance	970 µH
secondary turns	14
Primary resistance	1.26 Ω
Secondary resistance	0.04 Ω

voltages with fixed dead time (0.3 us). The oscillation frequency depends on the capacitor and equivalent resistance values. To obtain the perfect dc output signal, UC3842 is fed by the output and the input voltage.

Loop 8: represents a photocoupler (PC817); where it used isolate L6561 from the output signal.

Loop 9: represents a photocoupler (PC817); where it used isolate UC3842 from the output signal.

Loop 10: represents a three-terminal adjustable shunt regulator (TL431); where it used to feedback the controller by the output reference current.

Loop 11: represents TL431; where it used to feedback the controller by the output reference voltage.

Loop 12: represents feedback to L6561 by the input current and voltage.

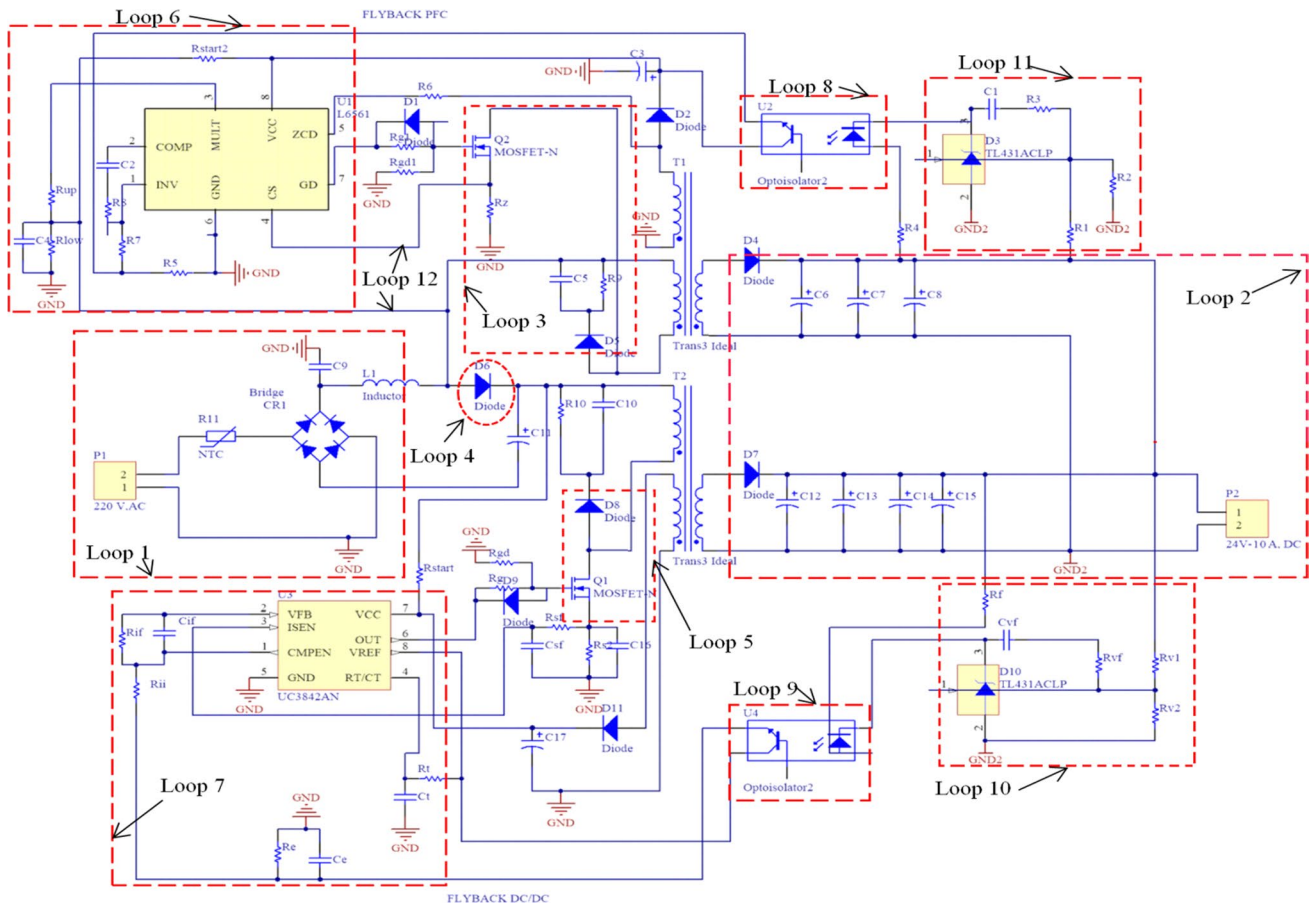


Fig. 12 A closed-loop control circuit for a parallel flyback converter

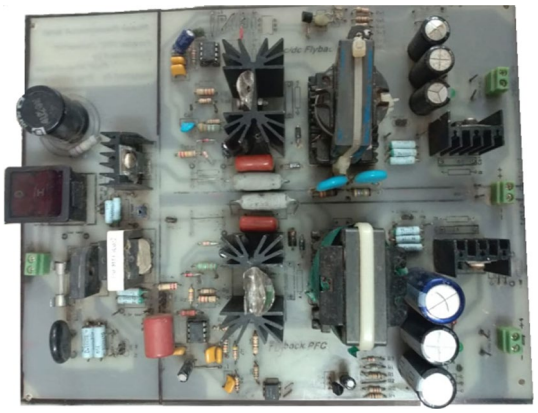


Fig. 13 A prototype of a parallel flyback converter

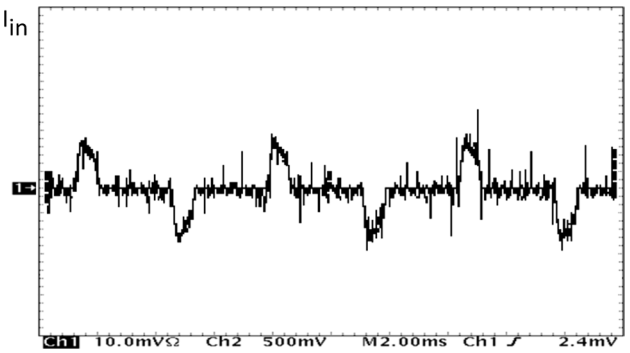


Fig. 14 Measured input current without PFC loop

5.2 Prototype Results

A prototype circuit in Fig. 13 is simulated implemented and tested. The circuit was tested at the input voltage of 220 V_{rms} and the load is 6.8 A which means 70% of the rated circuit power. When the circuit was operated using single flyback converter-I without PFC loop "Flyback converter-II", the ac input current is shown in Fig. 14, the PF is 0.67 and THD is 19.2%. While, when the circuit is operated using a parallel flyback converter the input current waveforms before and after the bridge are shown in Fig. 15. Flyback converter-II generates the input current to be sinusoidal and in phase with the input voltage. Therefore, the PF is "0.99" nearly unity. Also, the THD is 1.36%, all harmonics values are compatible with the IEC 61,000–3-2 Class C [25]. With zero voltage crossing and recycling the energy stored in the leakage inductance, the circuit efficiency is up to 94.4%. Figures 16 and 17 shows the coupled inductors voltage waveforms of the two MOSFETs.

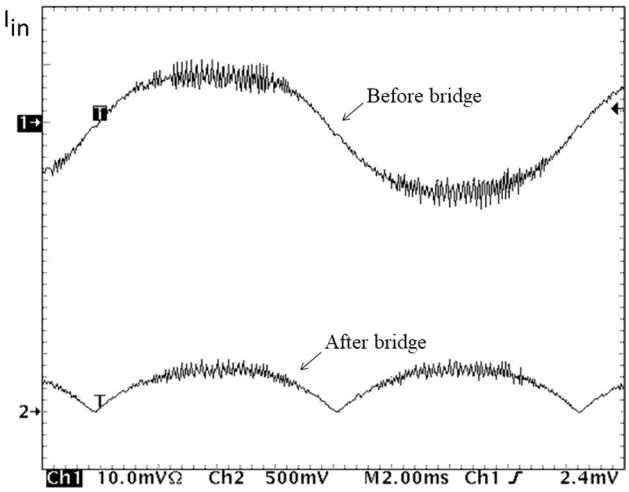


Fig. 15 Measured input current with PFC loop

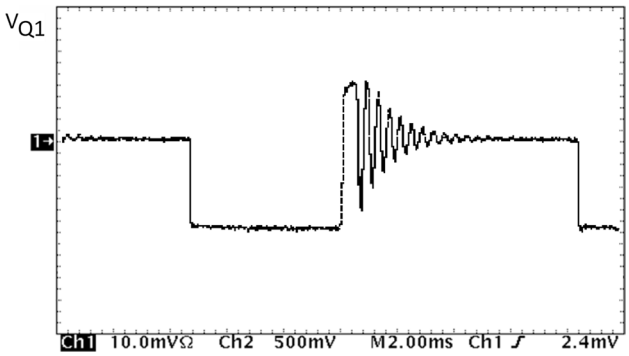


Fig. 16 Measured voltage of the MOSFET Q1

To check the circuit ability to operate in the case of a universal input, the circuit was tested by changing the input voltage from 80 to 260 V_{rm}. It was obtained that; the output voltage is remaining constant 24 V for all value of the input voltage is displayed in Fig. 18.

5.3 Comparison Between Practical and Theoretical

In order to verify the practical and theoretical results, a simulation for the proposed model using MATLAB software is made. The simulation model is tested at the load current

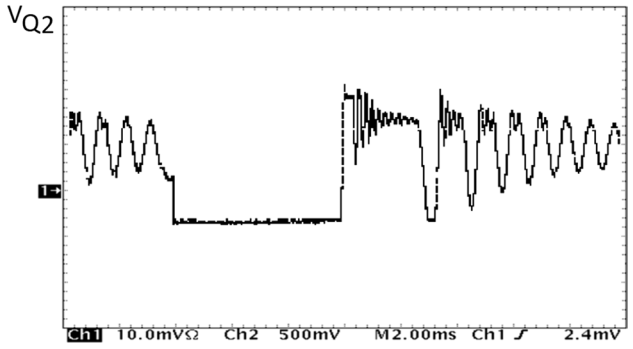


Fig. 17 Measured voltage of the MOSFET Q2

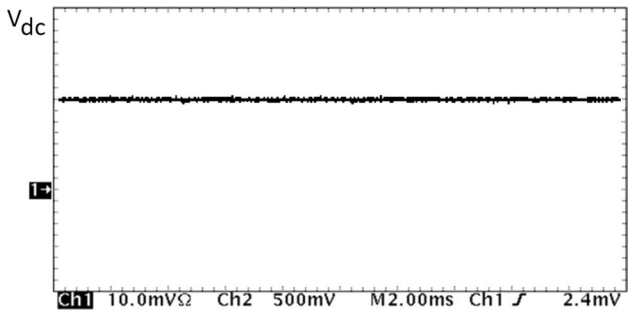


Fig. 18 Measured output voltage for a universal input

of 1.5 A, with a total output power of 20 W and the input voltage is varying from 80 to 260 V_{rms}. The voltage and current for the ac input THD for current are shown in Figs. 19 and 20, respectively. Also, the dc current before and after the inductance "L_{dr}" and the output current and voltage are shown in Fig. 21.

The comparison results between practical and theoretical are shown in Table 3 and Fig. 22, it is noticed that a perfect matching in all results.

5.4 Comparison With The Other Works

To ensure the accuracy and speed of the proposed model, the result is compared by the result from a single flyback converter in [2], and dual series flyback converters in [10]. Table 4 displayed the comparison results which were conducted on the rated power. It can be noticed that the superiority of the proposed model by using a parallel flyback converter. However, the series flyback converters in [10] produce good results but it can't deal with universal input and if a malfunction occurs in any converters, the load feeding is interrupted. However, in the proposed model, if a failure occurs in any converters, the load is still feeding because the circuit converts to a single flyback converter. Therefore, a led indicator has been added to each flyback converter

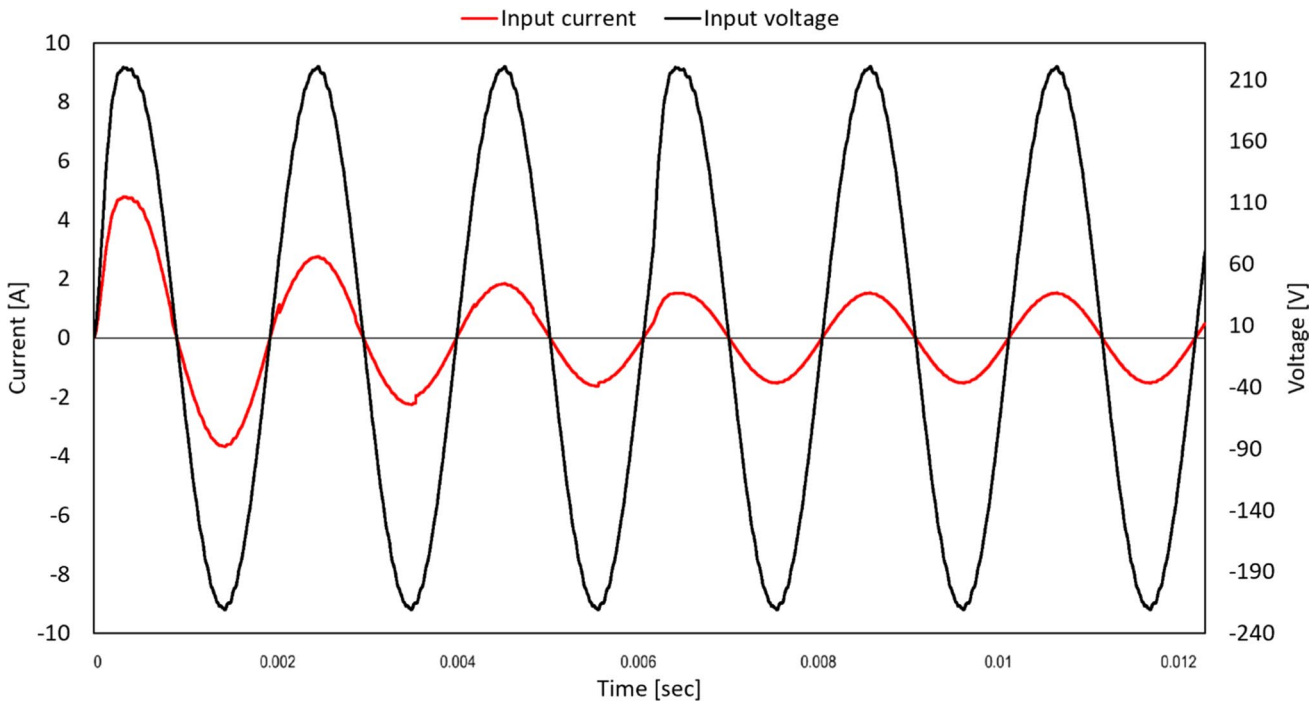


Fig. 19 Simulation results of ac input voltage and current

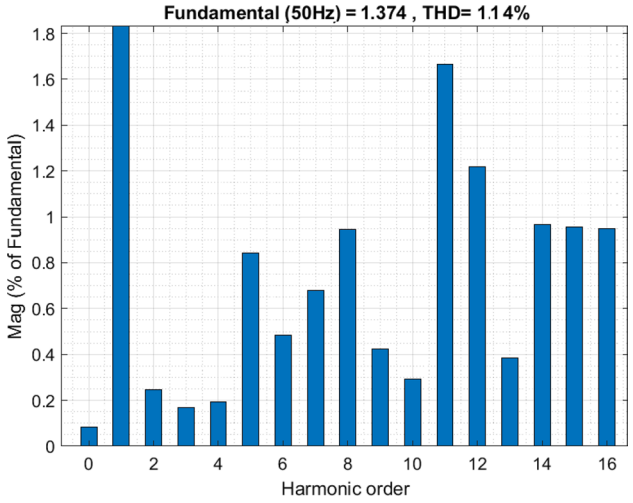


Fig. 20 Simulation THD analysis values for the current

in the proposed model to distinguish if a malfunction has occurred or not.

Finally, the circuit was tested at a different matrix of LEDs load range from 25 to 100% of rated power and charging a set of batteries. The circuit efficiency, PF, and THD are shown in Fig. 23 over a load range. It can be observed that PF is almost one, while the THD between 1.2 and 5.9%. The minimum circuit efficiency is 83.9% at 25% rated power.

6 Conclusion

With high pentration of the smart devices, ac/dcpower supply withch are increased. Power supply must be achieved both load and supply requirements. The load requirements are the best regulation, fast dynamic, and low ripples. The

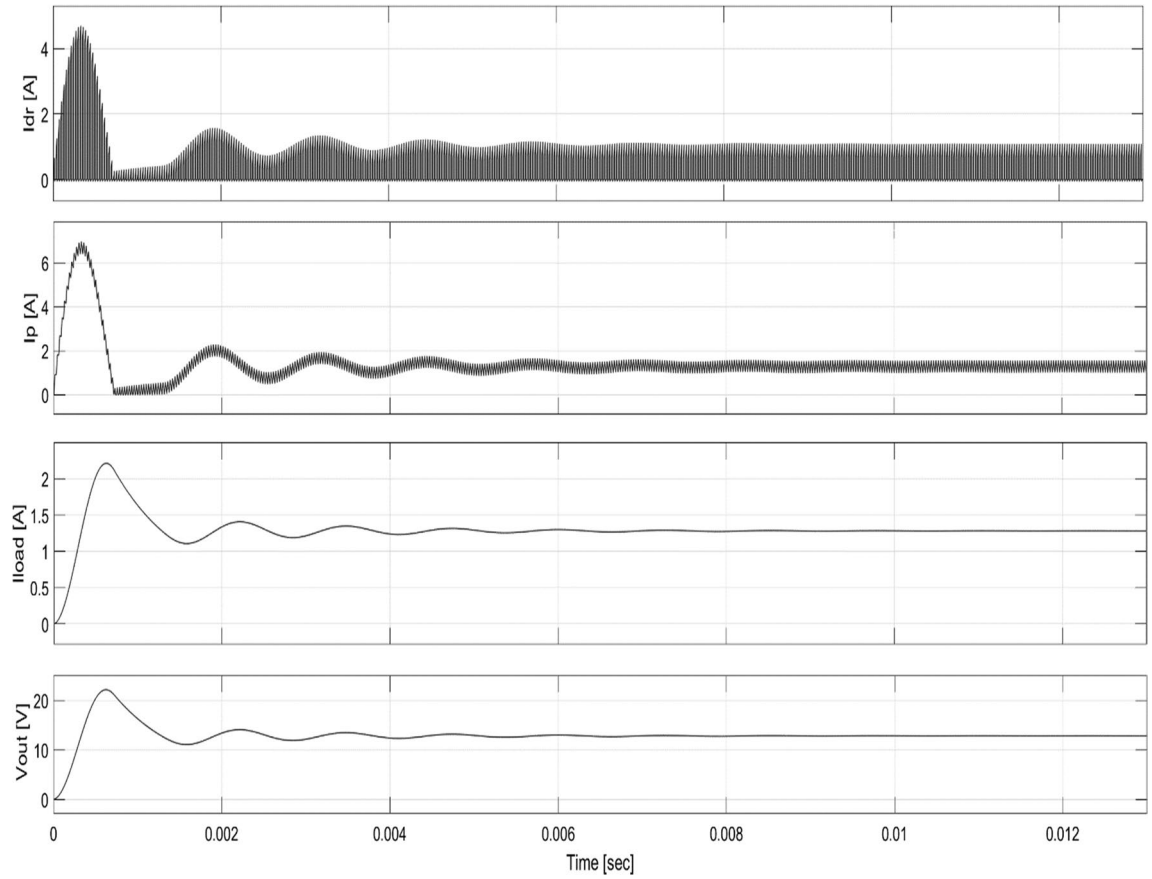


Fig. 21 Simulation results of dc current and voltage

Table 3 Practical and simulation comparison results

Parameter	Simulation Results	Practical Results
K_v	1.2	1.2
$\hat{I}_p$	3.705	3.716
I_{rmsp}	1.078	1.097
$\hat{I}_s$	13.1	13.07
I_{rmss}	3.79	3.75
P_{in}	56.47	56.73
n	6.41	6.43
L_p	940 µH	970 µH
A_{min}	0.5 cm^2	0.684 cm^2
$F^1(K_v)$	0.343	0.343
$F^2(K_v)$	0.254	0.254
$F^3(K_v)$	0.209	0.209
C_o	5417 µF	Three 2200 µF
η %	85	84.6

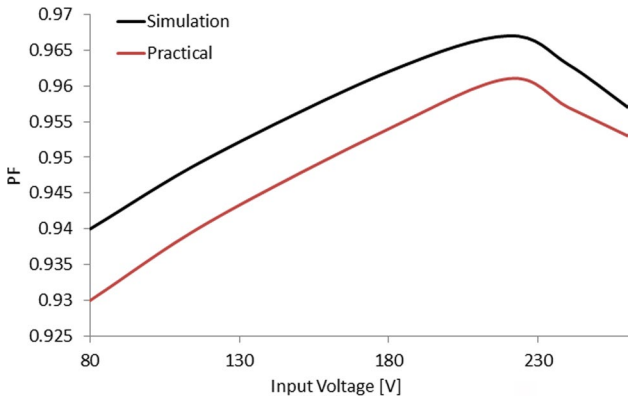


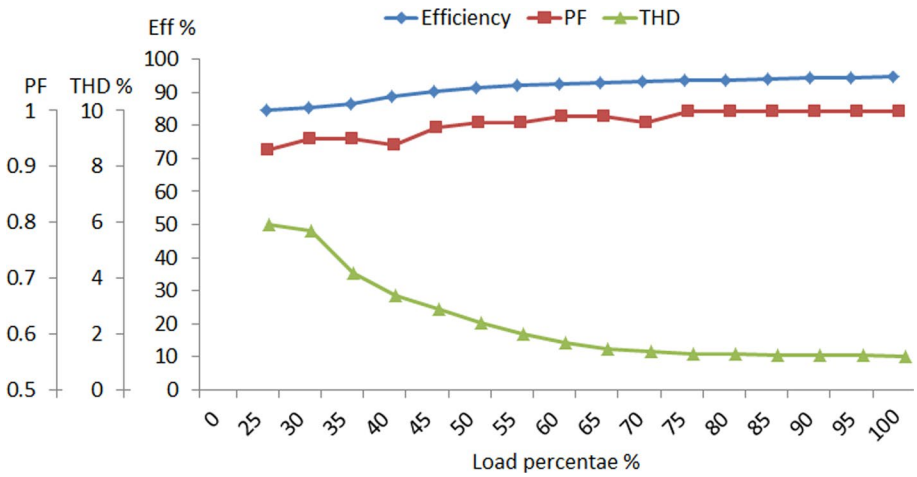
Fig. 22 PF comparison between experimental and theoretical results

Table 4 Comparison between different techniques

Techniques	η %	PF	THD %
Single flyback converter [2]	87.4	0.81	3.7
Series flyback converters [10]	94.9	0.97	1.42
Proposed model	96.2	0.97	1.2

supply requirements are good power factor and low harmonics. To enhance the system performance power factor correction is an essential tool. In this paper, a parallel flyback converter is designed and implemented. The first converter is used to regulate the output voltage by tunning the switching on/off periods while the switching period is remaining constant. The second converter is used to enhancing the power factor and reducing the harmonics by generating the input current to be in phase with the voltage. The controller of the second converter based on keeping switching on-period fixed while the frequency and switching period are variable. In this proposed circuit, the first converter is designed to operate with a very fast dynamic response than the second converter. The mathematical model of each part in the proposed circuit is designed to achieve a unity PF and reduced the power supply harmonies. A 220 W prototype circuit is designed. This circuit is able to stabilize the output voltage even if the input voltage is reduced by 60%. The designed circuit improved the supply PF and reduced the harmonics. Also, the introduced model is simulated and compared by other techniques. All exclusive results are proved the effectiveness and superiority of the proposed technique.

Fig. 23 Efficiency, PF, and THD, for different load



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