Designing of the Interleaved Flyback Inverter for PV Applications

Shivaprasad Hiremath
M.Tech, Power Electronics Engineering, Rashtreeya Vidyalaya College of Engineering, Bengaluru, India.

Dr. A. sreedevi
Assistant Professor, Dept. of Electrical and Electronics Engg., Rashtreeya Vidyalaya College of Engineering, Bengaluru, India

Abstract –Nowadays renewable energy resources are attaining the more importance because they are readily available and ecofriendly in nature. But the cost required for the implementation of the inverter is costly and solar energy source is intermittent in the nature. To solve these problems an interleaved flyback inverter is proposed. This topology provides the interleaving feature that reduces the voltage stress on the switches and ripple in the output voltage is less that reduces the size of the output filter capacitor. The cost and size of the flyback converter is less compared to other isolated dc-dc converters.RCD snubber circuit is used to protect the switch from the high dv/dt and provides the path for the flux resetting of the transformer. The efficiency of the converter topology increases. In this paper designing of interleaved flyback converter for PV applications and RCD snubber circuit has been carried.

Index Terms–Interleaved, Isolated, flux resetting isolated, RCD snubber, flux resetting, EMI effect.

1. INTRODUCTION

Solar Energy is a most readily available source of energy. It is most important renewable energy source because it is non-polluting in nature. At the end of 21^{st} century, it has been estimated that renewable energy sources might contribute up to 20%to 30% of the total energy consumption. Solar energy is intermittent in nature and this makes solar energy systems totally vulnerable to a wide range of inputs and because of this reason, we cannot provide stable DC voltage across the load. There are various topologies present in the DC-DC converters for the PV applications. The main constraints for the designing of the converters are size, weight and isolation is required to isolate the source from load. Transformer is used to achieve the isolation. It provides the isolation between the source and load. It provides the safety to load whenever the faults occur at the load side. To meet the above requirements isolated buck-boost converter that is flyback converter is preferred [2-3].Flyback converters are extensively used for low power applications due to its simple structure, low cost. Transient response for flyback converter is fast due to absence of the output inductor[4].But it has drawbacks of switching losses, low efficiency and voltage stress on the MOSFET switch[5].In order to overcome the above drawbacks interleaved flyback converter topology is used. In interleave topology two identical converters are connected in parallel. It has the advantages of reduced input current ripples, output voltage ripples, size of the filtering components [6].The voltage stress on the MOSFET switches are less compared to the conventional flyback converter [7].

Interleaved flyback converter consists of two MOSFET switches for its operation. The MOSFET switches in the converter will experience high voltage stress due to transformer leakage inductance and parasitic components in power converter [8]. So in order to reduce the voltage stress suitable snubber circuit is employed across the MOSFET switch. RCD snubber circuit is employed across the switch, it is widely used for low power applications due to its simple design [9].

The advantages of interleaved flyback topology over single flyback topology are

- The size of the transformer and semiconductor RMS and peak current reduces.
- Input and output RMS current reduces.
- Electromagnetic interference (EMI) is reduced due to the lower value of peak currents.
- There is a reduction in the heat dissipated by the electronic components.

2. BLOCK DIAGRAM

The Block diagram of the proposed interleaved flyback inverter is shown below. This proposed topology can be used to convert DC-DC, DC-AC for the providing the supply to the AC loads.

The Input to the converter can be given from the 20-30V solar panel. Interleaved flyback converter provides the110V output Dc voltage .The output voltage of the interleaved flyback converter is regulated by using the Current Mode PWM controller. Full bridge Inverter is used to convert the 110 Dc voltage to AC voltage by using the Sine PWM techniques.

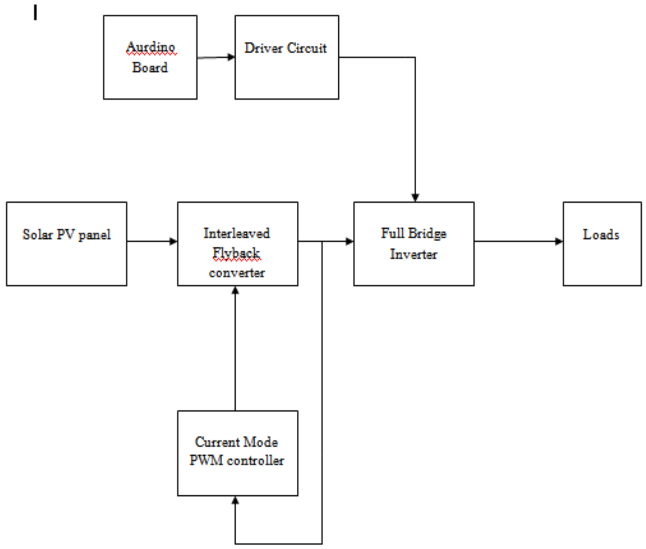

Fig 1. Block Diagram of Interleaved Flyback Inverter

3. CIRCUIT OPERATION

Interleaved flyback topology is a parallel combination of two identical flyback converters, whose power transistors are turned on at alternate half cycles and whose secondary currents are added through their rectifying diodes. . Interleaved flyback converter provides the power levels twice as high as the single flyback converters.Figure.2 shows the circuit diagram of interleaved flyback converter.

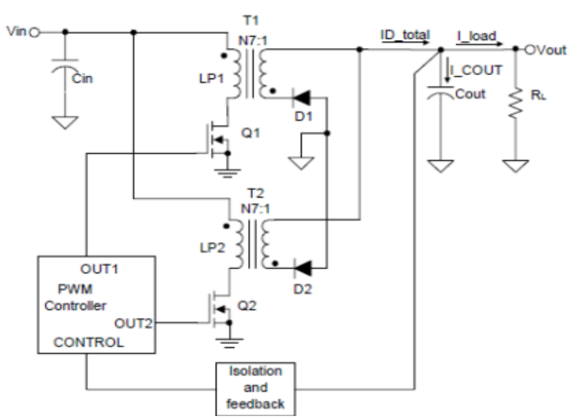

Fig 2. Circuit Diagram of Interleaved Flyback converter

There are two modes of operation for the interleaved flyback converter.

In mode 1 switch Q1 is on and Q2 is in off state. In the first cycle operation of the interleaved flyback converter switch Q1 is turned on, Q2 is turned off. When Q1 turns on, the current IQ1 flows through the closed path Q1,T1 and Vdc.During this cycle the energy is stored in the Transformer T1.Because of the inverted polarity of the secondary winding of the transformer T1,the diode D1 is reverse biased. Since Q2 is off, the IQ2 is zero. Even the diode D2 is forward biased no current is transferred to the load, because the energy stored in the transformer T2 is zero in the previous cycle.

In Mode 2 the switch Q2 is turned on,Q1 is turned off, the current IQ2 flows through the path Q2,T2 and Vdc.During this cycle energy is stored in the Transformer T2. Because of the inverted polarity of the secondary winding of the transformer T2,the diode D2 is reverse biased. Since switch Q1 is off, the current through Q1 is zero. The diode D1 is forward biased.The current in the magnetizing inductance of Transformer T1 flows through the dot end of the transformer and the diode D2.

When Q1 is turned OFF, Q2 is turned ON, When Q2 turns on, the current IQ2 flows through the closed path Q2, T2 and Vdc. During this period energy is stored in the magnetizing inductance of the transformer T2. Because of dot convention the diode D2 is reverse biased. Since Q1 is OFF, the current IQ2 is 0. The diode D1 is forward biased. The current in the magnetizing inductance of transformer T1 finds the path through the dot end of the transformer and D1. The current Is1 charges the output filter capacitor to the voltage Vo.

4. DESIGNING OF INTERLEAVED FLYBACK CONVERTER

Designing of the Interleaved flyback converter has been done for the 45W power rating.

Specification of the proposed converter are given below

- Input voltage range : 20-30 V
- Output Voltage : 110V
- Output power : 45W
- Efficiency : 75%
- Switching Frequency : 100KHz
- Duty Ratio : 0.4

Input Current is given by

$$Iin = \frac{Pin}{Vimin} = \frac{60}{20} = 3A$$

Primary peak current is given by

$$Ipp = \frac{2 \times Iin}{D} = \frac{2 \times Iin}{0.4} = 15A$$

Primary Inductance is given by

$$Lp = \frac{Vimin \times D}{Ipp \times fs} = \frac{20 \times 0.4}{15 \times 100 \times 10^3} = 5.3uH$$

The voltage gain expression for the Flyback converter is given by

$$\frac{Vo}{Vin} = \frac{(n \times D)}{(1-D)} = 8.5$$

The output current is given by the equation

$$Io = \frac{Po}{Vo} = \frac{45}{110} = 0.4A$$

The output resistance is given by

$$Ro = \frac{Vo}{Io} = \frac{110}{0.4} = 275ohm$$

The ripple voltage is 1% of the output voltage

$$\Delta Vo = 0.01 \times 110 = 1.1V$$

Output capacitor is given by

$$C = \frac{D}{\left(\frac{\Delta Vo}{Vo}\right) \times R \times fs} = 1.4uF$$

Primary turns of the Transformer is calculated by

$$Np = \frac{Vimin}{Bm \times Ac \times fs} = 15\ Turns$$

Secondary turns is given by

$$Ns = n \times Np = 130 \text{ Turns}$$

Designing of the snubber circuit

Reflected voltage for the flyback converter is given by

$$Vref = \left(\frac{Np}{Ns}\right) \times Vo = \left(\frac{1}{8.5}\right) \times 110 = 13V$$

Snubber voltage is 2 to 3 times of the reflected voltage

Vsn = 2 to 3of the Vref = 40V

Snubber resistance is given by

$$Rsn = \frac{Vsn^2}{\left(0.5 \times Ll \times Ipp^2 \times \left(\frac{Vsn}{Vsn-n}\right) \times Vo \times fs\right)} = 1.3kohm$$

Sunbber capacitance is given by

$$Csn = \frac{Vsn}{(0.1 \times Vsn \times Rsn \times fs)} = 0.75nF$$

5. RESULTS AND DISCUSSIONS

In this section, interleaved flyback converter is simulated. PSIM Software is used for simulating the circuits. PSIM is a simulation software package that is designed specifically for the power electronics simulations. Fig3. Show the simulations of the interleaved flyback converter.

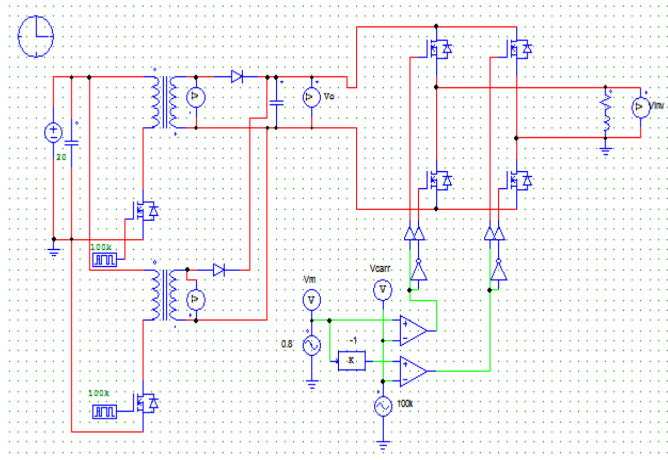

Fig 3. Simulation Circuit of Flyback inverter

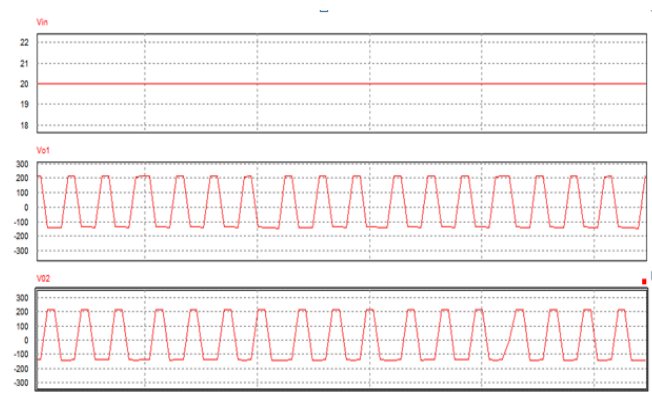

Fig 4. Input Voltage (Vin) and Voltage across flyback converter1 and converter2.

Description: The above waveforms indicate the output voltage of the flyback converter 1 and flyback converter 1.For the input voltage of 20V the voltage across the flyback converter 1 and converter2 is 110V.

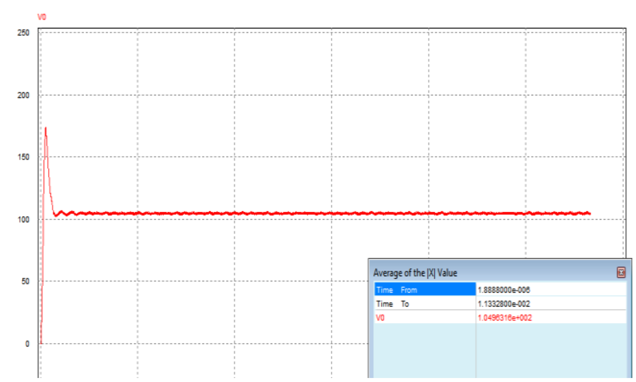

Fig 5.Outvoltage of the interleaved flyback converter

Description:The above waveforms indicate the output voltage of the interleaved flyback converter. Output voltage is 110V for the 20V input voltage.

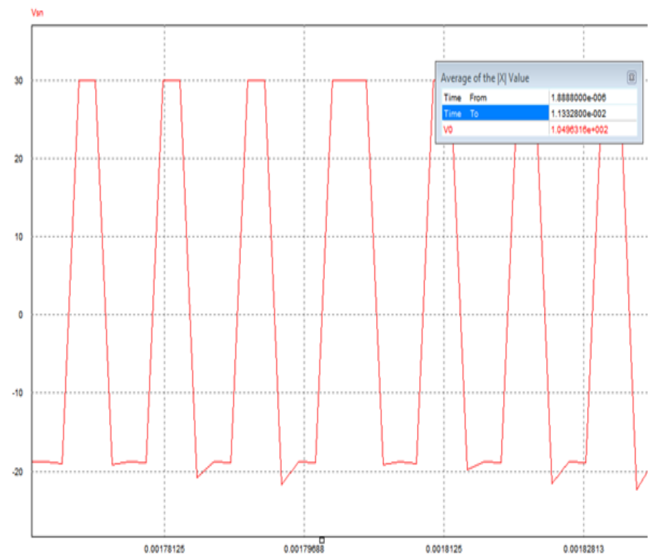

Fig 6.Voltage across the switches of the interleaved flyback converter

Description: The above waveforms indicate the output voltage across the switch1 of the interleaved flyback converter.

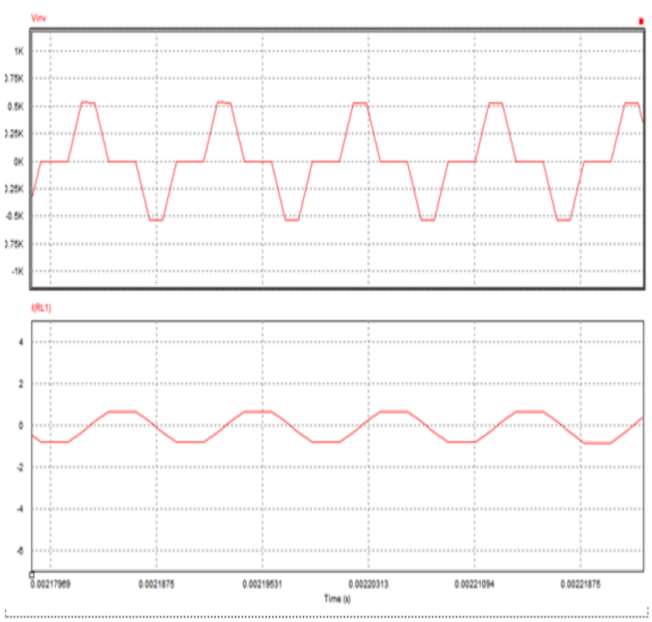

Fig 7.Outvoltage and Output current of the inverter

Description:The above waveforms indicate the output voltage and output current of the interleaved flyback inverter.

6. CONCLUSION

Design procedure and the simulation of the interleaved flyback converter has been proposed in this paper and RCD Snubber circuit is designed to protect the switch from high dv/dt voltages. Interleaved flyback converter provides the lesser output ripple and it avoids the usage of the bulky capacitor at the output side.The Converter is capable of providing 110V from the 20V input source and it is operating at a frequency of 100KHz. Filter Circuit has been designed in order to minimize the ripple in the output voltage.

REFERENCES

[1] L. Umanand, "Power Electronics Essentials and Santosh.
[2] Abdulrahman Alassi, Ayat Al-Aswad, Adel Gastli, Lazhar Ben Brahim, Ahmed Massoud," Assessment of Isolated and Non-Isolated DC-DC Converters for Medium-Voltage PV Applications," Department of Electrical Engineering, Qatar University, Doha, Qatar.2017
[3] V. Ramanarayana, "Course Material on Switched Mode Power Conversion", Department of Electrical Engineering Indian Institute of Science Banglore 560012, Jan 15, 2008.
[4] Nasir Coruh, Satilmis Urgun, Tarik Erfidan," Design and Implementation of Flyback Converters", Department of Electrical Engineering Kocaeli University, Kocaeli, Turkey,2010 IEEE Conference.
[5] Watson R, Lee F C, Hua G C, "Utilization of an active-clamp circuit to achieve soft switching in flyback converters", Journal of Power Electronics. IEEE, 2005.
[6] T Anuradha,Dr V Senthil Kumar "Design and Analysis of High Efficiency Soft Switched Int1erleaved Flyback Converter," Conference on Power, Energy and Control (ICPEC), 2013
[7] Hongmei Wang, Haixiao Ma,Yangguang Yan "Research on the Interleaved Flyback DC/DC Converter," IEEE Conference on Industrial Electronic and Applications (ICIEA 2006).
[8] Garcia-Caraveo, A.,Soto, A., Gonzalez, R, and Banuelos-Sanchez, p., "Brief review on snubber circuits", 20th International Conference on Electronics, Communications and computer (CONIELECOMP), Cholula, Feb. 2010, pp. 271-275.
[9] Chih-Hung Wu, Tsorng-Juu Liang, Senior Member, IEEE, Kai-Hui Chen, Wen-Yu Huang, Po-Yen Lin, Yi-Ju Lu, and Jhih-Sian Li, "Design and Implementation of a Novel Interleaved Flyback Converter with Leakage Energy Recycled", IEEE 2015.
[10] Fairchild Semiconductor, Application Note AN-4147 "Design Guidelines for RCD snubber of Flyback Converters".

Authors

Shivaprasad B Hiremath'25 from Gadag, Karnataka and pursuing post graduation in Power Electronics from R V College of Engineering, Bengaluru and graduated from Basaveshwara Enginering college,Bagalkot.Paper Presentation in "National Conference on Knowledge Dissemination of PG Projects and Research Works" .

Dr.A.Sreedevi , Associate Professor, R V College of Engineering Bengaluru.PhD from Visvesvaraya Technological University Belagavi,M.E. in Control Systems from Pune University. . Has 28 Years of teaching experience and author of more than 17 papers in National and international Journals and conferences.