DRE TDM firmware requirements

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Concerned Models **BB** ☐ **DM** ☐ **EM** ☐ **STM** ☐ **QM** ☐ **FM** ☒ **FS** ☐ **All** ☐

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Summary	
Annexes	

Keywords	

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Applicable Documents (AD)			
AD	**Title**	**Reference**	**Version**
AD01	XIFU DRE requirements document	XIFU-RD-13200-00420-CNES	2.0
AD02	Design and VHDL handbook for VLSI development, CNES Edition		2.1

Reference Documents (RD)			
RD	**Title**	**Reference**	**Version**
RD01	Transition edge sensors	Irwin and Hilton 2005	
RD02	XIFU TDM detection chain definition document	XIFU-DD-10000-00422-CNES	1

List of Abbreviations			

- Table of Contents -

1. SCOPE OF THE DOCUMENT

This document defines the requirements of the firmware which drives the Time Domain Multiplexed (TDM) readout of the detector array onboard Athena X-IFU.

2. DESCRIPTION OF THE XIFU DETECTION CHAIN

2.1. Athena / X-IFU and the DRE

Athena is designed to implement the Hot and Energetic Universe science theme selected by the European Space Agency for the second large mission of its Cosmic Vision program. The Athena science payload consists of a large aperture high angular resolution X-ray optics and twelve meters away, two interchangeable focal plane instruments: The X-ray Integral Field Unit (X-IFU) and the Wide Field Imager. The X-IFU is a cryogenic X-ray spectrometer, based on a large array of Transition Edge Sensors (TES) micro-calorimeters operated at 90 mK and offering a 2.5 eV spectral resolution.

In the X-IFU, the "Digital Readout Electronics" (DRE) drives the TDM readout of the 3168 superconducting TES of the detector array. For this, it reads the TES current measured by the instrument amplification chain (MUX SQUIDs, AMP SQUIDS and LNA) and it linearizes the entire detection chain with an active feedback loop. The DRE performs both, analogue and digital signal processing (A/D and D/A conversion, analogue filtering, digital filtering, feedback management...). The digital processing is done by the firmware of the DRE-DEMUX.

2.2. The Time Domain Multiplexing (TDM)

In order to readout the 3168 TES of the X-IFU Focal Plan Array (FPA) a multiplexed readout technique is mandatory. For the X-IFU a Time Domain Multiplexing (TDM) method is used.

Each TES pixel (which is equivalent to a resistor) is biased with a DC-voltage provided by the WFEE. The detection of an X-ray photon changes the TES resistance and modulates its current at a low frequency (kHz range). In each detection chain a column of SQUIDs (so-called MUX SQUIDs or SQUIDs SQ1) reads sequentially the current of the TESs. Each detection chain includes a “blind” TES for calibration purposes. The current is amplified by a second stage SQUID (so-called AMP SQUID or SQUID SQ2) and a low noise amplifier in the WFEE. From this signal the DRE-DEMUX shall derive:

- A feedback to be applied at the MUX SQUID in order to linearize the detection chain.
- The measurement of the TES current.

The DRE shall apply a feedback to the AMP SQUID in order to compensate for the SQ1 offset variations across the column.

The TDM cold front-end electronics is presented in Figure 1. Details about the TDM technique can be found in RD02 section 3.1.

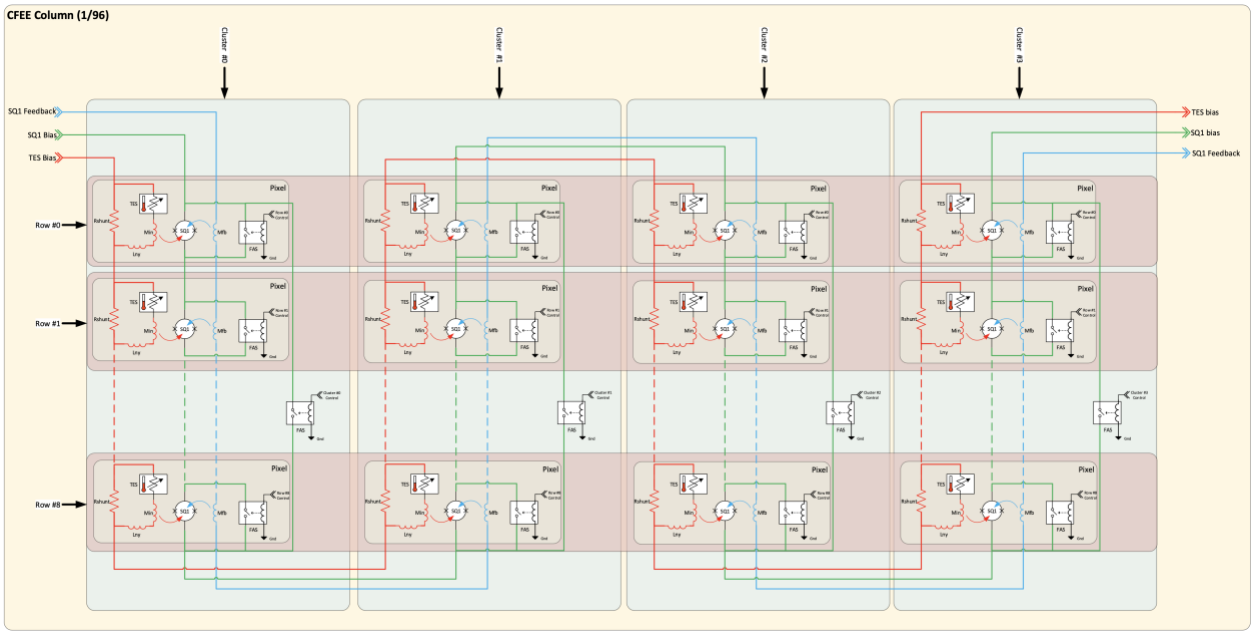

Figure 1: TDM cold front end electronics with the TES, the FAS and the MUX SQUIDs.

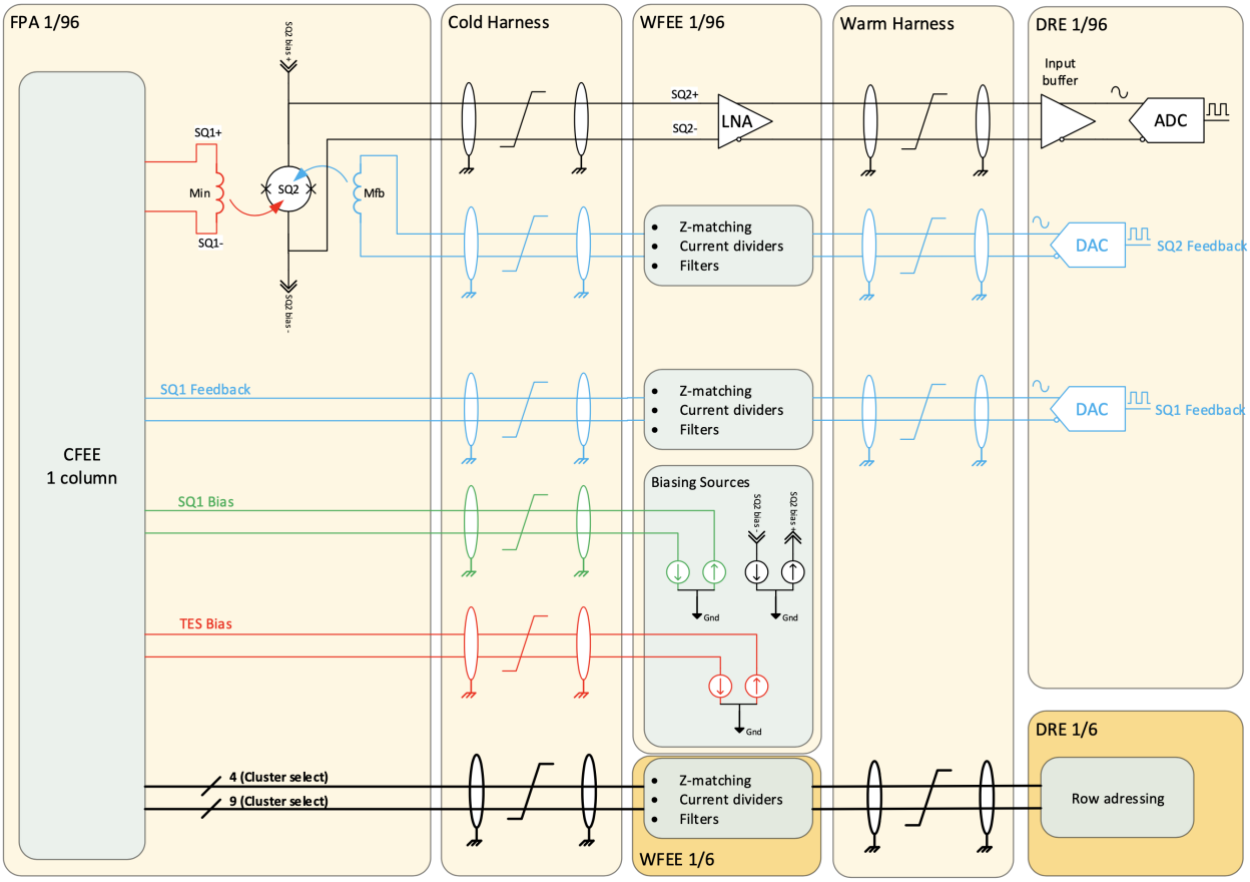

Figure 2: TDM detection chain with a focus on the AMP SQUIDs, the WFEE and the DRE.

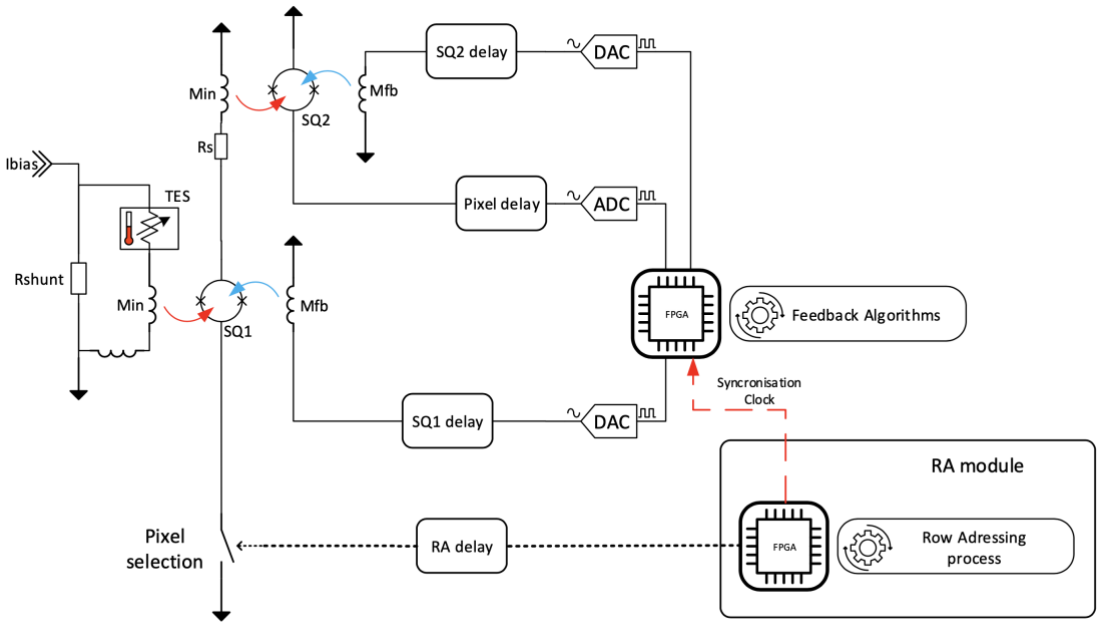

Figure 3: Diagram of the detection chain with a focus on the DRE functionalities.

3. FORMAT OF THE REQUIREMENTS

In this document the requirements have the following format:

Title:	**Title of the requirement**
Reference:	Reference of the requirement as follows: DRE-DMX-FW-XXXX - DRE-DMX-FW defines the applicability of the requirement. Here: DRE (DRE) | |> DEMUX (DMX) | |> Firmware (FW) - XXXX is a four-digit number aiming to define a specific reference for each requirement. This number is increased 10 by 10.
Description:	Short, clear, unambiguous description of the requirement.
Nature:	Nature of the requirement: o FUNC for Functional o PERF for Performances o ENVI for Environment o IF for Interfaces o DES for Design o DEV for Development o OP for Operational o QA for Quality Assurance o SAD for Safety, Availability, Dependability o AIT for Assembly Integration Testing o VERI for Verification o INS for Inspection o GSE for Ground Segment Equipment o ILS for Integrated Logistics Support o Others (acronym to be specifically clarified)
Higher level req.:	Reference of the higher-level requirement which implies this one.
Verification level:	At which level of the integration flow will it be possible to verify this requirement?
Verification method:	What will be the verification methods: o Analysis o Tests o Design
Comment:	Complementary description if needed.

4. FIRMWARE REQUIREMENTS

4.1. General requirements

Title:	**Host FPGA**
Reference:	DRE-DMX-FW-0010
Description:	The firmware shall be operated on a NG-Large FPGA (ref. NX1H140TSP).
Nature:	
Higher level req.:	
Verification level:	
Verification method:	
Comment:	

Title:	**CNES VHDL handbook**
Reference:	DRE-DMX-FW-0020
Description:	The firmware shall be compliant with design and VHDL handbook for VLSI developments, CNES edition, (AD02)
Nature:	QA
Higher level req.:	
Verification level:	
Verification method:	
Comment:	

Title:	**Firmware external reference clock**
Reference:	DRE-DMX-FW-0030
Description:	The firmware shall use an external reference clock with a frequency higher than 100MHz and lower than 120MHz.
Nature:	FUNC
Higher level req.:	
Verification level:	
Verification method:	
Comment:	The external reference clock is provided by the row address module.

Title:	**Number of columns**
Reference:	DRE-DMX-FW-0040
Description:	The firmware shall process 4 columns
Nature:	FUNC

Higher level req.:	
Verification level:	
Verification method:	
Comment:	

Title:	**Multiplexing factor**
Reference:	DRE-DMX-FW-0050
Description:	The firmware shall apply a multiplexing factor multFact = 34.
Nature:	FUNC
Higher level req.:	
Verification level:	
Verification method:	
Comment:	The multiplexing factor is the number of pixels per column. Among the 34 pixels to be processed by the firmware 33 are “science” pixels and one is used for calibration purposes.

Title:	**Synchronization**
Reference:	DRE-DMX-FW-0060
Description:	The firmware shall synchronize the pixel sequence processing with the rising edge of an external synchronization signal “sync”.
Nature:	FUNC
Higher level req.:	
Verification level:	
Verification method:	
Comment:	The “sync” signal is provided by the row address module to the DEMUX modules. Its frequency is fFrame.

4.2. Error signal

Title:	**Error signal: Reference of the ADC**
Reference:	DRE-DMX-FW-0070
Description:	For each column, the firmware shall drive an ADC AD9254S to do the acquisition of the error signal from the detection chain
Nature:	FUNC
Higher level req.:	
Verification level:	
Verification method:	
Comment:	

Title:	**Error signal: Clock for the ADC**
Reference:	DRE-DMX-FW-0080
Description:	The firmware shall provide the clock signal to the ADCs in charge of the acquisition of the error signals.
Nature:	FUNC
Higher level req.:	
Verification level:	
Verification method:	
Comment:	

Title:	**Error signal: Sampling frequency of the ADC**
Reference:	DRE-DMX-FW-0090
Description:	The sampling frequency of the ADCs in charge of the acquisition of the error signals shall be equal to the frequency of the reference clock (fRefClock).
Nature:	FUNC
Higher level req.:	
Verification level:	
Verification method:	
Comment:	

Title:	**Error signal: Fine timing correction**
Reference:	DRE-DMX-FW-0100
Description:	For each column, the firmware shall have the ability to delay the error signal by 0 t o 32 periods of the reference clock (fRef) according to a dedicated command.
Nature:	FUNC

Higher level req.:	
Verification level:	
Verification method:	
Comment:	Compensation of analog propagation delays (see Figure 4).

Title:	**Error signal: Boxcar filter**
Reference:	DRE-DMX-FW-0110
Description:	The firmware shall apply a boxcar type filter on the ADC data. The size of the boxcar shall be tunable by command between 1 and 16.
Nature:	FUNC
Higher level req.:	
Verification level:	
Verification method:	
Comment:	This is to reduce the noise on the error signal (see Figure 4).

Title:	**Error signal: Down-sampling**
Reference:	DRE-DMX-FW-0120
Description:	The firmware shall down-sample the error signal with a rate fRef / fRow.
Nature:	FUNC
Higher level req.:	
Verification level:	
Verification method:	
Comment:	The down-sampling selects a single error value per pixel and per frame. The Boxcar filtering and the down-sampling operations can be combined (no need to compute the boxcar outputs that will removed by the down-salmpling). The “Error signal fine timing correction” allows the selection of the valid data. (see Figure 4).

METTRE UNE FIGURE ICI POUR CLARIFIER LES TIMINGS

Figure 4: Timings of error signal input.

Title:	**Error signal: Coarse timing correction**
Reference:	DRE-DMX-FW-0130
Description:	For each column, the firmware shall have the ability to delay the error signal by 0 t o 33 periods of fRow according to a dedicated command.
Nature:	FUNC
Higher level req.:	
Verification level:	
Verification method:	
Comment:	Selection of pixel 0 among the 34 pixels of the column.

4.3. SQ1 feedback

Title:	**SQ1 feedback: computation of the feedback**
Reference:	DRE-DMX-FW-0140
Description:	For each column and sequentially for each pixel, the firmware shall compute a feedback signal according to the following formulas: FB(p, n+1) = FB(p, n) + ki(p).[E(p, n) - E(p, lp)] + dFB(p, n) dFB(p, n) = a(p).ki(p).E(p, n-1) + dFB(p, n-1) p is the pixel index, n is the frame index and a(p)=1/(1+τ) E(p, lp) is the value of the error signal for pixel p at lock point
Nature:	FUNC
Higher level req.:	
Verification level:	
Verification method:	
Comment:	This is the so-called Predictive Compensation 1 algorithm (PC1). τ = 1/(2π.fc') fc' is the normalized cutoff frequency: fc' = fc / (fRow / multFact) = fc / fFrame fc is the cutoff frequency (in Hz) of the low pass filter. The SQ1 feedback loop is illustrated on Figure 5.

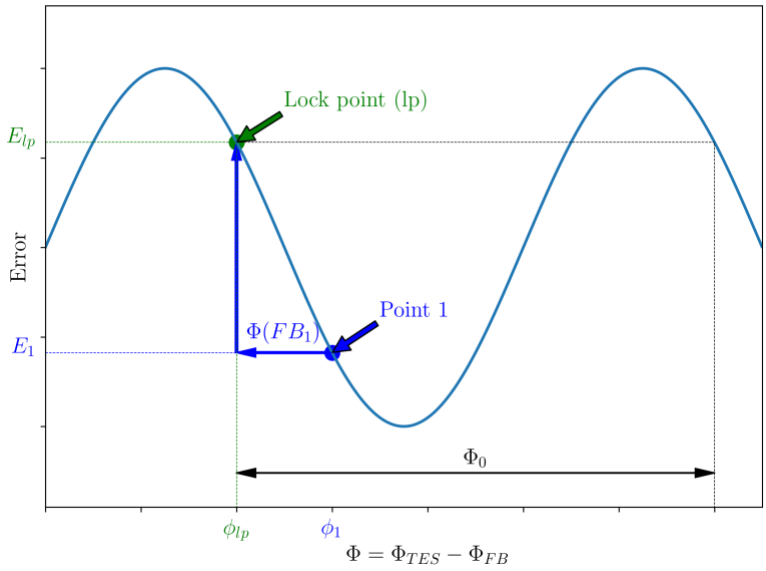

Figure 5 : Illustration of the feedback signal which brings the SQUID back to its lock point.

Title:	**SQ1 feedback: computation rate**
Reference:	DRE-DMX-FW-0150
Description:	The computation rate of the feedback signal for a column is fRow.
Nature:	FUNC
Higher level req.:	
Verification level:	
Verification method:	
Comment:	This corresponds to a computation rate of fFrame = fRow / multFact at pixel level.

Title:	**SQ1 feedback: “ki” parameter**
Reference:	DRE-DMX-FW-0160
Description:	The parameter “ki” of the feedback formula shall be configurable by command for each pixel between TBD and TBD, with a resolution TBD.
Nature:	FUNC
Higher level req.:	
Verification level:	
Verification method:	
Comment:	

Title:	**SQ1 feedback: “a” parameter**
Reference:	DRE-DMX-FW-0170
Description:	The parameter “a” of the feedback formula shall be configurable by command for each pixel between TBD and TBD, with a resolution TBD.

Nature:	FUNC
Higher level req.:	
Verification level:	
Verification method:	
Comment:	

Title:	**SQ1 feedback: pulse shaping**
Reference:	DRE-DMX-FW-0180
Description:	For each column, the firmware shall "up-sample" the MUX SQUID feedback data at the frequency of the reference clock and apply a digital filter according to the following formula: $Y(n) = (1+a).x(n) - a.y(n-1)$ x and y are respectively the input and the output of the filter, n is the sample index.
Nature:	FUNC
Higher level req.:	
Verification level:	
Verification method:	
Comment:	This so-called "pulse shaping" allows to digitally control the shape of the signal edges.

Title:	**SQ1 feedback: "a" parameter of pulse shaping**
Reference:	DRE-DMX-FW-0190
Description:	The parameter "a" of pulse shaping digital filter shall be configurable by command for each column between TBD and TBD, with a resolution TBD.
Nature:	FUNC
Higher level req.:	
Verification level:	
Verification method:	
Comment:	

Title:	**SQ1 feedback: Reference of the DAC**
Reference:	DRE-DMX-FW-0200
Description:	For each column, the firmware shall drive a DAC DAC5675A-SP to output the feedback signal for the SQUID SQ1.
Nature:	FUNC
Higher level req.:	
Verification level:	

Verification method:	
Comment:	

Title:	**SQ1 feedback: Clock for the DAC**
Reference:	DRE-DMX-FW-0210
Description:	The firmware shall provide the clock signal to the DACs in charge of the SQUID SQ1 feedback signals.
Nature:	FUNC
Higher level req.:	
Verification level:	
Verification method:	
Comment:	

Title:	**SQ1 feedback: Sampling frequency of the DAC**
Reference:	DRE-DMX-FW-0220
Description:	The sampling frequency of the DACs in charge of the SQUID SQ1 feedback signals shall be equal to the frequency of the reference clock (fRefClock).
Nature:	FUNC
Higher level req.:	
Verification level:	
Verification method:	
Comment:	Such a high frequency is mandatory to apply the pulse shaping.

Title:	**SQ1 feedback: Coarse timing correction**
Reference:	DRE-DMX-FW-0230
Description:	For each column, the firmware shall have the ability to delay the SQ1 feedback sig nal by 0 to 33 periods of fRow according to a dedicated command.
Nature:	FUNC
Higher level req.:	
Verification level:	
Verification method:	
Comment:	Selection of pixel 0 among the 34 pixels of the column.

Title:	**SQ1 feedback: Fine timing correction**
Reference:	DRE-DMX-FW-0240
Description:	For each column, the firmware shall have the ability to delay the SQ1 feedback sig nal by 0 to 31 periods of the reference clock (fRef) according to a dedicated comm

	and.
Nature:	FUNC
Higher level req.:	
Verification level:	
Verification method:	
Comment:	Compensation of analog propagation delays.

4.4. SQ2 feedback (offset compensation)

TBD

4.5. Science data

Title:	**Science data**
Reference:	DRE-DMX-FW-0250
Description:	For each column and sequentially for each pixel, the firmware shall compute the science data according to the following formula: SC(p, n) = [FB(p, n) – FB(p, lp)] + kmix(p).[E(p, n) – E(p, lp)] p is the pixel index, n is the frame index FB(p, lp) is the value of the feedback signal of pixel p at lock point E(p, lp) is the value of the error signal for pixel p at lock point
Nature:	FUNC
Higher level req.:	
Verification level:	
Verification method:	
Comment:	

Title:	**Science data: “kmix” parameter**
Reference:	DRE-DMX-FW-0260
Description:	The parameter “kmix” of the science data formula shall be configurable by comma nd for each pixel between TBD and TBD, with a resolution TBD.
Nature:	FUNC
Higher level req.:	
Verification level:	
Verification method:	
Comment:	

4.6. Auto-relock

Because of the SQUID characteristic periodicity, the DRE measures the SQUID flux modulo Φ_0. According to the slope of the characteristic at the lock point (the SQUID can be operated in the “falling” or in the “rising” slope) a positive or a negative feedback is applied to shift the operating point back to the initial lock position. If the skew rate of the input signal is too high the feedback loop may converge to a secondary lock point of the SQUID characteristic one (or even more) Φ_0 away from the initial lock point. This should be avoided because, in this case, the steady state of the feedback signal is far from I_{FB}=0 and this is an issue with respect to the dissipation at the 50 mK stage. The delock of the TDM feedback is explained in RD02 section 8.3.1 and in Figure 6.

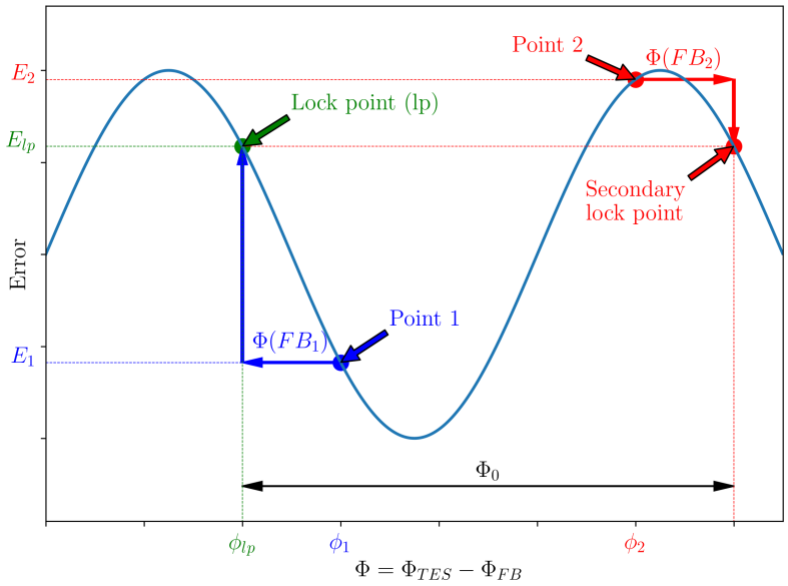

Figure 6: Illustration of the TDM delock in the case of a lock point in the SQUID "falling slope". During normal operations the skew rate at SQUID input is such that the feedback loop converges to the initial lock point. This is illustrated by the feedback "FB_1" which corrects the error "E_1" and brings the SQUID back to its initial lock point. For too high skew rates (in the case of energies above the X-IFU energy range for example) the error can cross the V_{lock} level. In this case the feedback loop converges on another lock point k.Φ_0 away from the initial lock point (k=1 in this plot for E_2 and FB_2).

Title:	**Auto-relock**
Reference:	DRE-DMX-FW-0270
Description:	For each pixel, if the SQUID remains far from its lock point (i.e. Fb – Fb0 higher t han FbThreshold) during too long (i.e. delay higher than relock delay) the firmwar e shall reset the feedback to its lock point value (i.e Fb0).
Nature:	FUNC
Higher level req.:	
Verification level:	
Verification method:	
Comment:	See Figure 7

Title:	**Relock delay (relockDelay)**
Reference:	DRE-DMX-FW-0280
Description:	The parameter "**relockDelay**" shall be configurable by command for each column between TBD and TBD, with a resolution TBD.
Nature:	FUNC
Higher level req.:	
Verification level:	
Verification method:	
Comment:	See Figure 7

Title:	**Feedback Threshold (fbThreshold)**
Reference:	DRE-DMX-FW-0290
Description:	The parameter "**fbThreshold**" shall be configurable by command for each column

	between TBD and TBD, with a resolution TBD.
Nature:	FUNC
Higher level req.:	
Verification level:	
Verification method:	
Comment:	See Figure 7

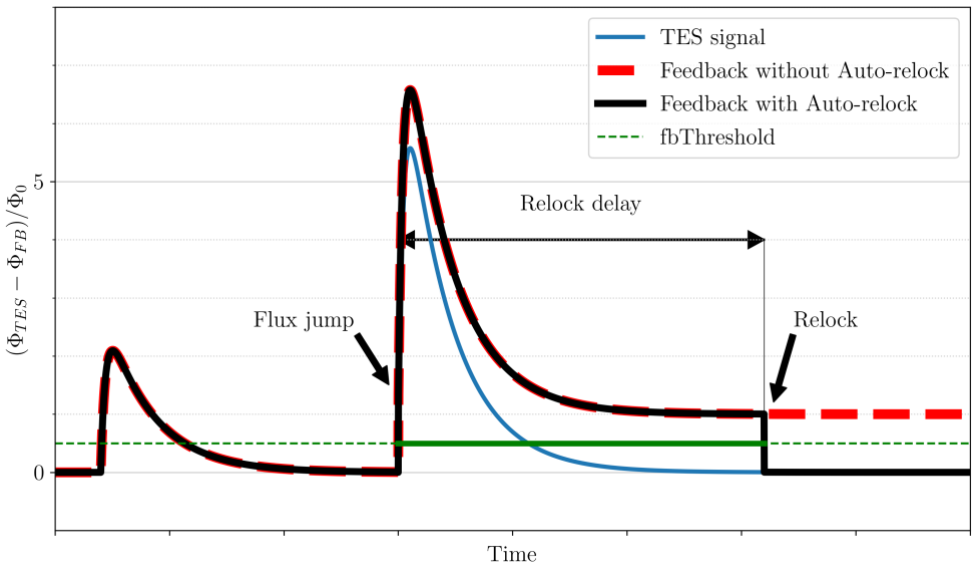

Figure 7: Relock process.

Title:	**Delock monitoring**
Reference:	DRE-DMX-FW-0300
Description:	The firmware shall monitor the number of Auto-relocks for each pixel and report t hese values in the housekeeping (TBC).
Nature:	FUNC
Higher level req.:	
Verification level:	
Verification method:	
Comment:	

4.7. Diagnostic functions

Title:	**Loop delay characterization for SQ1 feedback signal**
Reference:	DRE-DMX-FW-0310
Description:	For each column, the firmware shall have the ability to characterize the delay in th e SQ1 feedback loop (i.e. delay between the SQ1 feedback signal at firmware outp ut and the Error signal at firmware input).
Nature:	FUNC
Higher level req.:	
Verification level:	
Verification method:	
Comment:	

Title:	**Loop delay characterization for SQ2 feedback signal**
Reference:	DRE-DMX-FW-0320
Description:	For each column, the firmware shall have the ability to characterize the delay in th e SQ2 feedback loop (i.e. delay between the SQ2 feedback signal at firmware outp ut and the Error signal at firmware input).
Nature:	FUNC
Higher level req.:	
Verification level:	
Verification method:	
Comment:	

Title:	**Test patterns**
Reference:	DRE-DMX-FW-0330
Description:	For each column, the firmware shall have the ability to send 2 test patterns on each DAC output. The content of the test patterns shall be configurable by commands. The length of the test patterns is TBD.
Nature:	FUNC
Higher level req.:	
Verification level:	
Verification method:	
Comment:	

Title:	**Dump of raw data**
Reference:	DRE-DMX-FW-0340
Description:	The firmware shall have the ability to send a dump of raw data to the EP over a du ration of TBD s. The raw data are selected by command and can be one of the foll

	owing: - The ADC values of the error signal in column 0 - The ADC values of the error signal in column 1 - The ADC values of the error signal in column 2 - The ADC values of the error signal in column 3
Nature:	FUNC
Higher level req.:	
Verification level:	
Verification method:	
Comment:	A single acquisition of raw data can be requested at the time.

4.8. TM/TC

4.8.1. Management of analogue housekeepings

Title:	**Acquisition of analogue housekeepings**
Reference:	DRE-DMX-FW-0350
Description:	The firmware shall manage the acquisition of 16 (TBC) analogue housekeepings fr om the DEMUX module (voltages and temperatures). The frequency for the HK sa mpling is 2 Hz (TBC) +/- TBD Hz.
Nature:	FUNC
Higher level req.:	
Verification level:	
Verification method:	
Comment:	

4.8.2. Science data and housekeepings interface

The TM link between the TDM firmware and the EP shall optimize the number of wires with an acceptable signal frequency (i.e. lower than 50 MHz). With 4 columns per FPGA, 34 pixels per columns, 16 bits per value and a sampling rate of 150 Ksps, the data rate at the firmware outrput is 340 Mbits/s. 8 serial lines are needed to reduce the data rate per line below 50 Msps. The interface is handled with the following signals (see details on Figure 8, Figure 9, Table 1 and **Error! Reference source not found.**):

- A clock (CLK)
- A control line (CTRL)
- 8 data lines

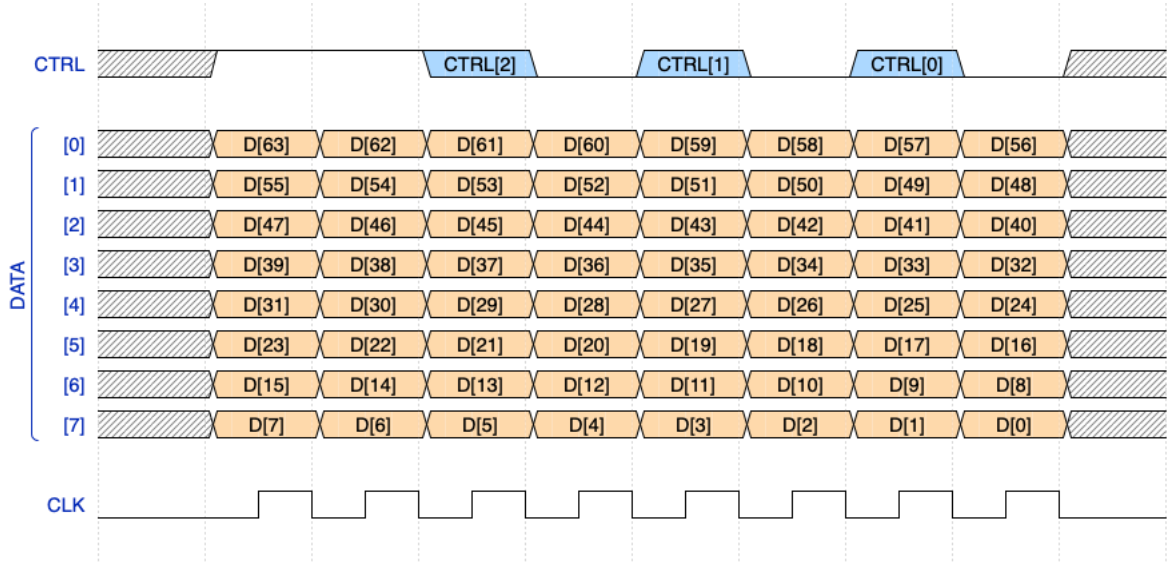

Figure 8: TM protocol for data and housekeepings.

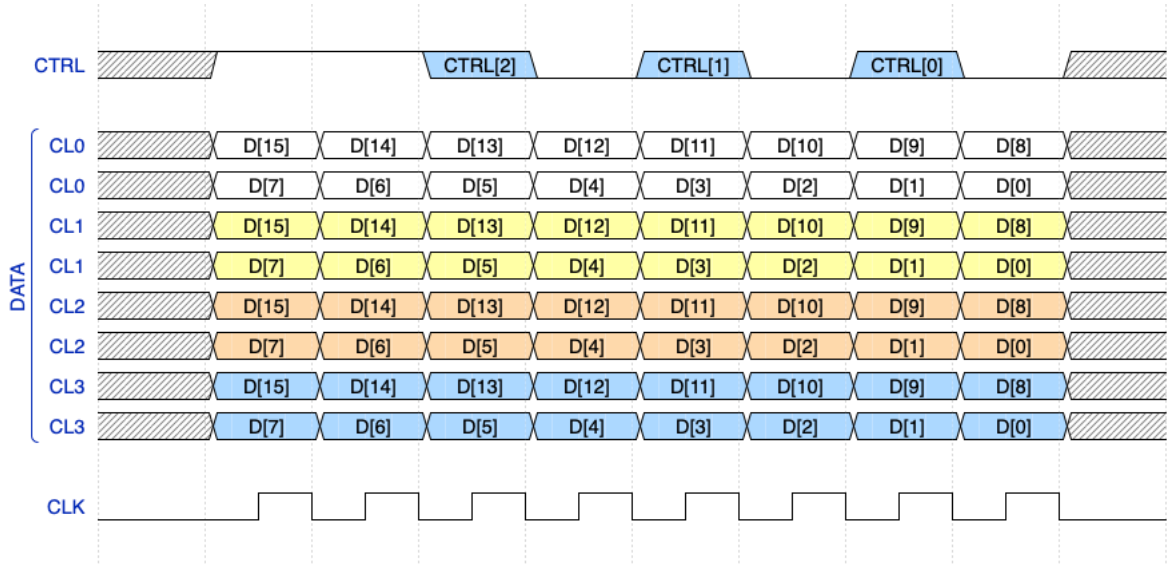

Figure 9: TM protocol for the transmission of data. Each pair of lines is dedicated to a column.

Table 1: Description of TM control parameter (CTRL).

CTRL		Type of Data	Comment
000	DAT	DATA word (Science or HK)	
001		First word of science data packet	
010		First word of ADC Col0 dump packet	
011		First word of ADC Col1 dump packet	
100		First word of ADC Col2 dump packet	
101		First word of ADC Col3 dump packet	
110		First word of HK data packet	
111	EOD	End of data (Science or HK)	

Title:	**Transfer of science data and housekeepings**
Reference:	DRE-DMX-FW-0360
Description:	The firmware shall transmit the science data and the housekeepings according to th e protocol described in Figure 8, Figure 9, Table 1.
Nature:	FUNC
Higher level req.:	
Verification level:	
Verification method:	
Comment:	

Title:	**Reception of telecommands**
Reference:	DRE-DMX-FW-0370
Description:	The firmware shall receive its telecommands according to the protocol defined in RDXX.
Nature:	FUNC
Higher level req.:	
Verification level:	
Verification method:	
Comment:	