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| **DRE TDM firmware requirements** |

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| **Prepared by** | *Signature* |  | **Accepted by** | *Signature* |
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| **Concerned Models** | **BB** |  | **DM** |  | **EM** |  | **STM** |  | **QM** |  | **FM** | X | **FS** |  | **All** |  |

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| **Summary** |  |
| **Annexes** |  |

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| **Applicable Documents (AD)** | | | |
| **AD** | **Title** | **Reference** | **Version** |
| **AD01** | XIFU DRE requirements document | XIFU-RD-13200-00420-CNES | 2.0 |
| **AD02** | Design and VHDL handbook for VLSI development, CNES Edition |  | 2.1 |
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| **Reference Documents (RD)** | | | |
| **RD** | **Title** | **Reference** | **Version** |
| **RD01** | Transition edge sensors | Irwin and Hilton 2005 |  |
| **RD02** | XIFU TDM detection chain definition document | XIFU-DD-10000-00422-CNES | 1 |
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| --- | --- | --- | --- |
| **List of Abbreviations** | | | |
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# Scope of the document

This document defines the requirements of the firmware which drives the Time Domain Multiplexed (TDM) readout of the detector array onboard Athena X-IFU.

# Description of the XIFU detection chain

## Athena / X-IFU and the DRE

Athena is designed to implement the Hot and Energetic Universe science theme selected by the European Space Agency for the second large mission of its Cosmic Vision program. The Athena science payload consists of a large aperture high angular resolution X-ray optics and twelve meters away, two interchangeable focal plane instruments: The X-ray Integral Field Unit (X-IFU) and the Wide Field Imager. The X-IFU is a cryogenic X-ray spectrometer, based on a large array of Transition Edge Sensors (TES) micro-calorimeters operated at 90 mK and offering a 2.5 eV spectral resolution.

In the X-IFU, the "Digital Readout Electronics" (DRE) drives the TDM readout of the 3168 superconducting TES of the detector array. For this, it reads the TES current measured by the instrument amplification chain (MUX SQUIDs, AMP SQUIDS and LNA) and it linearizes the entire detection chain with an active feedback loop. The DRE performs both, analogue and digital signal processing (A/D and D/A conversion, analogue filtering, digital filtering, feedback management...). The digital processing is done by the firmware of the DRE-DEMUX.

## The Time Domain Multiplexing (TDM)

In order to readout the 3168 TES of the X-IFU Focal Plan Array (FPA) a multiplexed readout technique is mandatory. For the X-IFU a Time Domain Multiplexing (TDM) method is used.

Each TES pixel (which is equivalent to a resistor) is biased with a DC-voltage provided by the WFEE. The detection of an X-ray photon changes the TES resistance and modulates its current at a low frequency (kHz range). In each detection chain a column of SQUIDs (so-called MUX SQUIDs or SQUIDs SQ1) reads sequentially the current of the TESs. Each detection chain includes a “blind” TES for calibration purposes. The current is amplified by a second stage SQUID (so-called AMP SQUID or SQUID SQ2) and a low noise amplifier in the WFEE. From this signal the DRE-DEMUX shall derive:

* A feedback to be applied at the MUX SQUID in order to linearize the detection chain.
* The measurement of the TES current.

The DRE shall apply a feedback to the AMP SQUID in order to compensate for the SQ1 offset variations across the column.

The TDM cold front-end electronics is presented in Figure 1. Details about the TDM technique can be found in RD02 section 3.1.

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| |  |  | | --- | --- | |  | Figure 1: TDM cold front end electronics with the TES, the FAS, the MUX SQUIDs and the AMP SQUIDs. | |  |
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# Format of the requirements

In this document the requirements have the following format:

|  |  |
| --- | --- |
| **Title:** | **Title of the requirement** |
| **Reference:** | Reference of the requirement as follows: XIFU-DRE-DMX-FW-R-XXXX  - XIFU-DRE-DMX-FW defines the applicability of the requirement. Here:  XIFU |  |> DRE |  |> DEMUX |  |> Firmware  - R stands for “**R**equirement”  - XXXX is a four-digit number aiming to define a specific reference for each requirement. This number is increased 10 by 10. |
| **Description:** | Short, clear, unambiguous description of the requirement. |
| **Higher level req.:** | Reference of the higher-level requirement which implies this one. |
| **Verification level:** | At which level of the integration flow will it be possible to verify this requirement? |
| **Verification method:** | What will be the verification methods? (simulation, tests) |
| **Comment:** | Complementary description if needed. |

# Firmware requirements

## General requirements

|  |  |
| --- | --- |
| **Title:** | **Host FPGA** |
| **Reference:** | XIFU-DRE-DMX-FW-R-0010 |
| **Description:** | The firmware shall be operated on a NG-Large FPGA (ref. NX1H140TSP). |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** |  |
| **Comment:** |  |

|  |  |
| --- | --- |
| **Title:** | **CNES VHDL handbook** |
| **Reference:** | XIFU-DRE-DMX-FW-R-0020 |
| **Description:** | The firmware shall be compliant with design and VHDL handbook for VLSI developments, CNES edition, (AD02) |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** |  |
| **Comment:** |  |

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| --- | --- |
| **Title:** | **Firmware external reference clock** |
| **Reference:** | XIFU-DRE-DMX-FW-R-0030 |
| **Description:** | The firmware shall use an external reference clock with a frequency > 100MHz and < 120MHz. |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** |  |
| **Comment:** | The external reference clock is provided by the row address module. |

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| **Title:** | **Number of columns** |
| **Reference:** | XIFU-DRE-DMX-FW-R-0040 |
| **Description:** | The firmware shall process 4 columns |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** |  |
| **Comment:** |  |

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| --- | --- |
| **Title:** | **Multiplexing factor** |
| **Reference:** | XIFU-DRE-DMX-FW-R-0050 |
| **Description:** | The firmware shall apply a multiplexing factor multFact = 34. |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** |  |
| **Comment:** | The multiplexing factor is the number of pixels per column. Among the 34 pixels to be processed by the firmware 33 are “science” pixels and one is used for calibration purposes. |

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| **Title:** | **Synchronization** |
| **Reference:** | XIFU-DRE-DMX-FW-R-0060 |
| **Description:** | The firmware shall synchronize the pixel sequence processing with the rising edge of an external synchronization signal “sync”. |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** |  |
| **Comment:** | The “sync” signal is provided by the row address module to the DEMUX modules. Its frequency is fFrame. |

## Error signal

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| **Title:** | **Error signal: Reference of the ADC** |
| **Reference:** | XIFU-DRE-DMX-FW-R-0070 |
| **Description:** | For each column, the firmware shall drive an ADC AD9254S to do the acquisition of the error signal from the detection chain |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** |  |
| **Comment:** |  |

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| **Title:** | **Error signal: Clock for the ADC** |
| **Reference:** | XIFU-DRE-DMX-FW-R-0080 |
| **Description:** | The firmware shall provide the clock signal to the ADCs in charge of the acquisition of the error signals. |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** |  |
| **Comment:** |  |

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| **Title:** | **Error signal: Sampling frequency of the ADC** |
| **Reference:** | XIFU-DRE-DMX-FW-R-0090 |
| **Description:** | The sampling frequency of the ADCs in charge of the acquisition of the error signals shall be equal to the frequency of the reference clock (fRefClock). |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** |  |
| **Comment:** |  |

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| **Title:** | **Error signal: Fine timing correction** |
| **Reference:** | XIFU-DRE-DMX-FW-R-0100 |
| **Description:** | For each column, the firmware shall have the ability to delay the error signal by 0 to 32 periods of the reference clock (fRef) according to a dedicated command. |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** |  |
| **Comment:** | Compensation of analog propagation delays (see Figure 2). |

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| **Title:** | **Error signal: Boxcar filter** |
| **Reference:** | XIFU-DRE-DMX-FW-R-0110 |
| **Description:** | The firmware shall apply a boxcar type filter on the ADC data. The size of the boxcar shall be tunable by command between 1 and 16. |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** |  |
| **Comment:** | This is to reduce the noise on the error signal (see Figure 2). |

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| **Title:** | **Error signal: Down-sampling** |
| **Reference:** | XIFU-DRE-DMX-FW-R-0120 |
| **Description:** | The firmware shall down-sample the error signal with a rate fRef / fRow. |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** |  |
| **Comment:** | The down-sampling selects a single error value per pixel and per frame.  The Boxcar filtering and the down-sampling operations can be combined (no need to compute the boxcar outputs that will removed by the down-salmpling).  The “Error signal fine timing correction” allows the selection of the valid data.  (see Figure 2). |

METTRE UNE FIGURE ICI POUR CLARIFIER LES TIMINGS

Figure 2: Timings of error signal input.

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| **Title:** | **Error signal: Coarse timing correction** |
| **Reference:** | XIFU-DRE-DMX-FW-R-0130 |
| **Description:** | For each column, the firmware shall have the ability to delay the error signal by 0 to 33 periods of fRow according to a dedicated command. |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** |  |
| **Comment:** | Selection of pixel 0 among the 34 pixels of the column. |

## SQ1 feedback

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| **Title:** | **SQ1 feedback: computation of the feedback** |
| **Reference:** | XIFU-DRE-DMX-FW-R-0140 |
| **Description:** | For each column and sequentially for each pixel, the firmware shall compute a feedback signal according to the following formulas:  FBp, n+1 = FBp, n + kip.Ep, n + dFBp, n  dFBp, n = ap.kip.Ep, n-1 + dFBp, n-1  p is the pixel index, n is the frame index and ap=1/(1+τ) |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** |  |
| **Comment:** | This is the so-called Predictive Compensation 1 algorithm (PC1).  τ = 1/(2π.fc’)  fc’ is the normalized cutoff frequency: fc’ = fc / (fRow / multFact) = fc / fFrame  fc is the cutoff frequency (in Hz) of the low pass filter. |

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| **Title:** | **SQ1 feedback: computation rate** |
| **Reference:** | XIFU-DRE-DMX-FW-R-0150 |
| **Description:** | The computation rate of the feedback signal for a column is fRow. |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** |  |
| **Comment:** | This corresponds to a computation rate of fFrame = fRow / multFact at pixel level. |

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| **Title:** | **SQ1 feedback: “ki” parameter** |
| **Reference:** | XIFU-DRE-DMX-FW-R-0160 |
| **Description:** | The parameter “ki” of the feedback formula shall be configurable by command for each pixel between TBD and TBD, with a resolution TBD. |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** |  |
| **Comment:** |  |

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| **Title:** | **SQ1 feedback: “a” parameter** |
| **Reference:** | XIFU-DRE-DMX-FW-R-0170 |
| **Description:** | The parameter “a” of the feedback formula shall be configurable by command for each pixel between TBD and TBD, with a resolution TBD. |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** |  |
| **Comment:** |  |

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| **Title:** | **SQ1 feedback: pulse shaping** |
| **Reference:** | XIFU-DRE-DMX-FW-R-0180 |
| **Description:** | For each column, the firmware shall “up-sample” the MUX SQUID feedback data at the frequency of the reference clock and apply a digital filter according to the following formula:  yn = (1+a) xn - a yn-1  xand y are respectively the input and the output of the filter, n is the sample index. |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** |  |
| **Comment:** | This so-called “pulse shaping” allows to digitally control the shape of the signal edges. |

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| **Title:** | **SQ1 feedback: “a” parameter of pulse shaping** |
| **Reference:** | XIFU-DRE-DMX-FW-R-0190 |
| **Description:** | The parameter “a” of pulse shaping digital filter shall be configurable by command for each column between TBD and TBD, with a resolution TBD. |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** |  |
| **Comment:** |  |

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| **Title:** | **SQ1 feedback: Reference of the DAC** |
| **Reference:** | XIFU-DRE-DMX-FW-R-0200 |
| **Description:** | For each column, the firmware shall drive a DAC DAC5675A-SP to output the feedback signal for the SQUID SQ1. |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** |  |
| **Comment:** |  |

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| **Title:** | **SQ1 feedback: Clock for the DAC** |
| **Reference:** | XIFU-DRE-DMX-FW-R-0210 |
| **Description:** | The firmware shall provide the clock signal to the DACs in charge of the SQUID SQ1 feedback signals. |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** |  |
| **Comment:** |  |

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| **Title:** | **SQ1 feedback: Sampling frequency of the DAC** |
| **Reference:** | XIFU-DRE-DMX-FW-R-0220 |
| **Description:** | The sampling frequency of the DACs in charge of the SQUID SQ1 feedback signals shall be equal to the frequency of the reference clock (fRefClock). |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** |  |
| **Comment:** | Such a high frequency is mandatory to apply the pulse shaping. |

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| **Title:** | **SQ1 feedback: Coarse timing correction** |
| **Reference:** | XIFU-DRE-DMX-FW-R-0230 |
| **Description:** | For each column, the firmware shall have the ability to delay the SQ1 feedback signal by 0 to 33 periods of fRow according to a dedicated command. |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** |  |
| **Comment:** | Selection of pixel 0 among the 34 pixels of the column. |

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| **Title:** | **SQ1 feedback: Fine timing correction** |
| **Reference:** | XIFU-DRE-DMX-FW-R-0240 |
| **Description:** | For each column, the firmware shall have the ability to delay the SQ1 feedback signal by 0 to 32 periods of the reference clock (fRef) according to a dedicated command. |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** |  |
| **Comment:** | Compensation of analog propagation delays. |

## SQ2 feedback (offset compensation)

TBD

## Science data

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| **Title:** | **Science data** |
| **Reference:** | XIFU-DRE-DMX-FW-R-0250 |
| **Description:** | For each column and sequentially for each pixel, the firmware shall compute the science data according to the following formula:  SCp, n = FBp, n + kmixp.Ep, n  p is the pixel index, n is the frame index |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** |  |
| **Comment:** |  |

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| **Title:** | **Science data: “kmix” parameter** |
| **Reference:** | XIFU-DRE-DMX-FW-R-0260 |
| **Description:** | The parameter “kmix” of the science data formula shall be configurable by command for each pixel between TBD and TBD, with a resolution TBD. |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** |  |
| **Comment:** |  |

## Auto-relock

Because of the SQUID characteristic periodicity, the DRE measures the SQUID flux modulo Φ0. According to the slope of the characteristic at the lock point (the SQUID can be operated in the “falling” or in the “rising” slope) a positive or a negative feedback is applied to shift the operating point back to the initial lock position. If the skew rate of the input signal is too high the feedback loop may converge to a secondary lock point of the SQUID characteristic one (or even more) Φ0 away from the initial lock point. This should be avoided because, in this case, the steady state of the feedback signal is far from *IFB*=0 and this is an issue with respect to the dissipation at the 50 mK stage. The delock of the TDM feedback is explained in RD02 section 8.3.1 and in Figure 4.

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|  | Figure 3: Illustration of the TDM delock in the case of a lock point in the SQUID “falling slope”. During normal operations the skew rate at SQUID input is such that the feedback loop converges to the initial lock point. This is illustrated by the feedback “*Fb1*” which corrects the error “*Error1*” and brings the SQUID back to its initial lock point. For too high skew rates (in the case of energies above the X-IFU energy range for example) the error can cross the *Vlock* level. In this case the feedback loop converges on another lock point k.Φ0 away from the initial lock point (k=1 in this plot for *Error2* and *Fb2*). |

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| **Title:** | **Auto-relock** |
| **Reference:** | XIFU-DRE-DMX-FW-R-0270 |
| **Description:** | For each pixel, if the SQUID remains far from its lock point (i.e. Fb – Fb0 > FbThreshold) during too long (i.e. delay > relock delay) the firmware shall reset the feedback to its lock point value (i.e Fb0). |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** |  |
| **Comment:** | See Figure 5 |

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| **Title:** | **Relock delay (relockDelay)** |
| **Reference:** | XIFU-DRE-DMX-FW-R-0280 |
| **Description:** | The parameter “**relockDelay**” shall be configurable by command for each column between TBD and TBD, with a resolution TBD. |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** |  |
| **Comment:** | See Figure 5 |

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| **Title:** | **Feedback Threshold (fbThreshold)** |
| **Reference:** | XIFU-DRE-DMX-FW-R-0290 |
| **Description:** | The parameter “**fbThreshold**” shall be configurable by command for each column between TBD and TBD, with a resolution TBD. |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** |  |
| **Comment:** | See Figure 5 |

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|  | Figure 4: Relock process. |

METTRE A JOUR CETTE FIGURE POUR FAIRE APPARAITRE fbThreshold

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| **Title:** | **Delock monitoring** |
| **Reference:** | XIFU-DRE-DMX-FW-R-0300 |
| **Description:** | The firmware shall monitor the number of Auto-relocks for each pixel and report these values in the housekeeping (TBC). |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** |  |
| **Comment:** |  |

## Diagnostic functions

|  |  |
| --- | --- |
| **Title:** | **Loop delay characterization for SQ1 feedback signal** |
| **Reference:** | XIFU-DRE-DMX-FW-R-0310 |
| **Description:** | For each column, the firmware shall have the ability to characterize the delay in the SQ1 feedback loop (i.e. delay between the SQ1 feedback signal at firmware output and the Error signal at firmware input). |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** |  |
| **Comment:** |  |

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| **Title:** | **Loop delay characterization for SQ2 feedback signal** |
| **Reference:** | XIFU-DRE-DMX-FW-R-0320 |
| **Description:** | For each column, the firmware shall have the ability to characterize the delay in the SQ2 feedback loop (i.e. delay between the SQ2 feedback signal at firmware output and the Error signal at firmware input). |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** |  |
| **Comment:** |  |

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| **Title:** | **Test patterns** |
| **Reference:** | XIFU-DRE-DMX-FW-R-0330 |
| **Description:** | For each column, the firmware shall have the ability to send 2 test patterns on each DAC output. The content of the test patterns shall be configurable by commands. The length of the test patterns is TBD. |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** |  |
| **Comment:** |  |

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| **Title:** | **Dump of raw data** |
| **Reference:** | XIFU-DRE-DMX-FW-R-0340 |
| **Description:** | The firmware shall have the ability to send a dump of raw data to the EP over a duration of TBD s. The raw data are selected by command and can be one of the following:   * The ADC values of the error signal in column 0 * The ADC values of the error signal in column 1 * The ADC values of the error signal in column 2 * The ADC values of the error signal in column 3 |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** |  |
| **Comment:** | A single acquisition of raw data can be requested at the time. |

## TM/TC

### Management of analogue housekeepings

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| --- | --- |
| **Title:** | **Acquisition of analogue housekeepings** |
| **Reference:** | XIFU-DRE-DMX-FW-R-0350 |
| **Description:** | The firmware shall manage the acquisition of 16 (TBC) analogue housekeepings from the DEMUX module (voltages and temperatures). The frequency for the HK sampling is 2 Hz (TBC) +/- TBD Hz. |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** |  |
| **Comment:** |  |

### Science data and housekeepings interface

The TM link between the TDM firmware and the EP shall optimize the number of wires with an acceptable signal frequency (i.e. < 50 MHz). With 4 columns per FPGA, 34 pixels per columns, 16 bits per value and a sampling rate of 150 Ksps, the data rate at the firmware outrput is 340 Mbits/s. 8 serial lines are needed to reduce the data rate per line below 50 Msps. The interface is handled with the following signals (see details on Figure 6, Figure 7, Table 15 and Table 16):

* A clock (CLK)
* A control line (CTRL)
* 8 data lines

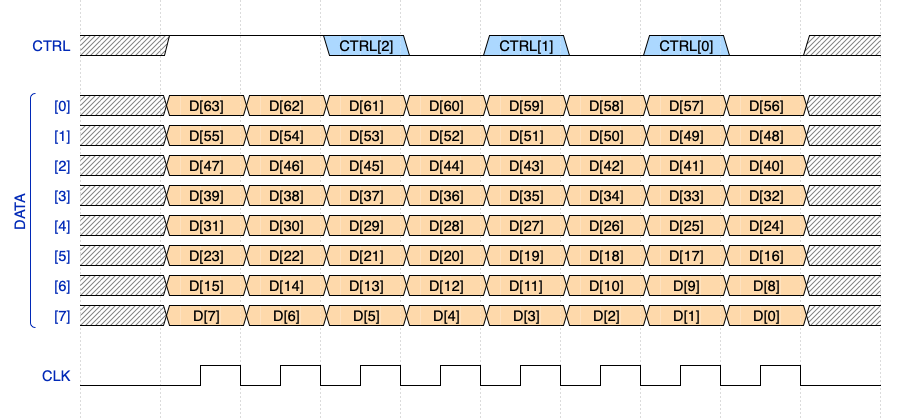


Figure 5: TM protocol for data and housekeepings.

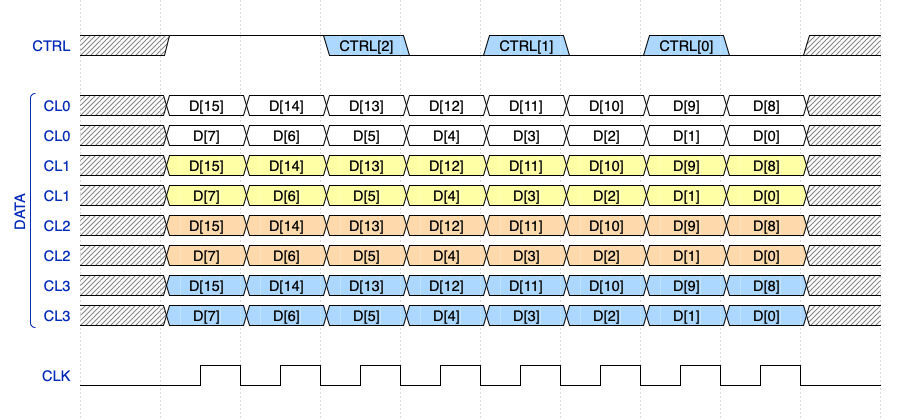


Figure 6: TM protocol for the transmission of data. Each pair of lines is dedicated to a column.

Table 15: Description of TM control parameter (CTRL).

|  |  |  |  |
| --- | --- | --- | --- |
| CTRL |  | Type of Data | Comment |
| 000 | DAT | DATA word (Science or HK) |  |
| 001 |  | First word of science data packet |  |
| 010 |  | First word of ADC Col0 dump packet |  |
| 011 |  | First word of ADC Col1 dump packet |  |
| 100 |  | First word of ADC Col2 dump packet |  |
| 101 |  | First word of ADC Col3 dump packet |  |
| 110 |  | First word of HK data packet |  |
| 111 | EOD | End of data (Science or HK) |  |

|  |  |
| --- | --- |
| **Title:** | **Transfer of science data and housekeepings** |
| **Reference:** | XIFU-DRE-DMX-FW-R-0360 |
| **Description:** | The firmware shall transmit the science data and the housekeepings according to the protocol described in Figure 6, Figure 7, Table 15. |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** |  |
| **Comment:** |  |

|  |  |
| --- | --- |
| **Title:** | **Reception of telecommands** |
| **Reference:** | XIFU-DRE-DMX-FW-R-0370 |
| **Description:** | The firmware shall receive its telecommands according to the protocol defined in RDXX. |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** |  |
| **Comment:** |  |