Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER– III(NEW) EXAMINATION – WINTER 2022

Subject Code:3130704 Date:27-02-2023

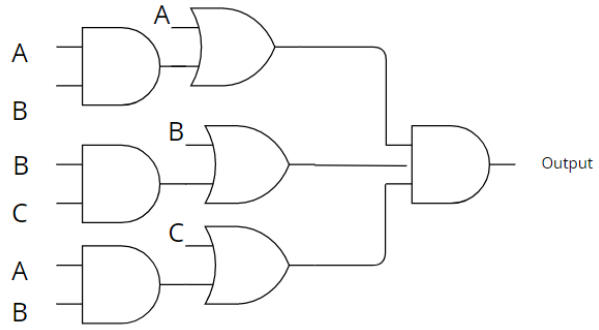
Subject Name:Digital Fundamentals

Time:02:30 PM TO 05:00 PM Total Marks:70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			Marks
Q.1	**(a)**	Implement NOR, AND, & OR gates using NAND gates only	**03**
	(b)	Wrtite the boolean expression for the logic diagram given below and simplify it as much as possible and draw the logica digarm that implements the simplified expression	**04**



	(c)	Do as directed: 1. Convert $(75.75)_{10}$ = (____) $_8$ = (____)16 2. Convert $(101.10)_{16}$ = (__)$_8$ 3. Add $(17)_{10}$ and $(-25)_{10}$ using 8-bit 2's complement	**07**
Q.2	**(a)**	Explain SR flip-flop using characteristic table & characteristic equation	**03**
	(b)	Explain 4-bit parallel binary adder with neat and clean diagram	**04**
	(c)	Obtain the set of prime implicants for Function F= $\sum$ m (1,2,3,5,6,7,8,9,12,13,15)	**07**
		OR	
	(c)	A combinational logic circuit is defined by the functions: F1= Σ (0,1,2,4) and F2= Σ (0, 5, 6,7). Implement the circuit with a PLA having three inputs, four product terms and two outputs.	**07**
Q.3	**(a)**	Differentiate synchronous counter and asynchronous counter	**03**
	(b)	Explain BCD adder using two 4-bit adder IC and a correction -detector circuit	**04**
	(c)	Do the conversion of JK flip flop to T flip flop and D flip flop to JK	**07**
		OR	
Q.3	**(a)**	Design 4 X 16 decoder using two 3 X 8 decoders	**03**
	(b)	List and explain in detail Binary codes with example	**04**
	(c)	Design mod-6 asynchronous counter using T flip flop	**07**
Q.4	**(a)**	Reduce the expression Σ (2, 3, 6,7,8,10,11,14) using K-map	**03**

	(b)	Do as directed: 1. Add 25+17 in BCD 2. Add 37 +28 in XS-3	**04**
	(c)	With a neat block diagram explain the function of encoder. Explain priority encoder?	**07**
		OR	
Q.4	**(a)**	Explain R-2R ladder type D/A converter	**03**
	(b)	Implement the following Boolean functions with a 3 x 1 multiplexer F (w, x, y, z) = Σ (2, 3, 5, 6, 11, 14, 15)	**04**
	(c)	Design Combinational circuit for Binary to Xs-3 conversion	**07**
Q.5	**(a)**	Compare TTL, ECL, & CMOS logic families.	**03**
	(b)	Draw truth table of 2-bit digital comparator	**04**
	(c)	List out various commonly used D/A converters. Draw & explain any one D/A converter.	**07**
		OR	
Q.5	**(a)**	A combinational logic circuit is defined by the functions: F1= Σ (0,1,2,5,7) and F2= Σ (1, 2,4, 6). Implement the circuit with a PROM	**03**
	(b)	Explain types of shift-register and their application	**04**
	(c)	List out various commonly used A/D converters. Draw & explain any one A/D converter	**07**

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GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–III (NEW) EXAMINATION – WINTER 2021

Subject Code:3130704 Date:23-02-2022

Subject Name:Digital Fundamentals

Time:10:30 AM TO 01:00 PM Total Marks:70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			MARKS
Q.1	**(a)**	Implement EX-NOR using NAND gate.	**03**
	(b)	Convert the decimal number 225.225 to octal and hexadecimal.	**04**
	(c)	Give classification of logic families and compare CMOS and TTL.	**07**
Q.2	**(a)**	Convert F(A,B,C) = BC+A into standard minterm form.	**03**
	(b)	With logic diagram and truth table, explain the working of 3 line to 8 line decoder.	**04**
	(c)	Explain Successive Approximation A/D converter in detail.	**07**
		OR	
	(c)	A combinational logic is defined by functions: $F_1(A,B,C) = \sum m\,(3,5,6,7)$ $F_2(A,B,C) = \sum m\,(0,2,4,7)$ Implement the circuit with PLA having 3 inputs, 4 product terms & 2 outputs.	**07**
Q.3	**(a)**	Simplify the Boolean expression: $F(x,y,z) = \sum m\,(0,1,3,4,5,7)$	**03**
	(b)	Explain S-R clocked flip flop.	**04**
	(c)	Design full adder circuit using decoder and multiplexer.	**07**
		OR	
Q.3	**(a)**	Generate AND & EX-OR gates using NOR gate.	**03**
	(b)	Implement D flip flop using JK flip flop.	**04**
	(c)	Design a counter to generate the repetitive sequence 0,4,2,1,6.	**07**
Q.4	**(a)**	What is race around condition in JK flip flop.	**03**
	(b)	Construct a ring counter with five timing signals.	**04**
	(c)	Design BCD to Excess 3 code converter using minimum number of NAND gates.	**07**
		OR	
Q.4	**(a)**	Explain 2-bit comparator circuit.	**03**
	(b)	Write a short note on FPGA.	**04**
	(c)	What is Digital to Analog converter? Draw and Explain R-2R DAC.	**07**
Q.5	**(a)**	Perform following operation using 2's complement method. $(11010)_2 - (1000)_2$	**03**
	(b)	Write a short note on Read Only Memory (ROM).	**04**
	(c)	Explain the working of 4 bit binary ripple counter.	**07**
		OR	
Q.5	**(a)**	Obtain the truth table of the function: F = xy+yz+zx .	**03**
	(b)	Implement following functions using ROM. $F_1 = \sum m\,(1,3,4,6)$ and $F_2 = \sum m\,(0,1,5,7)$.	**04**
	(c)	Explain in detail Dual Slope A/D converter.	**07**

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