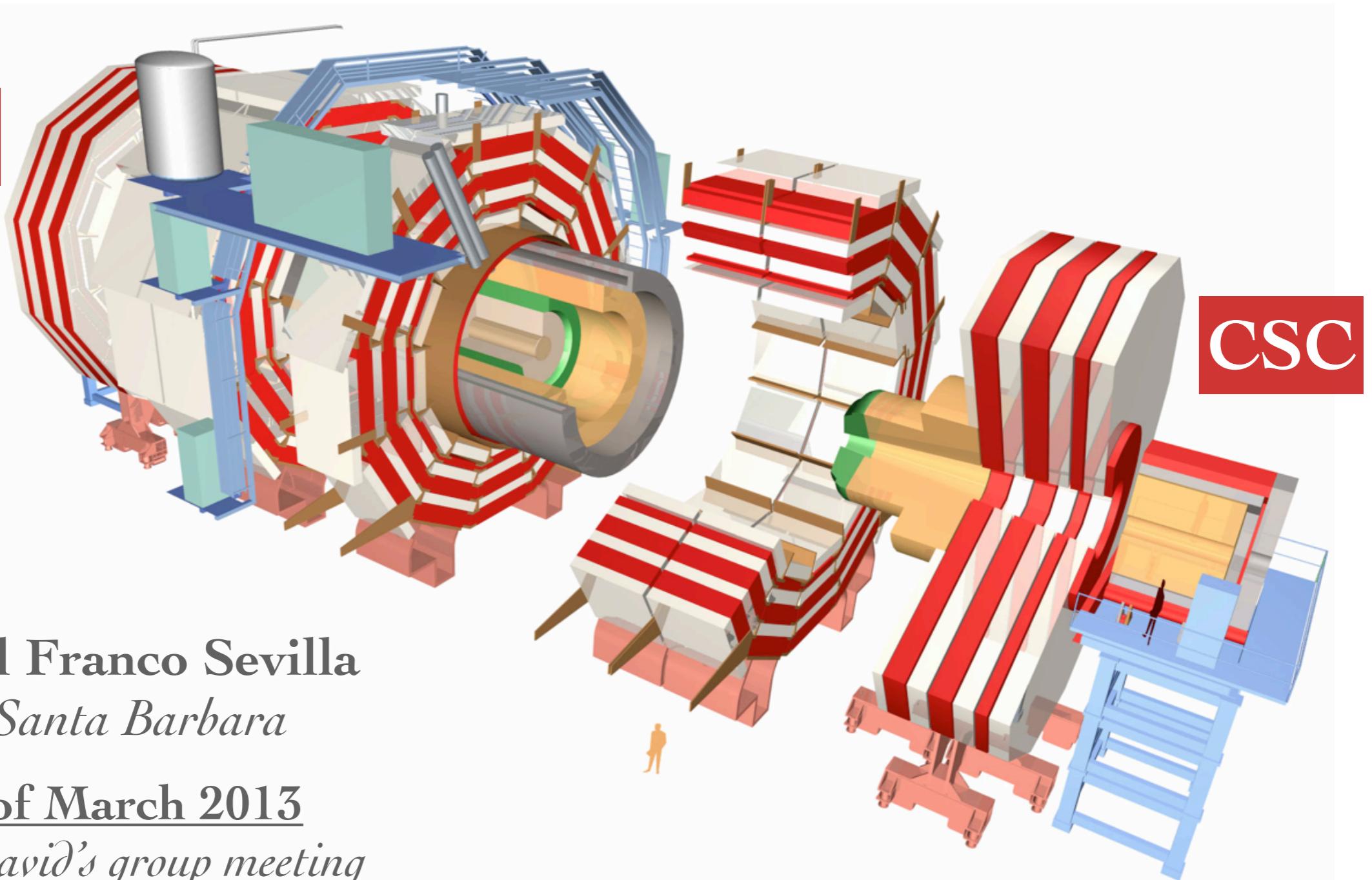


# *ODMB*: UCSB contribution to the CSCs upgrade

CSC



Manuel Franco Sevilla

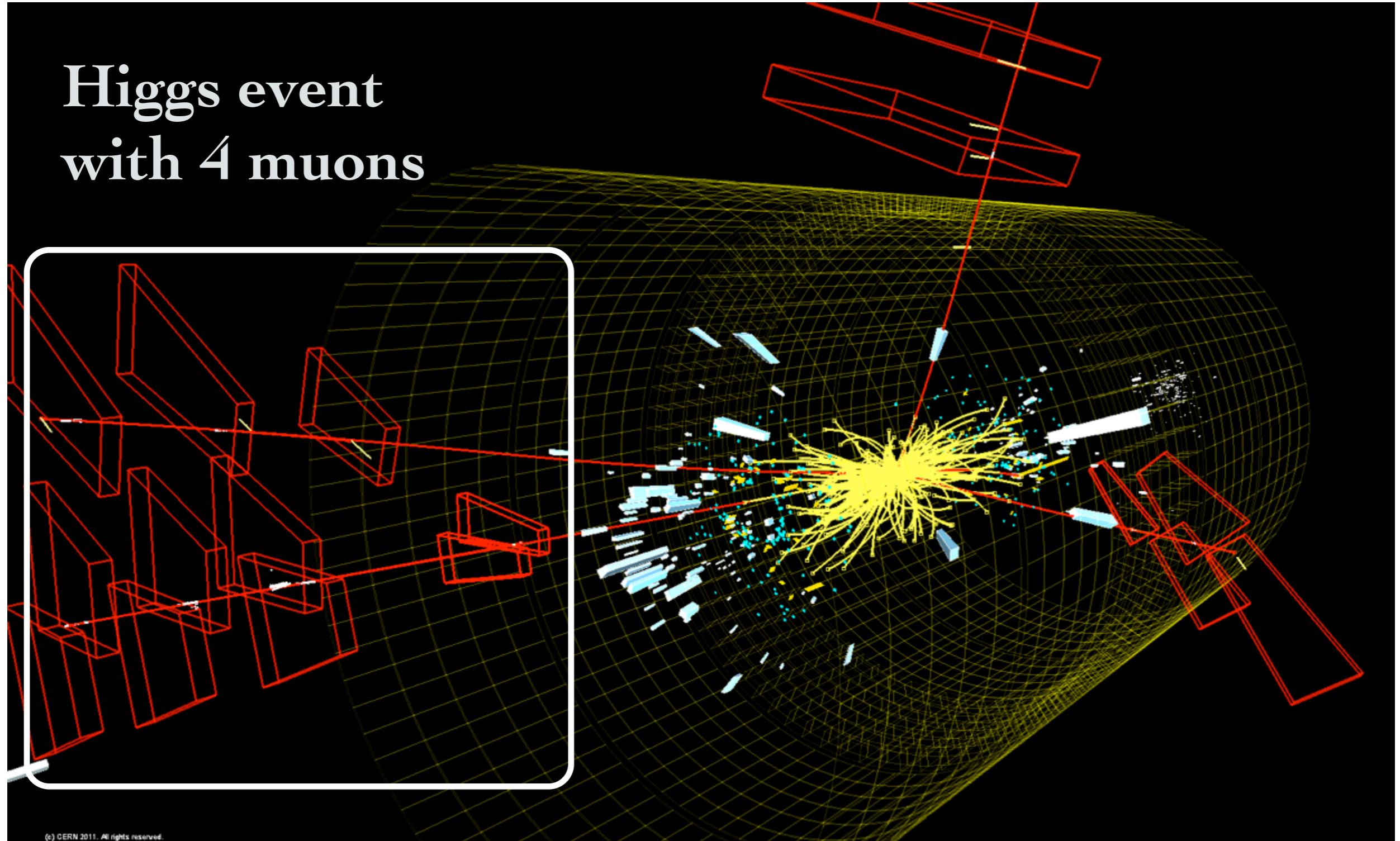
*UC Santa Barbara*

19<sup>th</sup> of March 2013

*Jeff e& David's group meeting*

# CSCs are important!

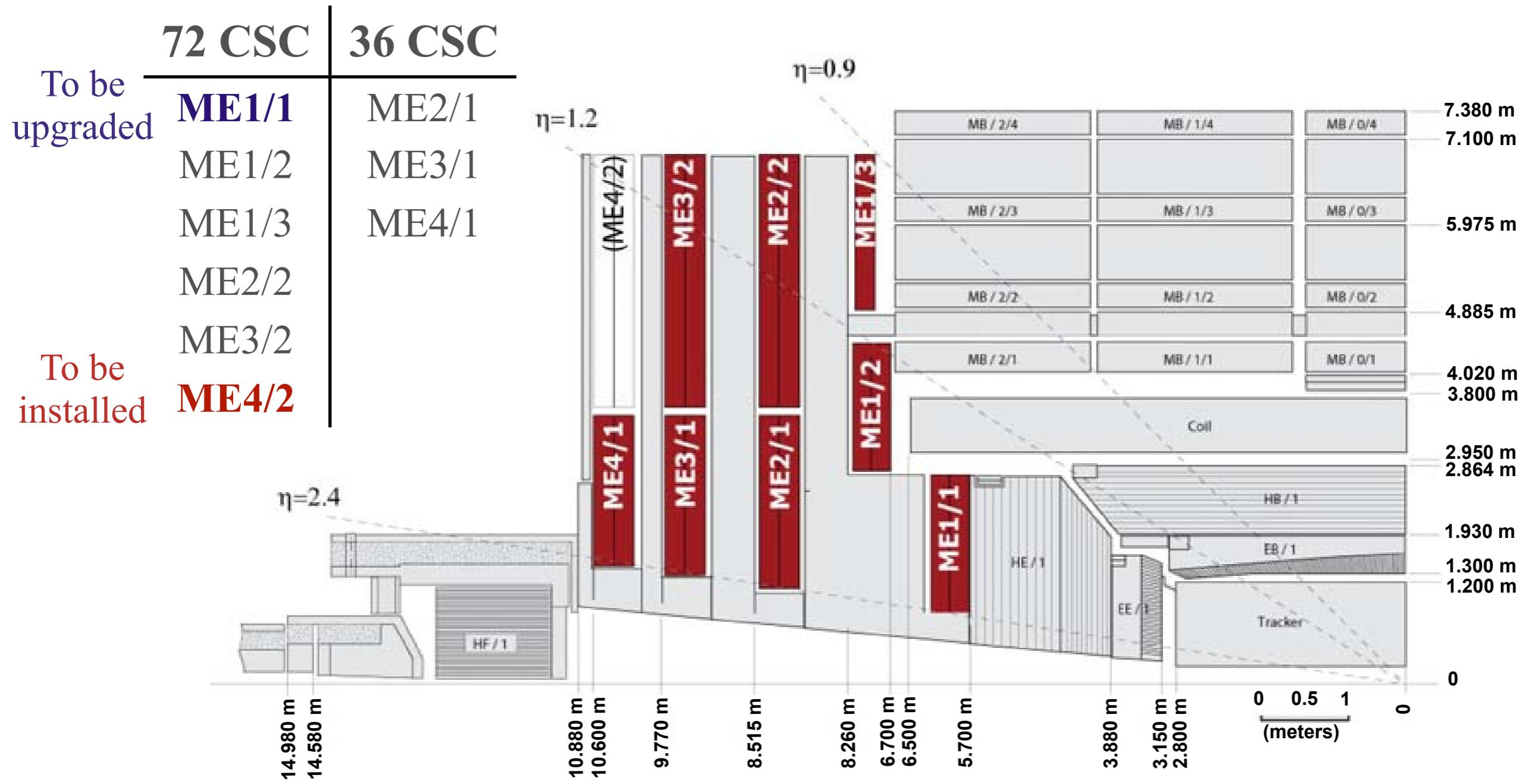
Higgs event  
with 4 muons



(c) CERN 2011. All rights reserved.

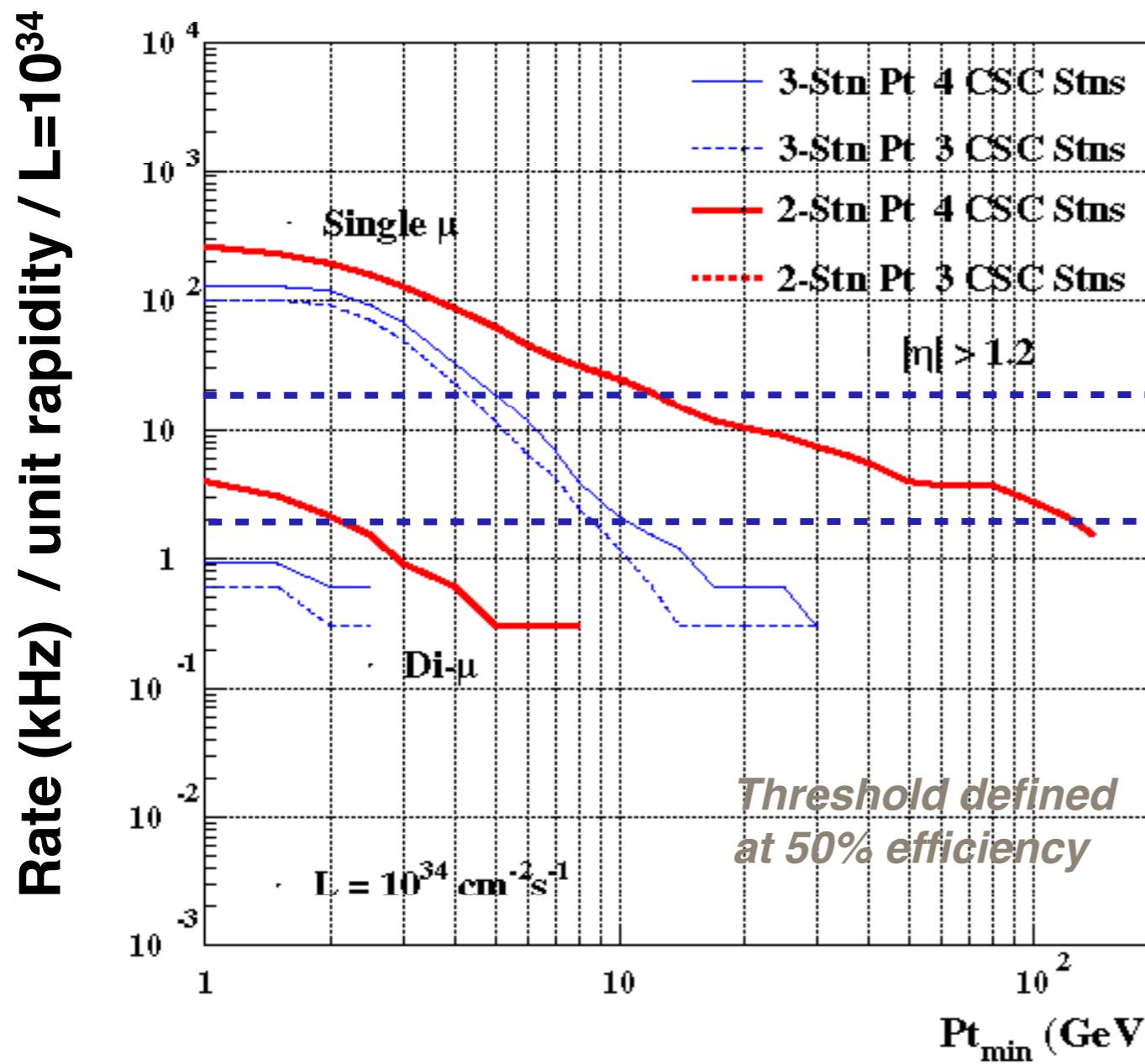
# Endcap muon system

- ~ Consists of 468 CSC (until now, no money/need for ME4/2)



# ME4/2 installation

- ~ L1 trigger uses **2 layers out of 3**, which is adequate for  $p_t > 15 \text{ GeV}$
- ~ With higher luminosities, **3 out of 4 required**



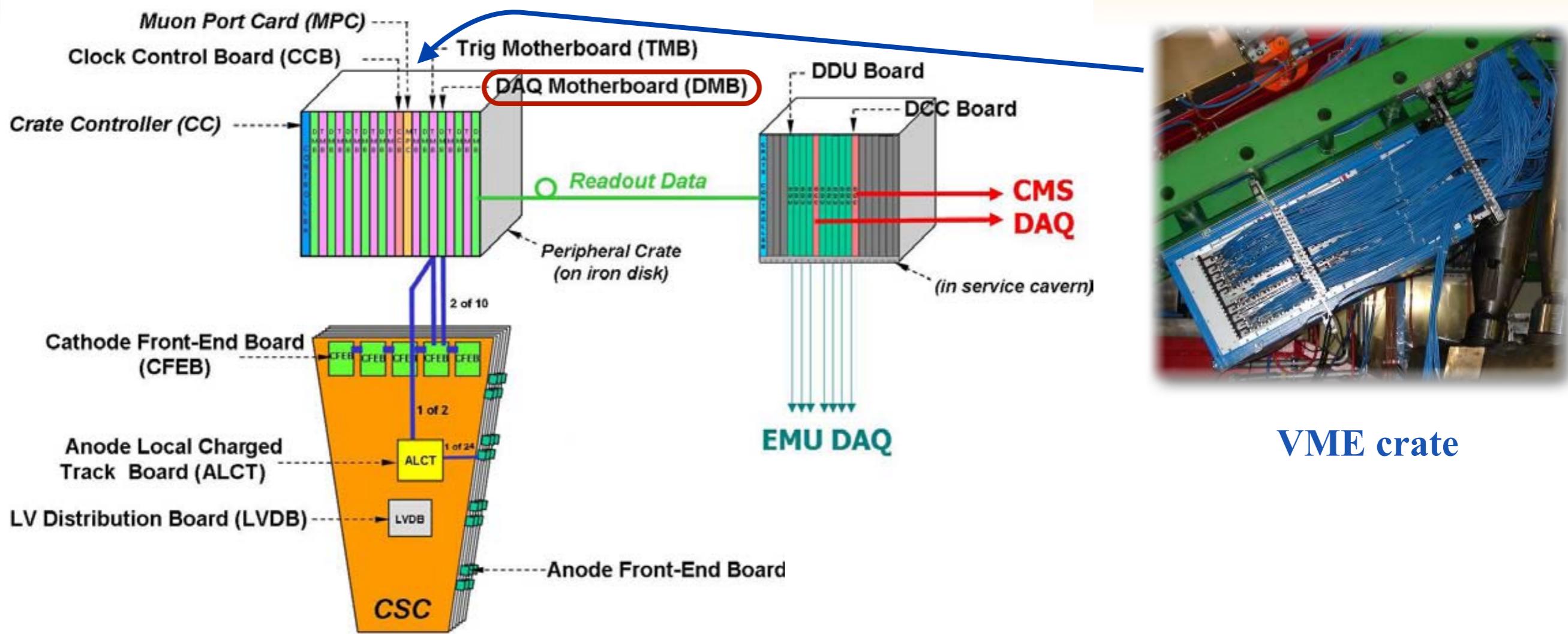
## Targets

$$\mathcal{L} = 10^{33} \text{ cm}^{-2} \text{s}^{-1}$$

$$\mathcal{L} = 10^{34} \text{ cm}^{-2} \text{s}^{-1}$$

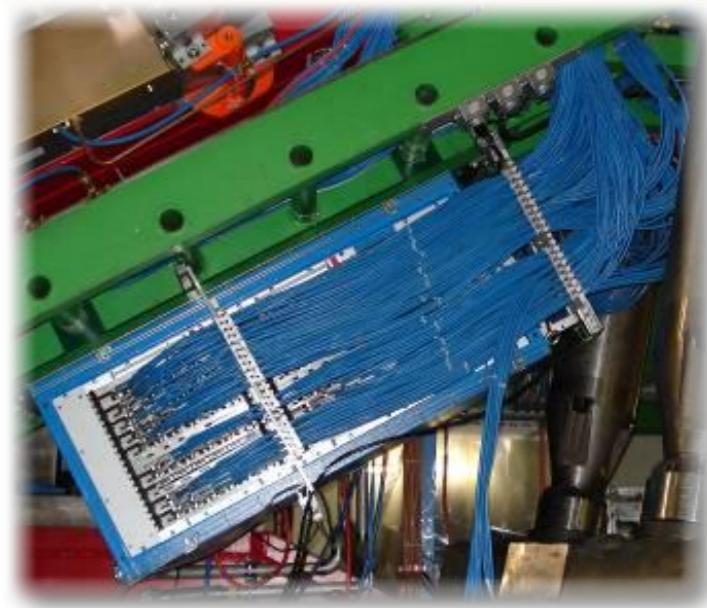
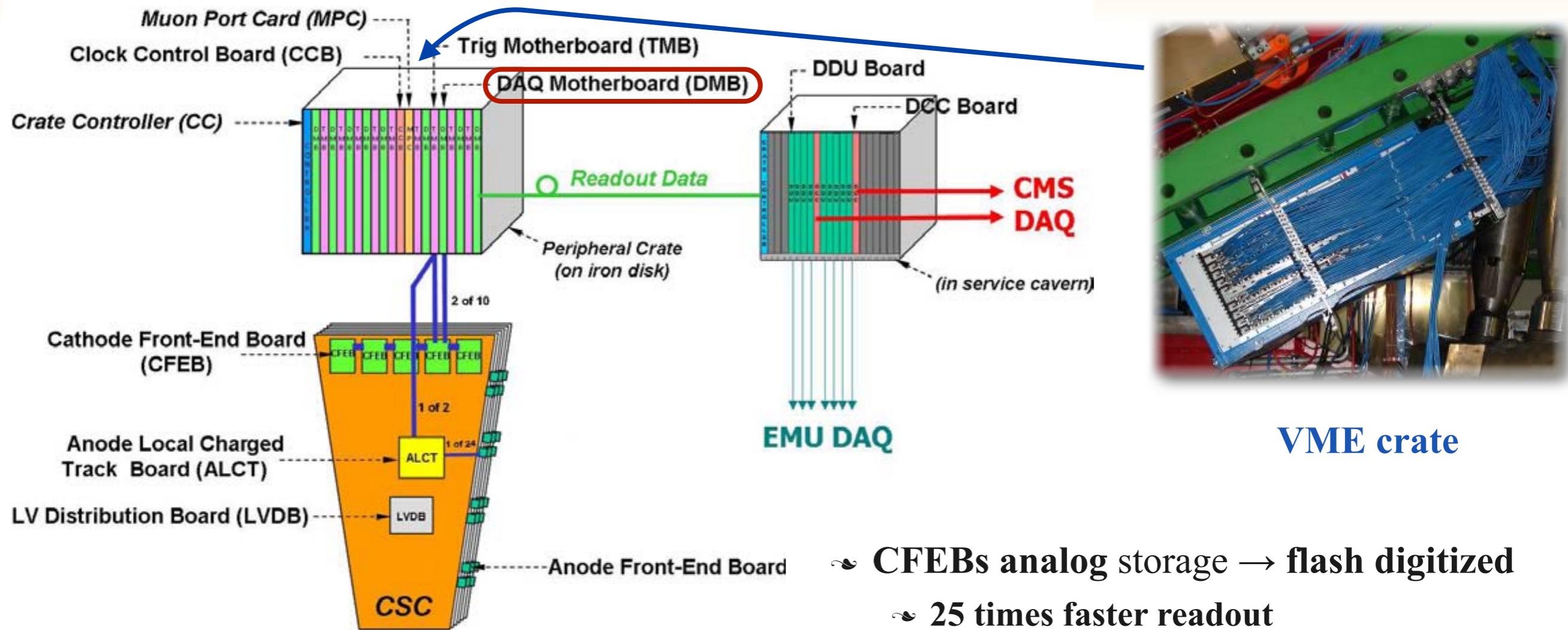
*ME4/2 will provide robust and low-background trigger for  $1.2 < \eta < 1.8$*

# ME1/1 upgrade



- ~ Innermost muon station, critical for **muon momentum resolution**
- ~ High particle rates at DAQ limit
- ~ *Largest source of deadtime to the entire CMS experiment*

# ME1/1 upgrade

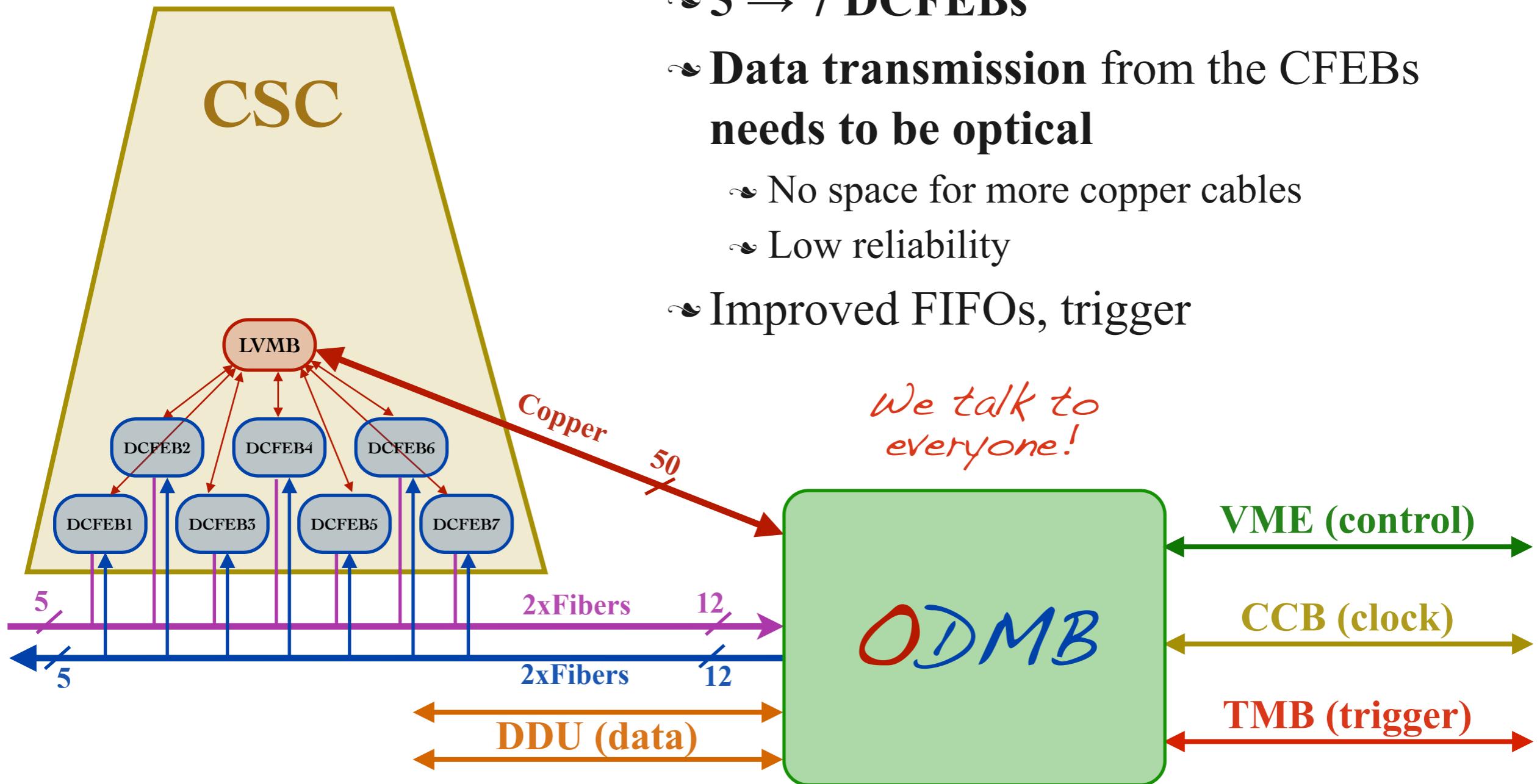


**VME crate**

- ~ Larger FPGA for ALCT
  - ~ Minimizes impact of neutron SEUs
- ~ Optical link for MPC
  - ~ More than 3  $\mu$  stubs per  $60^\circ$  sector

- ~ CFEBs analog storage  $\rightarrow$  flash digitized
- ~ 25 times faster readout
- ~ Smaller: 5 CFEBs  $\rightarrow$  7 DCFEBs
- ~ Restore trigger for  $2.1 < \eta < 2.4$
- ~ New optical DMBs and TMBs
  - ~ More trigger patterns, match ALCT timing  
 $\Rightarrow$  reduce ghosting

# DMB → ODMB

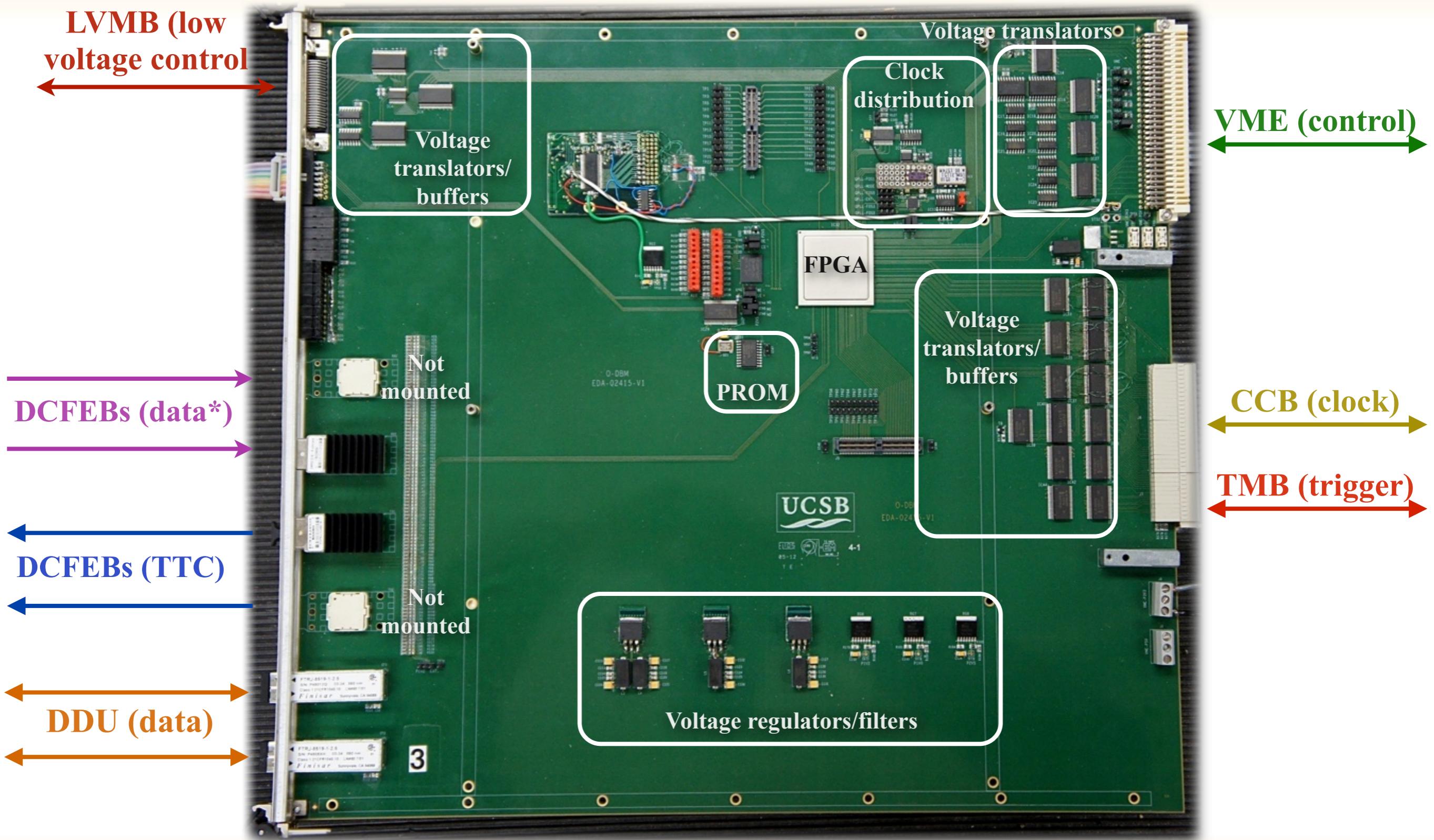


Three V1 Prototypes built in April 2012



# ODMB.V1

[u][c]  
[s][b]

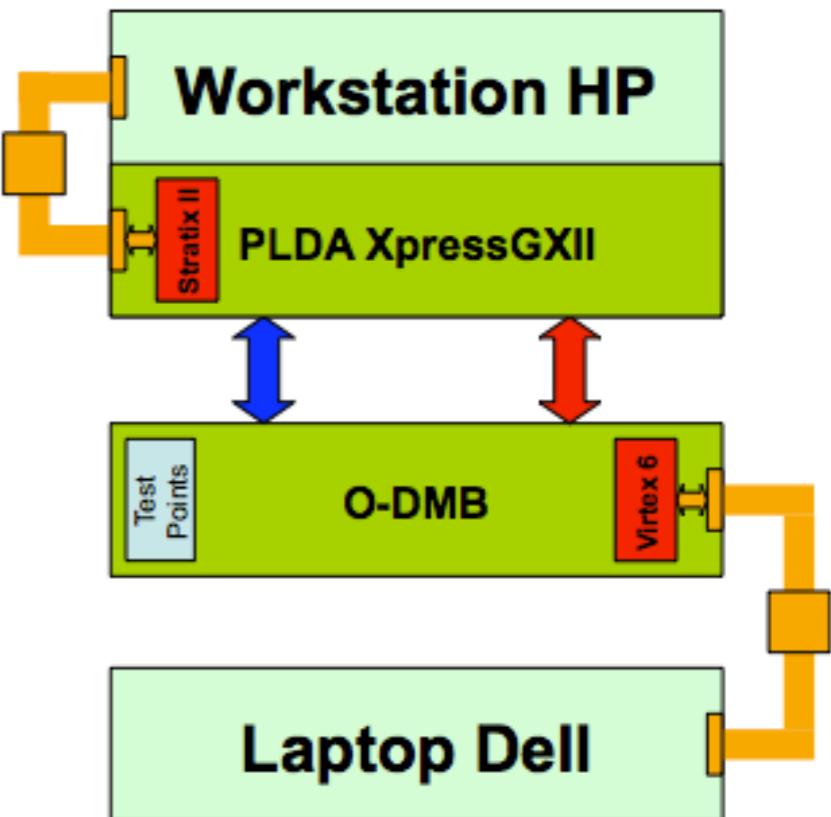


# Old test bench

- ~ VME crate emulated with another FPGA until Dec 2012
- ~ Difficult to make work...

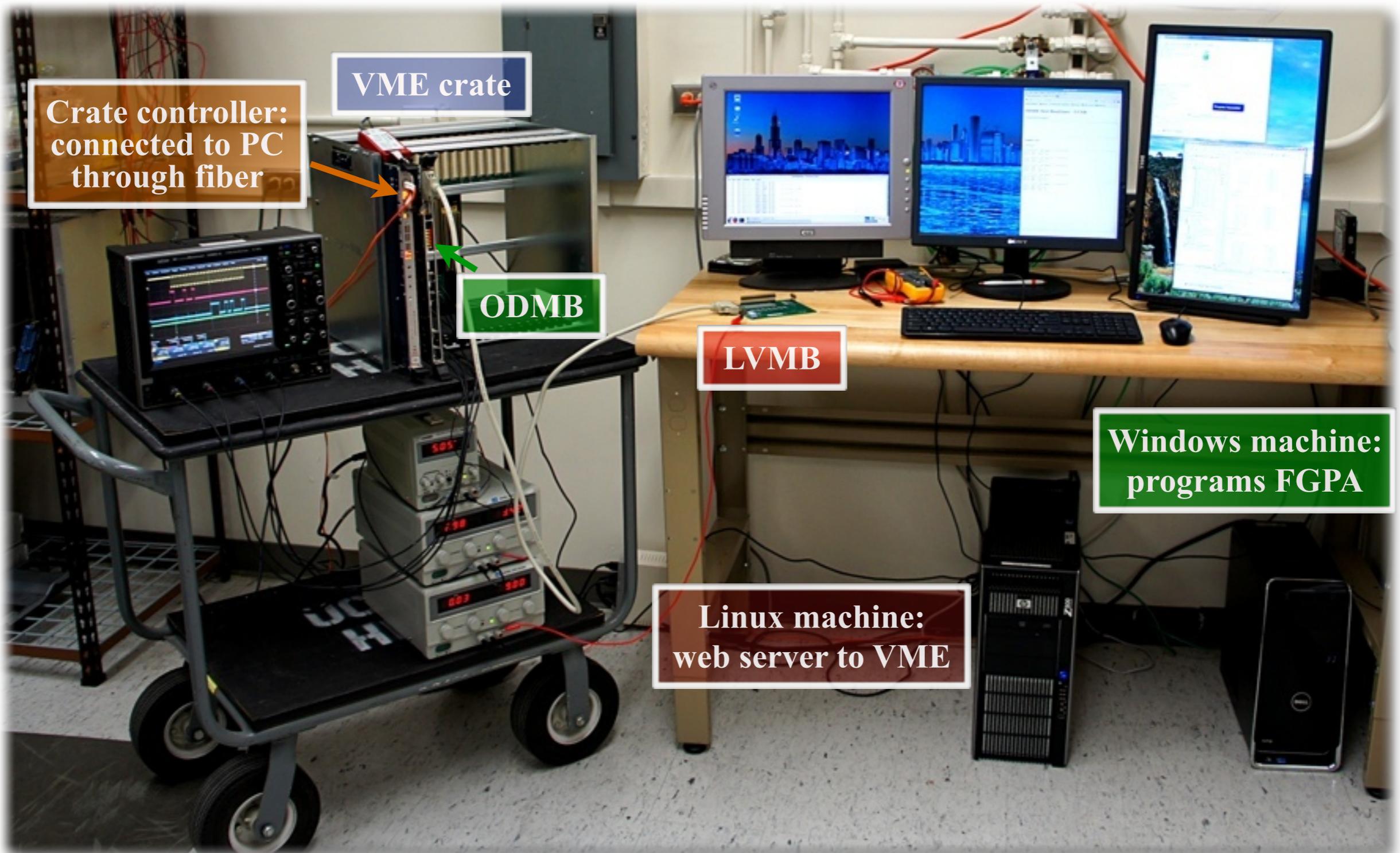


All in Guido's office!

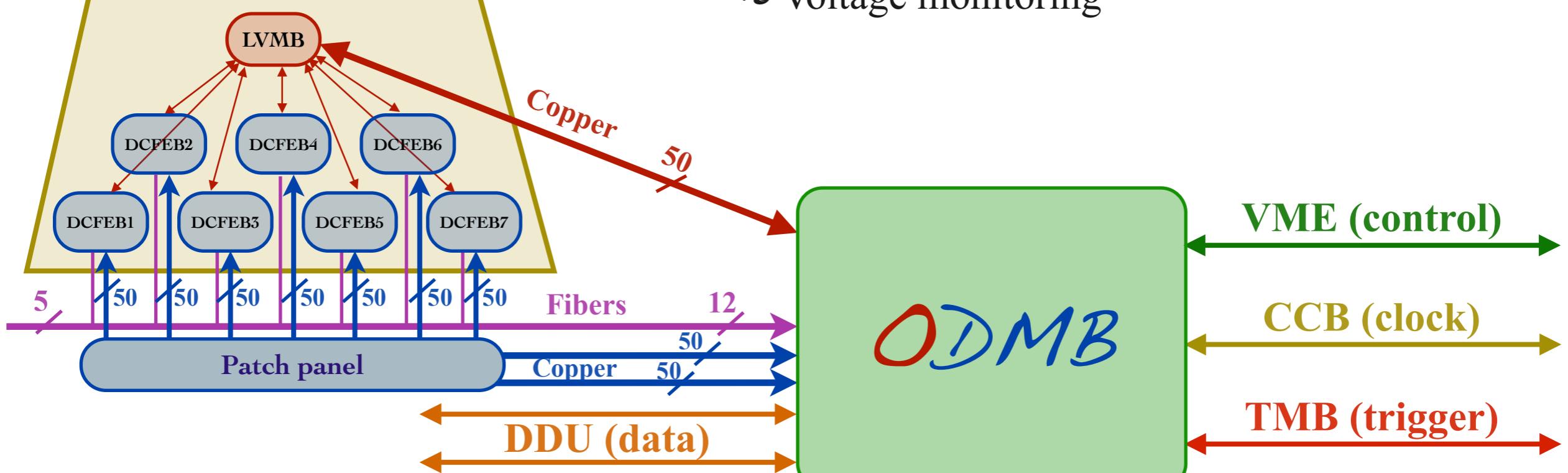


# New test bench

Manpower: Guido, Frank, Manuel, Kristen



## CSC

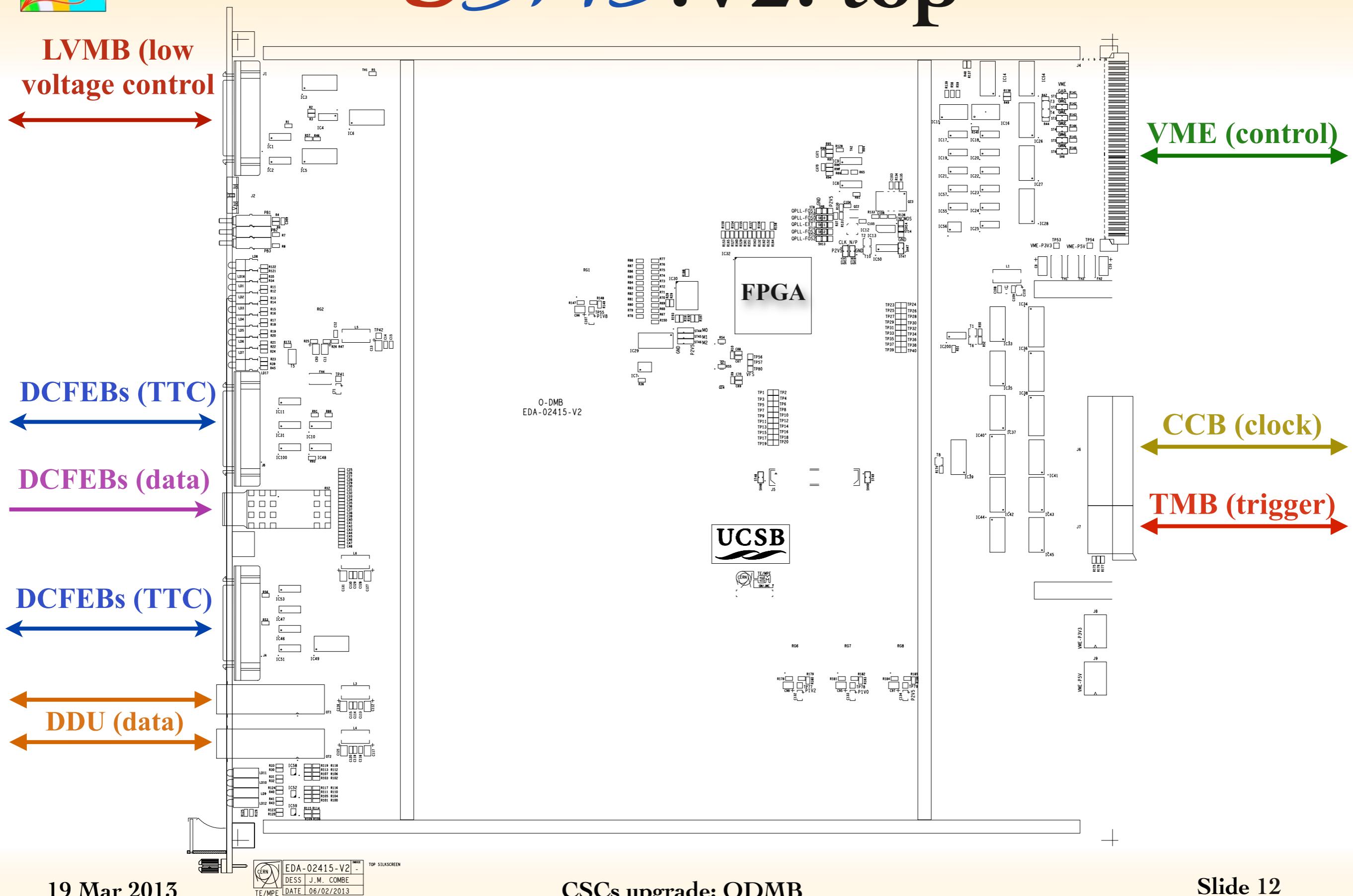


Prototype V2



# ODMB.V2: top

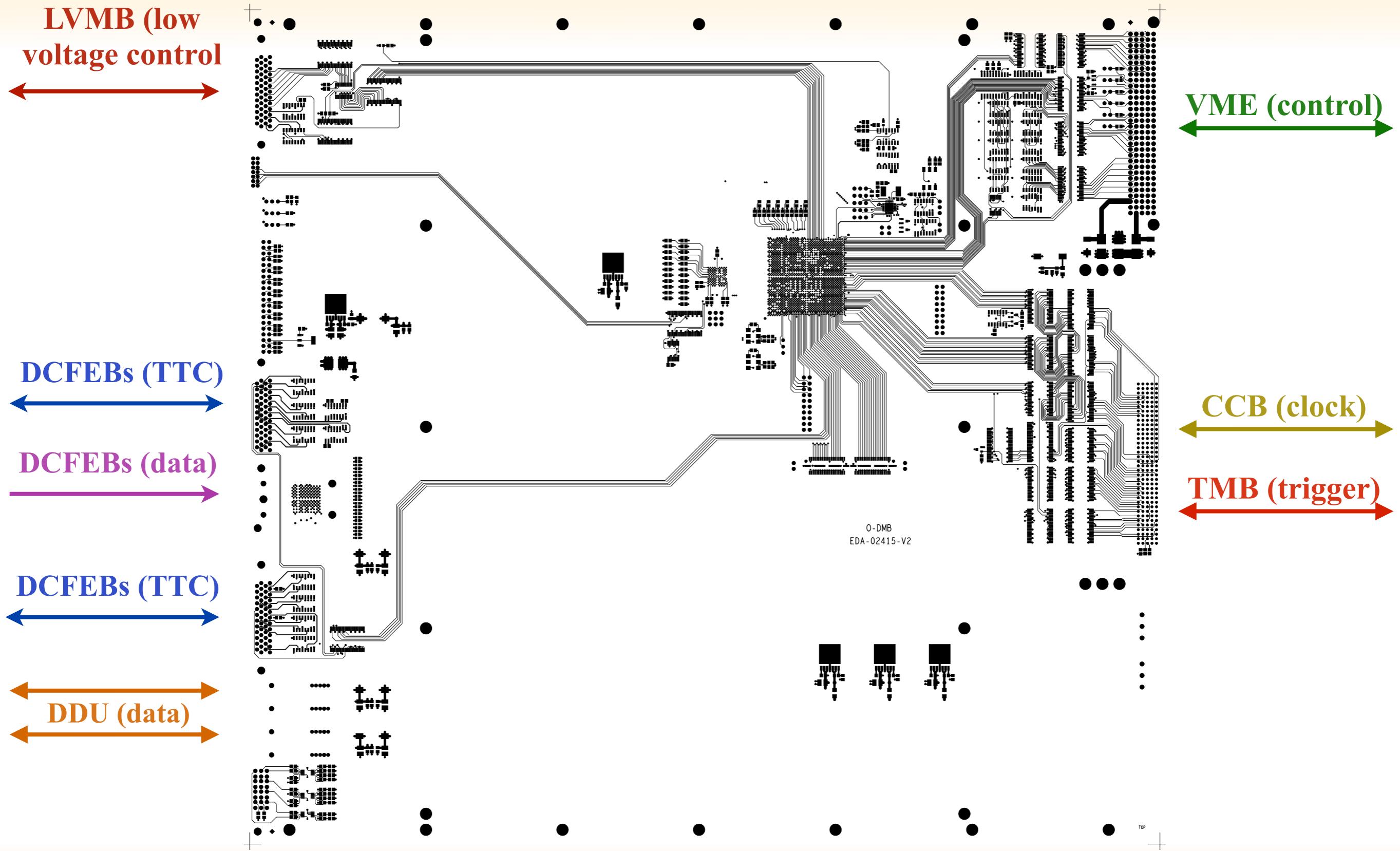
$$\begin{bmatrix} u \\ c \\ s \\ b \end{bmatrix}$$





# ODMB.V2: layer 1/12

[u][c]  
[s][b]



# Schedule

- ~ ODMB.V2 prototypes into production February
  - ~ Assembly to start this week
  - ~ We will have **3 months** to test them and fix any problems
- ~ Lots of work to finish writing **firmware**
  - ~ Translation of previous FW at 70% (schematics → VHDL)
  - ~ New features (FIFOs, trigger...)
  - ~ Systematic testing of all configurations

