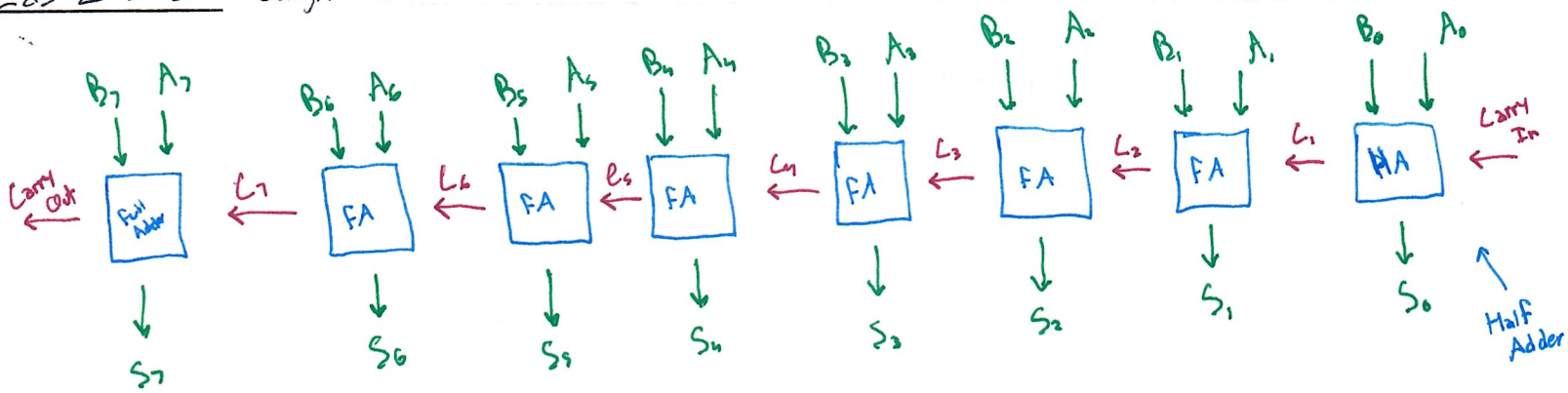
Vivian Do

CSC 3210

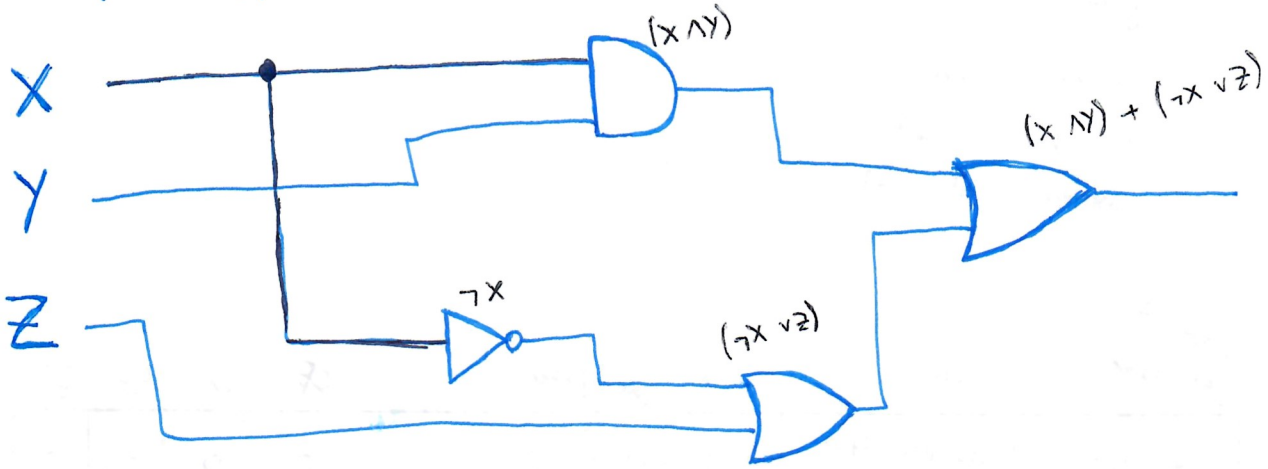
Lab 2 b & c

Lab 2 b 1: design a 8-bit adder with block diagram



Lab 2 b 2: draw circuit for boolean expression: P = (X and Y) or (not X or Z)

$P = (X \wedge Y) \vee (\neg X \vee Z)$



AND = 

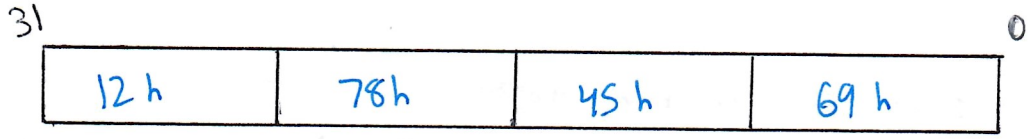
OR = 

NOT = 

Gates Needed

Lab 2 c 1 : store 12784569h in EAX register

12784569h → EAX register



4 bytes

Lab 2 c 2 : for each add instruction in this exercise, assume that EAX contains the given contents before instruction is executed

- numbers in hex
- fill out chart
- assume that numbers = signed integers

Contents of EAX (Before)	Instruction	Contents of EAX After	CF	OF	SF	ZF	
00000040	add eax, 40	10000000	0	0	0 (+vs)	0	(Non-zero results)
FFFFFF40	add eax, 40	FFFFFF80	0	0	1 (negative)	0	
00000040	add eax, -40	0	0	0	0 (+vs)	1	(zero result)

1) 0000 0040 => 0100 0000, 40 => 0100 0000
01 00 0000 + 01 00 0000 = 1000 0000

2) FF FF FF 40 + 0000 0040 = FFFFFF80

3) 00000040 - 00000040 = 0