



**FACULTY OF ENGINEERING AND TECHNOLOGY  
ELECTRICAL AND COMPUTER ENGINEERING  
DEPARTMENT  
ADVANCED DIGITAL DESIGN ENCS3310  
COURSE PROJECT**

Homework

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Section 2

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state	$x_1$	$x_2$	$Q$	notes
a	1	1	1	after c
b	0	1	0	" e
c	0	1	1	" a, f
d	1	0	0	" a, e, f
e	1	1	0	" b, d
f	0	0	1	" b, c, d

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- for the following truth table that shows the stable states for a machine implement the circuit using SR latches

	00	01	11	10
a	-,-	c,-	a,1	d,-
b	f,-	b,0	e,-	-,-
c	f,-	c,1	a,-	-,-
d	f,-	-,-	e,-	d,0
e	-,-	b,-	e,0	d,-
f	f,1	c,-	-,-	d,-



	ab	ac	ad	ae	af
b	ae, x				
c	✓	x			
d	ae, x	✓	ae, x		
e	x	✓	x	✓	
f	✓	cb, x	✓	✓	x
a	x				



maximum compatibles

(a, c) (a, f) (b, d) (b, e) (c, f) (d, e) (d, f)

to find minimum compatibles

	00	01	11	10
a, c, f	1,1	c,1	a,1	d,-
b, d, e	f,-	b,0	e,0	d,0

acf = A  
bde = B

↓  $x_1 x_2$

	00	01	11	10
$x_1' = y$	A	A,1	A,1	B,-
$y = 0$	A	A,1	A,1	B,-
$y = 1$	B	A,-	B,0	B,0

Transition table

↓  $x_1 x_2$

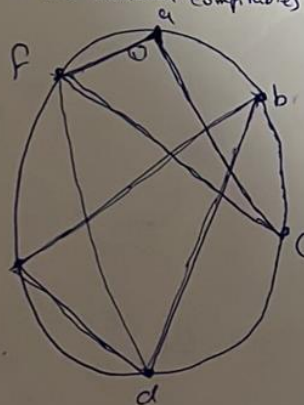
	00	01	11	10
$y = 0$	0	0	0	1
$y = 1$	0	1	1	1

$x_1' x_2'$   
 $y x_2$

↓  $x_1 x_2$

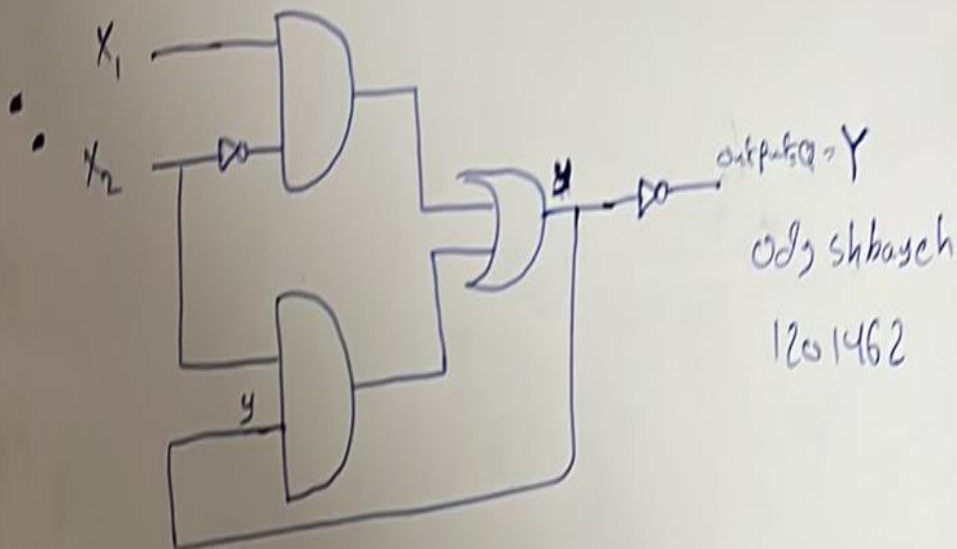
	00	01	11	10
$y = 0$	1	1	1	x
$y = 1$	x	0	0	0

$y' = \text{output}$



(a, f, c)  
(b, d, e)  
(d, f)

the circuit without implementing using SR latch is:



implementing the circuit using SR latch

Y maps  
S

	$X_1 X_2$			
$Y$	00	01	11	10
0	0	0	1	1
1	1	0	0	1

$$S = X_1 X_2' + X_2 Y$$

	$X_1 X_2$			
$R$	00	01	11	10
0	0	0	1	0
1	1	0	1	0

$$R = X_1 X_2 + X_2 Y$$

circuit

