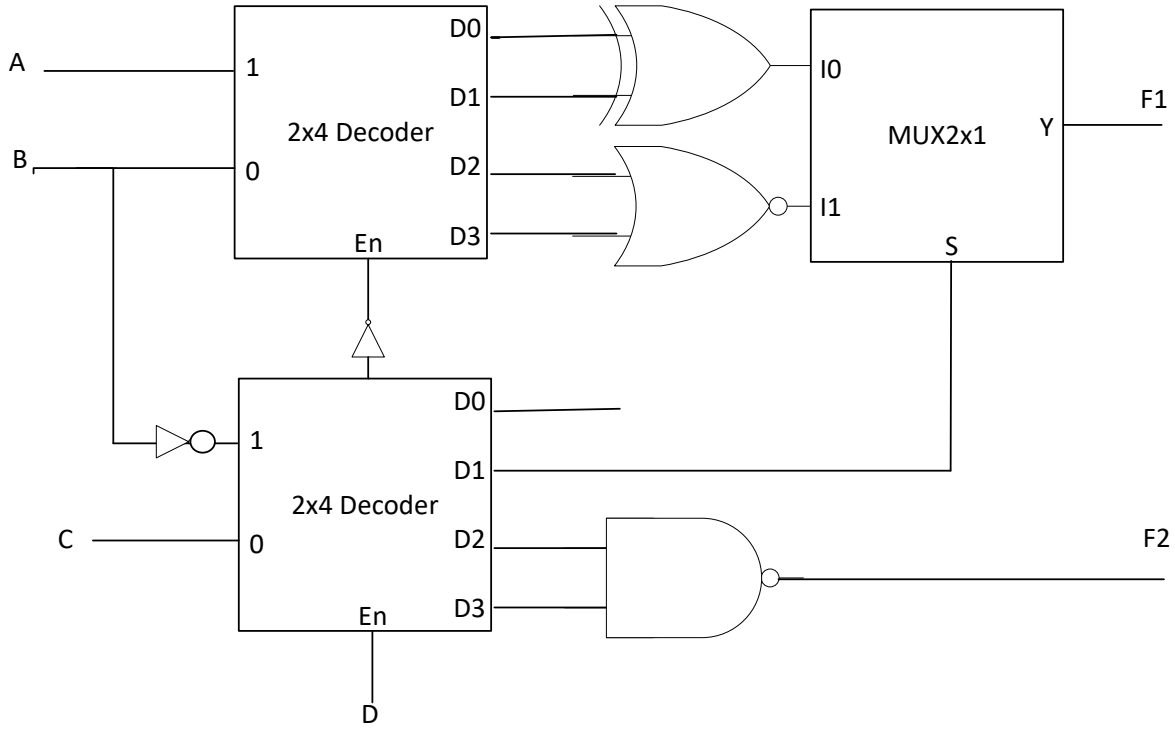
Faculty of Engineering and Technology
Electrical and Computer Engineering Department
Advanced Digital Design ENCS3310
HW#1 report and simulations.

Student name : ody shbayeh
Student ID :1201462

For the following circuit with 4 inputs (A,B,C,D) and two outputs F1, F2:

a. Write a Verilog description for the 2x4 decoder.
b. Write a Verilog description for the 2x1 MUX.
c. Writa a Structural Verilog Description for the Circuit.
d. Derive the truth table and the equations for F1 and F2, and then write a behavioral Verilog description for them.
e. Write a testbench that generates all the cases for part c (or part d).



a. Write a Verilog description for the 2x4 decoder.

```
1  //ody_shbayeh_1201462
2  //decoder with enable module
3      //when the enable is 1 the decoder works as usual
4      //when the enable is zero the output of the decoder is a don't care condition.
5  module decoder2to4(a, b, s, y);
6
7      input a, b, s;
8      output reg [0:3] y;
9
10     always @ (a, b, s)
11     begin
12         if (s == 1)
13         begin
14
15             y[0] <= ~a & ~b;
16             y[1] <= ~a & b;
17             y[2] <= a & ~b;
18             y[3] <= a & b;
19         end
20         else
21         begin
22             y[0] <= 'x;
23             y[1] <= 'x;
24             y[2] <= 'x;
25             y[3] <= 'x;
26
27         end
28     end
29     endmodule
30
```

B Write a Verilog description for the 2x1 MUX.

```
32 //odyshbayeh
33 //1201462
34 //mux 2x1 with selection
35
36 module mux2to1(a, b, s, y);
37     input a, b, s;
38     output reg y;
39
40     always @(a,b,s)
41     begin
42         if (s == 0)
43             y <= a;
44         else
45             y <= b;
46     end
47 endmodule
48
```

C Write a Structural Verilog Description for the Circuit.

```
49
50  //odyshbayeh
51  //1201464
52  //the full circuit module
53  module circuit(a,b,c,d,f1,f2);
54
55      input a,b,c,d;
56      output f1,f2;
57
58      wire [0:1] negbd;
59      wire [0:3] de1;
60      wire [0:3] de2;
61      wire r1;
62      wire r2;
63
64      assign negbd[0]=~b;
65      assign negbd[1]=~d;
66
67
68      decoder2to4 d1(a,b,negbd[1],de1[0:3]);
69      assign r1=de1[0]^de1[1];
70      assign r2= ~(de1[2] | de1[3]);
71
72
73      decoder2to4 d2(negbd[0],c,d,de2[0:3]);
74
75      mux2to1 m1 (r1,r2,de2[1],f1);
76      //another implemintation for the output f1 is :
77          //this is what i understood from task 4 is to write the structural implimentaion for the outputs f1&f2.
78           //assign f1 = (((~de2[1]) & r1) | ((de2[1]) & r2));
79          //also for f2 is : assign f2= ~(de2[2] & de2[3]);
80      nand(f2,de2[2],de2[3]);
81
82      assign f2= ~(de2[2] & de2[3]);
83
84  endmodule
85
```

D Derive the truth table and the equations for F1 and F2, and then write a behavioral Verilog description for them.

D	C	B	A	F1	F2
0	0	0	0	1	X
0	0	0	1	1	X
0	0	1	0	1	X
0	0	1	1	1	X
0	1	0	0	0	X
0	1	0	1	0	X
0	1	1	0	0	X
0	1	1	1	0	X
1	0	0	0	X	1
1	0	0	1	X	1
1	0	1	0	X	1
1	0	1	1	X	1
1	1	0	0	X	1
1	1	0	1	X	1
1	1	1	0	X	1
1	1	1	1	X	1

f1 = (((~de2[1]) & r1) | ((de2[1]) & r2));

f2 is : assign f2= ~(de2[2] & de2[3]);

e Write a testbench that generates all the cases for part c (or part d).

```
module tb_circuit;

    reg a, b, c, d;
    wire f1, f2;

    circuit uut(a, b, c, d, f1, f2);
    //for the following test inputs values i considered the input d wich is the enable for the decoders as the most significant bit
        //so that we can see both values for f1 and f2 when one only of the decoders were on .

    initial begin
        // Initialize inputs with 0 value and start the loops after 5ns.
        a = 0;
        b = 0;
        c = 0;
        d = 0;
        #5ns;
    end
    always #80ns d=~d;
        always #40ns a=~a;
            always #20ns b=~b;
                always #10ns c=~c;


endmodule

```

Simulation results of the test-bench :

Note * I considered the enable as the most significant bit and a as the least to get the simulation organaized.

The simulation time is : 160ns.