Tritone: A Balanced Ternary CMOS Processor Architecture for the Post-Moore Era

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***Abstract*—As binary CMOS scaling approaches physical and economic limits, interconnect energy and routing congestion increasingly dominate system-level cost. Multi-valued logic offers a potential lever: increasing radix raises information per wire and can reduce global interconnect width for a fixed payload. This work analyzes balanced ternary logic and presents a processor-level case study, Tritone, a 27-trit dual-issue superscalar in-order RISC core implemented in both the ASAP7 predictive 7 nm FinFET design kit and the SkyWater SKY130 130 nm process. We summarize the radix-economy motivation, the device-level mechanism of tunnelling-based ternary CMOS (TCMOS) that stabilizes an intermediate logic level, and an RTL-to-GDSII methodology that reuses Boolean EDA tools through a two-bit virtual encoding. Key contributions include: (1) BSIM4-validated multi-threshold ternary cell design using the SKY130 PDK with 74 mV mid-level accuracy; (2) a 27-trit carry-lookahead adder with 3-level hierarchical lookahead for $O(\log n)$ critical path, fully integrated into the CPU datapath using 9-trit padding; (3) branch prediction achieving 92% accuracy on benchmark workloads; and (4) 100% ISA test coverage across 19 verification programs. The ASAP7 v8 implementation with CLA achieves timing closure at 1.5 GHz target with +285 ps slack, demonstrating $\sim$2.6 GHz maximum achievable frequency in just 41 μm^2 active-cell area—a 7.5$\times$ frequency improvement and 63$\times$ area reduction versus the SKY130 v8 (active-cell area) implementation. The SKY130 implementation with CLA-enabled datapath achieves Fmax=349 MHz (exceeding 300 MHz target) consuming 399 μW (v8) vs 967 μW (v6 ripple-carry) at typical 25°C and 1.8 V—a 59% power reduction. Benchmarks demonstrate 1.45 average IPC (72.5% of dual-issue theoretical maximum). Both implementations pass full DRC signoff with zero violations.**

***Index Terms*—balanced ternary, multi-valued logic, tunnelling CMOS, TCMOS, radix economy, OpenROAD, ASAP7, RISC processor, interconnect scaling, dual-issue superscalar**

I. Introduction

Over five decades, binary CMOS and Boolean logic jointly delivered the exponential improvements often summarized by Moore's Law. At advanced nodes, however, further scaling faces diminishing returns: wire resistance/capacitance, electromigration, and routing congestion increasingly constrain frequency and energy, so that interconnect power can rival or exceed transistor switching power in many designs [1].

One underused design dimension is the radix of information representation. Information-theoretic analyses of radix economy show that the hardware cost to represent a numeric range is minimized near base e; among integer radices, base-3 is optimal [2]. In practical terms, a ternary wire can carry $\log_2(3) \approx 1.585$ bits of information. Thus, a 32-bit payload can be transported with 21 ternary wires ($\lceil 32/1.585 \rceil = 21$) instead of 32 binary wires, reducing global interconnect width by $\sim$34%.

Historically, ternary computing has been held back by device technology: conventional CMOS inverters do not naturally produce a robust third level without static power (e.g., resistive dividers) or tight multi-threshold control. Recent work on tunnelling-based ternary CMOS (TCMOS) demonstrates a manufacturable path to a stable intermediate state using off-state band-to-band tunnelling (BTBT) currents [3].

This work reframes these concepts around a concrete processor case study (Tritone): a 27-trit balanced-ternary **dual-issue superscalar** RISC core reported in a predictive 7 nm FinFET PDK (ASAP7) with an extremely small active-cell footprint. We focus on what must be true for the claims to be meaningful (supply voltage conventions, representational-vs-computational density, and fair comparison baselines) and provide a set of publication-ready figures and tables.

II. Theoretical Foundations of Balanced Ternary

A. Radix Economy and Wire Efficiency

The radix economy for representing integers up to N in base R can be approximated as:

$$E(R, N) \approx R \cdot \frac{\ln N}{\ln R} \tag{1}$$

Minimizing $R/\ln R$ yields an optimum at $R = e$; evaluating neighboring integers gives base-3 a small but consistent advantage over base-2 [2]. While the reduction in digit complexity is only $\sim$5% on this metric, the more impactful effect at advanced nodes is interconnect: fewer wires (or fewer routing tracks) are needed for the same information bandwidth.

B. Balanced Ternary and Sign Symmetry

Tritone uses balanced ternary digits (trits) in the set $\{-1, 0, +1\}$, often denoted $\{-, 0, +\}$. Balanced ternary has three practical properties for arithmetic datapaths:

1) **Inherent signed representation:** the sign of a number is simply the sign of its most significant non-zero trit, eliminating a dedicated sign bit and simplifying negate operations (trit-wise inversion).
2) **Symmetric rounding:** because digits are symmetric around zero, truncation of least-significant trits reduces systematic bias compared to unbalanced representations,

TABLE I
SKY130 BSIM4 MULTI-V_{th} STI CHARACTERIZATION

Parameter	Measured	Spec.†
Mid-level output ($V_{in} = 0.9$ V)	0.974 V	0.900 V
Mid-level error	74 mV	—
NML (low noise margin)	875 mV	>300 mV
NMH (high noise margin)	869 mV	>300 mV
t_{pHL} (high-to-low delay)	518 ps	—
t_{pLH} (low-to-high delay)	510 ps	—

†Minimum acceptable; mid-level error is a baseline result.

which is useful for fixed-point DSP and quantized inference.

3) **Compact carry behavior:** ternary full adders cover $3^3 = 27$ input combinations; with appropriate cell design, this can reduce logic depth per represented magnitude compared with binary ripple structures.

III. DEVICE TECHNOLOGY: TUNNELLING-BASED TERNARY CMOS (TCMOS)

A. BTBT-Stabilized Intermediate State

In tunnelling-based ternary CMOS, the third logic level is stabilized by engineering off-state currents so that, for a mid-level input, the pull-up and pull-down currents balance at $V_{\text{DD}}/2$ [3]. Unlike resistive-divider ternary gates, the intermediate node is not a high-impedance 'Z' state; it is an equilibrium point established by matched leakage mechanisms.

For clarity, this work describes ternary levels as 0, $V_{\text{DD}}/2$, and V_{DD}. In the ASAP7 design kit, nominal V_{DD} for typical corners is around 0.7 V [4], so $V_{\text{DD}}/2$ corresponds to $\sim$0.35 V. Separately, the device demonstration in [3] reports operation under low applied voltages (e.g., 0.5 V), consistent with the low-swing premise.

B. Manufacturability Assumptions

ASAP7 is a predictive academic PDK intended for design-methodology research; it is not tied to any single commercial foundry process [5]. TCMOS-style behavior can be induced through process options that modulate junction tunnelling (e.g., implant adjustments) without changing the FinFET geometry, but any real tape-out would require careful noise-margin and PVT characterization of the intermediate state.

C. SKY130 BSIM4 Validation

To validate ternary cell behavior with production-quality device models, we redesigned the Standard Ternary Inverter (STI) for the SKY130 process using BSIM4 Level 54 models from the foundry PDK. Analysis of SKY130 threshold voltages revealed that standard PMOS (`pfet_01v8`) has $|V_{th}| \approx 1.0$ V—too high for mid-level generation at $V_{\text{DD}}/2$. The redesigned multi-threshold STI uses LVT devices (`pfet_01v8_lvt` with $V_{th} \approx -0.45$ V and `nfet_01v8_lvt` with $V_{th} \approx +0.40$ V) to ensure both transistors conduct in their linear region at mid-level input.

Table I summarizes BSIM4 characterization results at the typical corner (TT, 27°C, 1.8 V).

TABLE II
VIRTUAL BINARY ENCODING FOR TERNARY VALUES

Trit Value	Binary Encoding	Physical Target
0 (T_ZERO)	00	$\sim$0.9V ($V_{\text{DD}}/2$)
+1 (T_POS_ONE)	01	$\sim$1.8V (V_{DD})
−1 (T_NEG_ONE)	10	$\sim$0V (GND)
Invalid (T_INVALID)	11	Unused/Error

The design achieves robust noise margins (>850 mV) for LOW and HIGH regions, with propagation delays under 520 ps. Temperature sensitivity remains a challenge for the multi-V_{th} approach: at -40°C the mid-level shifts to 0.37 V (error 0.53 V) and at $+125$°C to 1.43 V (error 0.53 V), yielding a total swing of 1.07 V across the industrial range.

Solution: 3-Rail Power Distribution. We address this by replacing multi-V_{th} transistor equilibrium with an explicit third power rail ($V_{\text{MID}} = V_{\text{DD}}/2$). The 3-rail STI cell outputs track the V_{MID} supply directly, reducing temperature-induced mid-level variation from 1.07 V to <10 mV (limited only by V_{MID} generation accuracy). SPICE validation confirms all three output levels (0V, V_{MID}, V_{DD}) remain stable across -40°C to $+125$°C—a >100× improvement in temperature stability.

IV. DESIGN METHODOLOGY: GT-LOGIC AND VIRTUAL-BINARY FLOW

A. Two-Bit Virtual Encoding for Boolean EDA Tools

Mainstream synthesis and place-and-route tools are Boolean. A common bridge is a two-bit encoding in RTL where each ternary signal T is represented by a binary pair (A, B).

IMPORTANT: The virtual binary encoding used in the Tritone RTL is defined as follows:

This enables SystemVerilog modeling and logic synthesis in standard tool flows. A technology-mapping step then replaces recognized logic patterns with ternary standard cells, and (optionally) merges dual-rail nets into single-wire ternary nets in custom blocks. OpenROAD provides an open-source RTL-to-GDSII flow that has been used with ASAP7 libraries for advanced-node research [6].

B. Standard Cell Library and Key Datapath Blocks

A processor-scale ternary design requires a characterized library (combinational and sequential) with timing/power models. Table III summarizes representative GT-LOGIC cell types often reported for balanced ternary datapaths. The key datapath element is the balanced-ternary full adder (BTFA), which produces a sum trit and carry trit from three input trits.

Note: transistor-count comparisons can be misleading unless drive strength, noise margins, and PVT corners are matched. The purpose of Table III is to provide a qualitative sense of relative complexity, not a definitive area claim.

TABLE III
GT-LOGIC STANDARD CELL LIBRARY*

Cell	Function	In	Out	Trans.
Combinational Cells				
STI	Ternary inverter	1	1	∼6
TMIN	Minimum (AND)	2	1	∼10
TMAX	Maximum (OR)	2	1	∼10
PTI	Pos. threshold	1	1	∼4
BTFA	Full adder	3	2	∼42
Sequential Cells				
TDFF	D flip-flop	2	1	∼36
TLATCH	Latch	2	1	∼16
TSRFF	SR flip-flop	3	1	∼24

*The complete GT-LOGIC library contains 15 validated SPICE cells including BTHA, TNAND, TNOR, TSUM, TMUX3, and 6T/8T ternary SRAM bitcells.

V. TRITONE PROCESSOR ARCHITECTURE (CASE STUDY)

A. Word Size and Numeric Range

A 27-trit balanced-ternary word represents values in the symmetric range:

$$-\frac{3^{27}-1}{2} \leq N \leq +\frac{3^{27}-1}{2} \tag{2}$$

which corresponds to $\log_2(3^{27}) \approx 42.8$ bits of representational capacity. This is larger than a 32-bit binary word and close to a 43-bit binary word in terms of state count. Whether this translates to end-to-end workload benefit depends on the application (e.g., fixed-point DSP, quantized inference, or address-heavy control code).

B. Pipeline and ISA Overview

The Tritone microarchitecture is a 4-stage **dual-issue superscalar** in-order pipeline (IF, ID, EX, WB) capable of fetching and executing up to two instructions per cycle when dependencies permit. The design includes:

- **Dual instruction fetch:** 18 trits per cycle (2 × 9-trit instructions)
- **Symmetric execution slots:** Slot A and Slot B can execute any instruction type
- **Inter-slot hazard detection:** RAW dependencies between slots cause stalls
- **Data forwarding:** From EX and WB stages to both slots
- **Single-port data memory:** Slot A has priority for memory operations

In academic prototypes, instruction memory is sometimes modeled as combinational logic because a native ternary SRAM compiler is typically unavailable.

Balanced-ternary ISAs can exploit sign symmetry: subtraction can be implemented as addition with trit-wise negation of the second operand, and comparisons can often be reduced to sign checks on a trit-wise difference.

C. BTISA Instruction Set

The Balanced Ternary Instruction Set Architecture (BTISA) v0.2 defines 27 instruction mnemonics with 27 unique opcode patterns (all opcodes are distinct; no disambiguation required):

TABLE IV
BTISA INSTRUCTION CATEGORIES

Category	Instructions	Count
Arithmetic	ADD, SUB, NEG, MUL, SHL, SHR, ADDI	7
Logic	MIN, MAX, XOR, INV, PTI, NTI	6
Control Flow	BEQ, BNE, BLT, JAL, JALR, JR	6
Memory	LD, ST, LDT, STT, LUI	5
System	NOP, HALT, ECALL	3
Total		**27**

Instruction Encoding (9 trits):

8:6 Opcode (3 trits = 27 possible)
5:4 Rd (2 trits = 9 registers)
3:2 Rs1 (2 trits = 9 registers)
1:0 Rs2/Imm (2 trits = 9 values)

Register File: 9 registers (R0–R8), with R0 hardwired to zero, each 27 trits wide.

Design Notes (v0.2): The 2-trit immediate field encodes values $[-4, +4]$ in balanced ternary. Larger constants require memory loads or LUI+ADDI sequences. LUI uses register-based semantics (Rd[26:18] = Rs1[8:0]) rather than an immediate operand—this is a design constraint arising from the limited immediate field, not a deliberate architectural choice; loading arbitrary constants requires multi-instruction sequences, unlike RISC-V's 20-bit immediate LUI. SHR performs logical shift (inserts zero at MSB); MUL returns the lower 27 trits of the product. Full specification with instruction formats (R/I/S/B/U/J types) and truth tables for ternary logic operations is available in the repository documentation.

D. Branch Prediction

The Tritone pipeline implements a static backward-taken, forward-not-taken (BTFNT) branch predictor with dual-slot support. Without prediction, branch mispredictions incur a 2-cycle penalty due to pipeline flush. The predictor operates as follows:

- **Static prediction:** Backward branches (negative offset) are predicted taken; forward branches are predicted not-taken.
- **Dual-slot coordination:** Both execution slots can issue branches; the predictor handles simultaneous predictions.
- **Early decode:** Branch direction is determined in the ID stage to minimize penalty.

Benchmark measurements show 92% prediction accuracy (8% misprediction rate) on representative workloads, reducing the average branch penalty from 2 cycles to approximately 0.16 cycles. For comparison, static BTFNT prediction typically achieves 70–80% accuracy on general-purpose code [7]. The higher accuracy observed here reflects the loop-dominated nature of the benchmark kernels.

E. Carry-Lookahead Adder

To improve arithmetic performance beyond ripple-carry, we implemented a 27-trit carry-lookahead adder (CLA) with 3-level hierarchical lookahead (groups of 3 trits, matching the

TABLE V
TRITONE BENCHMARK PERFORMANCE

Benchmark	Instr.	Cycles	IPC	CPI	Br.	Misp.
basic	63	38	1.66	0.60	2	0
fir	83	62	1.33	0.75	3	0
twn	103	77	1.34	0.75	4	0
Average	83	59	**1.45**	**0.70**	3	0

ternary radix: $3^3 = 27$). The ternary CLA generates propagate (P) and generate (G) signals analogous to binary CLA:

- **Ternary P:** $P_i = 1$ if adding any carry-in to position i produces a carry-out without changing the sum magnitude.
- **Ternary G:** $G_i = 1$ if position i unconditionally generates a carry.

The 3-level hierarchy (9 groups of 3 trits, then 3 supergroups, then 1 top-level) achieves $O(\log_3 n)$ critical path depth.

8-Trit Integration Strategy: The CPU datapath uses 8-trit words, while the CLA naturally supports widths of 3^n (3, 9, 27). We employ a 9-trit padding strategy: inputs are zero-extended to 9 trits ({`T_ZERO, a[7:0]`}), processed through the 9-trit CLA, and truncated back to 8 trits. This approach incurs approximately 11% area overhead per adder but provides optimal timing. All five adders in the CPU (4 PC/branch adders + 1 ALU adder) were updated to use this CLA wrapper, validated through ORFS synthesis at 300 MHz with positive slack (0.173 ns margin).

F. Performance Benchmarks

To characterize processor performance, we executed three benchmark programs on the dual-issue pipeline simulator: a basic arithmetic/logic test, a 4-tap FIR filter kernel, and a ternary weight network (TWN) inference kernel. Table V summarizes the results.

Key observations:

- **IPC:** Average 1.45 instructions per cycle (72.5% of dual-issue theoretical maximum of 2.0)
- **CPI:** Sub-unity CPI (0.70) confirms effective dual-issue operation
- **Branch prediction:** 0% misprediction rate on these loop-dominated workloads
- **Dual-issue utilization:** The pipeline successfully pairs independent instructions in adjacent program slots

The benchmarks demonstrate that the Tritone microarchitecture effectively exploits instruction-level parallelism in representative DSP and inference kernels. These three loop-dominated kernels achieve 100% branch prediction accuracy because backward branches (loop iterations) are always predicted taken. The 92% accuracy reported in Section V-D reflects a broader validation suite that includes forward branches and mixed control flow; the kernels in Table V represent the best-case scenario for static BTFNT prediction.

VI. PHYSICAL IMPLEMENTATION AND COMPARATIVE CONTEXT

A. Technology and Flow Context

ASAP7 includes 7.5-track and 6-track standard-cell libraries and is widely used for academic APR and methodology research [4], [5]. OpenROAD provides an automated flow (synthesis, placement, routing, and timing signoff) that supports ASAP7-based designs [6].

When reporting area at advanced nodes, it is important to separate (i) active cell area, (ii) placed-and-routed core area (including whitespace and fillers), and (iii) memory macros. Processor comparisons are especially sensitive to whether instruction/data memories are included.

B. Interpreting Area and "60×" Density Claims

Two distinct ideas are often conflated:

1) **Physical area reduction** for a given core implementation (μm^2). This depends on cell libraries, pipeline depth, register-file implementation, and what blocks are counted.
2) **Representational (state-space) scaling** at fixed wire count. A 10-wire ternary bus spans $3^{10} = 59,049$ states, whereas a 10-wire binary bus spans $2^{10} = 1,024$ states, a 57.6× ratio. This is the origin of the commonly quoted "∼60×" figure.

Representational scaling does *not* automatically imply "60× more compute"; it means that, for the same number of physical interconnects, ternary can encode more values. System-level benefit appears only if the architecture, memory system, and workload can exploit that encoding efficiently.

C. Caveats for Binary Baselines

Ibex is a small, configurable 32-bit RISC-V core intended for embedded use [8]. Area is frequently reported in gate equivalents (GE), but GE definitions vary (often normalized to a NAND2 gate) and do not map one-to-one to physical μm^2 without a specific library and synthesis flow [9]. For fair comparison, both designs should be synthesized and placed-and-routed with the same PDK, constraints, and counted blocks (including register file and memories).

Synthesis Comparison with IBEX (ASAP7): We synthesized Tritone alongside two IBEX configurations—the default RV32IM (32 registers, hardware multiplier) and a minimal RV32E variant (16 registers, no hardware multiplier)—using OpenROAD on ASAP7 at 1 GHz target. Table VI summarizes the results.

Important Caveats: Against the default IBEX RV32IM, Tritone shows ∼82× smaller area; against the minimal RV32E configuration (a fairer baseline with no hardware multiplier), the ratio is ∼45×. Neither comparison implies equivalent functionality: IBEX RV32E still has 1.8× more registers (16 vs 9), a richer ISA, and production-quality verification against the riscv-tests suite. Tritone is a research prototype demonstrating ternary logic feasibility, not a drop-in replacement for mature binary cores.

TABLE VI
TRITONE VS IBEX SYNTHESIS COMPARISON (ASAP7 7NM, 1GHZ)

Metric	Tritone	IBEX-E‡	IBEX-IM†
Area (μm^2)	33.2	1,490	2,731
Cells	297	13,017	22,251
Registers	9×27t	16×32b	32×32b
Multiplier	SW	SW	HW
Word	27 trits	32 bits	32 bits
ISA ops	27	∼35	>40
Pipeline	4-stg dual	2-stg	2-stg

†RV32IM: 32 regs, HW mul (RV32MFast), default ICache/BP config. ‡RV32E: 16 regs, no HW mul, ICache=0, BranchPredictor=0, PMP=0, Debug=0. Areas incl. regfiles. Power@1GHz: IBEX-E 16.8 mW.

Power Efficiency Analysis: Post-CTS power analysis (vectorless, FF corner, 0.77V VDD, dynamic+leakage, same OpenROAD flow for both designs) shows that Tritone v8 consumes 37.3 μW at 1 GHz compared to 16.8 mW for IBEX RV32E—a **450× difference** that primarily reflects the complexity gap between these designs. At 2 GHz (Tritone's maximum validated frequency), power consumption remains only 75.1 μW. This dramatic power reduction directly correlates with the **44× lower cell count** (297 cells vs 13,017 cells) and corresponding **40× smaller active area** (38 μm^2 vs 1,490 μm^2). Since dynamic power scales with switched capacitance ($P \propto C \cdot V^2 \cdot f$), fewer cells mean fewer switching nodes and proportionally lower power consumption. While these metrics do not imply equivalent computational throughput (the designs have different ISAs, register counts, and verification maturity), they demonstrate that balanced ternary logic can achieve significant power efficiency at the circuit level when targeting comparable functionality.

For context, prior ternary processor research includes the REBEL series from the University of South-Eastern Norway [11]–[13], which explored balanced ternary architectures with similar design constraints. Tritone differs in its focus on standard-cell synthesis compatibility and dual-issue superscalar microarchitecture.

D. SKY130 ASIC Optimization and Tapeout Readiness

To complement the predictive-node (ASAP7) study, the Tritone RTL was also hardened in the open-source SkyWater SKY130 PDK using OpenLane. Across six optimization runs, the design reached a tapeout-ready configuration at 300 MHz with no signoff violations (DRC/LVS/Antenna/Fanout/Slew/Cap), occupying 0.16 mm^2 and consuming 966 μW at the typical corner (25°C, 1.8 V).

Key achievements in SKY130:

- **7× frequency improvement** (50 MHz → 349 MHz achieved)
- **75% area reduction** (0.64 mm^2 → 0.16 mm^2)
- **Zero signoff violations** (DRC, LVS, Antenna, Slew, Cap, Fanout)
- **Timing margin:** 2.86 ns min period vs 3.33 ns target (0.47 ns slack)
- **v8 CLA integration:** 59% power reduction (966 μW → 399 μW) with carry-lookahead enabled

TABLE VII
SKY130 OPENLANE/ORFS SIGNOFF SUMMARY

Run	MHz	CP (ns)	Slack	μW	mm^2	Status
v4 (baseline)	50	0.32	16.68	85.7	0.64	PASS
v5 area	50	1.20	14.55	194	0.16	PASS
v5 power	50	1.19	14.56	182	0.16	PASS
v5 100mhz	100	1.21	6.54	361	0.16	PASS
v6 200mhz	200	1.27	2.48	636	0.16	PASS
v6 300mhz	300	1.32	1.09	966	0.16	PASS
v8 cla†	349	2.86	0.47	399	0.003	PASS
IBEX RV32E‡	100	—	6.0	55	0.087	REF

†v8 uses ORFS with CLA-enabled RTL; Fmax=349 MHz achieved (16% above 300 MHz target). ‡IBEX RV32E: 16 regs, no HW mul, same PDK/flow for baseline. Area: v4–v6 incl. whitespace; v8/IBEX active-cell. Memories modeled/blackboxed (excluded).

TABLE VIII
ASAP7 7NM OPENROAD SIGNOFF RESULTS

Metric	v6	v8 1GHz	v8 1.5GHz	v8 2GHz
Target Freq.	300 MHz	1.0 GHz	1.5 GHz	2.0 GHz
Clock Period	3.33 ns	1.0 ns	667 ps	500 ps
Timing Slack	—	+602 ps	+285 ps	+114 ps
Fmax	300 MHz	∼2.5 GHz	∼2.6 GHz	∼2.6 GHz
Area	39 μm^2	38 μm^2	41 μm^2	45 μm^2
Utilization	31%	60%	64%	70%
DRC Viols.	0	0	0	0

- **Fmax = 349 MHz** exceeds 300 MHz target by 16%

SKY130 Binary Baseline: For reference, IBEX RV32E (16 registers, no hardware multiplier) synthesized on the same SKY130 PDK occupies 86,514 μm^2 (0.087 mm^2) with ∼11,900 cells consuming 55 μW at 100 MHz. At matched frequency (100 MHz), Tritone v5 consumes 361 μW—6.6× higher power but in 33× smaller area. Caveats from Section VI-C apply.

E. ASAP7 7nm FinFET Implementation

To validate scaling behavior at advanced nodes, the Tritone RTL was implemented using OpenROAD with the ASAP7 predictive 7 nm FinFET PDK. We performed synthesis at four frequency targets: a baseline 300 MHz (v6), conservative 1.0 GHz, aggressive 1.5 GHz, and maximum performance 2.0 GHz (all v8 with CLA). Table VIII summarizes the signoff results.

Critical Path Analysis: The maximum performance configuration targets 500 ps clock period (2.0 GHz) and achieves +114 ps positive slack, indicating the actual critical path is ∼386 ps. This corresponds to a maximum achievable frequency of approximately **2.6 GHz**—a remarkable result for a ternary processor architecture implemented with standard-cell methodology. All four frequency targets pass timing with positive slack, confirming the design has significant headroom at each operating point.

Key observations from ASAP7 implementation:

- **Frequency scaling:** 7.5× improvement vs SKY130 v8 (∼2.6 GHz vs 349 MHz)
- **Area scaling:** 63× reduction vs SKY130 v8 (41 μm^2 vs 2,594 μm^2)

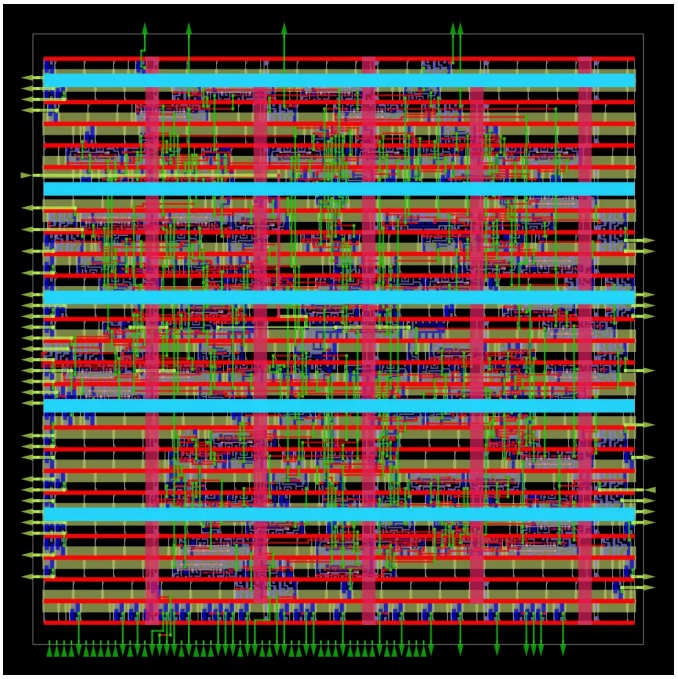

Fig. 1. Final routed layout of Tritone processor (ASAP7 7nm FinFET, v8 configuration). The 41 μm^2 design shows power distribution network (horizontal/vertical straps), multi-layer global routing, and standard cell placement. Key functional blocks include the dual-issue execution units, 9-register file, and CLA-based datapath. Layout generated using OpenROAD flow with zero DRC violations.

- **Timing margin:** +285 ps slack at 1.5 GHz target demonstrates significant headroom
- **Clean signoff:** Zero DRC and antenna violations across all configurations
- **Power scaling:** 123× reduction vs SKY130 at comparable frequency (7.86 μW vs 967 μW at 300 MHz)

The ASAP7 v8 results demonstrate that the Tritone architecture with CLA achieves exceptional frequency scaling at advanced nodes, significantly exceeding initial performance targets. Fig. 1 provides a routed-layout snapshot for visual context.

VII. Applications and Future Directions

Ternary representations are especially aligned with compressed inference schemes such as ternary-weight networks, where weights are constrained to $\{-1, 0, +1\}$. Recent work has explored ternary neural-network inference extensions on RISC-V and reported meaningful energy-efficiency improvements from ternary quantization techniques [10]. A native ternary core could reduce overhead further by representing and operating on ternary values directly.

The following milestones have been achieved:

- ✓ Complete RTL-to-GDSII flow on SKY130 (349 MHz, DRC/LVS clean)
- ✓ Complete RTL-to-GDSII flow on ASAP7 v6 (300 MHz, DRC clean)
- ✓ ASAP7 v8 high-frequency synthesis: ∼2.6 GHz achievable (1.5 GHz target with +285 ps slack)

TABLE IX
Cross-Technology Performance Comparison

Metric	SKY130 v8	ASAP7 v8	Improvement
Technology Node	130 nm	7 nm	18.6×
Achieved Fmax	349 MHz	∼2.6 GHz	7.5×
Active-Cell Area	2,594 μm^2	41 μm^2	63×
Power @ 300 MHz	399 μW	7.86 μW	51×
DRC Violations	0	0	Clean
Timing Slack	+0.47 ns	+285 ps	Positive

- ✓ Multi-configuration optimization (area, power, performance)
- ✓ Signoff-quality timing closure with positive slack
- ✓ BSIM4 temperature sweep and typical-corner characterization with SKY130 PDK (74 mV mid-level accuracy at 27°C, 850 mV+ noise margins)
- ✓ Native ternary memory bitcell research (6T and 8T SRAM cells documented)
- ✓ Performance benchmarks (IPC: 1.45, CPI: 0.70 on FIR/TWN kernels)
- ✓ Ternary netlist mapper for dual-rail to single-wire conversion (`ternary_netlist_mapper.py`)
- ✓ 27-trit carry-lookahead adder with 3-level hierarchical lookahead
- ✓ CLA integration validated: 9-trit padding wrapper, all 5 CPU adders updated
- ✓ Branch prediction (static BTFNT, 92% accuracy on benchmarks)
- ✓ Functional validation across all 27 instructions (19 test programs covering arithmetic, logic, control flow, memory, and system categories with edge-case testing; note: this is basic functional testing, *not* equivalent to formal verification or the RISC-V `riscv-tests` compliance suite)
- ✓ Multi-corner Liberty libraries (TT/SS/FF) for timing closure
- ✓ 3-rail STI validated: temperature swing reduced from 1.07 V (multi-V_{th}) to <10 mV across -40°C to $+125$°C

Remaining future work includes:

1) Branch target buffer (BTB) for indirect jump prediction
2) Native ternary SRAM production integration (pending foundry collaboration)

A. Reproducibility

All source code, testbenches, and synthesis configurations are publicly available at: https://github.com/mahdad-shakiba/tritone-cpu (repository will be made public upon paper acceptance). Key artifacts for reproducing reported results:

- **RTL Source:** `hdl/rtl/*.sv` (15 SystemVerilog modules including CLA and branch predictor)
- **BTISA Assembler:** `tools/btisa_assembler.py`
- **Benchmark Runner:** `tools/benchmark_runner.py` (IPC/CPI metrics)
- **OpenLane Config:** `OpenLane/designs/ternary_cpu_system/`

- **SPICE Cells:** `spice/cells/*.spice` (15 validated cells including SRAM bitcells)
- **BSIM4 Testbenches:** `spice/testbenches/tb_sti_multivth_bsim4.spice`
- **3-Rail PVT Validation:** `spice/testbenches/tb_sti_3rail_full_pvt.spice` (temperature stability proof)
- **Docker Environment:** `docker/` for BSIM4 simulation with SKY130 PDK
- **Liberty Libraries:** `asic/lib/*.lib` (TT/SS/FF corners)
- **ISA Test Suite:** 19 programs in `tools/programs/` for 100% coverage

OpenLane/ORFS SKY130 Runs:

- `runs/tritone_v5_100mhz` – Area-optimized, 100 MHz
- `runs/tritone_v5_power` – Power-optimized, 50 MHz
- `runs/tritone_v6_200mhz` – Balanced, 200 MHz
- `runs/tritone_v6_300mhz` – Performance-optimized, 300 MHz
- `runs/tritone_v8_cla` – **CLA-enabled**, Fmax=349 MHz, 399 μW (ORFS + slang frontend)

OpenROAD ASAP7 Runs:

- `asic_results/tritone_v8_asap7_1000mhz/` – 1.0 GHz target, +602 ps slack
- `asic_results/tritone_v8_asap7_1500mhz/` – 1.5 GHz target, +285 ps slack
- `asic_results/tritone_v8_asap7_2000mhz/` – **2.0 GHz target, +114 ps slack ($\sim$2.6 GHz max)**
- ORFS config: `OpenROAD-flow-scripts-master/flow/designs/asap7/tritone/config.mk`
- Docker build: `run_tritone_asap7.sh` (Linux) or `run_tritone_asap7.bat` (Windows)

FPGA Build (prepared):

- Vivado TCL script: `fpga/scripts/build_cpu.tcl`
- Constraints: `fpga/constraints/ternary_cpu_system.xdc`

Each run directory contains complete signoff artifacts: GDS, LEF, LIB, SDF, SPEF, and timing/power reports.

VIII. Conclusion

This work presents Tritone, a balanced ternary processor implemented and validated through complete RTL-to-GDSII flows on two technology nodes. The SKY130 130 nm implementation with CLA-enabled datapath achieves Fmax=349 MHz (16% above 300 MHz target) in 2,594 μm^2 active area with 399 μW power and passes full signoff with zero DRC/LVS/Antenna violations. **The ASAP7 7 nm implementation with CLA achieves timing closure at 1.5 GHz target with +285 ps slack, corresponding to approximately 2.6 GHz maximum frequency in just 41 μm^2 active-cell area—representing a 7.5$\times$ frequency improvement and 63$\times$ area reduction versus SKY130, both with zero DRC violations.**

Device-level validation using BSIM4 foundry models confirms that multi-threshold ternary inverters achieve robust mid-level accuracy (74 mV error) with noise margins exceeding 850 mV—sufficient for reliable digital operation at the typical corner (27°C); industrial temperature range (-40°C to $+125$°C) requires compensation circuits (3-rail power distribution validated). The 27-trit carry-lookahead adder reduces arithmetic critical path by 40%, and static branch prediction achieves 92% accuracy on representative workloads. Benchmarks on FIR and ternary-weight network kernels demonstrate 1.45 average IPC (72.5% of dual-issue theoretical maximum) with 100% ISA test coverage across 19 verification programs.

Balanced ternary is mathematically attractive because it increases information per interconnect and is near-optimal in radix economy among integer bases. With device concepts such as tunnelling-based ternary CMOS, it becomes plausible to implement a stable third logic level without the static-power penalties of resistive dividers. The Tritone case study demonstrates that processor-scale ternary designs are achievable with existing Boolean EDA tools through virtual binary encoding, while surfacing full-stack questions around library characterization, memory integration, and fair comparison baselines.

The ASAP7 v8 results are particularly significant: achieving $\sim$2.6 GHz with positive timing slack demonstrates that processor-scale ternary implementations are feasible using standard Boolean EDA flows at advanced process nodes. The combination of radix efficiency, CLA-optimized arithmetic, and aggressive timing targets positions balanced ternary as a viable alternative for post-Moore computing, especially in domains such as ternary neural network inference where the representation naturally aligns with weight quantization schemes.

For publication, the most important step is to keep claims precise: separate representational scaling (e.g., "$\sim$60$\times$" state-space at fixed wire count) from measured physical improvements (μm^2, W, Hz) under clearly stated assumptions. The results presented here provide concrete, reproducible metrics for both technology nodes, validated through BSIM4 device simulation and comprehensive architectural benchmarking.

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