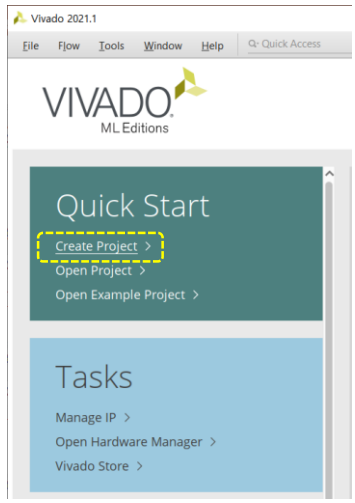
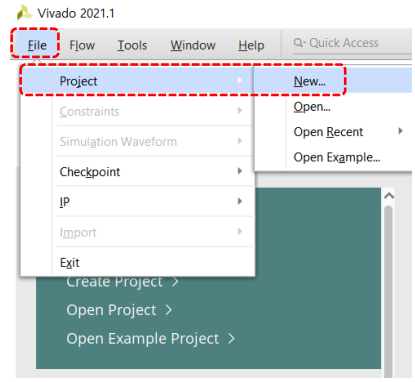
Xilinx Vivado Design Suite

1. Vivado Design Suite
2. Vivado IDE
3. **Project 생성**
4. 설계 입력
5. RTL Simulation
6. Design Synthesis
7. Design Implementation
8. FPGA Device Programming

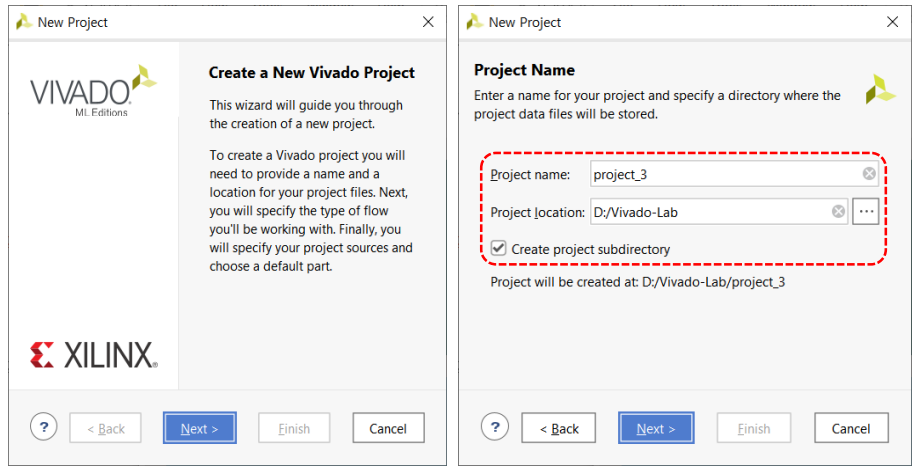
3.1 Project 생성 – New Project





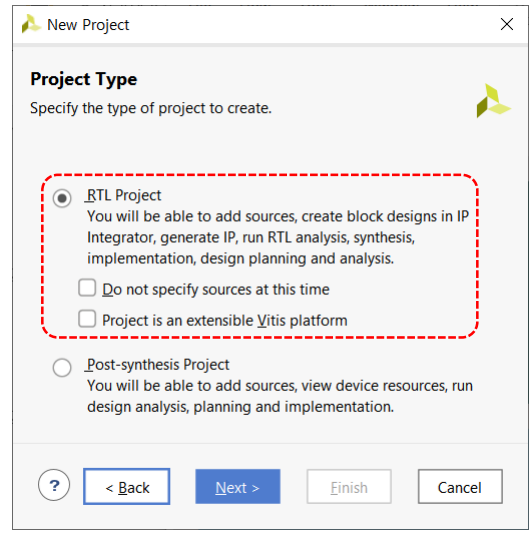
3.1 Project 생성 – New Project

❑ **Project Name, Location 설정**



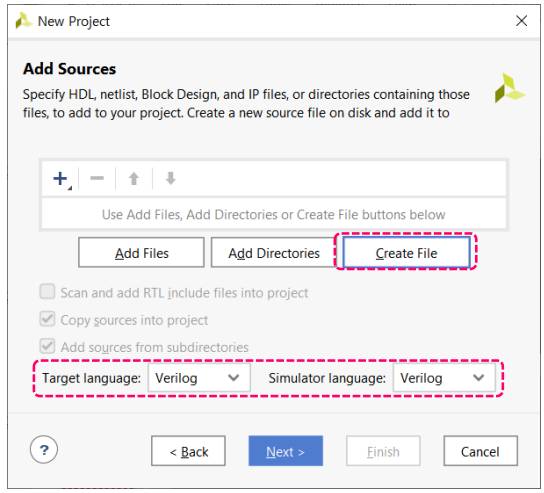
3.1 Project 생성 – New Project

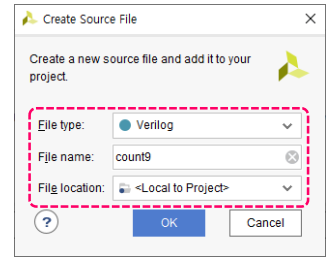
❑ **Project Type 설정**



3.2 Project 생성 – Add Sources

❑ **Add or Create Sources**

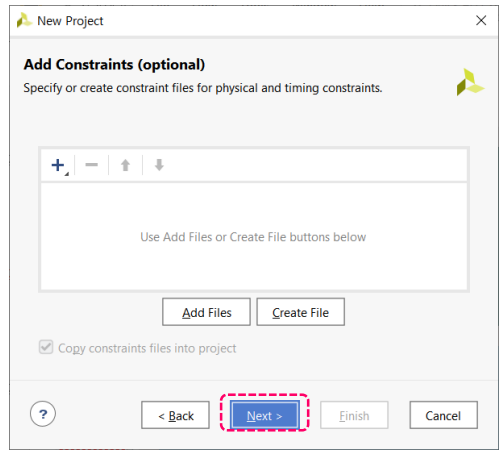




3.3 Project 생성 – Add Constraints

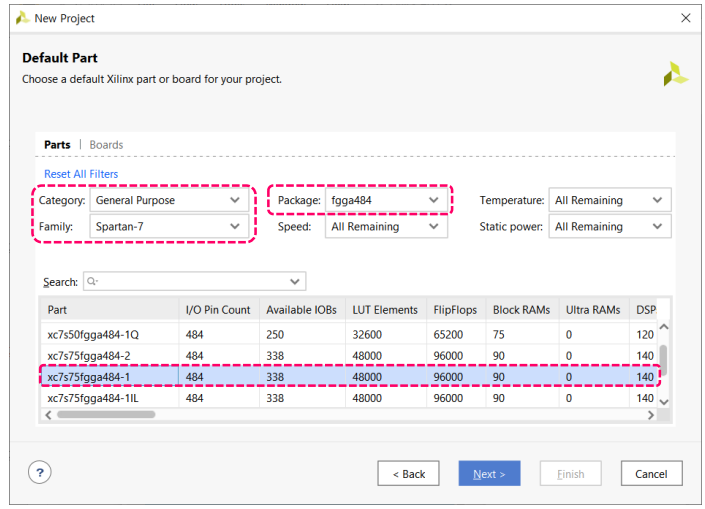
❑ **Add Constraints**

❖ **Constraint 파일(Xilinx Design Constraint; XDC) 생성 및 기존 파일 추가**



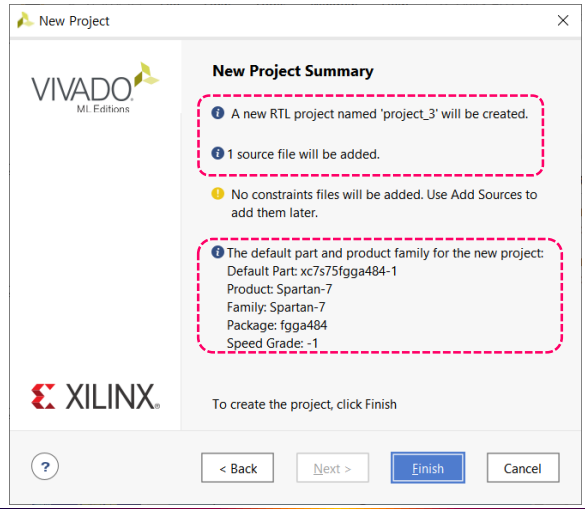
3.4 Project 생성 – Default Part

- Default Part; FPGA 디바이스 및 보드 선택 (xc7s75fgga484-1)



3.5 Project 생성 – Project Summary

- New Project Summary



3.6 Project 생성 – 완료된 상태