# Xilinx Vivado Design Suite



1. Vivado Design Suite
2. Vivado IDE
3. Project 생성
4. 설계 입력
5. RTL Simulation
6. **Design Synthesis**
7. Design Implementation
8. FPGA Device Programming

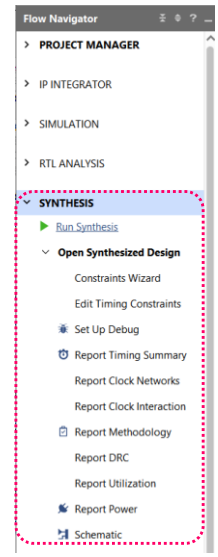


# 6. 설계합성(Design Synthesis)



- **Synthesis에서 이용할 수 있는 프로세스들**
  - **Constraints Wizard: Timing constraints 생성**
  - **Edit Timing Constraints: Timing constraints 수정**
  - **Set Up Debug: Debug 코어 설정**
  - **Report Timing Summary**
  - **Report Clock Networks**
  - **Report Clock Interaction**
  - **Report Methodology**
  - **Report DRC**
  - **Report Utilization**
  - **Report Power**
  - **Schematic: 합성 후의 회로도 보기**

Report 생성

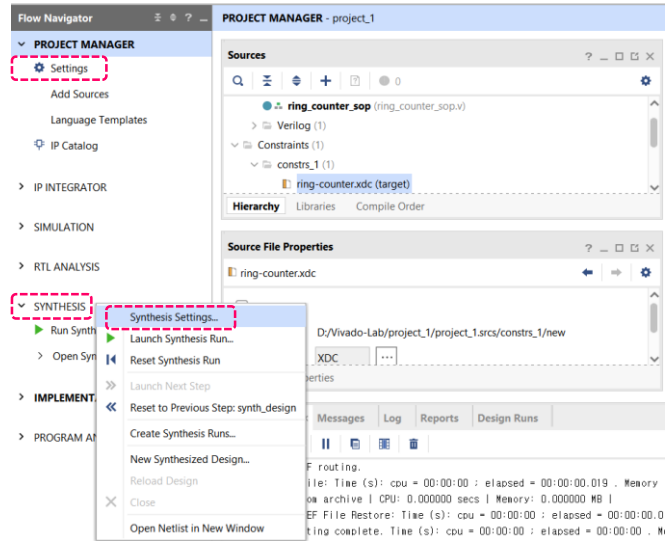


# 6. 설계합성(Design Synthesis)



❑ **Synthesis 설정**

❖ 면적, 속도, 전력소모 등 합성 과정에 적용되는 최적화 옵션을 지정

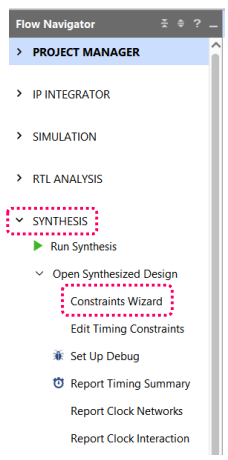


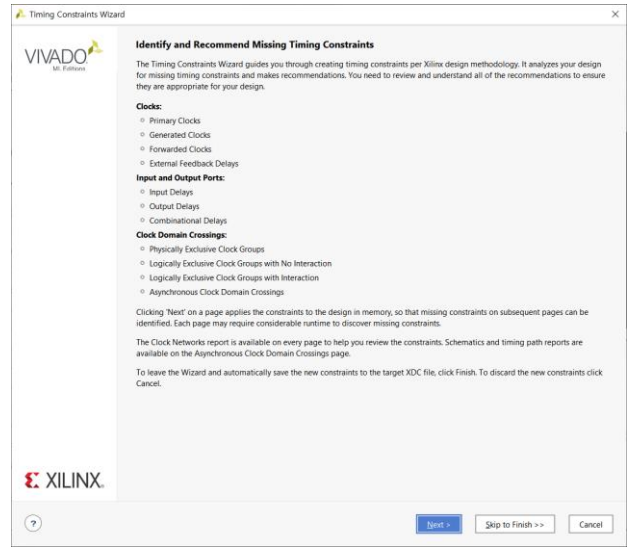



# 6. 설계합성(Design Synthesis)



❑ **Timing Constraints 설정**

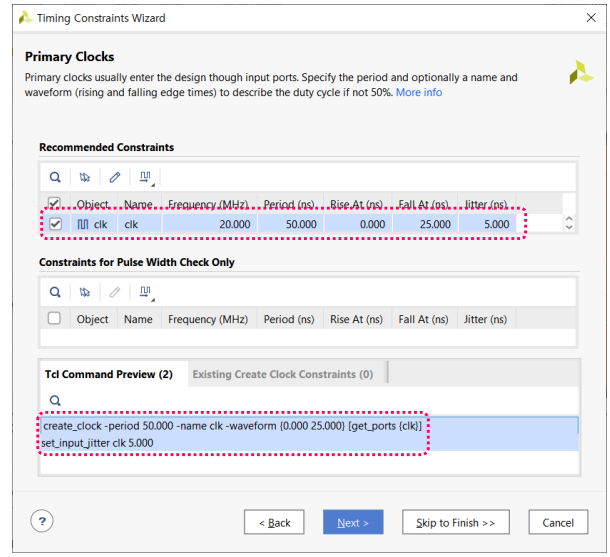


# 6. 설계합성(Design Synthesis)



- Timing Constraints 설정
  - Primary clock, input/output delay 등 합성 과정에 적용되는 constraints 설정

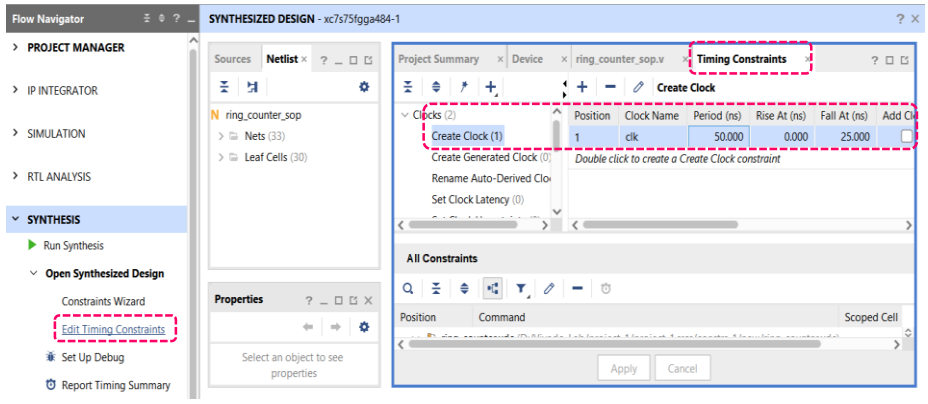





# 6. 설계합성(Design Synthesis)



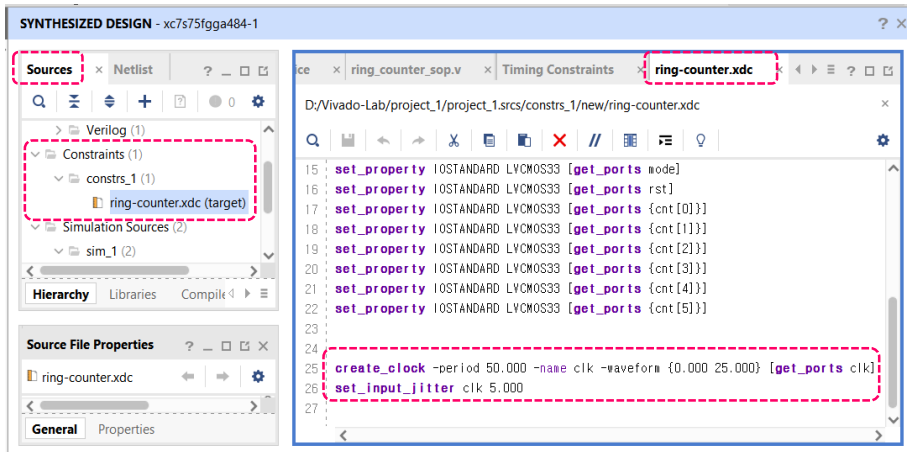
- Timing Constraints 수정



# 6. 설계합성(Design Synthesis)



❑ **Xilinx Design Constraints(XDC) 파일 확인**

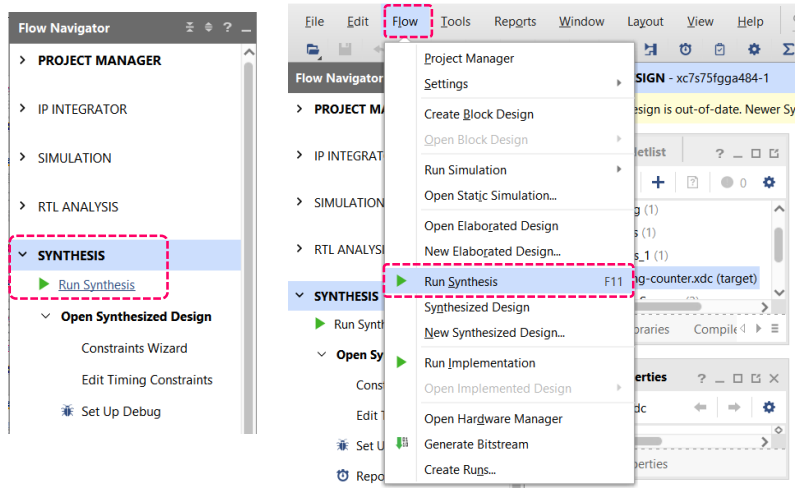





# 6. 설계합성(Design Synthesis)



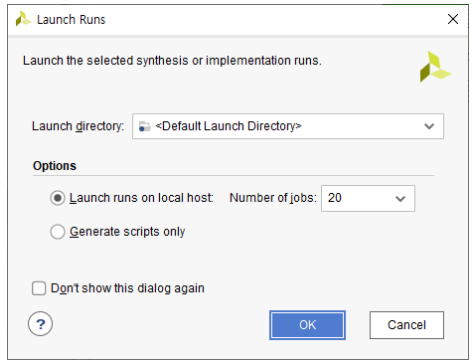
❑ **Synthesis 실행**

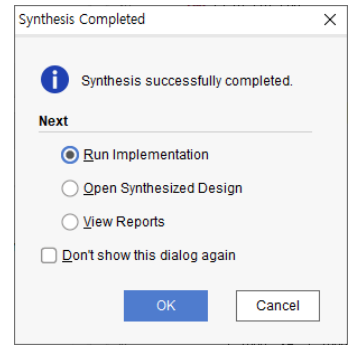


# 6. 설계합성(Design Synthesis)



❑ **Synthesis 실행**






# 6. 설계합성(Design Synthesis)