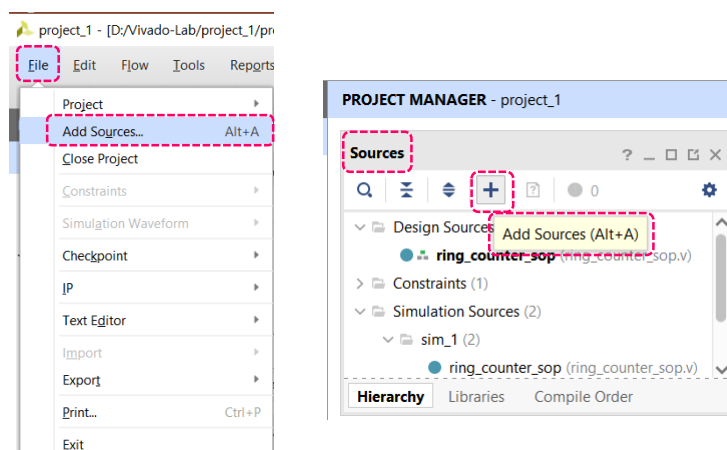


1. Vivado Design Suite
2. Vivado IDE
3. Project 생성
4. 설계 입력
5. RTL Simulation
6. Design Synthesis
7. Design Implementation
8. FPGA Device Programming

## 4.1 설계입력 – Add Sources

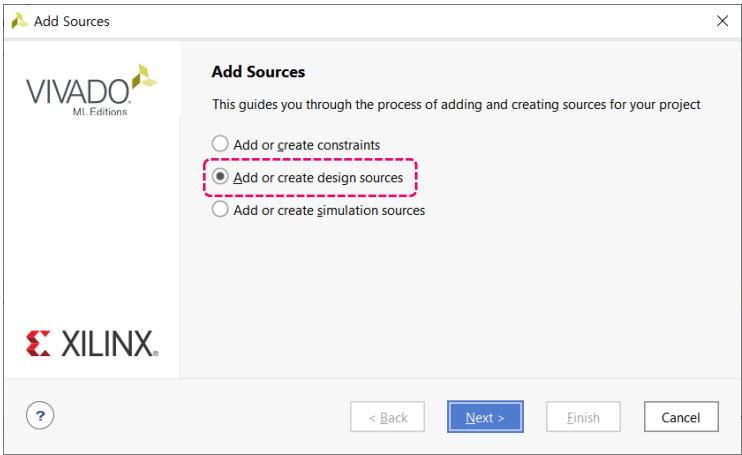
### □ Add Sources



# 4.1 설계입력 – Add Sources

3

## Add or Create Design Sources



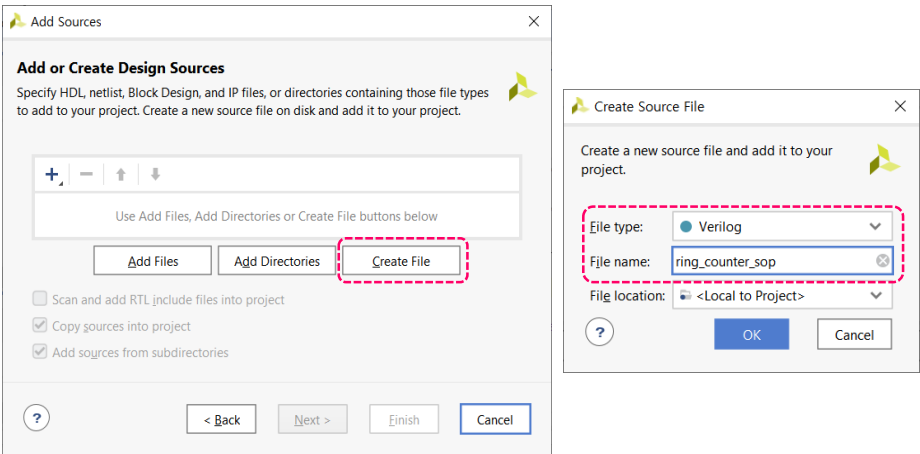
Verilog HDL

Xilinx Vivado Design Suite

# 4.1 설계입력 – Add Sources

4

## Create Design Sources



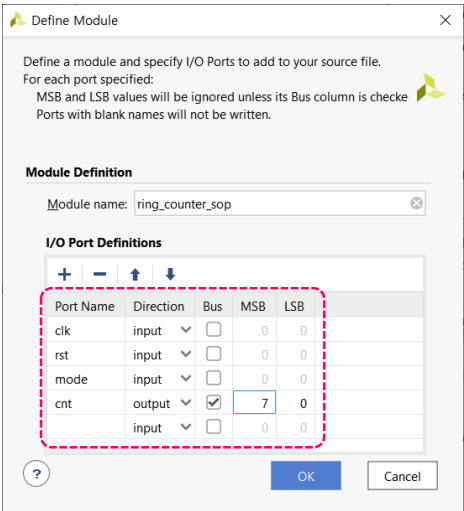
Verilog HDL

Xilinx Vivado Design Suite

## 4.2 설계입력 – Define Module

5

### Define Module; 회로의 입력과 출력 포트 지정

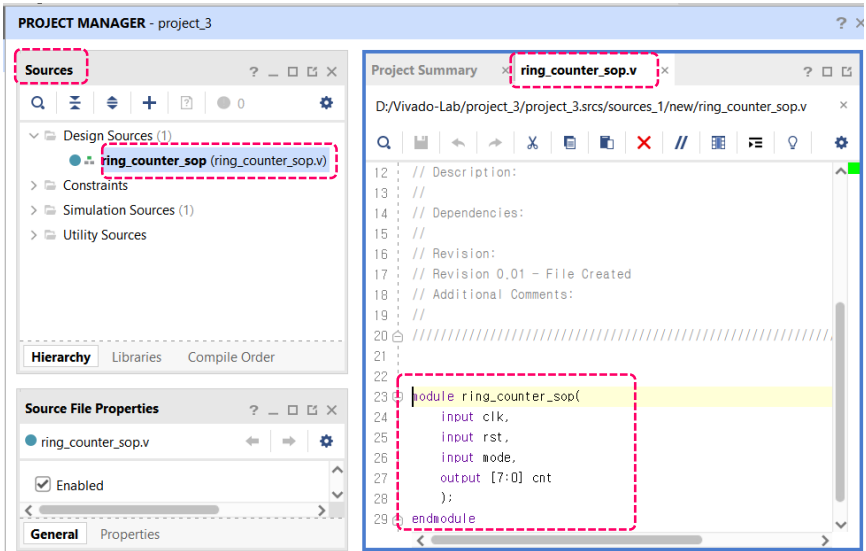


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## 4.3 설계입력 – Text Editor

6

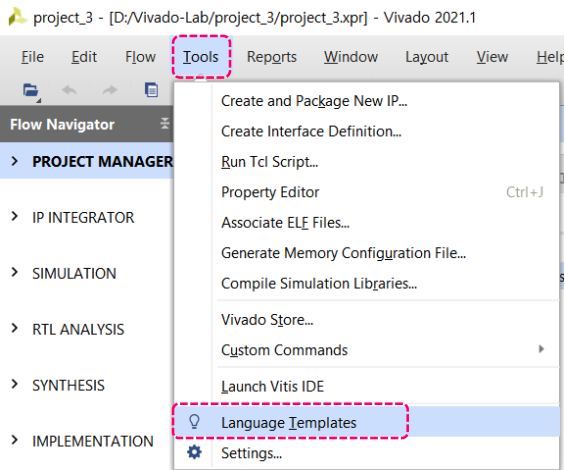


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# 4.4 설계입력 – Language Templates

7

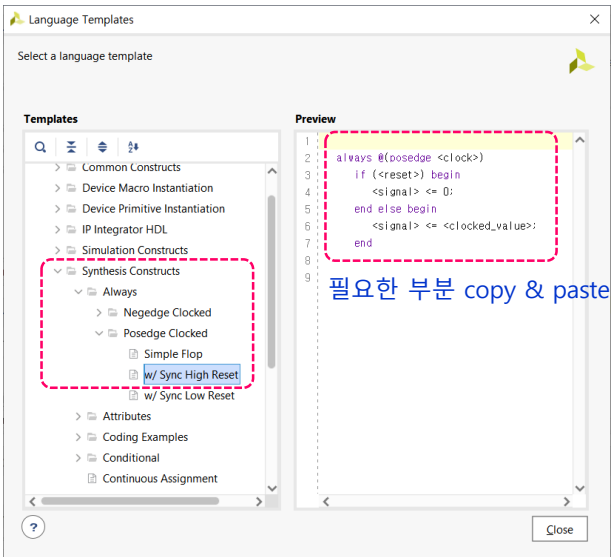


Verilog HDL

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# 4.4 설계입력 – Language Templates

8



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