Verilog를 이용한 RTL 시스템 반도체 설계

➢ Digilent 보드 파일 설치

[Reference]

https://digilent.com/reference/programmable-logic/guides/installing-vivado-and-vitis

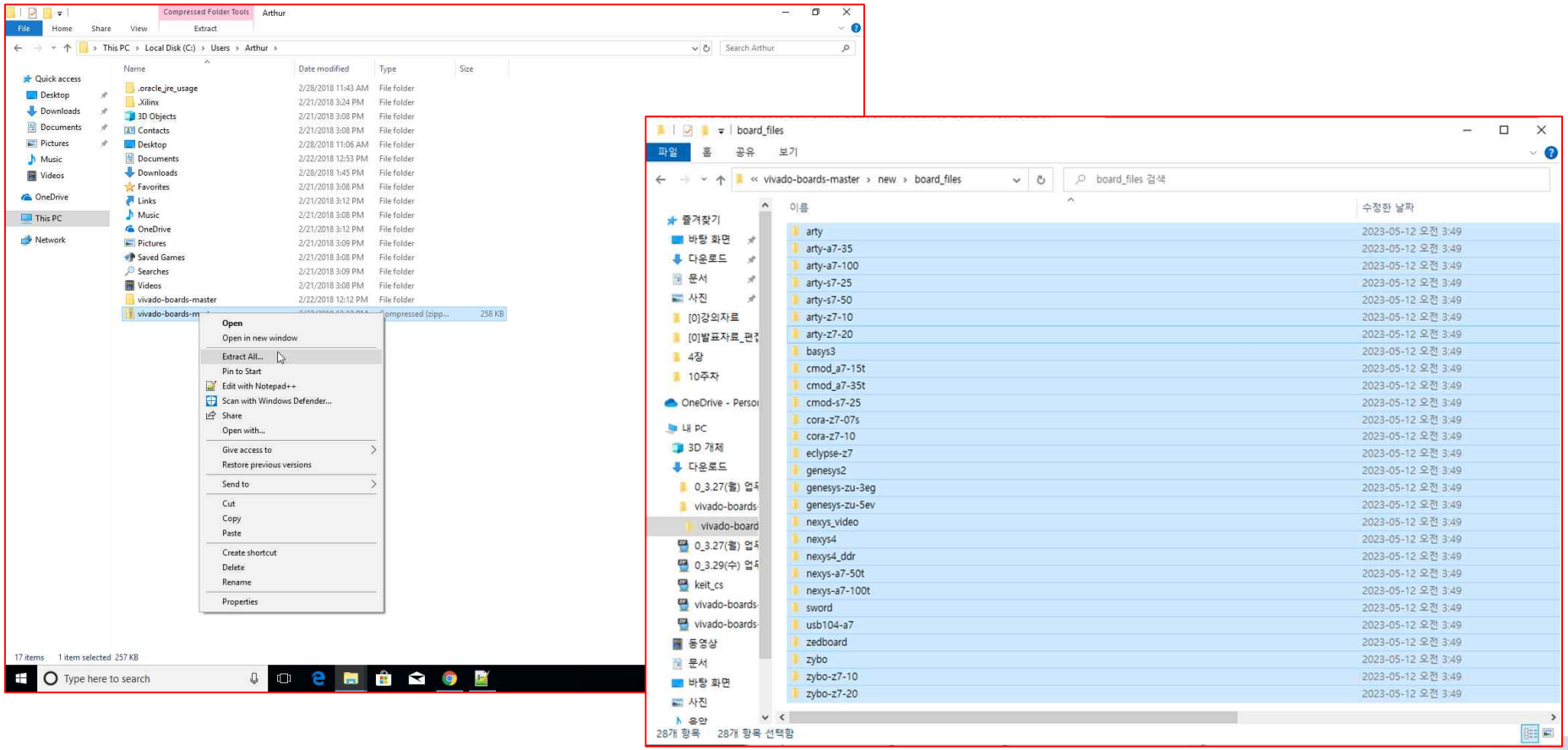
https://github.com/Digilent/vivado-boards/archive/master.zip?_ga=2.18848817.949290295.1683704263-1713577471.1683439375

❖ Installing Digilent Board Files

➢ Install Digilent's Board Files

→ Download the most recent Master Branch ZIP Archive (https://github.com/Digilent/vivado-boards/archive/master.zip?_ga=2.20372912.949290295.1683704263-1713577471.1683439375) of Digilent's vivado-boards Github repository and extract it.

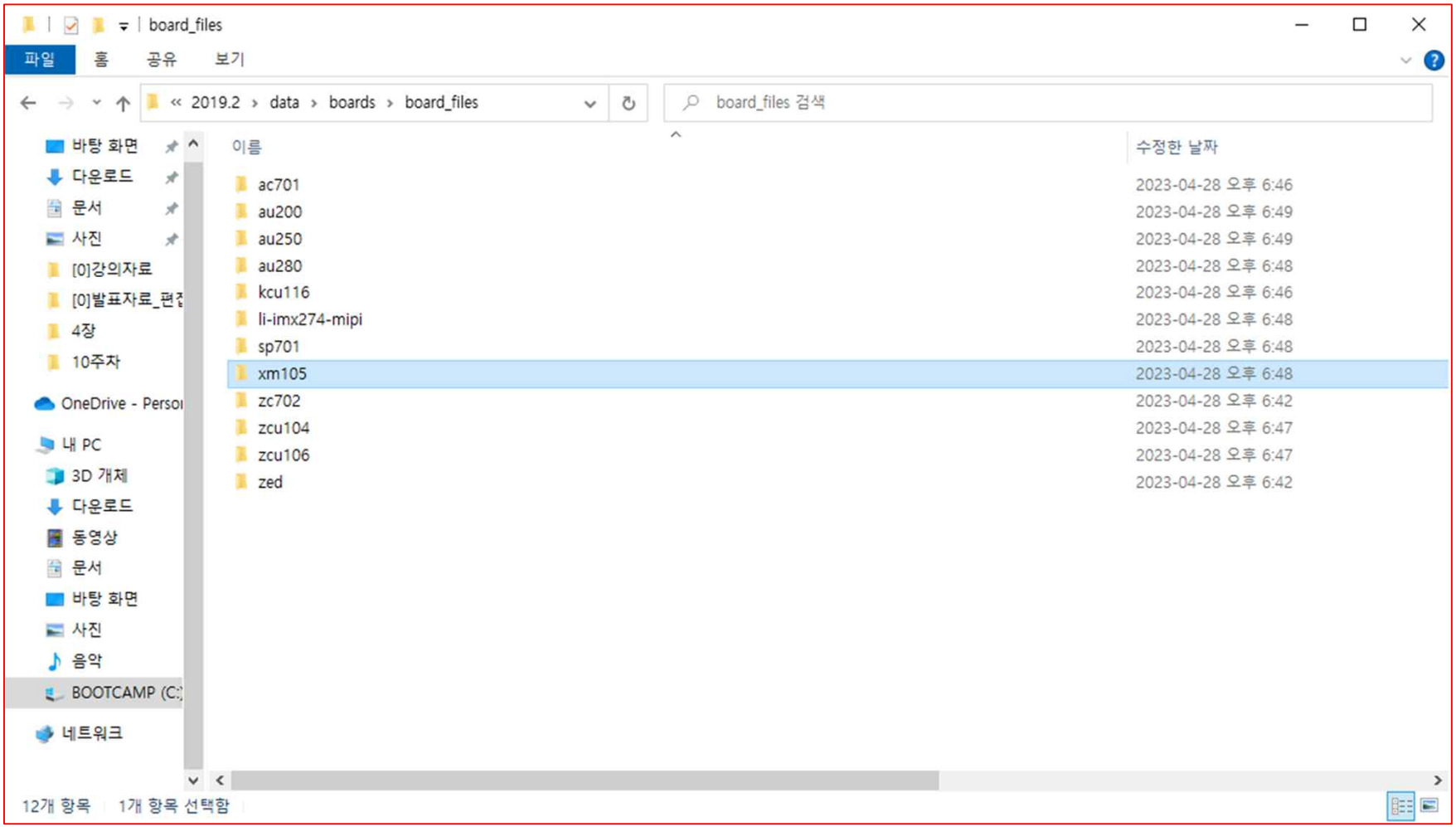
→ [Select All] - [Copy (Ctrl+C)]



❖ Vivado, Vitis 및 Digilent 보드 파일 설치

➢ Install Digilent's Board Files

→ Under this folder, navigate to its [<version>/data/boards/board_files] directory → [2019.2/data/boards/board_files]



❖ Vivado, Vitis 및 Digilent 보드 파일 설치

➢

→ Copy all of the folders found in vivado-boards' new/board_files folder[vivado-boards-master/new/board_files], then paste them into this folder