FPGA 실습장비 소개

Kyung-Wook Shin
kwshin@kumoh.ac.kr

School of Electronic Eng.,
Kumoh National Institute of Technology

FPGA 실습 KIT 구성

a. Audio In/Out ports
b. SD card socket
c. Expansion port
d. EEPROM
e. SDRAM
f. SRAM
g. ADC in port
h. DAC out port
i. Bluetooth
j. USB to Serial
k. RS232C

1. FPGA Device-Spartan7 (XC7S75-FGGA484-1)
2. PROM (s25FL128s)
3. JTAG port
4. Clock control block
5. DIP switch
6. Keypad
7. Button switch
8. LED
9. 7-Segment display
10. Text LCD
11. Full Color LED
12. TFT LCD
13. Piezo
14. STEP MOTOR
15. Image sensor

규 격 (1)

구 분	사 양
FPGA Device	Xilinx Spartan-7 (XC7S75-FGGA484-1)
Configuration ROM	Spansion s25FL128s (128Mb)
Clock	50 MHz base board Oscillator 1EA (0 Hz ~ 50 MHz)
DIP Switch	User 8-bit DIP Switch
Keypad	3 x 4 Keypad Switch
Button Switch	User Push-button (8 EA)
LED	LED array (8 EA)
7-Segment display	7-Segment display array (8 EA)
Text LCD	16 characters x 2 lines text display
Full color LED	RGB LED module (4 EA)
TFT LCD	Color LCD (800 x 480 pixels, 5 inch)
Piezo	Piezo buzzer
Step motor	Step motor with magnetic sensor and LEDs

규 격 (2)

구 분	사 양
Image sensor	640x480 VGA, 0.3-Megapixel, Lens Size 1/6inch
Audio ports	Stereo Audio Codec, 8 ~ 96kHz, Integrated Headphone Amplifier Audio input and output ports
Expansion port	25 X 2 I/O Expansion port (5V Supply)
EEPROM	2048 x 8-bit(16k) Two Wire Serial EEPROM
SDRAM	4M x 16-bit x 4 Banks(256Mb) Synchronous DRAM
SRAM	256K x 16-bit (4Mb) High Speed Static RAM
ADC	8-bit digital output (32 MSPS sampling)
DAC	8-bit digital input (125 MSPS)
Bluetooth	Bluetooth 1.2V, UART Interface
USB to serial	USB to Serial Interface
RS232C	RS232C Serial port

Xilinx FPGA Device Families

❑ **Device families of Xilinx® 7 series FPGAs**

Maximum Capability	ARTIX-7 Lowest Power and Cost	KINTEX-7 Industry's Best Price/Performance	VIRTEX-7 Industry's Highest System Performance	ZYNQ-7000 Extensible Processing Platform
Logic Cells	20K – 355K	70K – 480K	285K – 2,000K	30K – 350K
Block RAM	12 Mb	34 Mb	65 Mb	240KB – 2180KB
DSP Slices	40 – 700	240 – 1,920	700 – 3,960	80 – 900
Peak DSP Perf.	504 GMACS	2,450 GMACs	5,053 GMACS	1080 GMACS
Transceivers	4	32	88	16
Transceiver Performance	3.75Gbps	6.6Gbps and 12.5Gbps	12.5Gbps, 13.1Gbps and 28Gbps	6.6Gbps and 12.5Gbps
Memory Performance	1066Mbps	1866Mbps	1866Mbps	1333Mbps
I/O Pins	450	500	1,200	372
I/O Voltages	3.3V and below	3.3V and below 1.8V and below	3.3V and below 1.8V and below	3.3V and below 1.8V and below

Xilinx FPGA Device Families

❑ **Device families in the 7-series provide solutions to address the different price/performance/power requirements**

- ❖ **Spartan®-7 Family: Optimized for low cost, lowest power, and high I/O performance**
- ❖ **Artix™-7 family: Lowest price and power for high volume and consumer applications**
  - **Battery powered devices, automotive, commercial digital cameras**
- ❖ **Kintex™-7 family: Best price/performance**
  - **Wireless and wired communication, medical, broadcast**
- ❖ **Virtex-7 family: Highest performance and capacity**
  - **High-end wired communication, test and measurement, advanced RADAR, high-performance computing**
- ❖ **Zynq-7 family: Xilinx SoC architecture that integrates a dual-core or single-core ARM® Cortex™-A9 based processing system (PS) and 28 nm Xilinx programmable logic (PL) in a single device.**

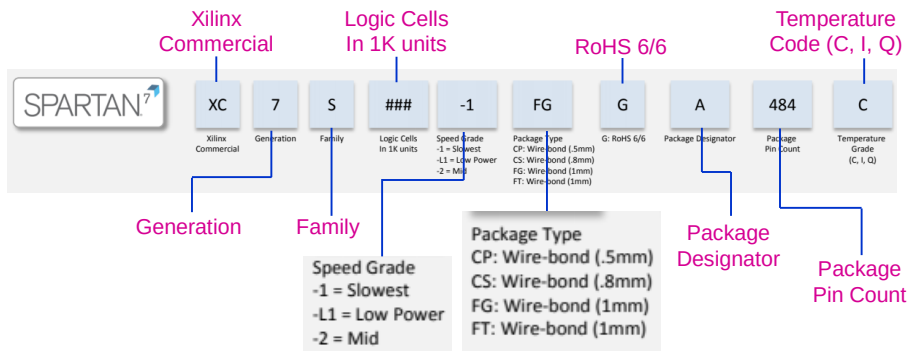
Spartan-7 FPGAs

		I/O Optimization at the Lowest Cost and Highest Performance-per-Watt (1.0V, 0.95V)					
	Part Number	XC7S6	XC7S15	XC7S25	XC7S50	XC7S75	XC7S100
Logic Resources	Logic Cells	6,000	12,800	23,360	52,160	76,800	102,400
	Slices	938	2,000	3,650	8,150	12,000	16,000
	CLB Flip-Flops	7,500	16,000	29,200	65,200	96,000	128,000
Memory Resources	Max. Distributed RAM (Kb)	70	150	313	600	832	1,100
	Block RAM/FIFO w/ ECC (36 Kb each)	5	10	45	75	90	120
	Total Block RAM (Kb)	180	360	1,620	2,700	3,240	4,320
Clock Resources	Clock Mgmt Tiles (1 MMCM + 1 PLL)	2	2	3	5	8	8
I/O Resources	Max. Single-Ended I/O Pins	100	100	150	250	400	400
	Max. Differential I/O Pairs	48	48	72	120	192	192
Embedded Hard IP Resources	DSP Slices	10	20	80	120	140	160
	Analog Mixed Signal (AMS) / XADC	0	0	1	1	1	1
	Configuration AES / HMAC Blocks	0	0	1	1	1	1
Speed Grades	Commercial Temp (C)	-1,-2	-1,-2	-1,-2	-1,-2	-1,-2	-1,-2
	Industrial Temp (I)	-1,-2,-1L	-1,-2,-1L	-1,-2,-1L	-1,-2,-1L	-1,-2,-1L	-1,-2,-1L
	Expanded Temp (Q)	-1	-1	-1	-1	-1	-1

Package[1]	Body Area (mm)	Ball Pitch (mm)	Available User I/O: 3.3V SelectIO™ HR I/O					
CPGA196	8x8	0.5	100	100				
CSGA225	13x13	0.8	100	100	150			
CSGA324	15x15	0.8			150	210		
FTGB196	15x15	1.0	100	100	100	100		
FGGA484	23x23	1.0				250	338	338
FGGA676	27x27	1.0					400	400

1. Packages with the same last letter and number sequence, e.g., A484, are footprint compatible with all other Spartan-7 devices with the same sequence. The footprint compatible devices within this family are outlined.

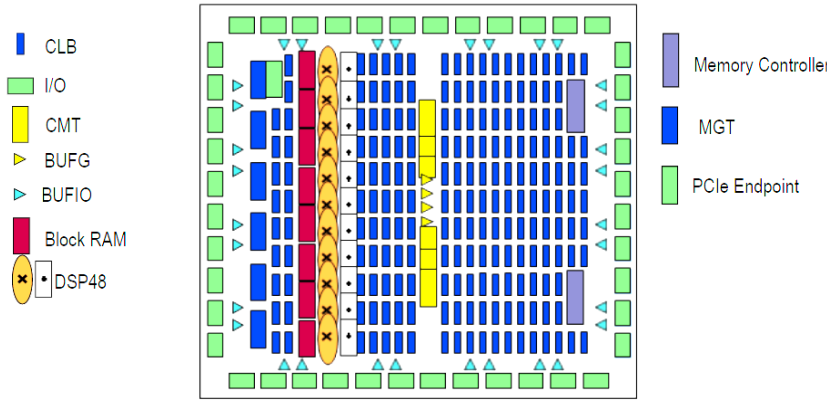
XC7S75-FGGA484-1



Notes:
-L1 is the ordering code for the lower power, -1L speed grade.
-L2 is the ordering code for the lower power, -2L speed grade.
C = Commercial (Tj = 0°C to +85°C) E = Extended (Tj = 0°C to +100°C) I = Industrial (Tj = –40°C to +100°C) Q = Expanded (Tj = –40°C to +125°C)

Spartan7 FPGA

❑ FPGA Architecture (Spartan6)

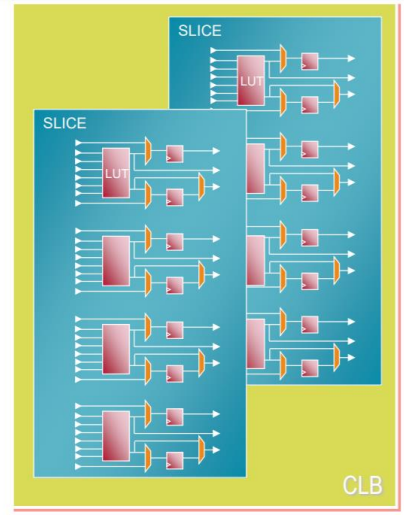


- CLB: Configurable Logic Block
- CMT: Clock Management Tile
- MGT: Multi-Gigabit Transceiver

Spartan7 FPGA

❑ Configurable Logic Block (CLB)

- Two side-by-side slices per CLB
  - Slice_M are memory-capable
  - Slice_L are logic and carry only
- Four 6-input LUTs per slice
  - Consistent with previous architectures
  - Single LUT in Slice_M can be a 32-bit shift register or 64 x 1 RAM
- Two flip-flops per LUT
  - Excellent for heavily pipelined designs
  -



Spartan7 FPGA

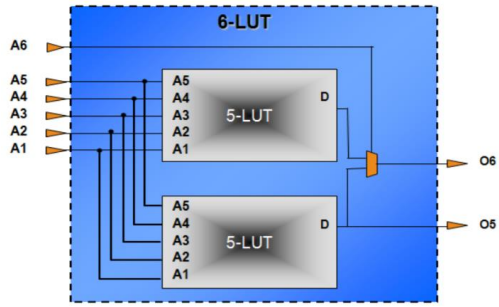
❑ 6-Input LUT with Dual Output

❖ LUTs can be two 5-input LUTs with common input

– Minimal speed impact to a 6-input LUT

– One or two outputs

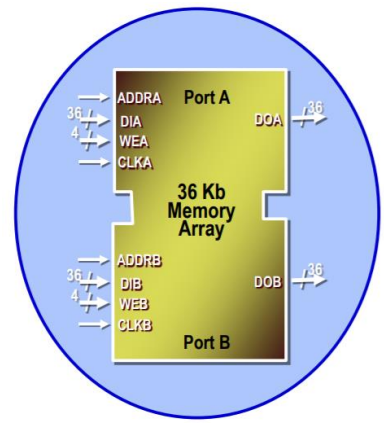
❖ Any function of six variables or two functions of five variables



Spartan7 FPGA

❑ Block RAM

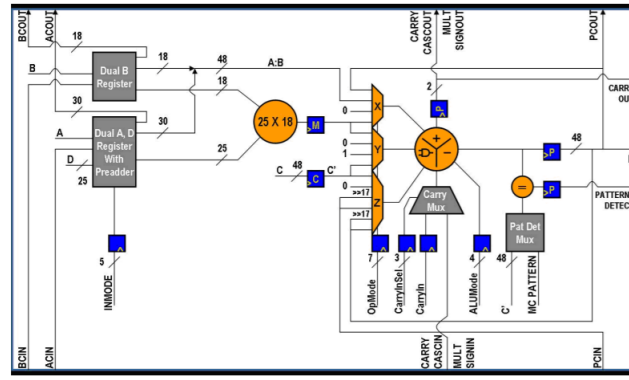
- 36K/18K block RAM
  - All Xilinx 7 series FPGA families use same block RAM as Virtex-6 FPGAs
- Configurations same as Virtex-6 FPGAs
  - 32k x 1 to 512 x 72 in one 36K block
  - Simple dual-port and true dual-port configurations
  - Built-in FIFO logic
  - 64-bit error correction coding per 36K block
  - Adjacent blocks combine to 64K x 1 without extra logic



Spartan7 FPGA

❑ DSP Slice

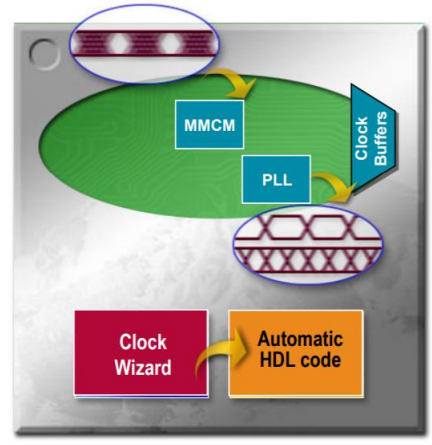
- All 7 series FPGAs share the same DSP slice
  - 25x18 multiplier
  - 25-bit pre-adder
  - Flexible pipeline
  - Cascade in and out
  - Carry in and out
  - 96-bit MACC
  - SIMD support
  - 48-bit ALU
  - Pattern detect
  - 17-bit shifter
  - Dynamic operation (cycle by cycle)



Spartan7 FPGA

❑ Clocking Resources

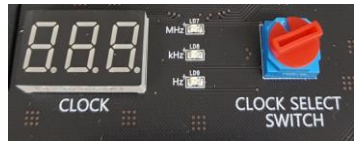
- Based on the established Virtex-6 FPGA clocking structure
  - All 7 series FPGAs use the same unified architecture
- Low-skew clock distribution
  - Combination of paths for driving clock signals to and from different locations
- Clock buffers
  - High fanout buffers for connecting clock signals to the various routing resources
- Clock regions
  - Device divided into clock regions with dedicated resources
- Clock management tile (CMT)
  - One MMCM and one PLL per CMT
  - Up to 24 CMTs per device



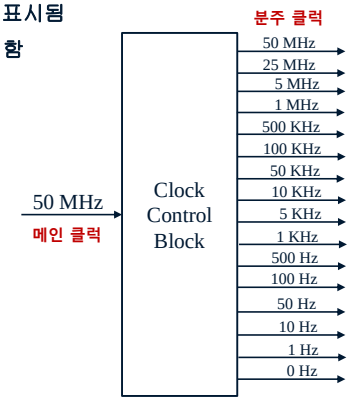
Clock Select (1)

❑ Clock Block

- ❖ FPGA 내부 회로에서 사용될 클럭 신호를 생성
- ❖ 50 MHz 메인 클럭을 16가지의 주파수로 분주하여 사용
- ❖ 설정된 클럭 주파수 값이 7-세그먼트에 표시되고,
  클럭 주파수 range (MHz, KHz, Hz)가 LED에 표시됨
- ❖ CLOCK Select Switch로 클럭 주파수를 선택함



주파수 값 표시 | 주파수 range 표시 | 클럭 선택 스위치



Clock Select (2)

❑ 분주클럭 주파수

Clock SW	클럭 주파수	Clock SW	클럭 주파수	Clock SW	클럭 주파수	Clock SW	클럭 주파수
0	0Hz	4	100Hz	8	10kHz	C	1MHz
1	1Hz	5	500Hz	9	50kHz	D	5MHz
2	10Hz	6	1kHz	A	100kHz	E	25MHz
3	50Hz	7	5kHz	B	500kHz	F	50MHz

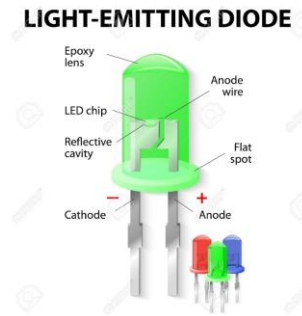
❑ 핀 구성

FPGA Signal	Pin	Description
CLK_MAIN[0]	B6	Main Clock Input
CLK_MAIN[1]	M8	Main Clock Input
CLK_MAIN[2]	M15	Main Clock Input
CLK_MAIN[3]	P15	Main Clock Input

LED Array (1)

❑ LED 배열

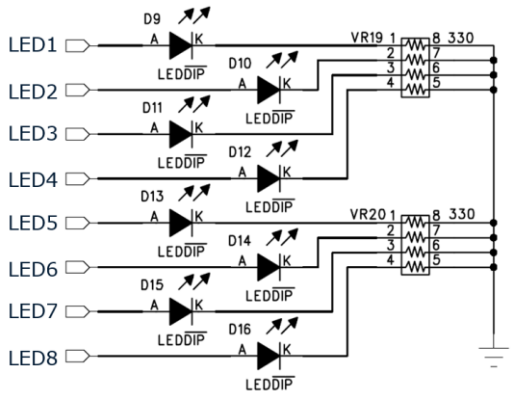
- ❖ 8개의 DIP 타입 LED
- ❖ 비트 단위의 출력 확인 또는 동작상태 확인을 위해 사용됨
- ❖ LED의 Anode 단자에 디지털신호 '1'이 인가되면, LED가 발광 됨



▪ 장비에 전원을 연결할 때 LED의 특성상 미세한 전류 흐름에 의해 희미하게 LED가 켜지는 경우가 있으나, 이는 장비의 고장이 아니며 프로그램 되지 않는 디바이스의 잔류 전류가 남아서 나타나는 현상임

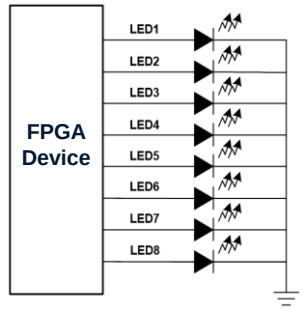
LED Array (2)

❑ 회로도



LED Array (3)

❑ 핀 구성

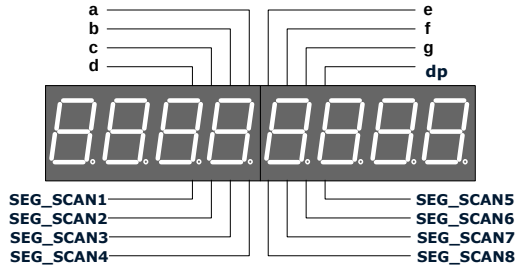


FPGA Signal	Pin	Description
LED1	U5	D1 LED display
LED2	V1	D2 LED display
LED3	V4	D3 LED display
LED4	V5	D4 LED display
LED5	W1	D5 LED display
LED6	W2	D6 LED display
LED7	W3	D7 LED display
LED8	Y1	D8 LED display

7-Segment Array (1)

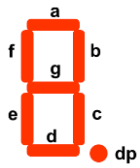
❑ 7-Segment 배열

- ❖ 8개의 7-세그먼트 표시장치로 구성됨
- ❖ 각 7-세그먼트 데이터 입력 라인은 공통으로 연결됨
- ❖ 표시될 7-세그먼트를 SEG_SCAN1 ~ SEG_SCAN8로 제어함



7-Segment Array (2)

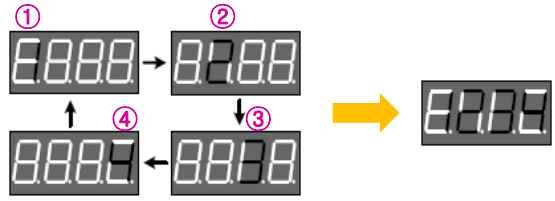
❑ 7-Segment 배열



Display Data	Decode Data							
	a	b	c	d	e	f	g	dp
0	1	1	1	1	1	1	0	0
1	0	1	1	0	0	0	0	0
2	1	1	0	1	1	0	1	0
3	1	1	1	1	0	0	1	0
4	0	1	1	0	0	1	1	0
5	1	0	1	1	0	1	1	0
6	1	0	1	1	1	1	1	0
7	1	1	1	0	0	0	0	0
8	1	1	1	1	1	1	1	0
9	1	1	1	1	0	1	1	0
A	1	1	1	0	1	1	1	0
B	0	0	1	1	1	1	1	0
C	1	0	0	1	1	1	0	0
D	0	1	1	1	1	0	1	0
E	1	0	0	1	1	1	1	0
F	1	0	0	0	1	1	1	0

7-Segment Array (3)

❑ 동 작



① SEG_SCAN = “0111”, SEG_DATA = “0110_0000”

② SEG_SCAN = “1011”, SEG_DATA = “1101_1010”

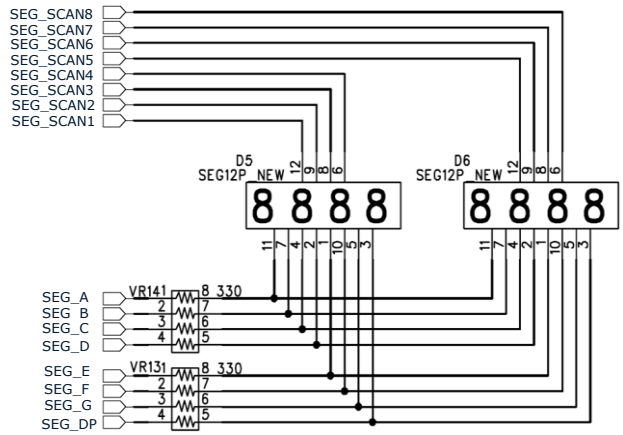
③ SEG_SCAN = “1101”, SEG_DATA = “1111_0010”

④ SEG_SCAN = “1110”, SEG_DATA = “0110_0110”

- 4까지의 숫자를 표시하고, 다시 처음으로 돌아가 위의 내용을 반복
- 약 1ms 이상의 주기로 반복하면 잔상효과에 의해 “1234”의 숫자가 모두 켜져 있는 것처럼 표시됨

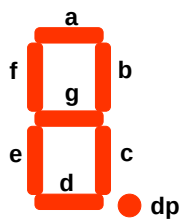
7-Segment Array (4)

❑ 회로도



7-Segment Array (5)

❑ 핀 구성

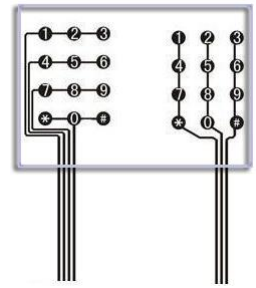


a = SEG_A
b = SEG_B
c = SEG_C
d = SEG_D
e = SEG_E
f = SEG_F
g = SEG_G
dp = SEG_DP

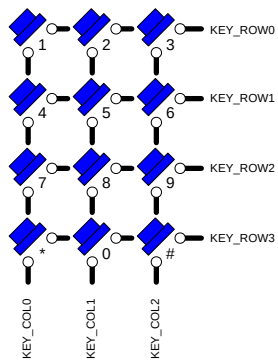
FPGA Signal	Pin	Description
SEG_A	P1	Segment Data A
SEG_B	N5	Segment Data B
SEG_C	N4	Segment Data C
SEG_D	N3	Segment Data D
SEG_E	N1	Segment Data E
SEG_F	M5	Segment Data F
SEG_G	M4	Segment Data G
SEG_DP	M3	Segment Data Dot
SEG_SCAN1	T2	Segment scan1
SEG_SCAN2	T1	Segment scan2
SEG_SCAN3	R5	Segment scan3
SEG_SCAN4	R4	Segment scan4
SEG_SCAN5	R3	Segment scan5
SEG_SCAN6	R2	Segment scan6
SEG_SCAN7	P3	Segment scan7
SEG_SCAN8	P2	Segment scan8

Key Pad (1)

- **Key Pad**
  - 4행 x 3열의 12개 키로 구성됨
  - 스캔 방식으로 동작하여 어떤 키가 눌려졌는지 결정됨
    - 키 패드의 열(column) 핀을 스캔으로 구동



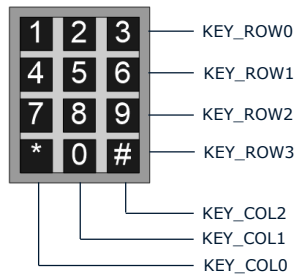
Key Pad (2)



FPGA → Key Pads	버튼 누름	Key Pads → FPGA
KEY_COL[2:0]		KEY_ROW[3:0]
"001"	버튼 1	"0001"
"001"	버튼 4	"0010"
"001"	버튼 7	"0100"
"001"	버튼 *	"1000"
"010"	버튼 2	"0001"
"010"	버튼 5	"0010"
"010"	버튼 8	"0100"
"010"	버튼 0	"1000"
"100"	버튼 3	"0001"
"100"	버튼 6	"0010"
"100"	버튼 9	"0100"
"100"	버튼 #	"1000"
"XXX"	버튼 안 누름	"0000"

Key Pad (3)

❑ 핀 구성

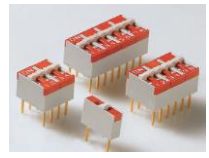


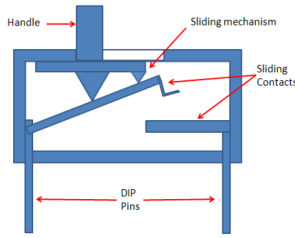
FPGA Signal	Pin	Description
KEY_COL0	V8	Column0 Data
KEY_COL1	AA8	Column1 Data
KEY_COL2	Y8	Column2 Data
KEY_ROW0	AA9	Row0 Data
KEY_ROW1	AB9	Row1 Data
KEY_ROW2	AA10	Row2 Data
KEY_ROW3	AB10	Row3 Data

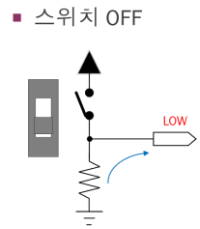
DIP Switch (1)

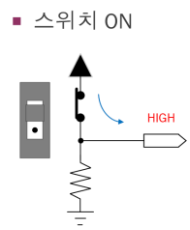
❑ DIP 스위치

- ❖ 8-비트의 버스 입력을 위한 DIP 스위치
- ❖ 데이터의 입력이나 회로의 동작모드 설정을 위한 스위치로 사용됨
- ❖ 스위치를 위로 올리면 '1'의 값이 전달되고, 내리면 '0'의 값이 FPGA로 전달됨



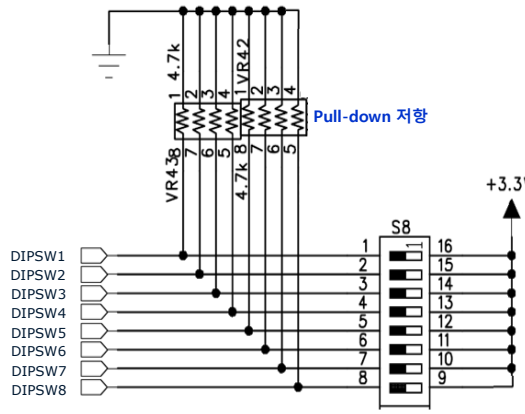






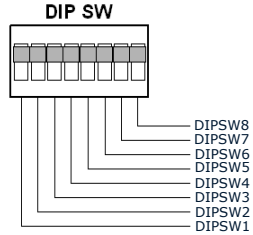
DIP Switch (2)

❑ 회로도



DIP Switch (3)

❑ 핀 구성



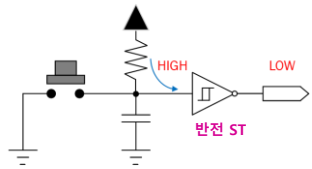
FPGA Signal	Pin	Description
DIPSW1	AB3	Bus Switch Data1
DIPSW2	AB4	Bus Switch Data2
DIPSW3	Y4	Bus Switch Data3
DIPSW4	Y5	Bus Switch Data4
DIPSW5	W5	Bus Switch Data5
DIPSW6	V6	Bus Switch Data6
DIPSW7	AB5	Bus Switch Data7
DIPSW8	AA6	Bus Switch Data8

Button Switch (1)

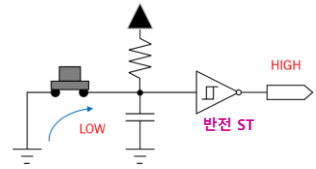
❑ **Button Switch**

- ❖ **bit 단위의 사용자 신호 입력을 위해 사용**
- ❖ **스위치가 눌러지면 '1'이 출력됨**
- ❖ **스위치가 안 눌러지면 '0'이 출력됨**
- ❖ **버튼 스위치가 눌려 질 때 발생하는 채터링 잡음을 제거하기 위한 회로(Schmitt Trigger)가 내장됨**

▪ 스위치 OFF 시

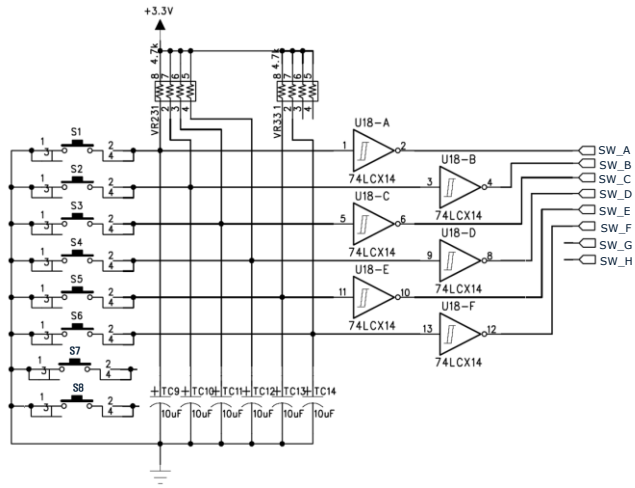


▪ 스위치 ON 시



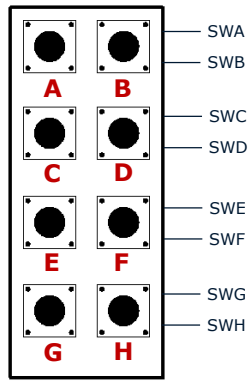
Button Switch (2)

❑ 회로도



Button Switch (3)

❑ 핀 구성



FPGA Signal	Pin	Description
SW_A	Y6	Detected High
SW_B	V7	Detected High
SW_C	AB6	Detected High
SW_D	Y7	Detected High
SW_E	W7	Detected High
SW_F	AB7	Detected High
SW_G	AA7	Detected High
SW_H	W8	Detected High

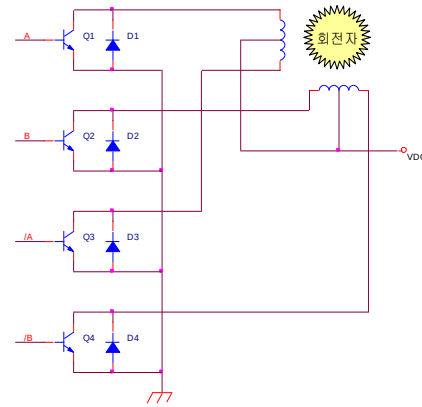
Step Motor (1)

❑ **Step Motor**

- ❖ 인가되는 펄스에 의해 일정한 각도(스텝)씩 회전
- ❖ 스텝 각이 1.8도라면, 200펄스를 인가해야 1회전함
- ❖ 시간당 펄스 수 (펄스의 주파수)에 따라 모터의 회전 속도가 달라짐
- ❖ 1상 여자, 2상 여자, 1-2상 여자 방식으로 구동
  - ➢ 4비트 신호(A, B, /A, /B)에 의해 구동됨
- ❖ 자기센서(magnetic sensor): 모터가 회전할 때 자석에 의한 자기를 감지하여 펄스를 출력하며, 이 펄스를 이용하여 모터의 회전 수를 계수

Step Motor (2)

- BJT가 ON되면, 공통단자로부터 A상이나 /A상, 또는 B상이나 /B 상으로 전류가 흐름
- BJT가 OFF일 때는 전류가 흐르지 않음
- 전류가 흐를 때에는 항상 그 방향이 일정하므로 유니폴라 구동 방식이라고 함
- 다이오드는 역기전력으로부터 모터를 보호하기 위한 용도로 사용
- A, B, /A, /B에 HIGH를 인가하여 해당하는 BJT를 ON시키면, BJT의 컬렉터에 연결되어 있는 코일에 전류가 흐르게 되며, 코일이 여자(excitation) 됨



유니폴라 구동 회로

Step Motor (3)

➢ 유니폴라 구동 스텝모터 여자방식

	스텝 1	스텝 2	스텝 3	스텝 4
A	1	0	0	0
B	0	1	0	0
/A	0	0	1	0
/B	0	0	0	1

1상 여자

	스텝 1	스텝 2	스텝 3	스텝 4
A	1	0	0	1
B	1	1	0	0
/A	0	1	1	0
/B	0	0	1	1

2상 여자

	스텝 1	스텝 2	스텝 3	스텝 4	스텝 5	스텝 6	스텝 7	스텝 8
A	1	1	0	0	0	0	0	1
B	0	1	1	1	0	0	0	0
/A	0	0	0	1	1	1	0	0
/B	0	0	0	0	0	1	1	1

1 – 2상 여자

Step Motor (4)

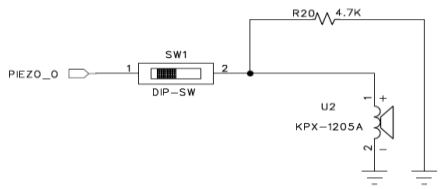
❑ 핀 구성

FPGA Signal	Pin	Description
STEP_A	AB2	Data-A
STEP_/A	AA2	Data-/A
STEP_B	AA3	Data-B
STEP_/B	AA1	Data-/B
STEP_Sensor	Y3	Data from magnetic sensor

Piezo (1)

❑ Piezo

❖ 인가되는 펄스의 주파수에 따라 소리가 발생



Signal Name	Pin
PIEZO	W4

음계	옥타브		
	3	4	5
도	130.8128 Hz	261.6256 Hz	523.2511 Hz
레	146.8324 Hz	293.6648 Hz	587.3295 Hz
미	164.8138 Hz	329.6276 Hz	659.2551 Hz
파	174.6141 Hz	349.2282 Hz	698.4565 Hz
솔	195.9977 Hz	391.9954 Hz	783.9909 Hz
라	220.0000 Hz	440.0000 Hz	880.0000 Hz
시	246.9417 Hz	493.8833 Hz	987.7666 Hz

TEXT LCD (1)

- Text LCD
  - 16문자 X 2의 표시부

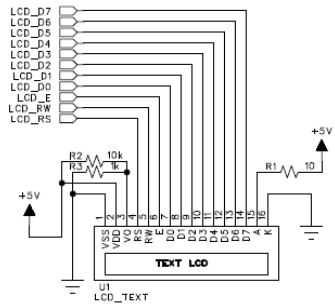
Instruction	CODE									
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Display Clear	0	0	0	0	0	0	0	0	0	1
Cursor Home	0	0	0	0	0	0	0	0	1	X
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B
Cursor/Display Shift	0	0	0	0	0	1	S/C	R/L	X	X
Function Set	0	0	0	0	1	IF	N	X	X	X
CGRAM Address Setting	0	0	0	1	ACG					
DDRAM Address Setting	0	0	1	ADD						
Busy Flag & Address Reading	0	1	BF	AC						
Busy Writing to CG or DDRAM	1	0	Write Data							
Data Reading from CG or DDRAM	1	1	Read Data							

TEXT LCD (2)

- DD-RAM : Display Data RAM
- CG-RAM : Character Generator RAM
- ACG : CG-RAM Address
- ADD : DD-RAM Address
- ACC : Address Counter
- I/D = 1 : Increment, I/D = 0 : Decrement
- S = 1 : Display shift enabled, S = 0 : Cursor shift enabled
- S/C = 1 : Display shift S/C = 0 : Cursor move
- R/L = 1 : Shift to the right R/L = 0 : Shift to the left
- IF = 1 : 8bit IF = 0 : 4bit
- N = 1 : 2Lines display N = 0 : 1 Line display
- BF = 1 : Busy (Internally operation)
  BF = 0 : Not busy (Instruction acceptable)

TEXT LCD (3)

❑ 핀 구성



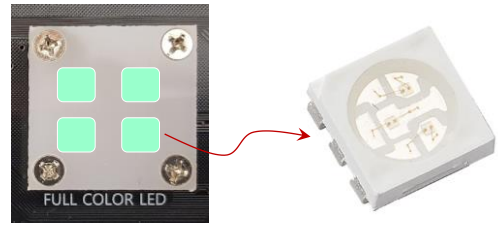
- R2와 R3에 의해 문자 표시의 휘도 값 설정함
- 15, 16번은 Back Light에 대한 전원

FPGA Signal	Pin	Description
LCD_D0	L4	LCD Data0
LCD_D1	L1	LCD Data1
LCD_D2	K5	LCD Data2
LCD_D3	K4	LCD Data3
LCD_D4	K3	LCD Data4
LCD_D5	K2	LCD Data5
LCD_D6	K1	LCD Data6
LCD_D7	J3	LCD Data7
LCD_E	L5	Enable Signal for read/write LCD
LCD_RS	M2	LCD Register Select (0 = instruction, 1 = data)
LCD_RW	M1	Read/Write (0 : FPGA → LCD 1 : FPGA ← LCD)

Full Color LED (1)

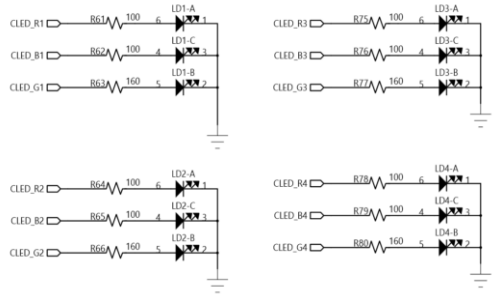
❑ Full Color LED

- ❖ RGB LED 4개로 구성됨
- ❖ R(Red), G(Green), B(Blue) 3가지 색의 LED를 하나의 Device로 합친 LED
- ❖ R, G, B의 각 LED를 밝기 제어함으로써 원하는 색의 빛을 만들어 냄



Full Color LED (2)

❑ 핀 구성



Signal Name	Pin	Signal Name	Pin
CLED_R1	C2	CLED_R3	C3
CLED_G1	C1	CLED_G3	B3
CLED_B1	D1	CLED_B3	B2
CLED_R2	D4	CLED_R4	E5
CLED_G2	C4	CLED_G4	D5
CLED_B2	A3	CLED_B4	A4

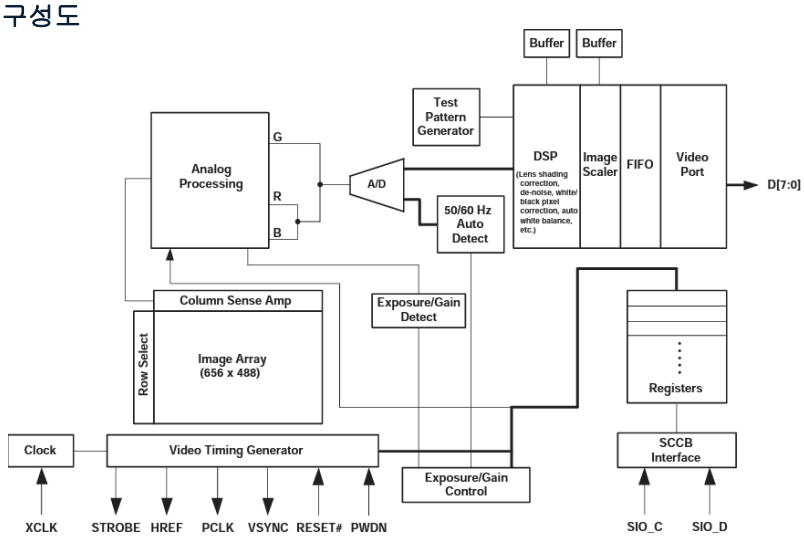
CMOS Image Sensor (1)

❑ CMOS image sensor (카메라 모듈)

Part	사 양
Photosensitive Array	640 x 480
Output Format	YUV/YCbCr/RGB565/RGB555 Raw RGB Data(8bit)
Lens size	1/6 inch
Vision angle	25°
Max Frame rate	30fps VGA

CMOS Image Sensor (2)

❑ 구성도



CMOS Image Sensor (3)

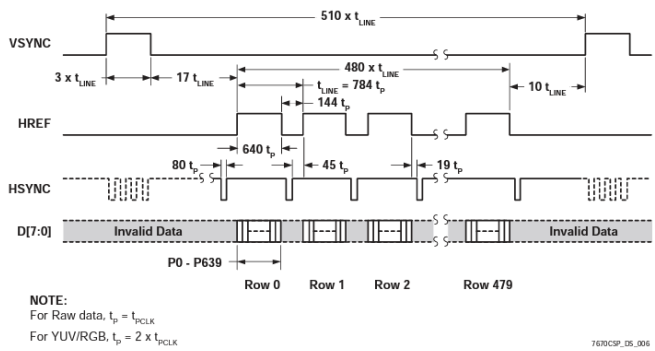
❑ 프레임(Frame) 동작 타이밍

❖ VSYNC는 프레임 동기 신호

➢ 1개의 프레임에는 510개의 t_{LINE} (HREF 단위)의 시간이 카운트 됨

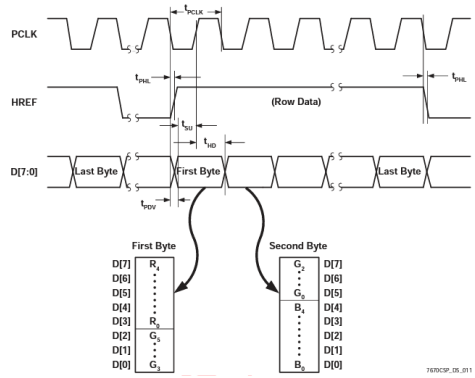
➢ 라인을 나타내는 HREF가 총 480개 카운트 됨

➢ 1개의 라인에는 640 + 144개의 t_P (PCLK)이 카운트 됨



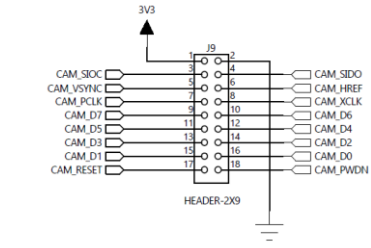
CMOS Image Sensor (4)

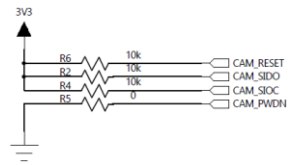
- RGB565 출력의 수평(라인) 타이밍(Horizontal Timing)
  - HREF 신호가 HIGH인 동안에 PCLK 펄스 마다 픽셀 데이터가 D[7:0] 핀에서 병렬 출력
  - HREF 신호는 하나의 라인 픽셀 데이터가 출력되는 동안 HIGH가 유지됨
  - RGB565 데이터는 16-b이므로, 2개의 8-b 값을 받아 그림과 같이 RGB565 데이터로 변환하는 과정이 필요함



CMOS Image Sensor (5)

- 회로도





Part	기 능
CAM_SIOC	SCCB Clock Pin
CAM_SIDO	SCCB Data Pin
CAM_XCLK	System Clock (in)
CAM_PCLK	Pixel Clock(out)
CAM_VSYNC	Vertical synchronization (out)
CAM_HREF	Horizontal synchronization(out)
CAM_D0-7	Video Parallel output(out)
CAM_RESET	Reset(in, Active Low)
CAM_PWDN	Powe down(in, Active High)

CMOS Image Sensor (6)

❑ 핀 구성

FPGA Signal	Pin	FPGA Signal	Pin
CAM_SIOC	C5	CAM_D0	C9
CAM_SIDO	A5	CAM_D1	B8
CAM_XCLK	A6	CAM_D2	C8
CAM_PCLK	C6	CAM_D3	D8
CAM_VSYNC	F6	CAM_D4	E8
CAM_HREF	D6	CAM_D5	A7
CAM_RESET	B9	CAM_D6	B7
CAM_PWDN	A9	CAM_D7	D7

Bluetooth

❑ 무선 통신을 위한 **Bluetooth** 모듈

❖ **RS232C** 통신과 같이 **TxD**와 **RxD** 라인을 제어하여 통신

구 분	사 양
Bluetooth Spec	Bluetooth Specification V1.2
통신 거리	최대 30M
Antenna	Chip Antenna
통신 속도	9,200 BPS
Interface	UART(TTL Level)

신호	기 능
RxD	Bluetooth Module 의 Data Receive Pin
TxD	Bluetooth Module의 Data Transmit Pin
Status	외부 장치와 접속을 시도하거나 끊어졌을 때, LED가 깜빡임

FPGA Signal	Pin
XURXD2	T3
XUTXD2	T5