Vivado 설계 실습

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Verilog HDL

Xilinx Vivado 설계 실습

Vivado 설계 흐름

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- 1. Vivado project 생성
- 2. 설계 입력
- 3. RTL 시뮬레이션
- 4. 설계 합성
- 5. 설계 구현
- 6. FPGA 디바이스 프로그래밍

Verilog HDL

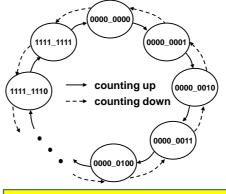
설계실습 예제 회로

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- □ 8비트(256진) 증가/감수 계수기
 - ❖ mode=0; +1씩 증가하는 증가 계수기(up counter)로 동작
 - ❖ mode=1; -1씩 감소하는 감소 계수기(down counter)로 동작
 - ❖ Active-high 동기식 리셋을 가짐

공가/감소 계수기의 공식		
rst	mode	동작
0	0	+1씩 증가
	1	-1씩 감소

0000 0000으로 초기화



증가/감소 계수기의 상태천이도

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설계실습 예제 회로 - Verilog source code 4

```
module counter_ud (clk, rst, mode, cnt);
 input
                 clk, rst, mode;
 output [7:0]
                  cnt;
          [7:0]
 reg
                  cnt;
always @(posedge clk) begin
  if (rst) cnt <= 0;
   else begin
      if (mode) cnt <= cnt - 1;
      else cnt <= cnt + 1;</pre>
   end
end
endmodule
```

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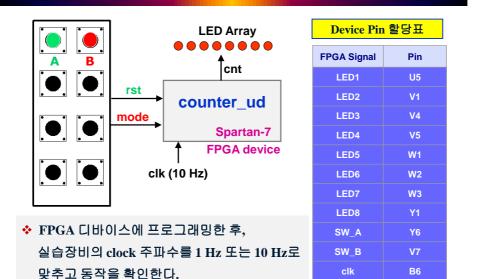
설계실습 예제 회로 – Verilog Testbench

```
module tb_counter_ud;
              clk, rst, mode;
 wire [7:0] cnt;
  counter_ud U0 (clk, rst, mode, cnt);
 initial begin
    clk = 0;
    mode = 0;
 always
    #10 clk = ~clk;
 always
    #320 mode = ~mode;
  initial begin
             rst = 0;
   #5 rst = 1;
   #30 rst = 0;
   #100 rst = 1;
   #30 rst = 0;
 end
endmodule
```

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설계실습 예제 회로 – 실습회로 구성도

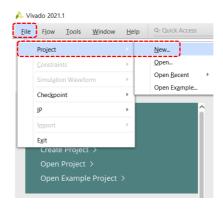


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1. Project 생성







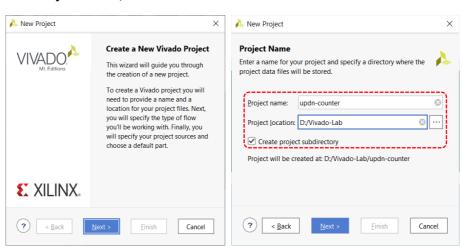
Verilog HDL

Xilinx Vivado 설계 실습

1.1 Project 생성 – New Project

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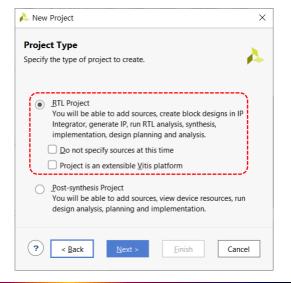


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1.1 Project 생성 – New Project

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■ Project Type 설정



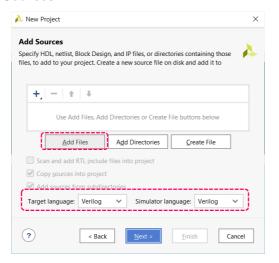
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Xilinx Vivado 설계 실습

1.2 Project 생성 – Add Sources

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Add Sources



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1.2 Project 생성 – Add Sources

Add Source Files Look <u>i</u>n: Source Recent Directories tb counter ud.v D:/Source nodule counter_ud (clk, rst, mode, cnt); clk, rst, mode; [7:0] cnt; [7:0] cnt; output reg always @(posedge clk) begin if (rst) cnt <= 0; else begin if (mode) cnt <= cnt - 1; else cnt <= cnt + 1; end File name: "counter_ud.v" "tb_counter_ud.v" Files of type: Design Source Files (.vhd, vhdl, vhf, vhdp, vho, v, vf, verilog, vr, vg, vb, tf, vlog, vp, v

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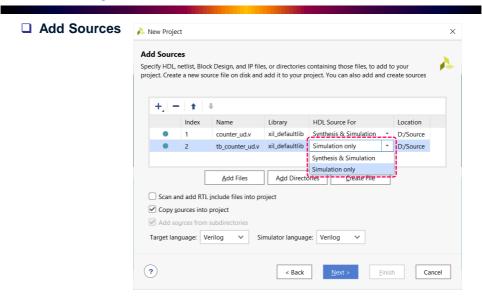
Add Sources

Xilinx Vivado 설계 실습

1.2 Project 생성 – Add Sources

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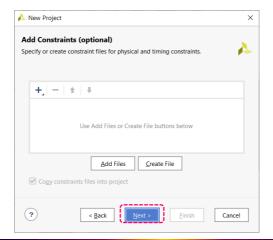
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1.3 Project 생성 – Add Constraints

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- Add Constraints
 - ❖ Constraint 파일(Xilinx Design Constraint; XDC) 생성 및 기존 파일 추가



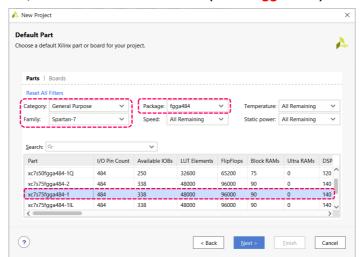
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1.4 Project 생성 – Default Part

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□ Default Part; FPGA 디바이스 및 보드 선택 (xc7s75fgga484-1)

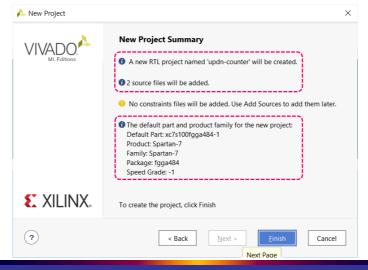


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1.5 Project 생성 – Project Summary

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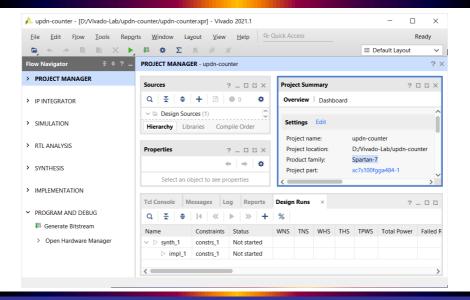


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1.6 Project 생성 – 완료된 상태

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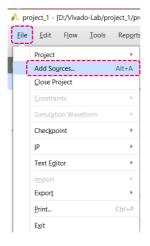


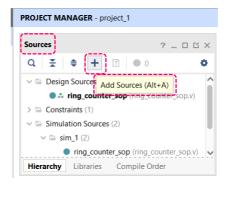
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2.1 설계입력 - Add Sources

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Add Sources





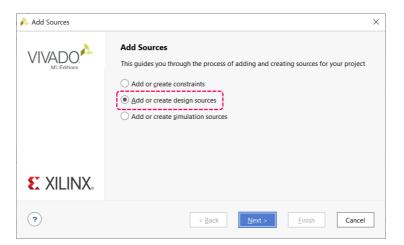
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Xilinx Vivado 설계 실습

2.1 설계입력 - Add Sources

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■ Add or Create Design Sources

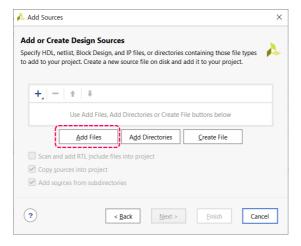


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2.1 설계입력 – Add Files

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□ Add Design Sources



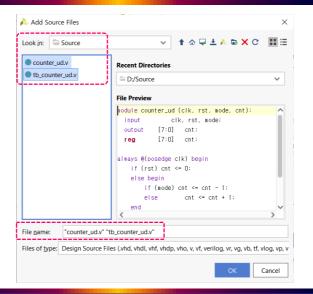
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Xilinx Vivado 설계 실습

2.1 설계입력 - Add Files

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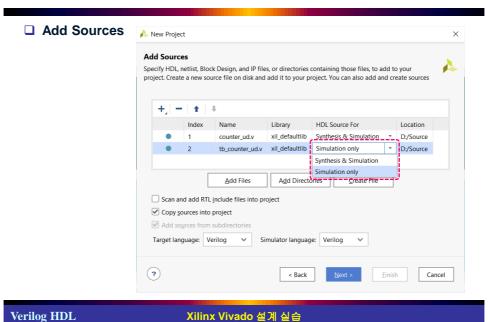
Add Sources



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2.1 설계입력 - Add Files

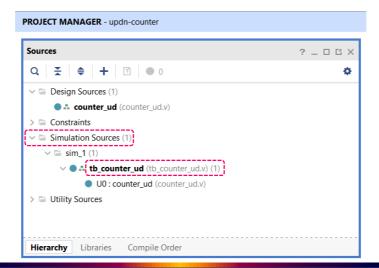
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3.1 RTL 시뮬레이션

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□ 테스트벤치 파일 확인

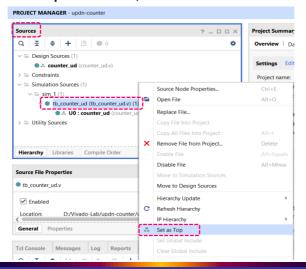


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3.2 RTL 시뮬레이션 – Top 모듈 지정

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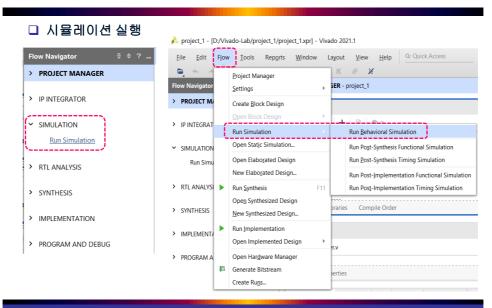
□ 테스트벤치를 top 모듈로 설정; 테스트 벤치 파일 우클릭 → Set as Top



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Xilinx Vivado 설계 실습

3.3 RTL 시뮬레이션 – Run Simulation

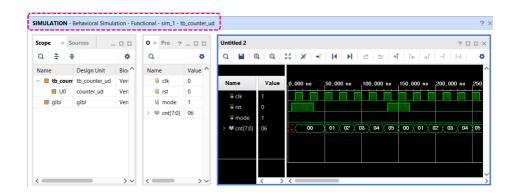


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3.4 RTL 시뮬레이션 - 결과 확인

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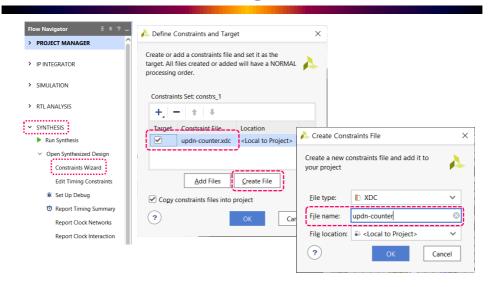
□ 시뮬레이션 결과 확인



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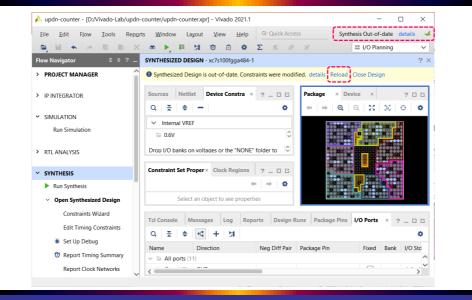
Xilinx Vivado 설계 실습

4.1 설계 합성 – Timing Constraints 설정 26



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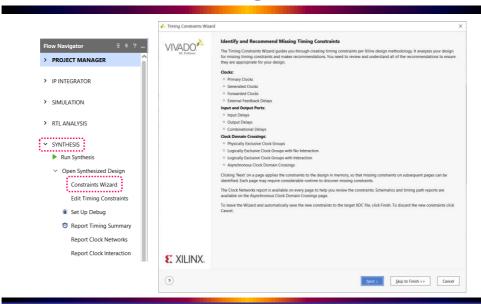
4.1 설계 합성 – Timing Constraints 설정 27



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Xilinx Vivado 설계 실습

4.1 설계 합성 – Timing Constraints 설정 28



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4.1 설계 합성 – Timing Constraints 설정 29

A Timing Constraints Wizard ■ Timing Constraints 설정 **Primary Clocks** Primary clock, Primary clocks usually enter the design though input ports. Specify the period and optionally a name and waveform (rising and falling edge times) to describe the duty cycle if not 50%. More info input/output delay 등 Recommended Constraints 합성 과정에 적용되는 O p O m ☑ Object Name Frequency (MHz) Period (ns) Bise At (ns) Fall At (ns) litter (ns) constraints 설정 ☑ [I]] clk clk 20.000 50.000 0.000 25.000 5.000 Constraints for Pulse Width Check Only Object Name Frequency (MHz) Period (ns) Rise At (ns) Fall At (ns) Jitter (ns) Tcl Command Preview (2) Existing Create Clock Constraints (0) Q create clock-period 50.000 -name clk -waveform (0.000 25.000) [get_ports {clk}] set_input_jitter clk 5.000

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Xilinx Vivado 설계 실습

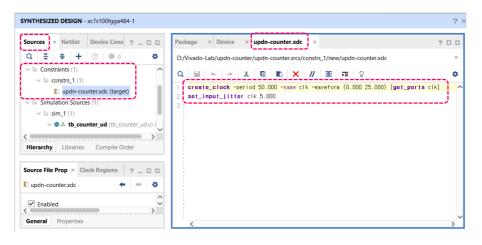
4.2 설계 합성 - XDC 파일 확인

?

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< <u>Back</u> Next > <u>Skip to Finish >> Cancel</u>

□ Xilinx Design Constraints(XDC) 파일 확인

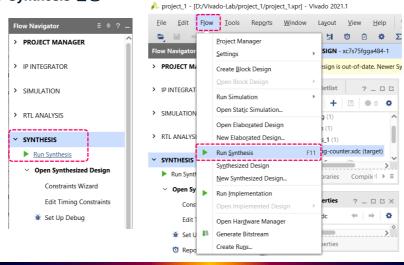


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4.3 설계 합성 – Run Synthesis

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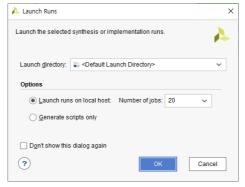
Verilog HDL

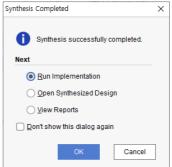
Xilinx Vivado 설계 실습

4.3 설계 합성 – Run Synthesis

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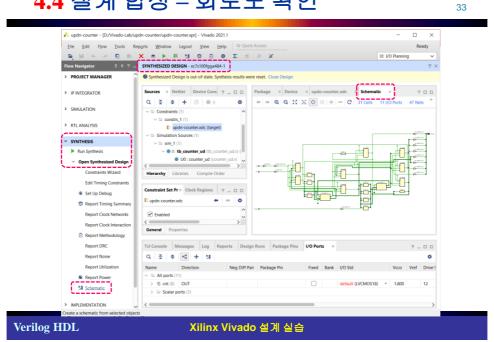
■ Synthesis 실행





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4.4 설계 합성 – 회로도 확인



5.1 설계 구현 - 디바이스 핀 할당

I/O Planning

✓ ■ Default Layout > PROJECT MANAGER □ Debug Q = 0 0 ∨ □ Constraints (1)
 ∨ □ constrs_1 (1) > RTL ANALYSIS updn-counter.xdc (target) Edit Timing Constraints ¥ Set Up Debug Report Clock Networks Report Clock Interaction Report DRC Report Noise Q 불 🛊 🖪 + 별 Report Utilization Neg Diff Pair Package Pin Fixed Bank I/O Std ★ Report Power default (LVCMOS18) * ∨ 1 cnt (8) OUT Schematic **Verilog HDL** Xilinx Vivado 설계 실습

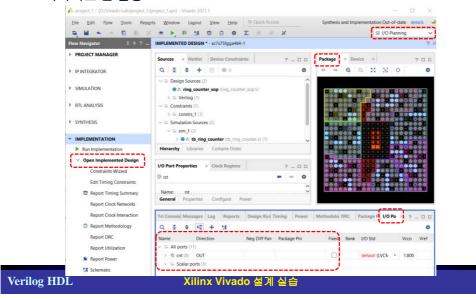
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5.1 설계 구현 - 디바이스 핀 할당

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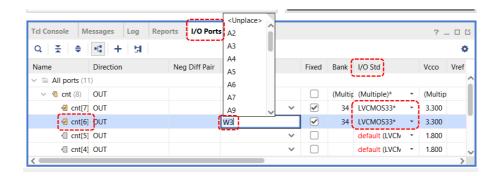




5.1 설계 구현 - 디바이스 핀 할당

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- □ 디바이스 핀 할당(I/O Ports 탭)
 - ❖ port 선택, Package Pin 컬럼에 핀 할당(핀 할당 테이블 참조)
 - ❖ I/O Std 컬럼; LVCMOS33으로 선택

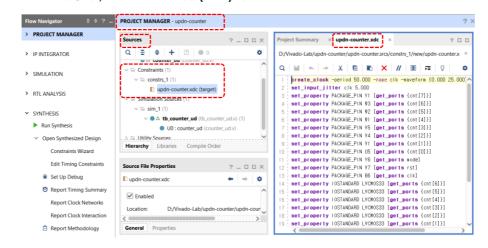


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5.2 설계 구현 - XDC 파일 확인

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❖ 저장 후, Constraints 파일(XDC) 확인



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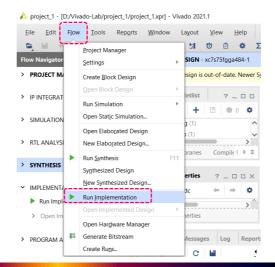
Xilinx Vivado 설계 실습

5.3 설계 구현 – Run Implementation

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■ Implementation 실행



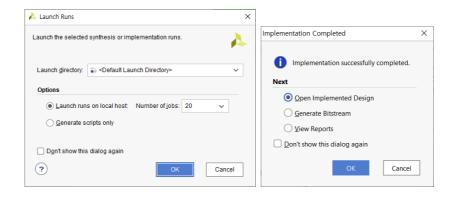


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5.3 설계 구현 - Run Implementation

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■ Implementation 실행

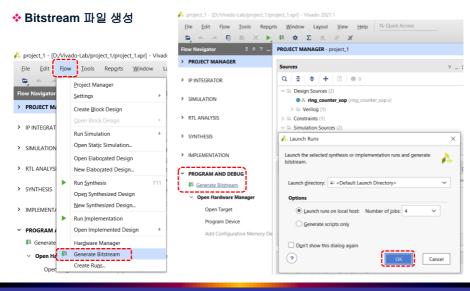


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6.1 FPGA 디바이스 프로그래밍

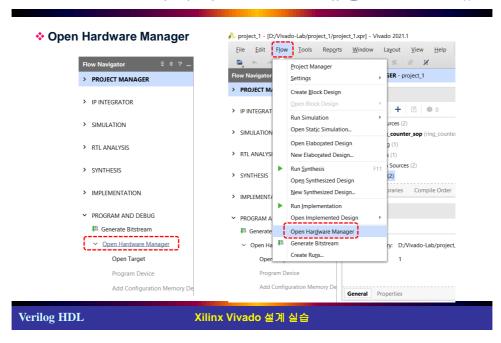
40



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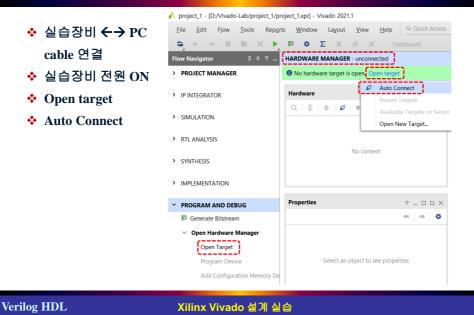
6.1 FPGA 디바이스 프로그래밍

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6.1 FPGA 디바이스 프로그래밍

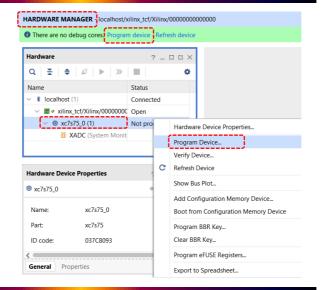
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6.1 FPGA 디바이스 프로그래밍

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- ❖ FPGA 디바이스 선택
- ❖ Program Device 실행



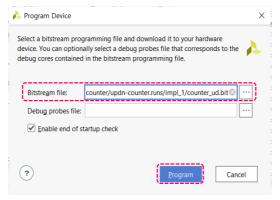
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6.1 FPGA 디바이스 프로그래밍

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- ❖ Bitstream 파일 선택
- ❖ Program Device 실행

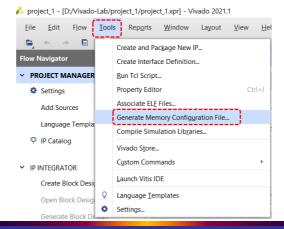


❖ FPGA 실습장비의 clock 주파수를 1 Hz 또는 10 Hz로 맞추고 동작을 확인한다.

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- ❖ 실습 키트에 장착된 configuration ROM 이용
 - > s25FL128s (128 Mb) SPI Flash Memory (Spansion)
- ❖ 비트 스트림 파일을 configuration ROM에 저장할 수 있는 .mcs 파일로 변환

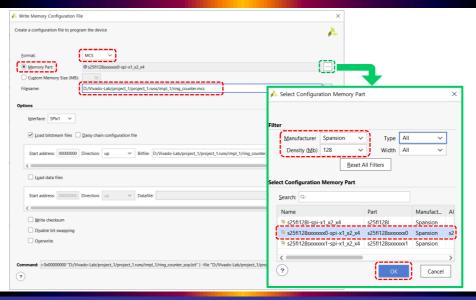


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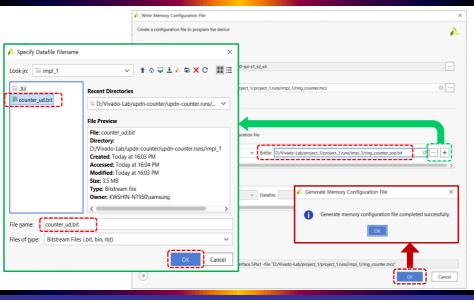
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6.2 Flash Memory 프로그래밍

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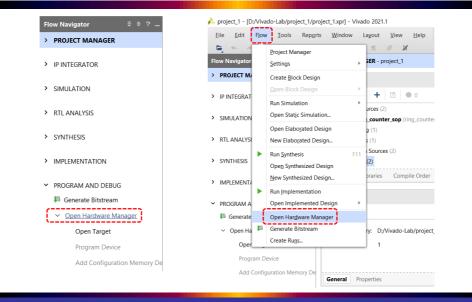
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Xilinx Vivado 설계 실습

6.2 Flash Memory 프로그래밍

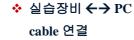
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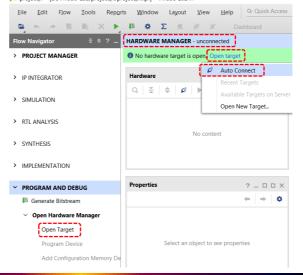


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project_1 - [D:/Vivado-Lab/project_1/project_1.xpr] - Vivado 2021.1



- ❖ 실습장비 전원 ON
- Open target
- ***** Auto Connect



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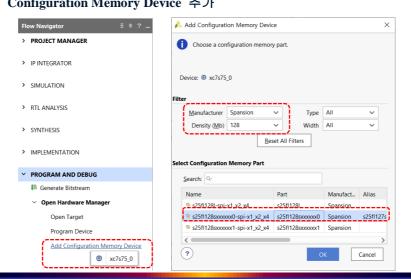
Xilinx Vivado 설계 실습

6.2 Flash Memory 프로그래밍

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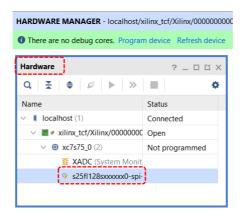




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❖ Configuration Memory Device 추가



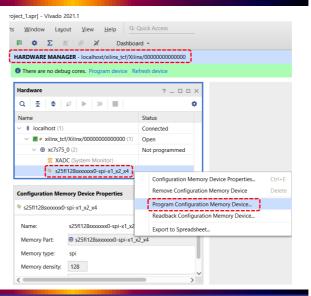
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6.2 Flash Memory 프로그래밍

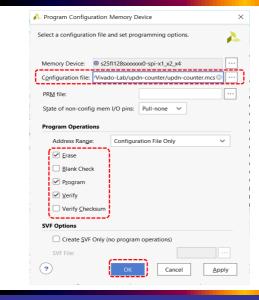
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- ❖ Flash 메모리 선택
- ❖ Program Configuration Memory 실행



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- 1 FPGA 보드의 Reconfig스위치 click
- ② Flash 메모리 → FPGA 프로그래밍 정보 로딩
- ③ FPGA 실습장비 동작 확인

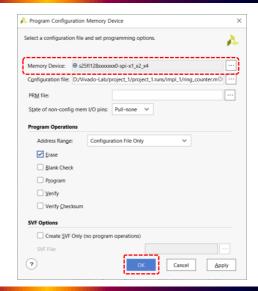
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Xilinx Vivado 설계 실습

6.2 Flash Memory 프로그래밍

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❖ Flash 메모리 정보 지우기



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