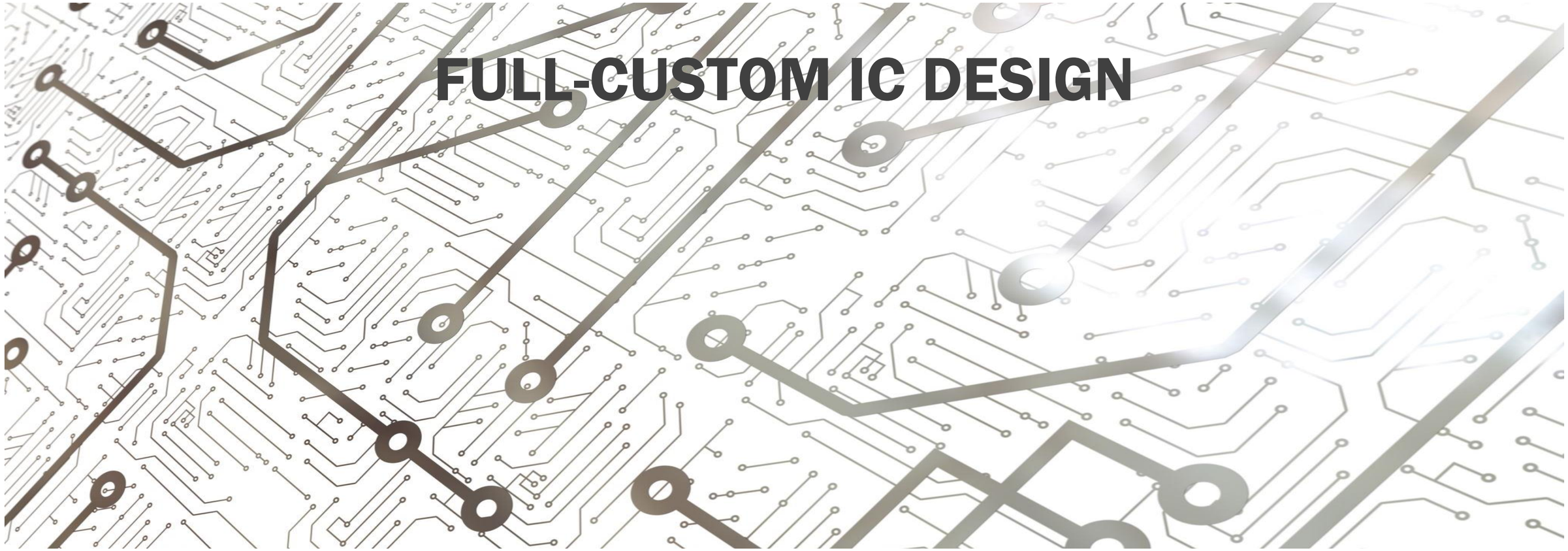
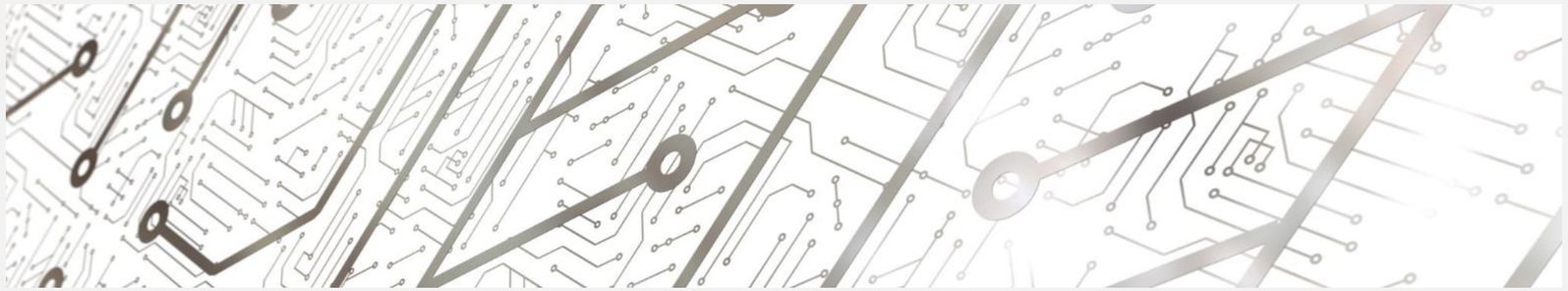


FULL-CUSTOM IC DESIGN

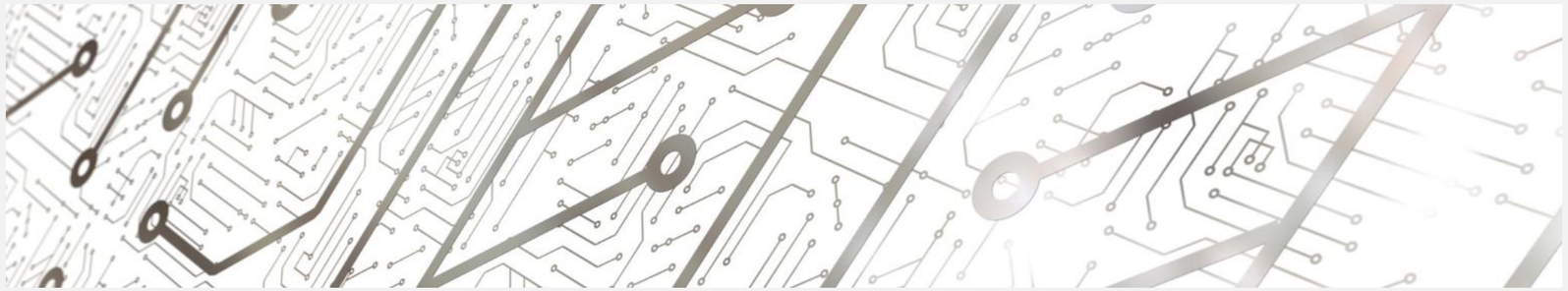
CADENCE VIRTUOSO

PH. D. BYOUNGJIN LEE



4Bit Adder & Subtractor

Tools



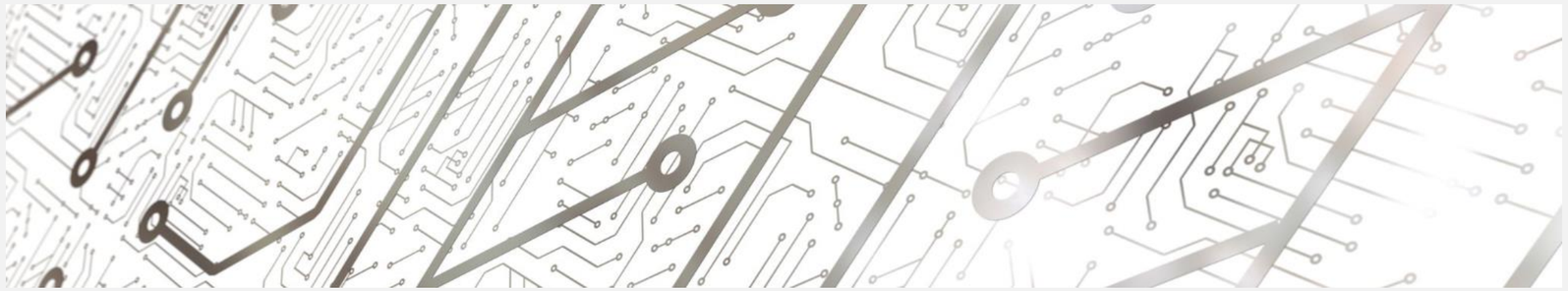
Cadence Virtuoso Schematic Editor / Layout Editor

Cadence Virtuoso Spectre / ADE

Assura DRC / LVS

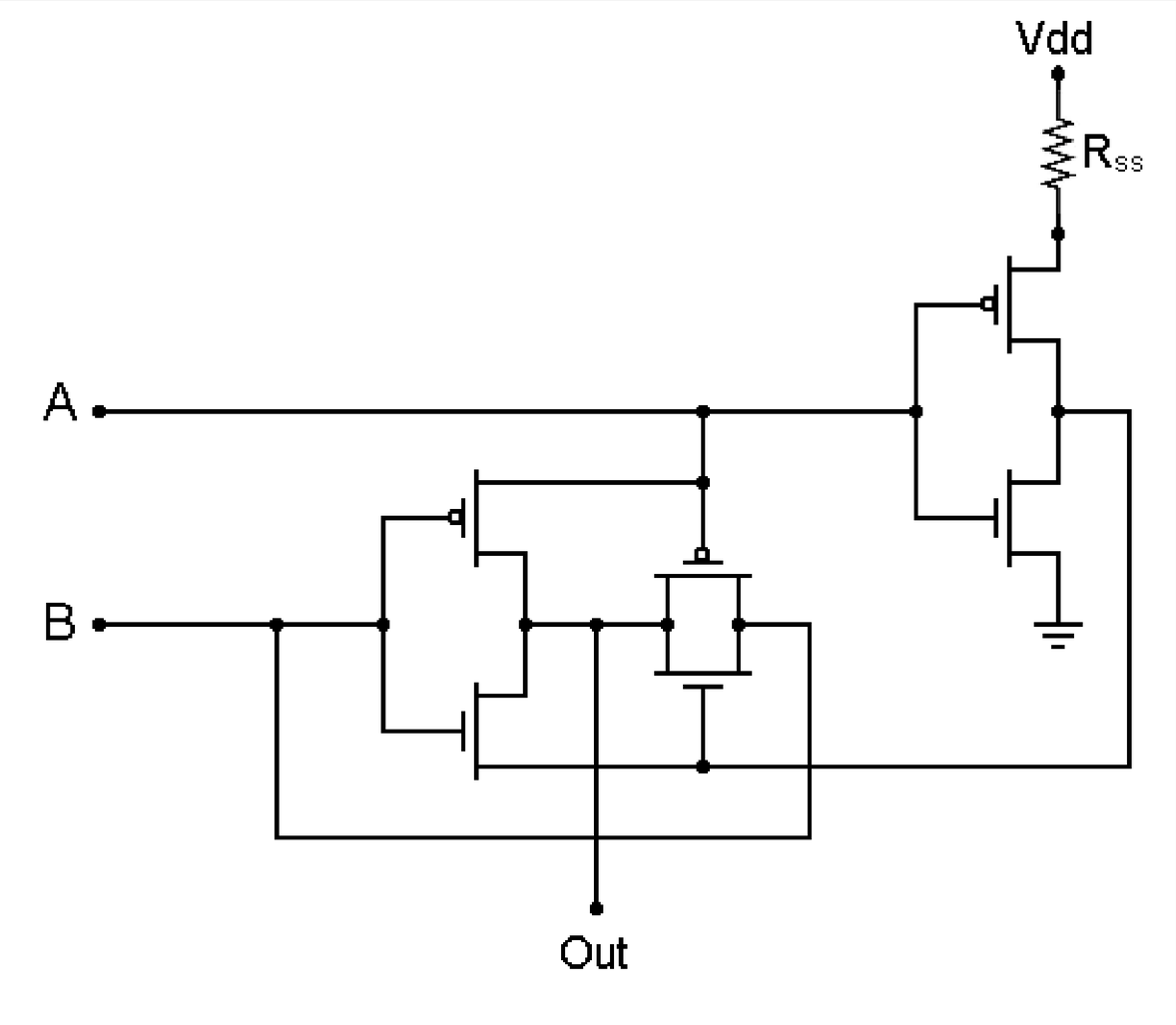
GPDK090

01.

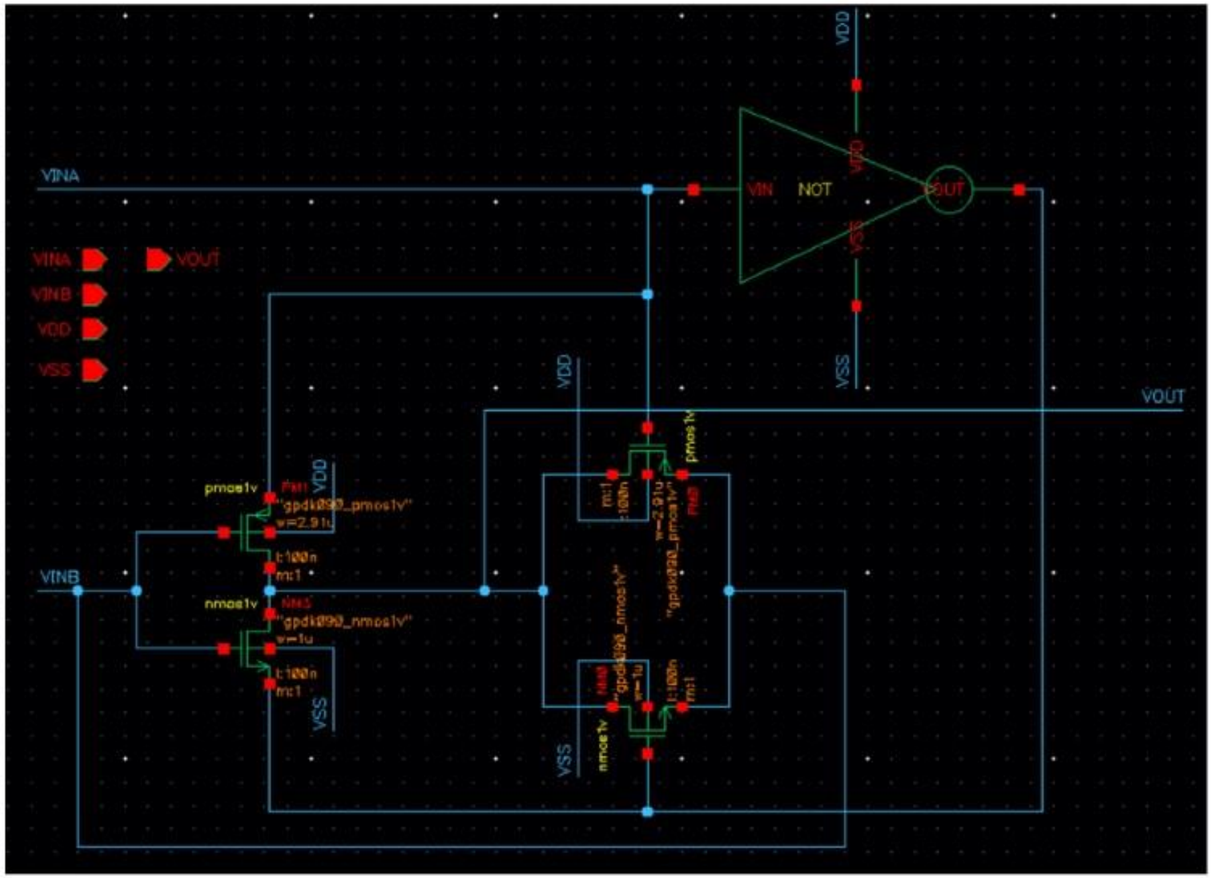


XOR Gate

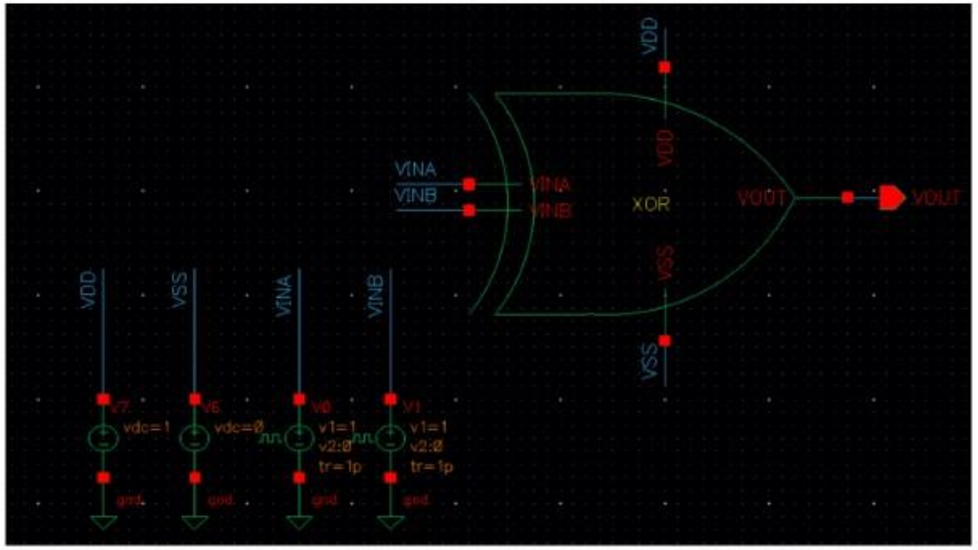
XOR CMOS Schematic



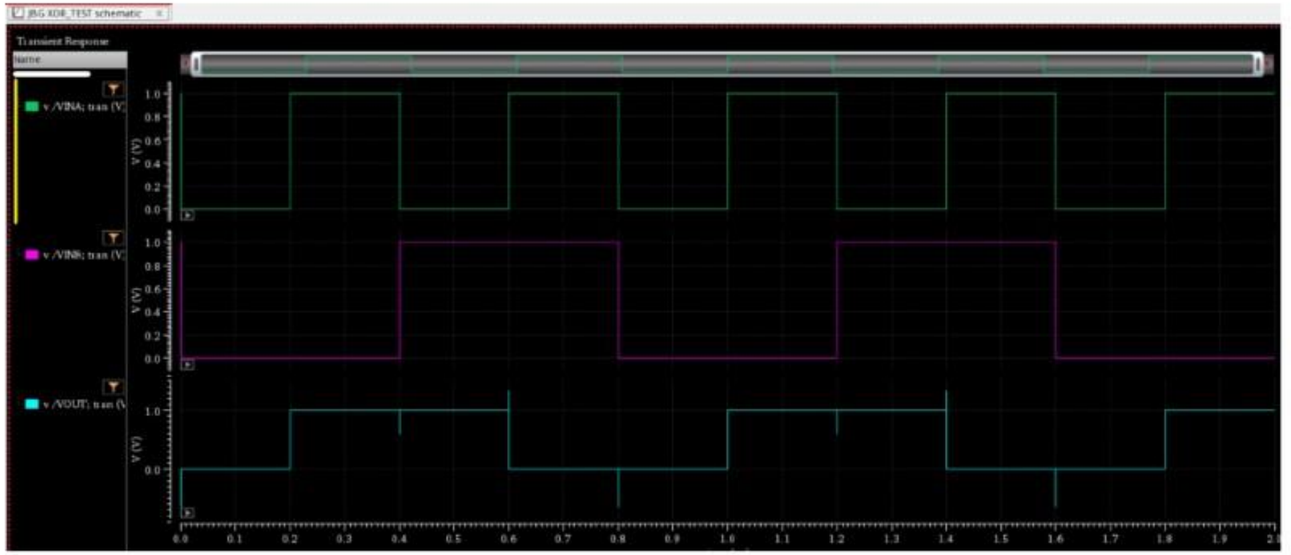
XOR - schematic



XOR - simulation setting, wave form

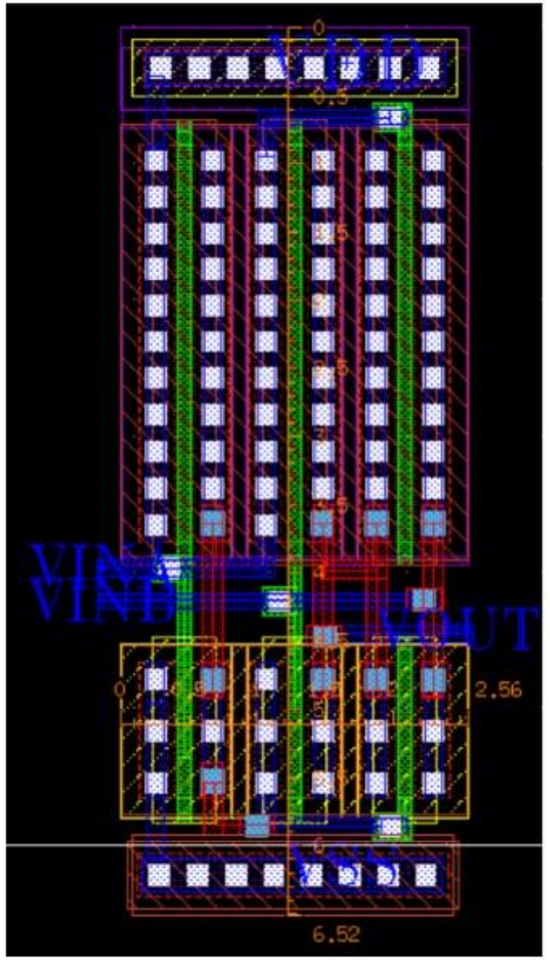


Simulation setting



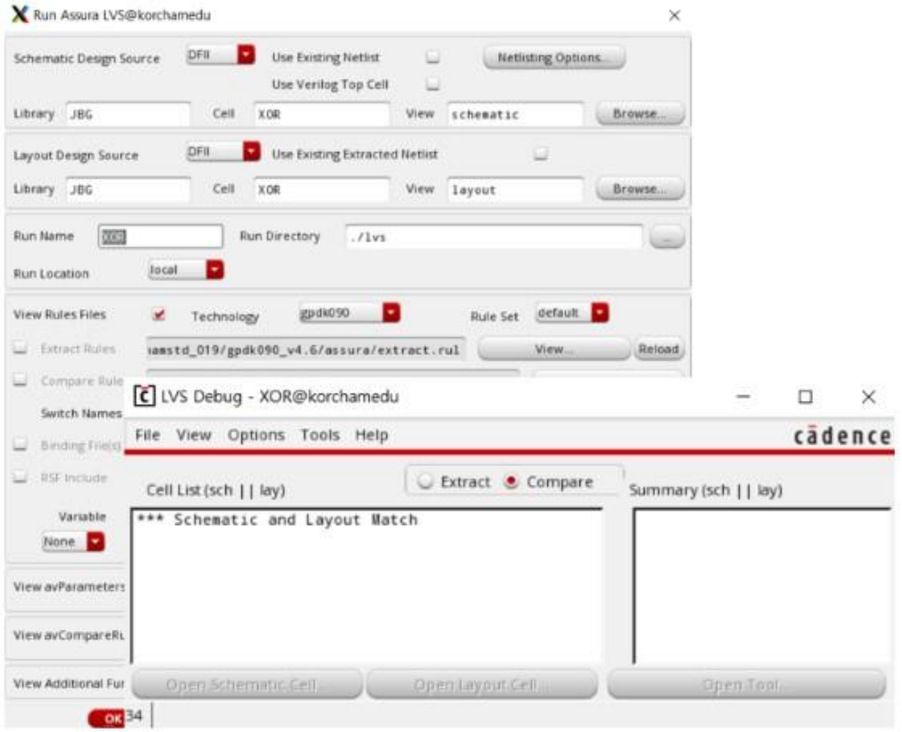
Wave form

XOR - Layout



Width : 6.52um
Length : 2.56um

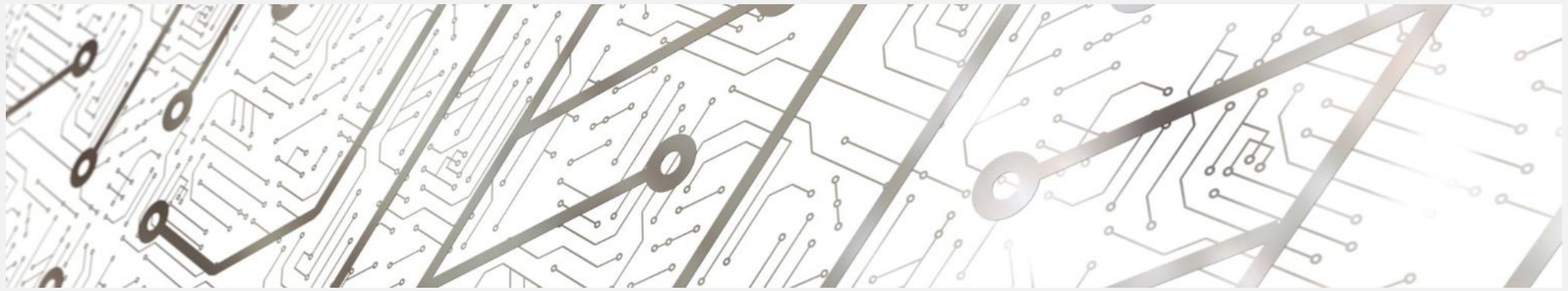
XOR - Layout LVS/DRC



LVS

DRC

02.



4BIT ADDER

4Bit Adder

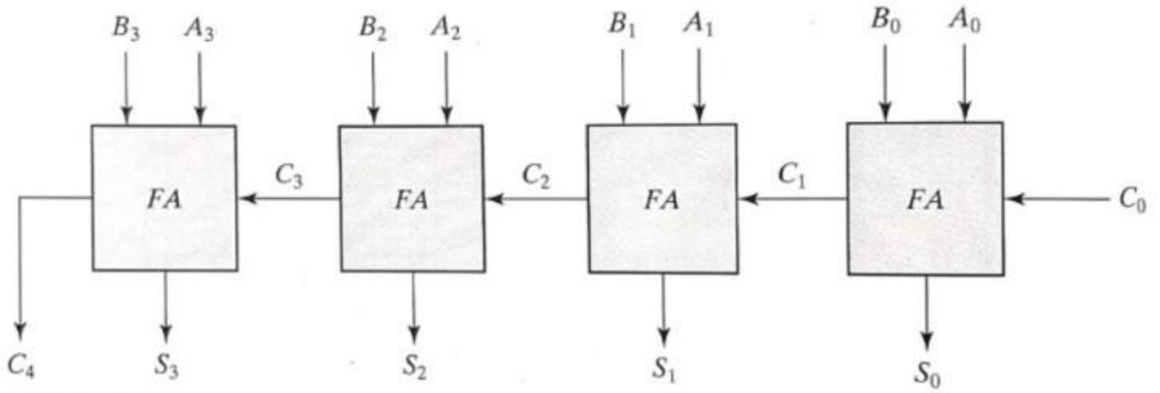


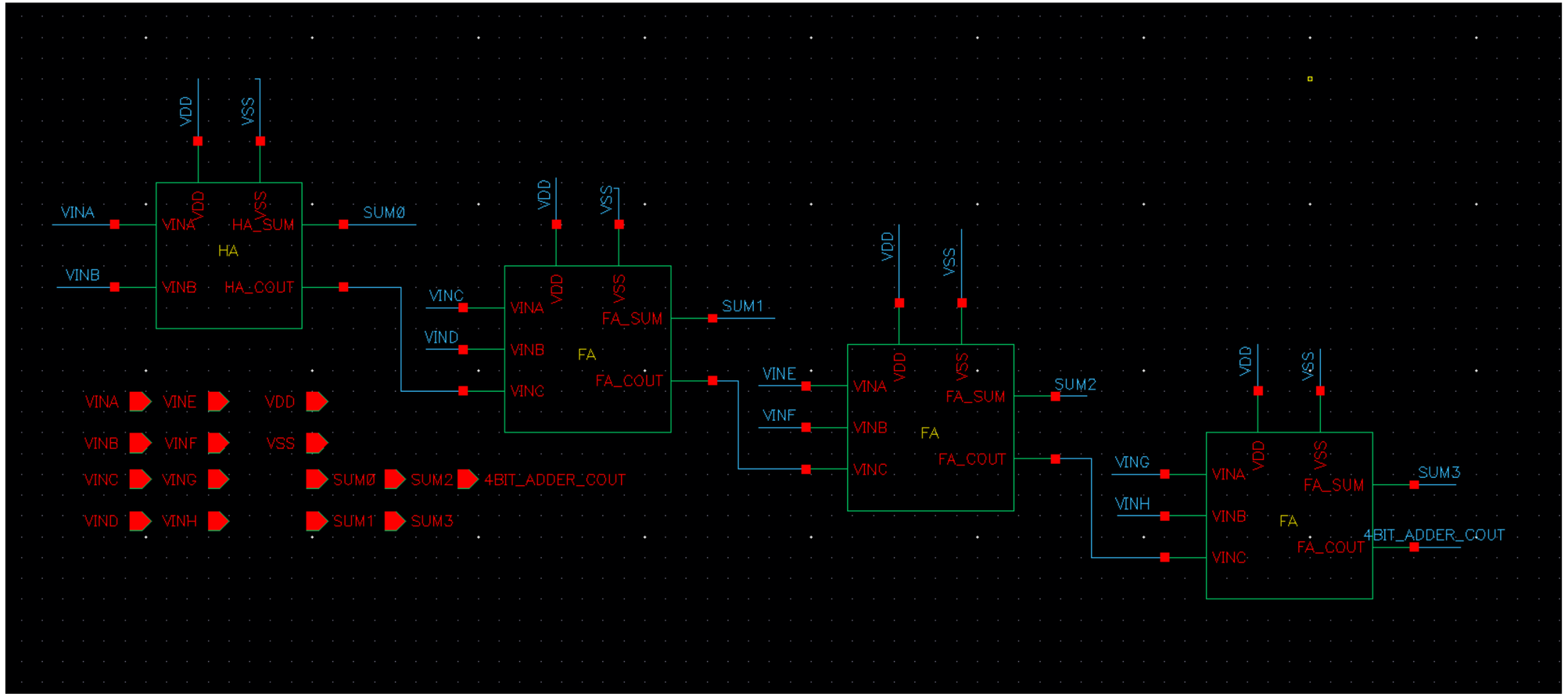
FIGURE 4.9
Four-bit adder

Input A와 Input B를 Full Adder로 계산한다

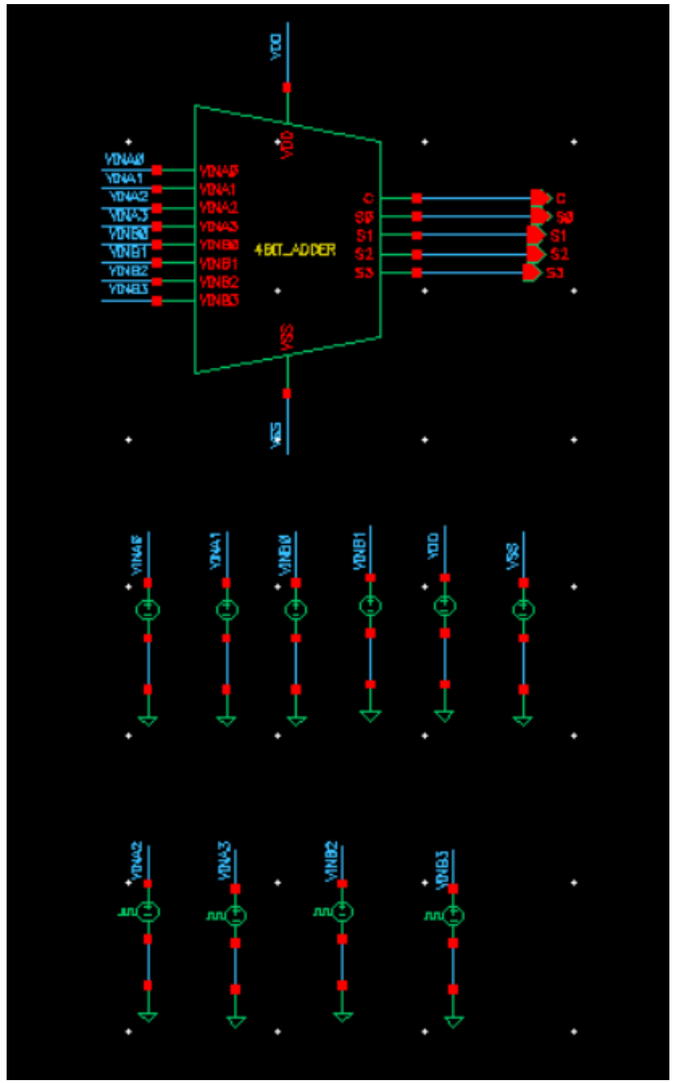
(첫 C in은 0으로 설정 해주기 때문에 첫 Full Adder는 Half Adder로 대체 가능하다)

Full Adder의 C out값은 다음 Full Adder의 C in으로 넘겨주고, S(sum) 값은 출력해준다

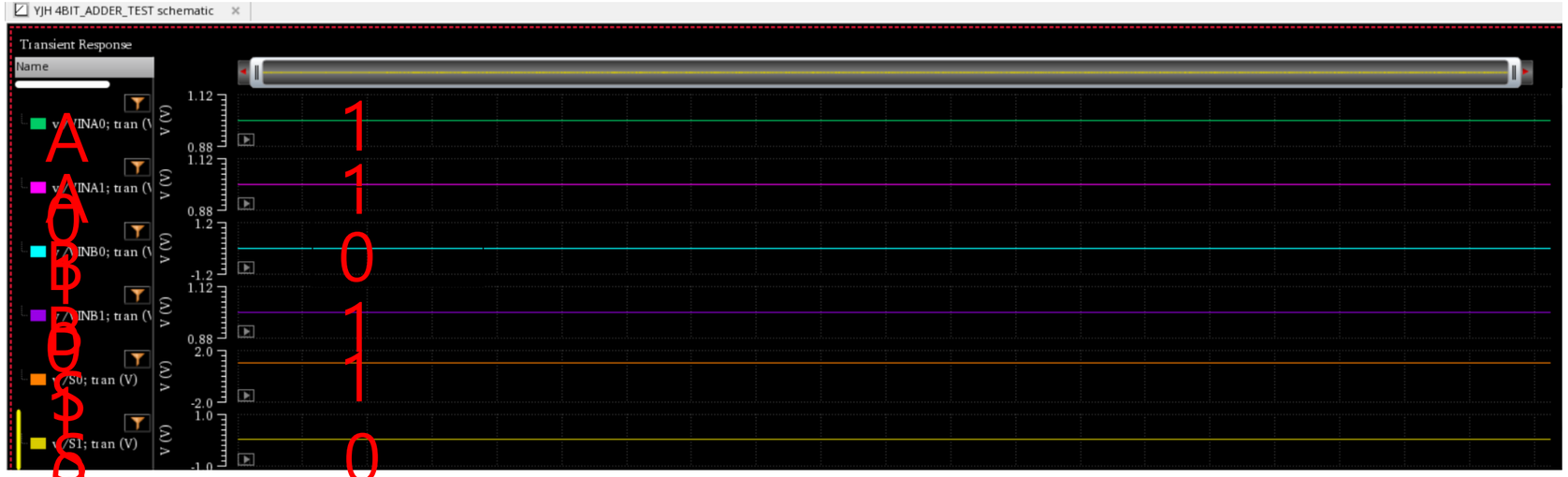
Schematic


VDD
VSS
VINA
VINB
HA
HA_SUM
HA_COUT
SUM0
VINC
VIND
FA
FA_SUM
FA_COUT
SUM1
VINE
VINF
SUM2
VING
VINH
SUM3
4BIT_ADDER_COUT

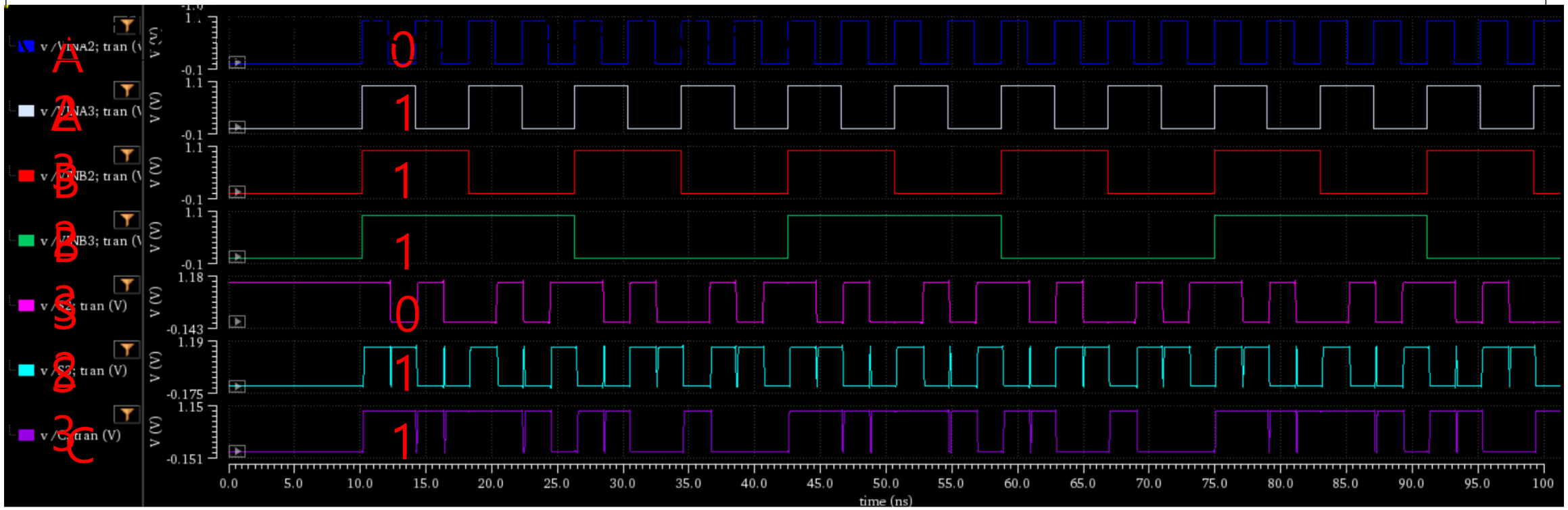
4Bit Adder simulation setup



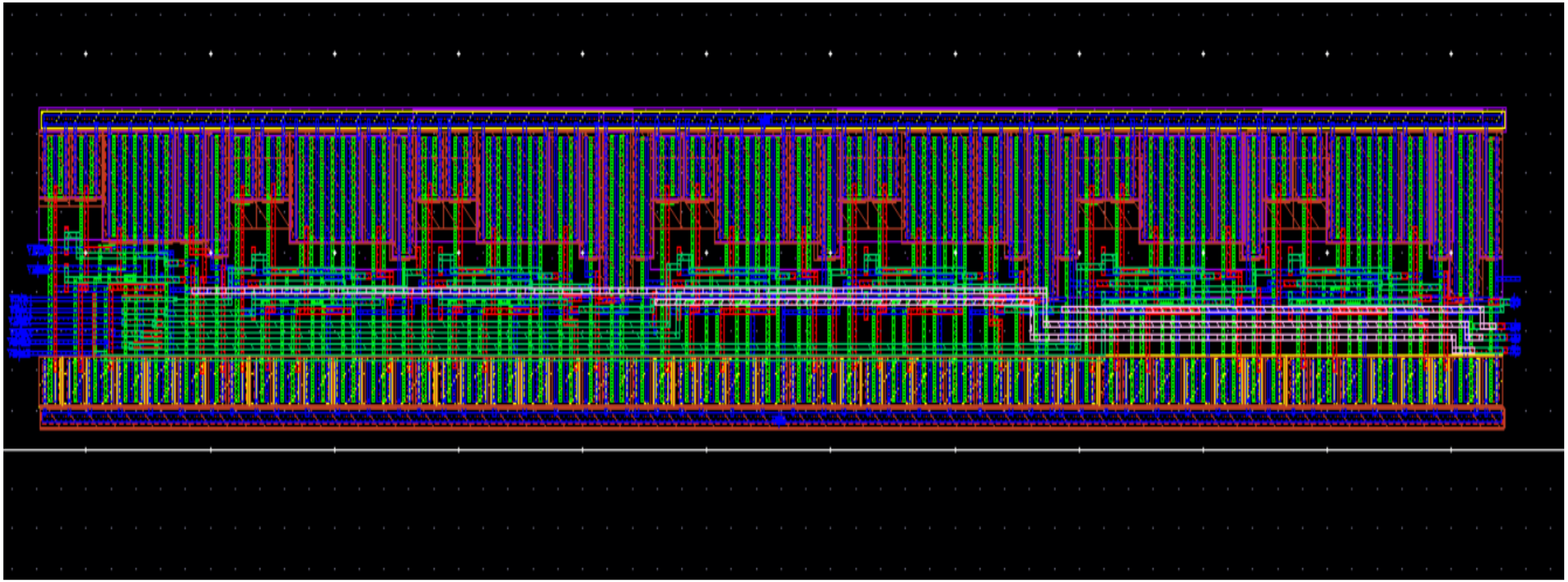
Wave Form



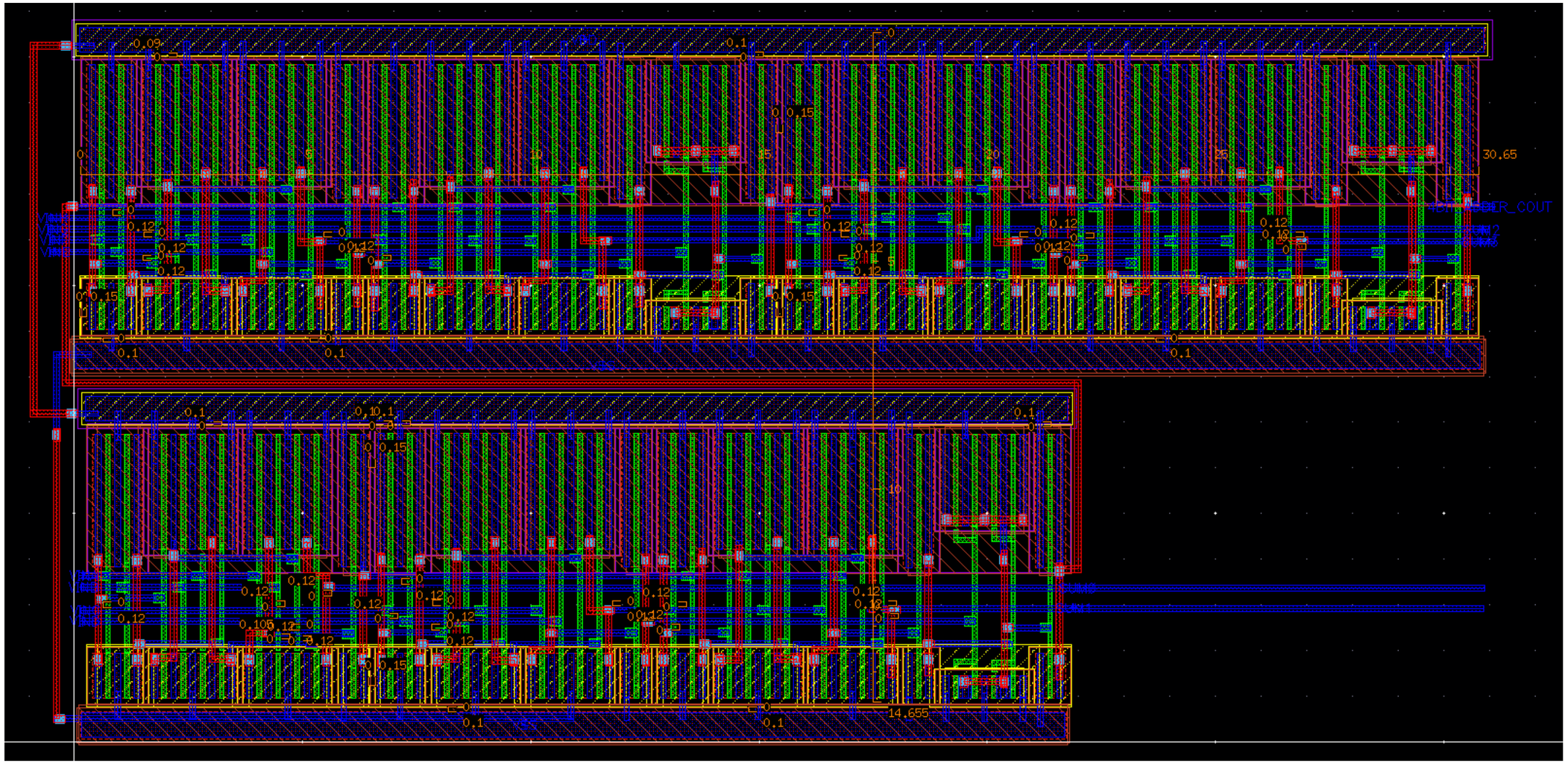
A0+B0 -> S0=1 A1+B1 -> S1 = 0 (C1=1) A2+B2+(C1) -> S2=0



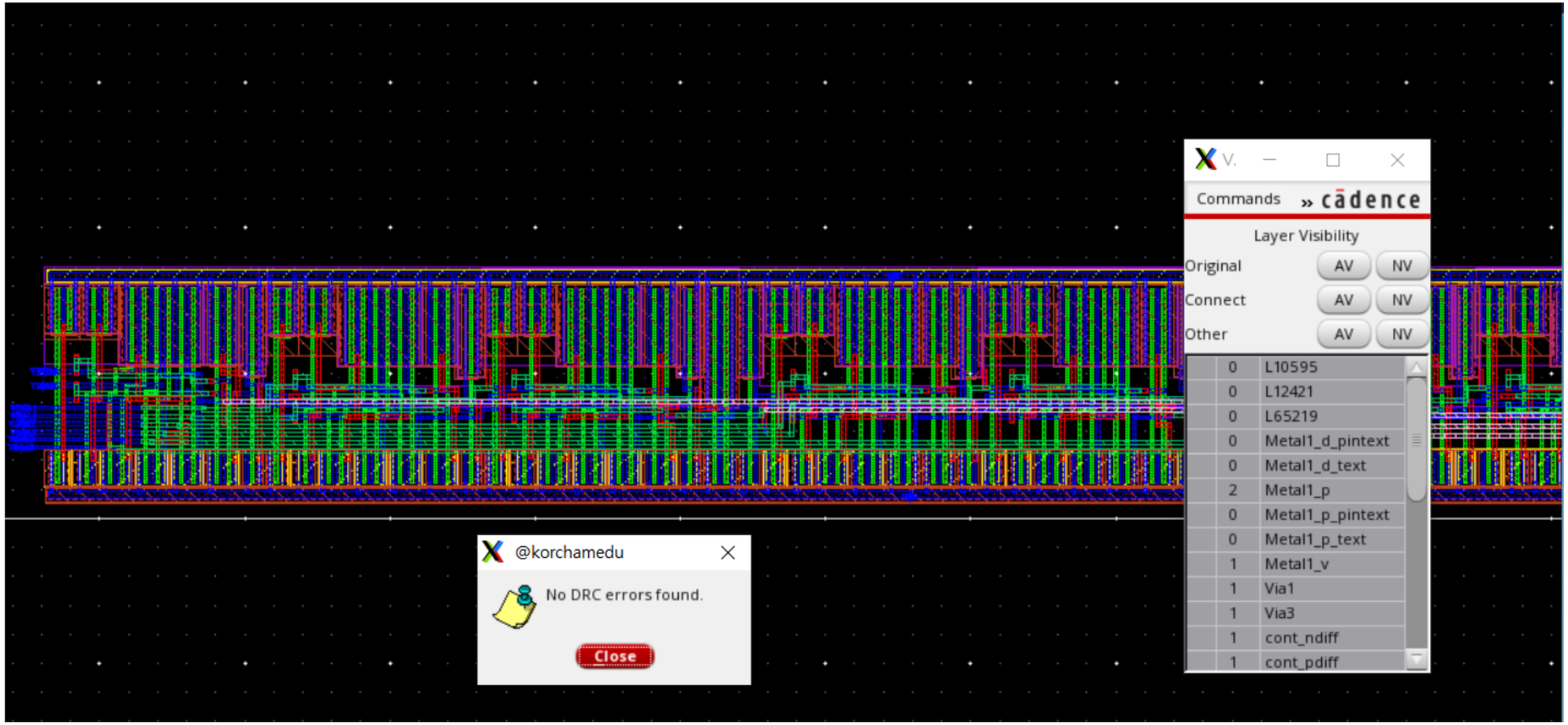
4Bit Adder (Layout)



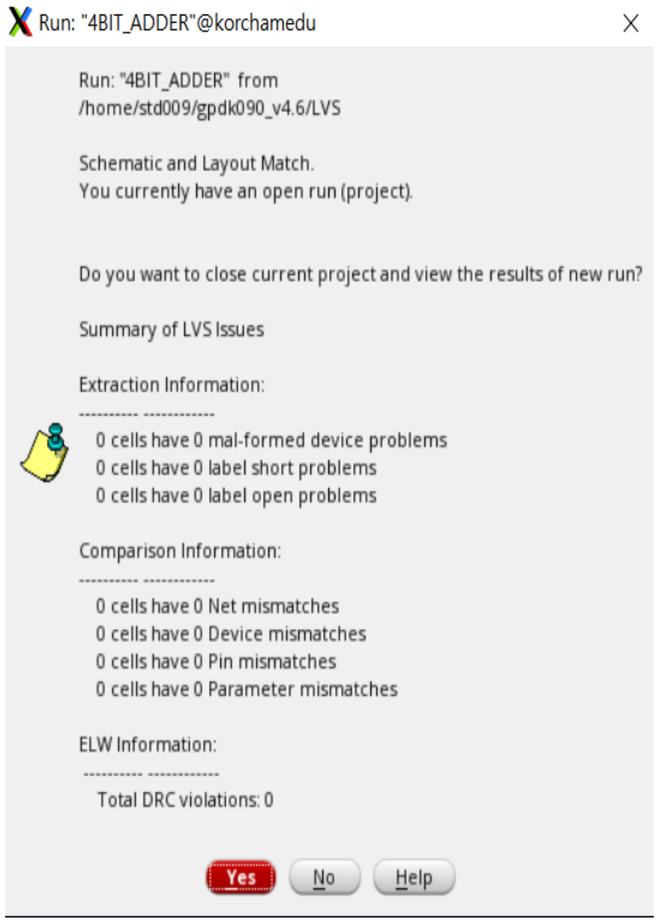
4Bit Adder (Layout)

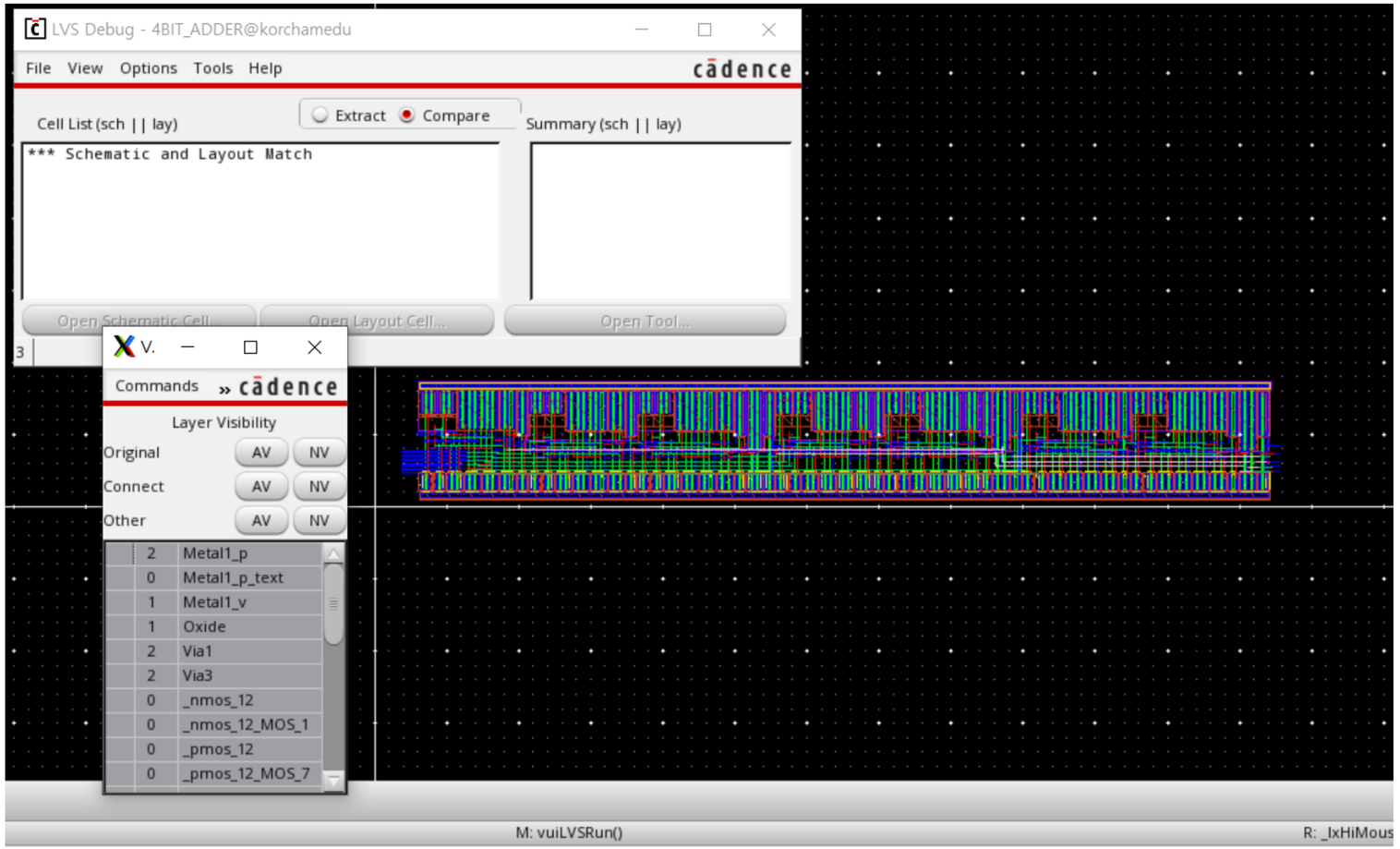


4Bit Adder (DRC)

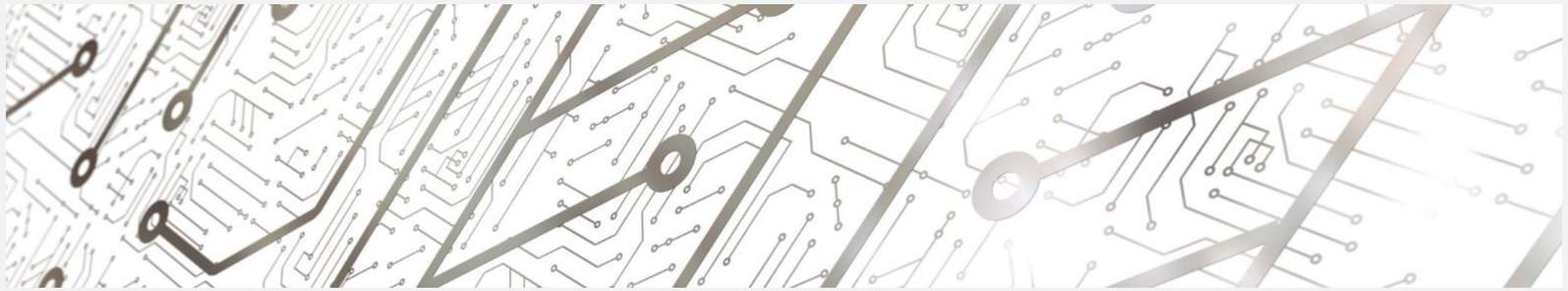


4Bit Adder (LVS)





03.



4BIT ADDER / SUBTRACROR

4Bit Adder/Subtractor

1. 4비트 가감산기의 뺄셈은 뺄셈이 아닌, Input 하나를 음수 형태로 바꾼 후 덧셈을 하는 방식이다.

2. 2의 보수를 취함으로써 음수로 바꿀 수 있다(다음 페이지)

3. 각 자릿수를 반전시키는 것은 XOR gate를, 가장 낮은 자리에 1을 더하는 것은 첫 Full Adder의 Cin 값을 1로 설정하는 것을 통해서 구성할 수 있다.

2의 보수

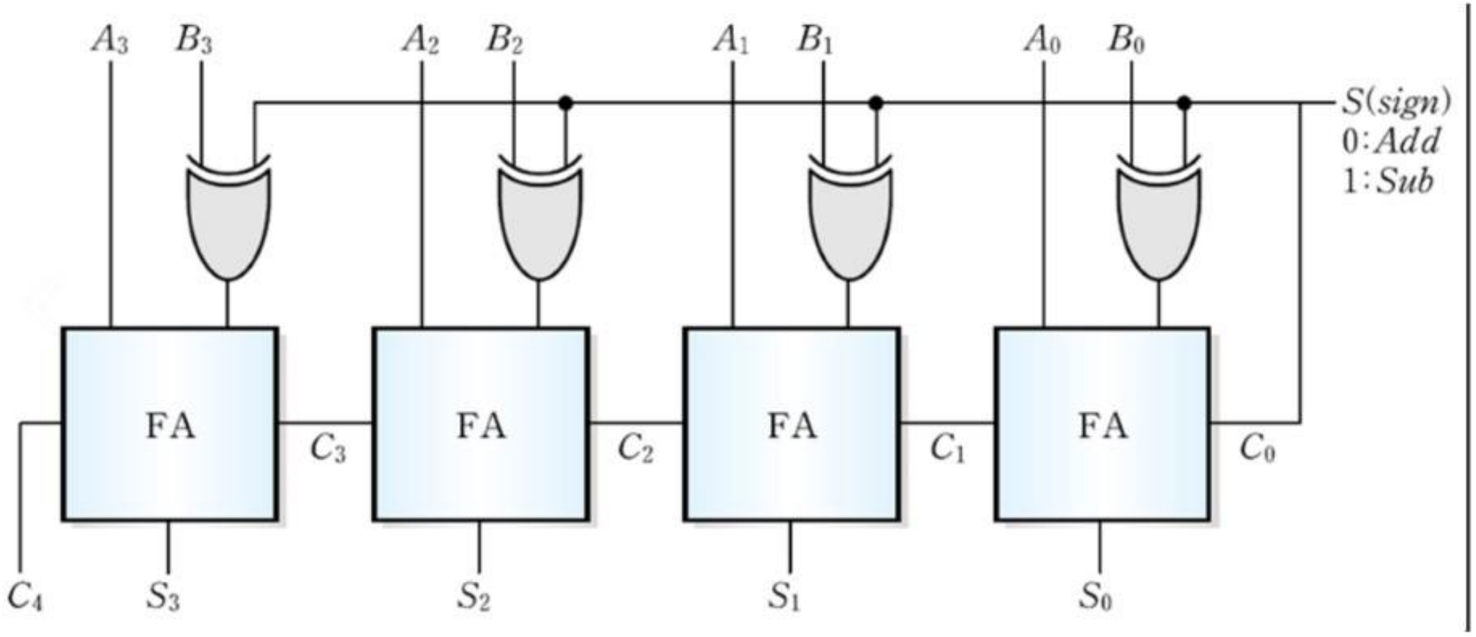
각 자릿수를 반전 시킨 후(1의 보수)

1을 더하면 2의 보수이다

Ex) 1001 -> 반전 -> 0110 (1의 보수)

0110 + 0001 = 0111 (2의 보수)

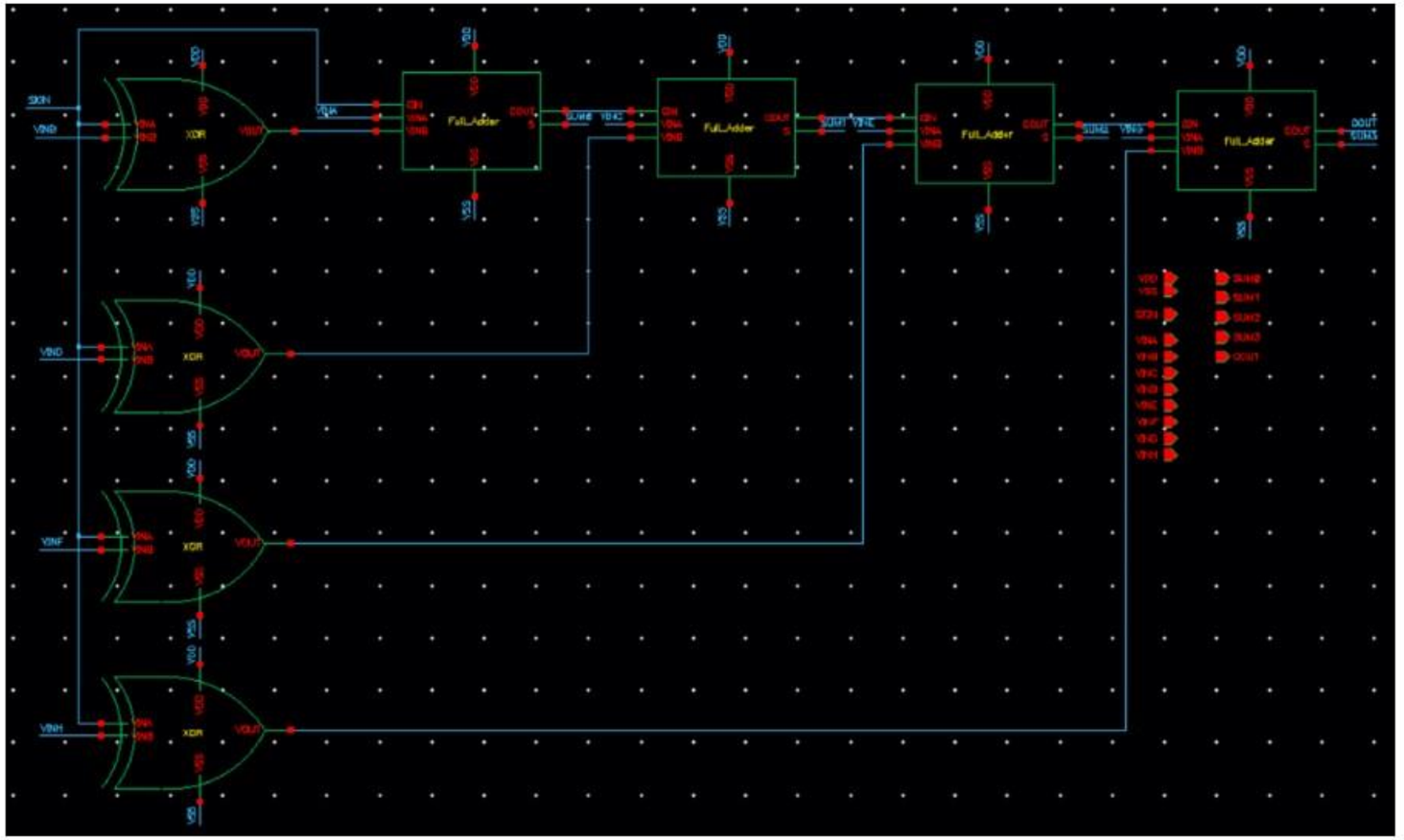
4Bit Adder/Subtractor 구성



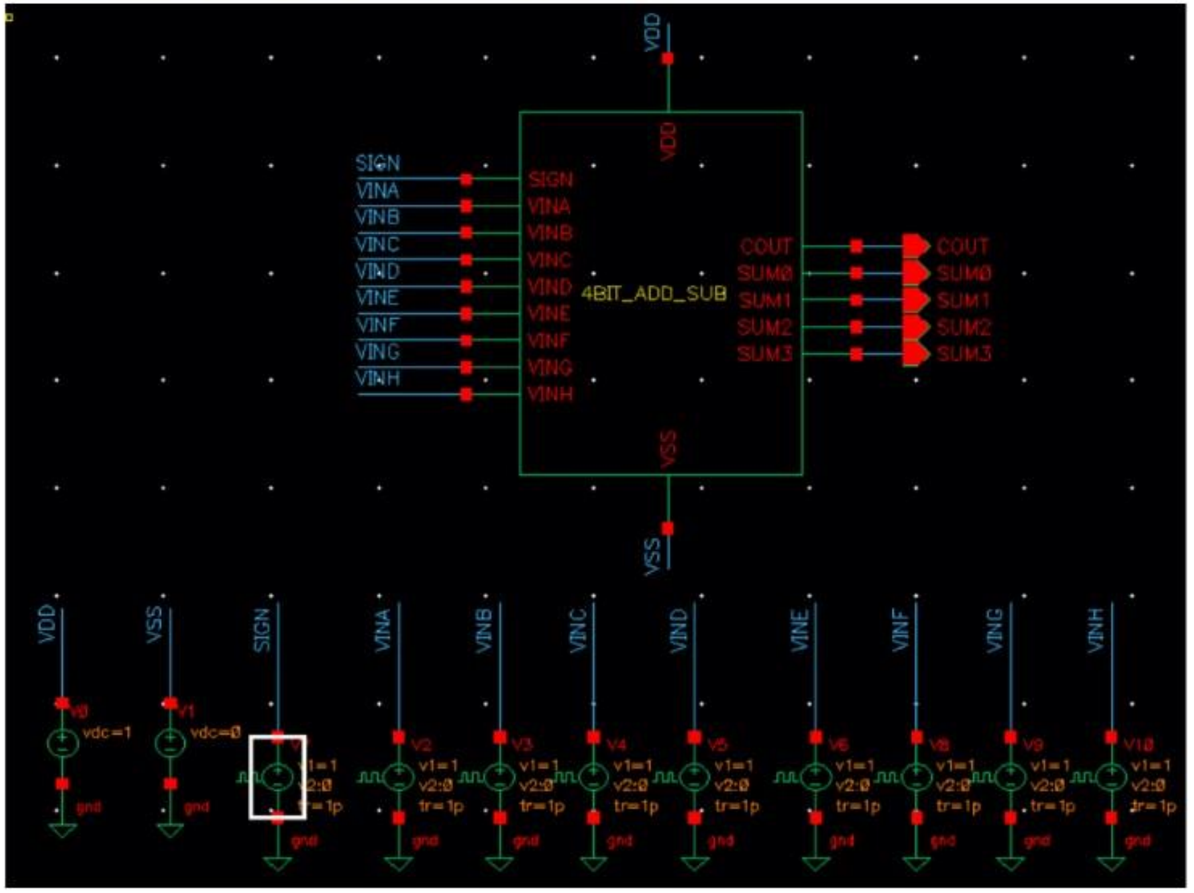
1의 보수 : XOR gate에 입력 신호로 1과 함께 넣으면 출력된다

2의 보수 : 첫번째 Full Adder의 Cin값을 1로 설정한다.

4Bit Adder Subtractor - schematic



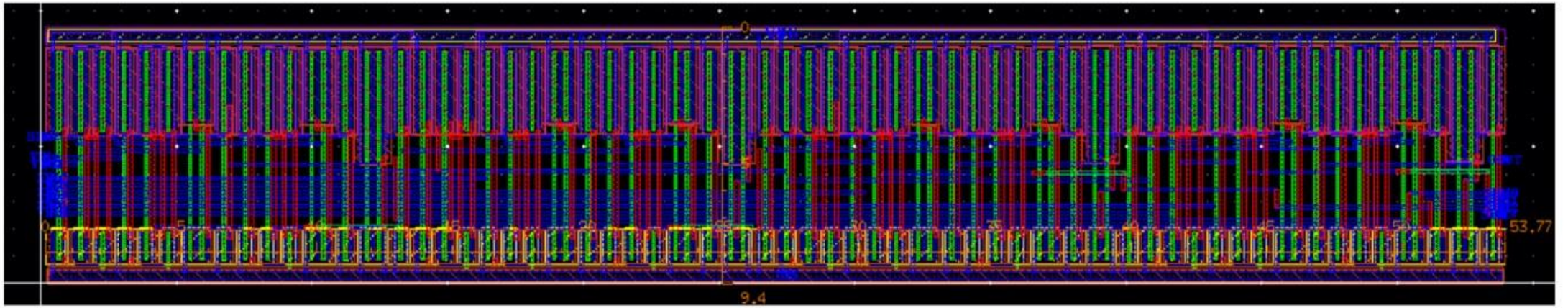
4Bit Adder Subtractor - simulation setting



4Bit Adder-Subtractor - Simulation1

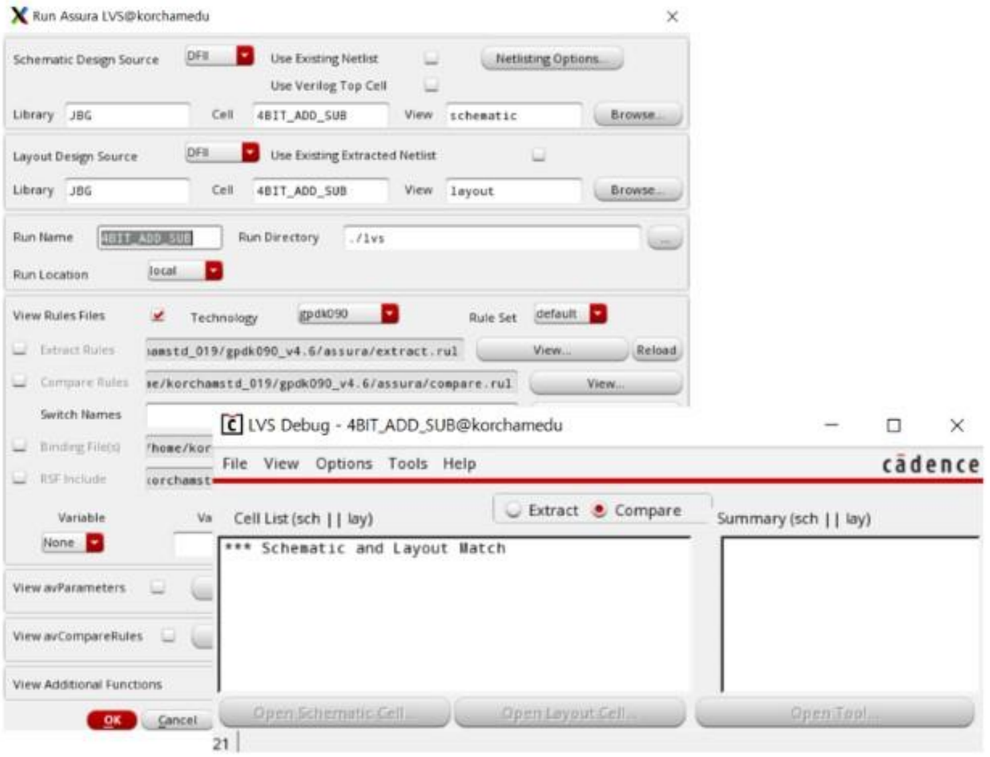
4Bit Adder-Subtractor - Simulation2

4Bit Adder-Subtractor - Layout



Width : 9.4um
Length : 53.77um

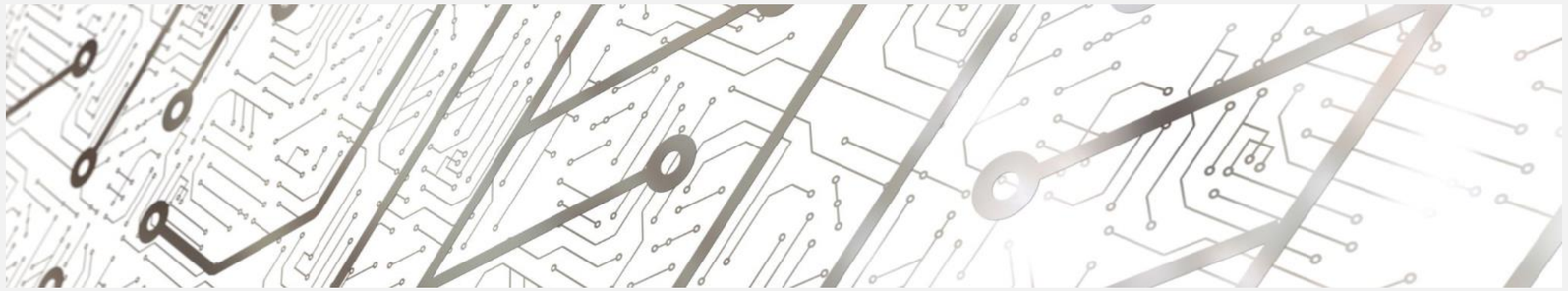
4Bit Adder-Subtractor - Layout LVS/DRC



LVS

DRC

Contact



Email : byoungjin@hanmail.net

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