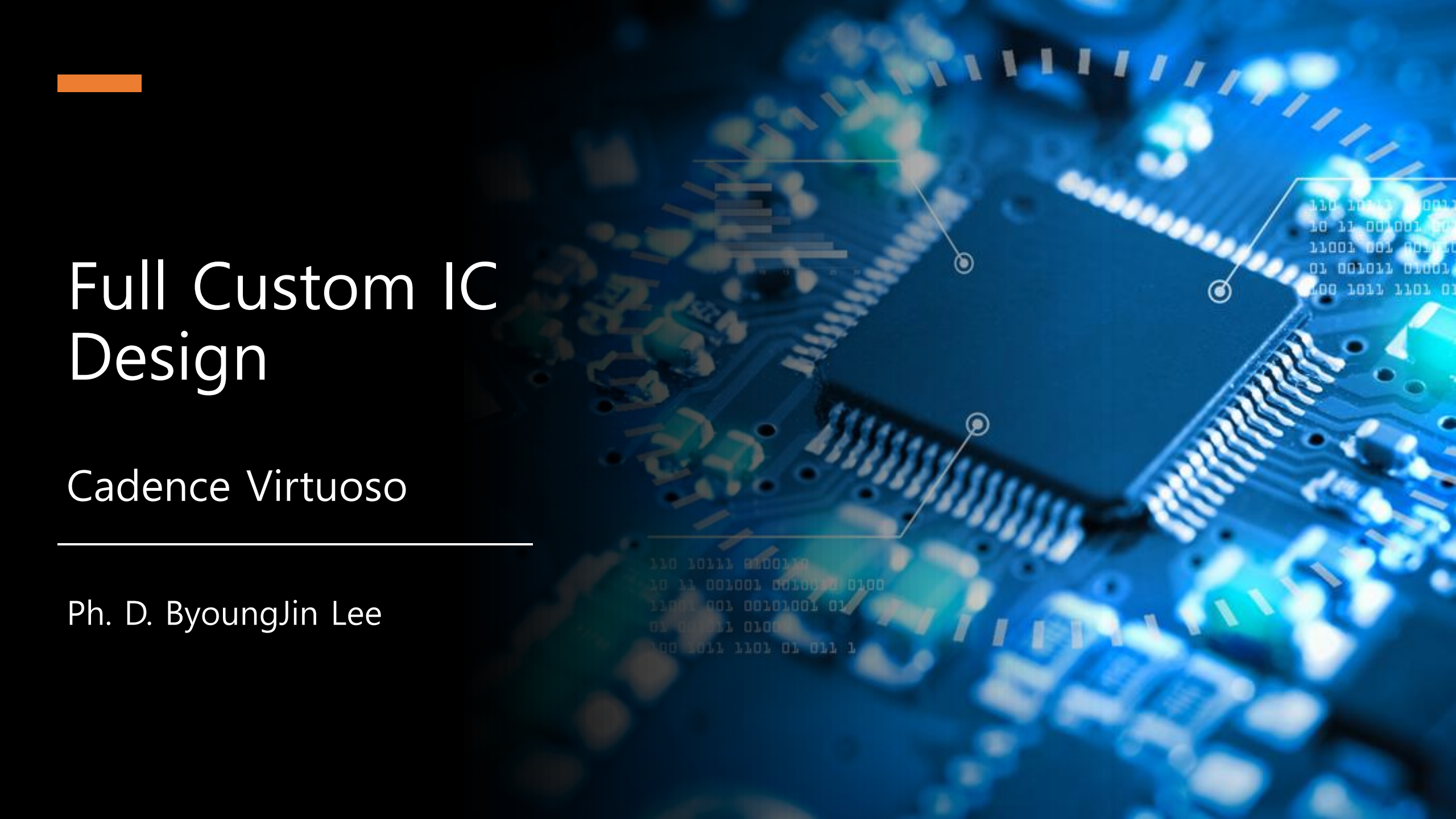
Full Custom IC Design

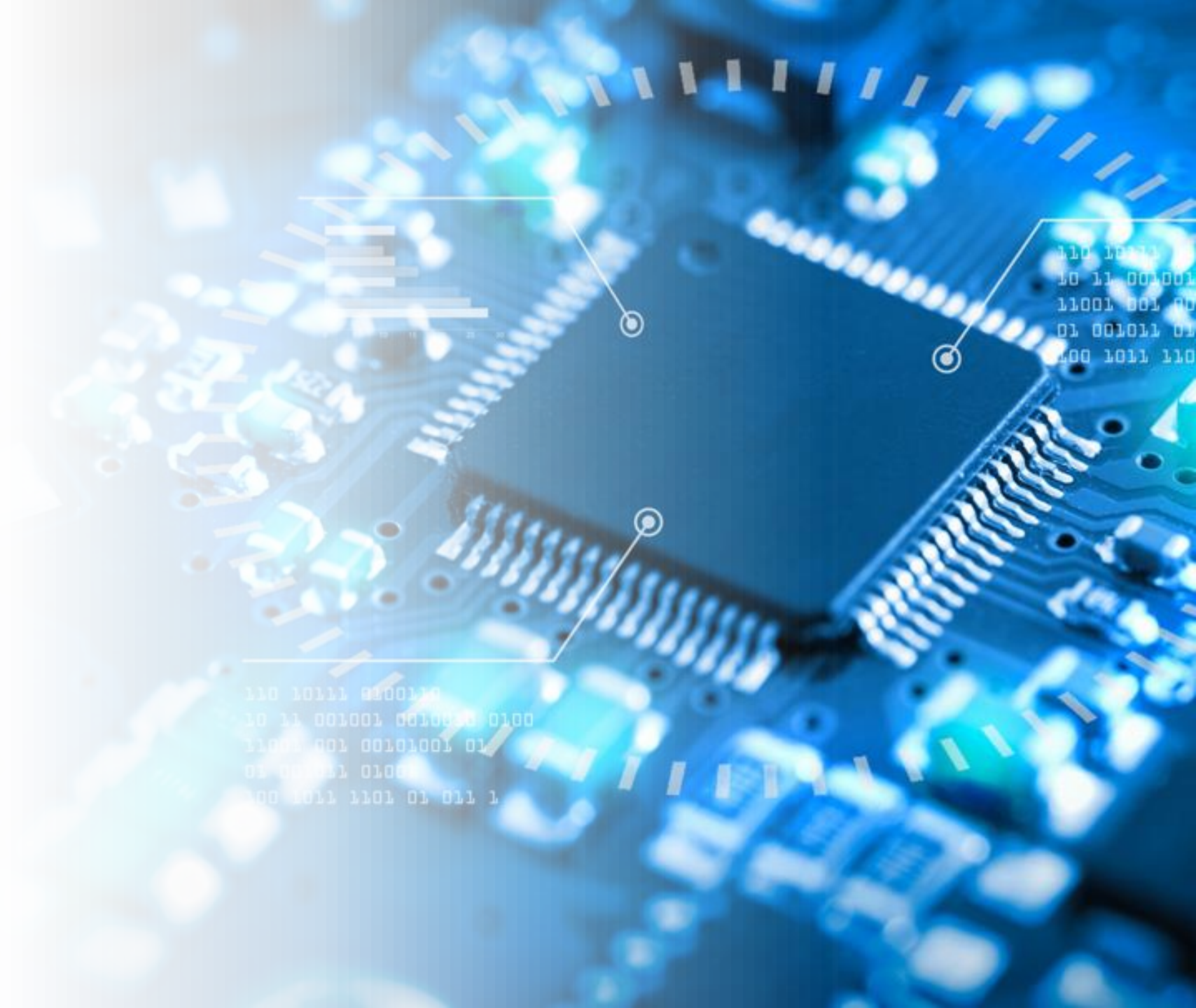
Cadence Virtuoso

Ph. D. ByoungJin Lee



4*1 MUX (MUltipleXer)

VLSI Circuits Design Example



CONTENTS

Tools

Cadence Virtuoso Schematic Editor / Layout Editor

Cadence Virtuoso Spectre / ADE

Assura DRC / LVS

GPDK090

순 서

- 4*1 MUX
- Circuit design(logic gate, Switch)
- Schematic
- Circuit simulation
- Layout
- DRC, LVS

4*1MUX(Multiplexer)

- 복수회로에서 입력되는 4개의 신호 중 어느 하나의 입력신호를 선택하여 출력회로에 내보내주는 논리 회로

$$OUT = \overline{S1}\cdot\overline{S0}\cdot A + \overline{S1}\cdot S0\cdot B + S1\cdot\overline{S0}\cdot C + S1\cdot S0\cdot D$$

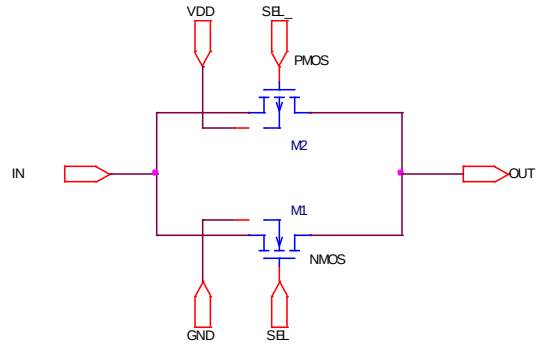
MUX 진리표		
S1	S0	OUT
0	0	A
0	1	B
1	0	C
1	1	D

구현 방법

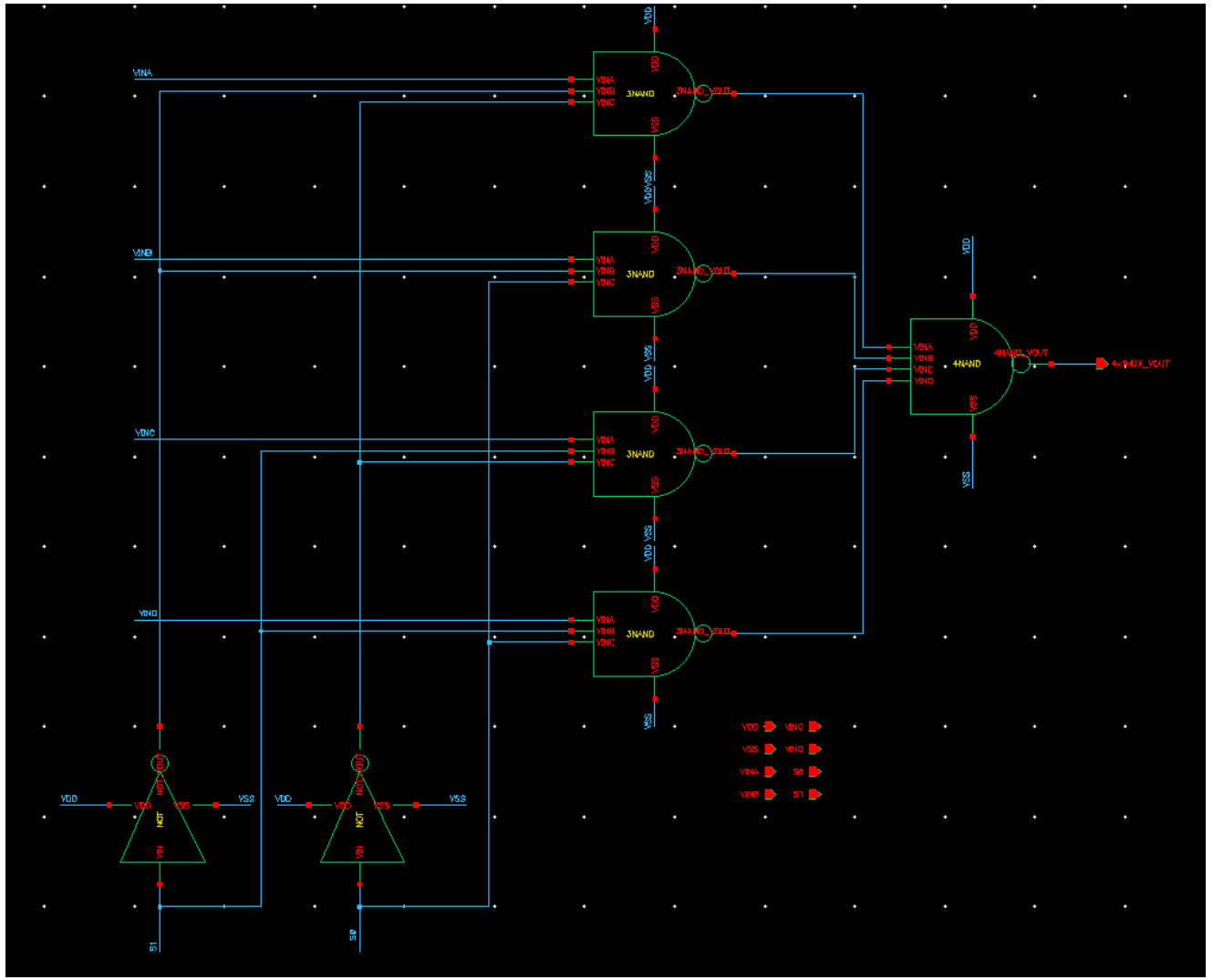
- CMOS Tr.로 스위치를 구현하여 4*1 MUX를 구성하였다.
- Tr.의 수를 줄일 수 있는 장점이 있다.

  - Logic gate
  - (Inverter) (2*2) + (3Nand) 4*6 + (4Nand) 1*8 = 36개

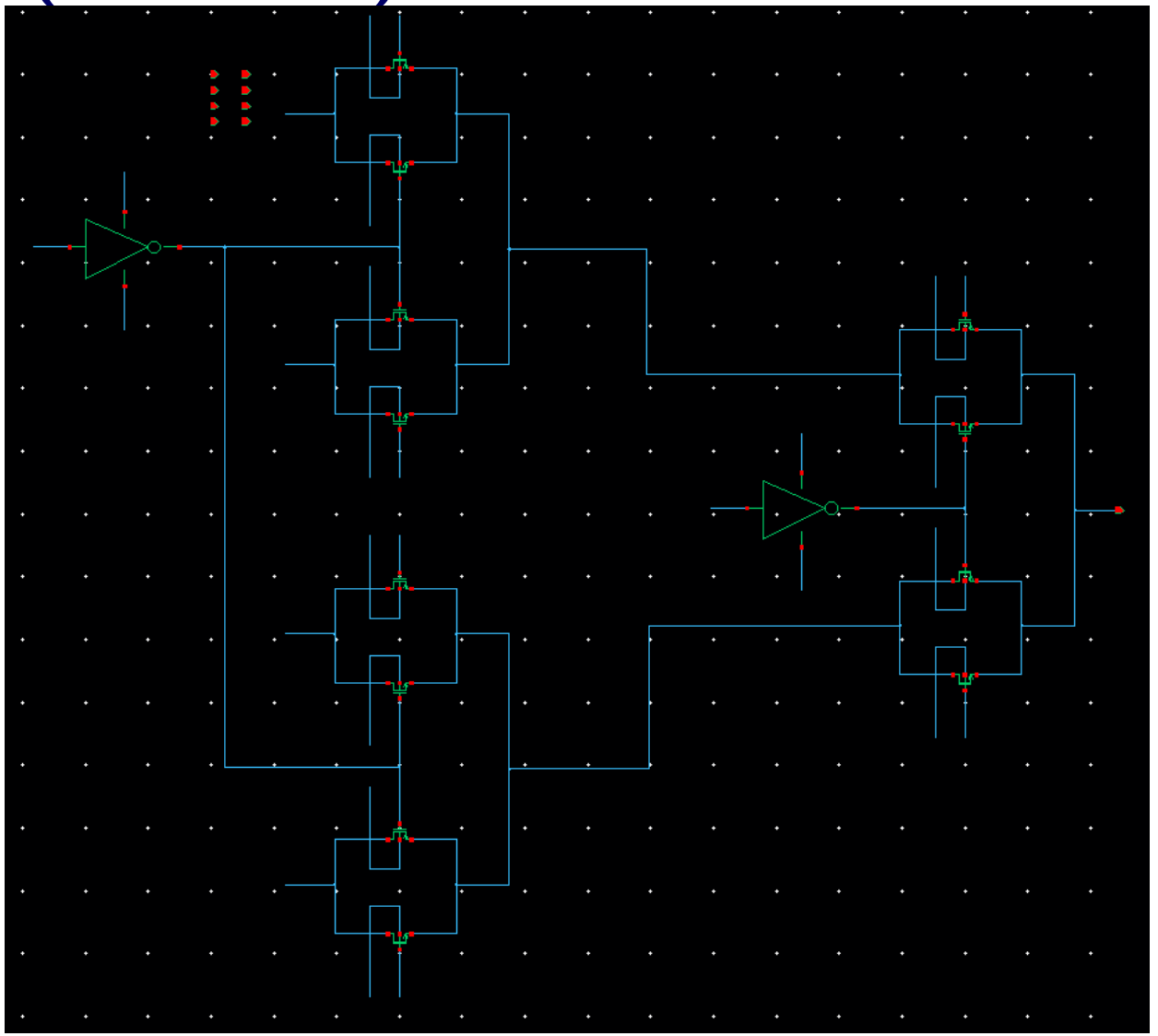
  - CMOS switch
  - (CMOS) 2*6 + (Inverter) 2*2 =16개



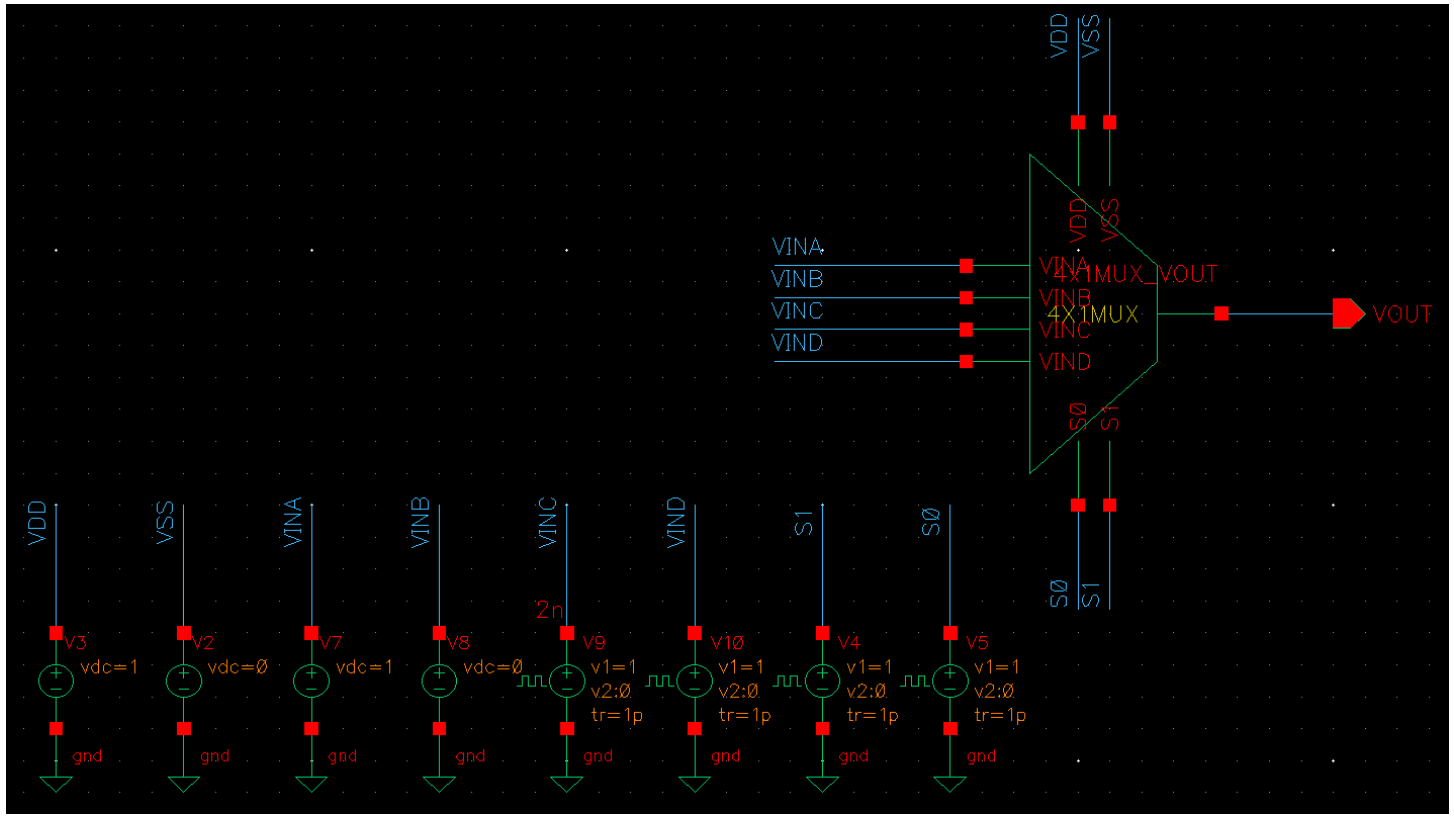
Schematic(Logic gate)



Schematic(Switch)



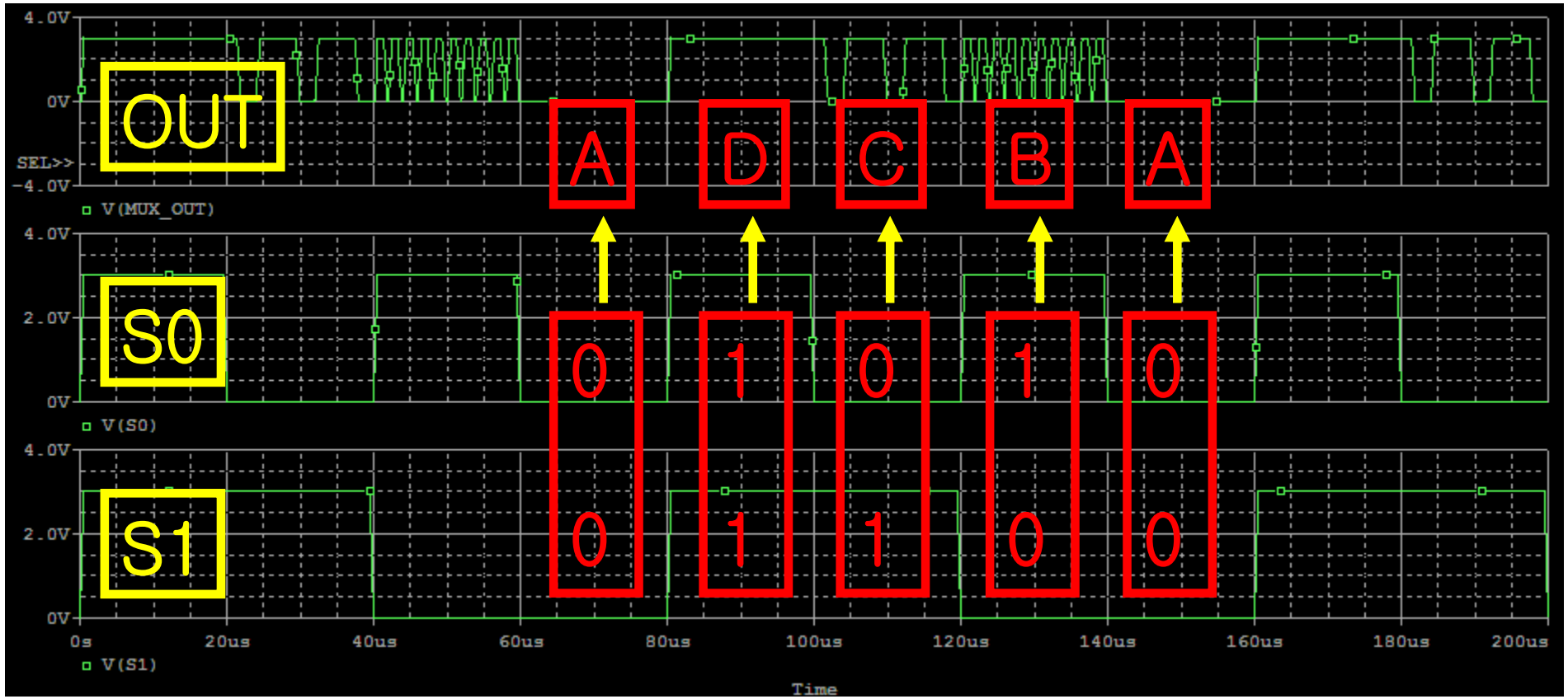
4*1 MUX simulation setup



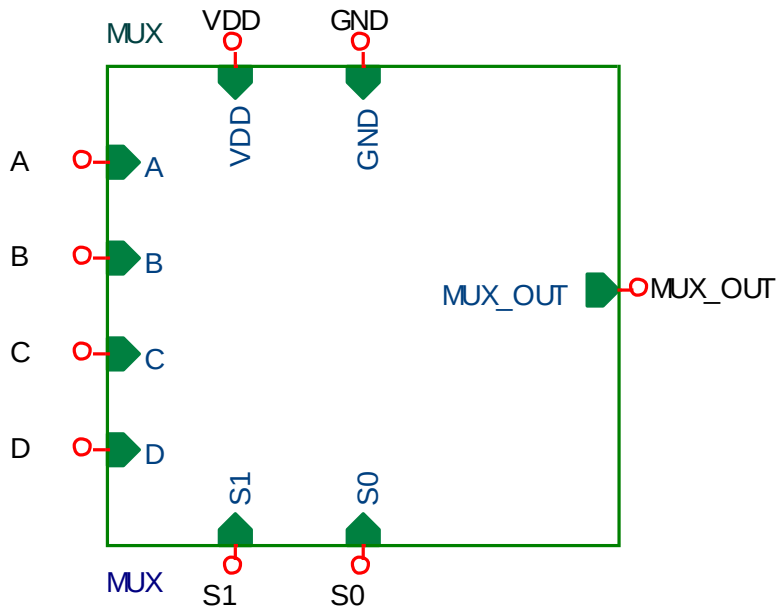
Wave Form


5.0V
2.5V
SEL>>
0V
V(D)
D
4.0V
2.0V
0V
V(C)
C
4.0V
2.0V
0V
V(B)
B
1.0uV
0V
-1.0uV
V(A)
A
0s
20us
40us
60us
80us
100us
120us
140us
160us
180us
200us
Time

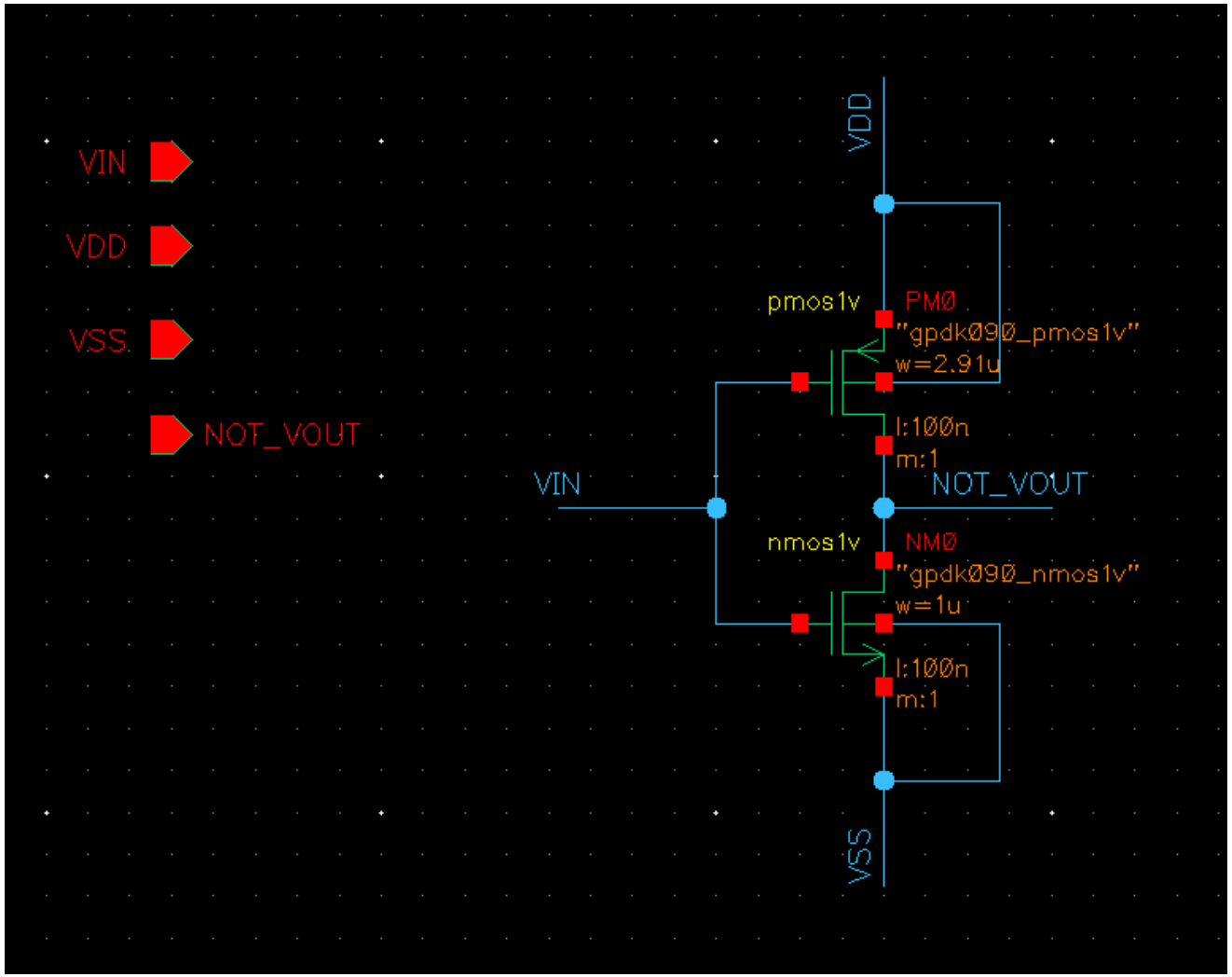
Wave Form


4.0V
0V
SEL>>
-4.0V
V(MUX_OUT)
OUT
A
D
C
B
A
4.0V
2.0V
0V
V(S0)
S0
0
1
0
1
0
4.0V
2.0V
0V
V(S1)
S1
0
1
1
0
0
0s
20us
40us
60us
80us
100us
120us
140us
160us
180us
200us
Time

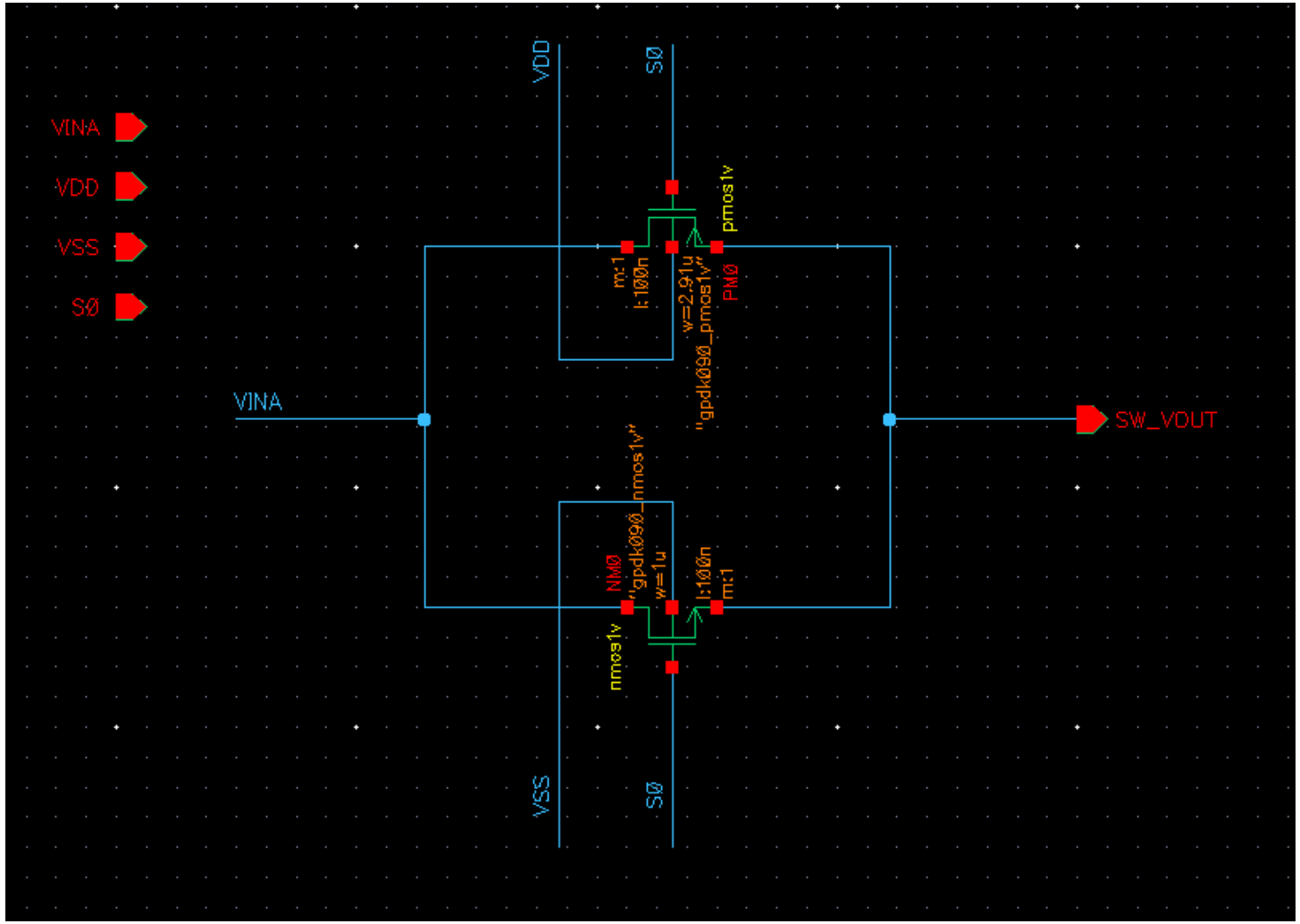
4*1 MUX 블록 외부 PORT



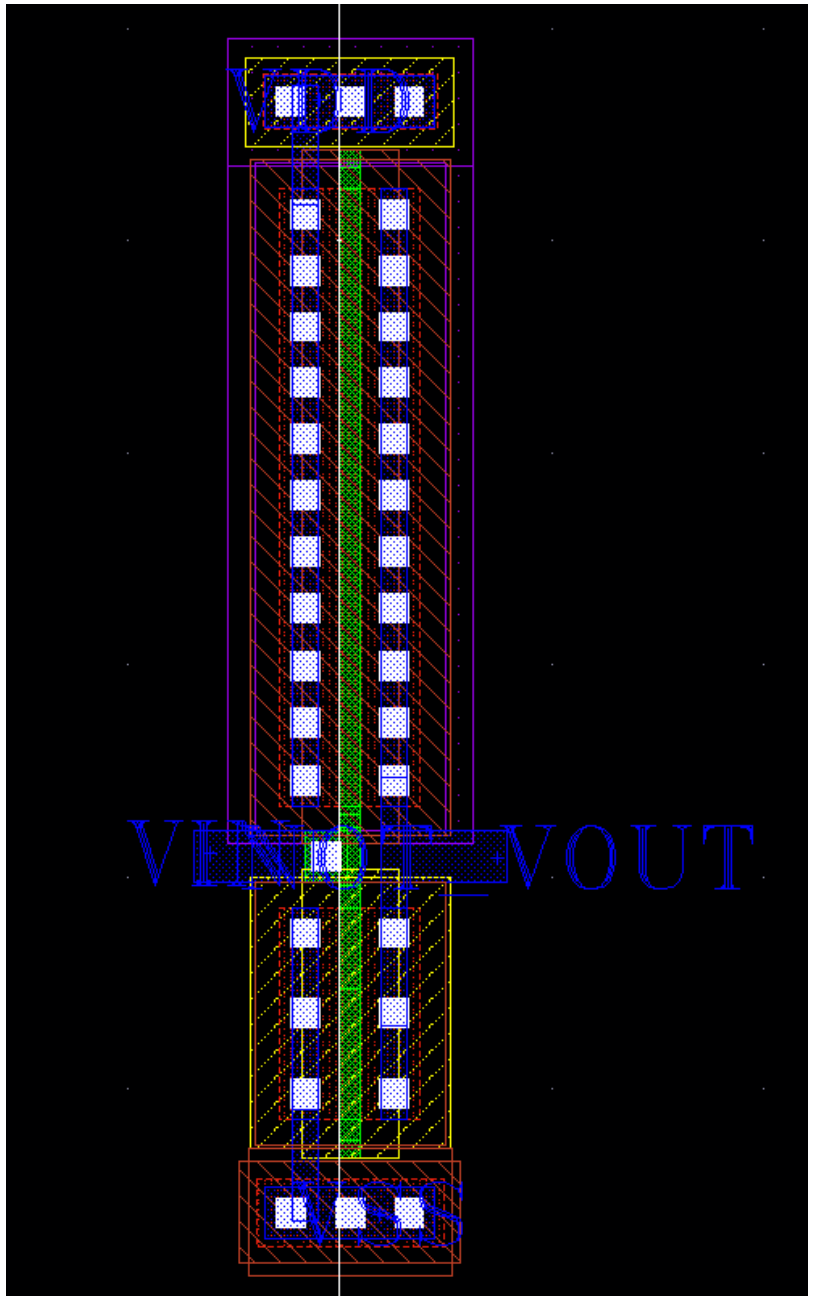
Inverter Schematic



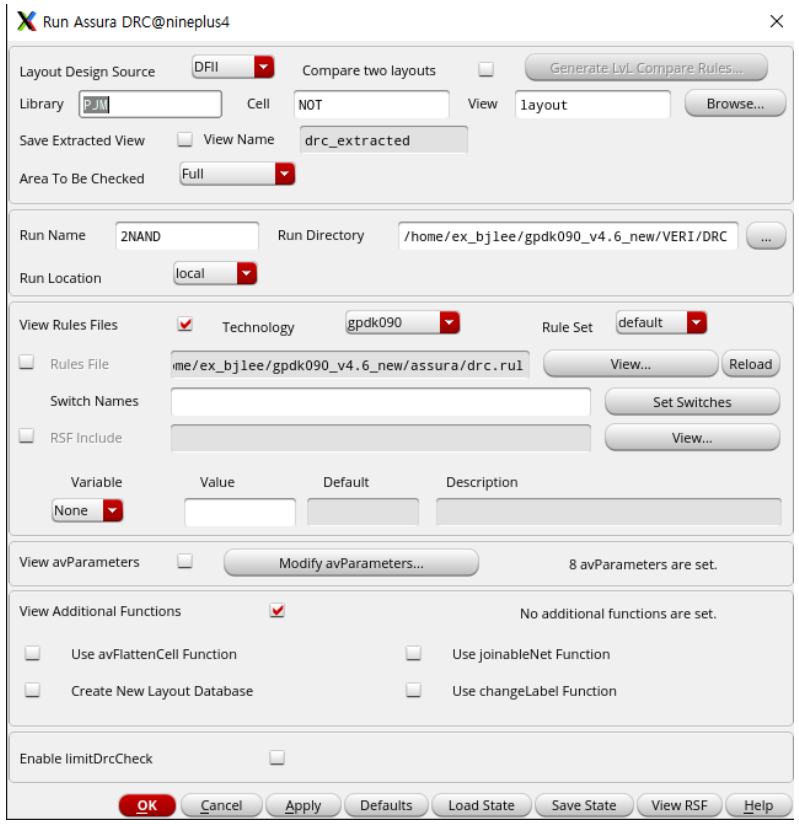
Switch Schematic

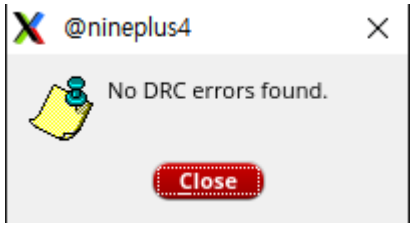


Inverter (Layout)

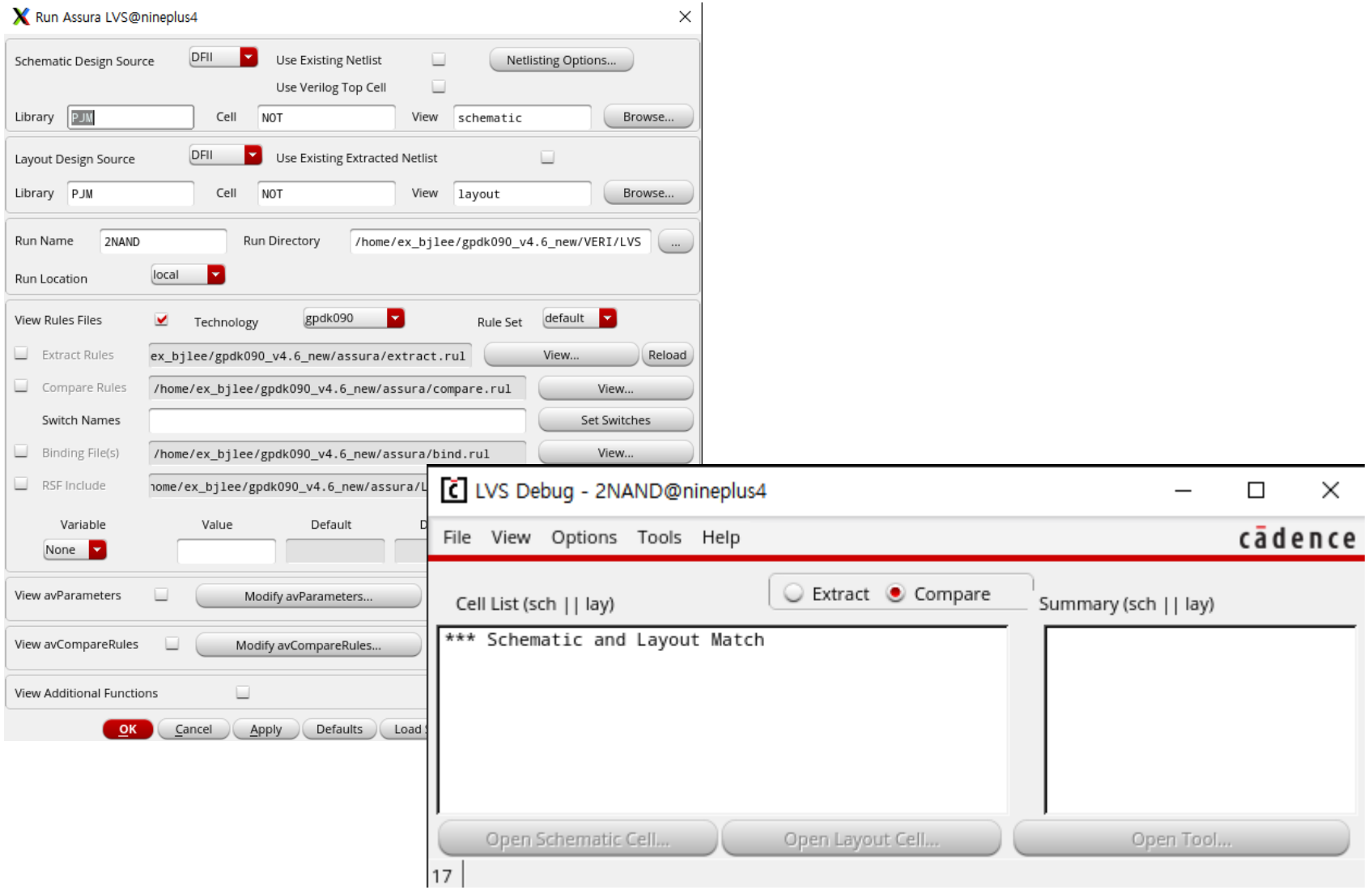


Inverter (DRC)

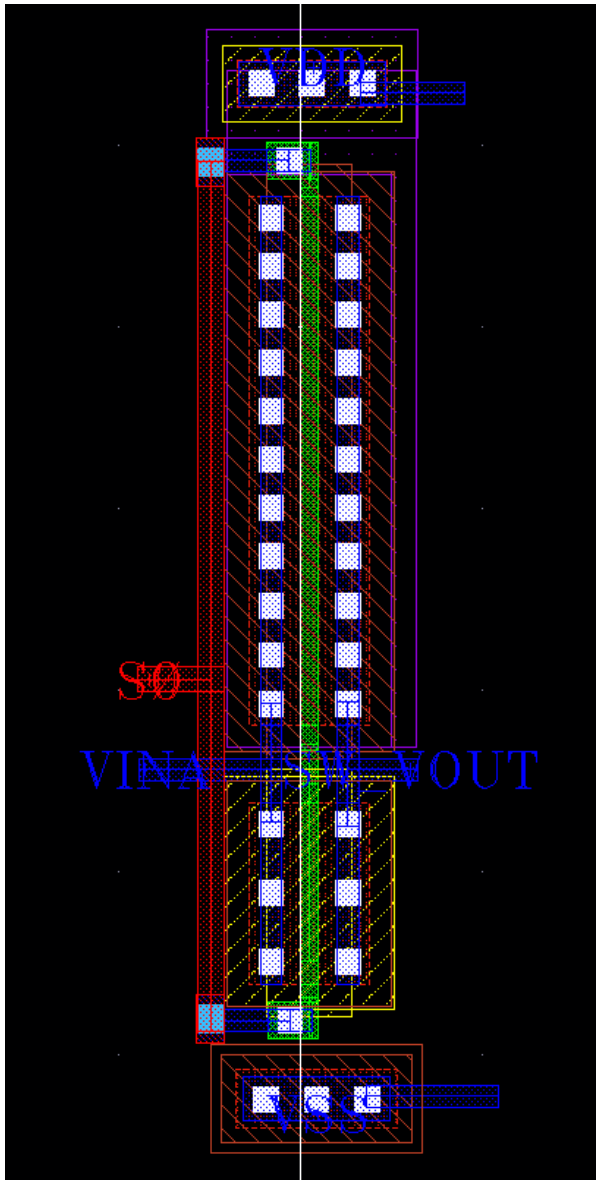




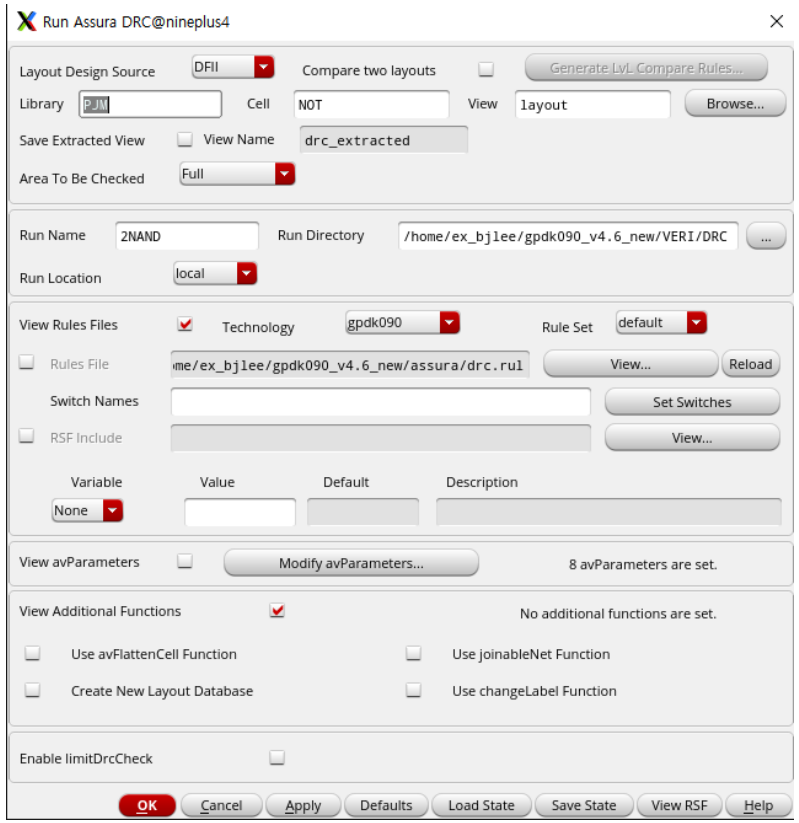
Inverter (LVS)

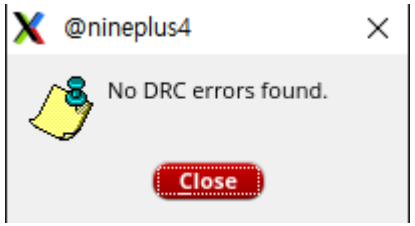


Switch (Layout)

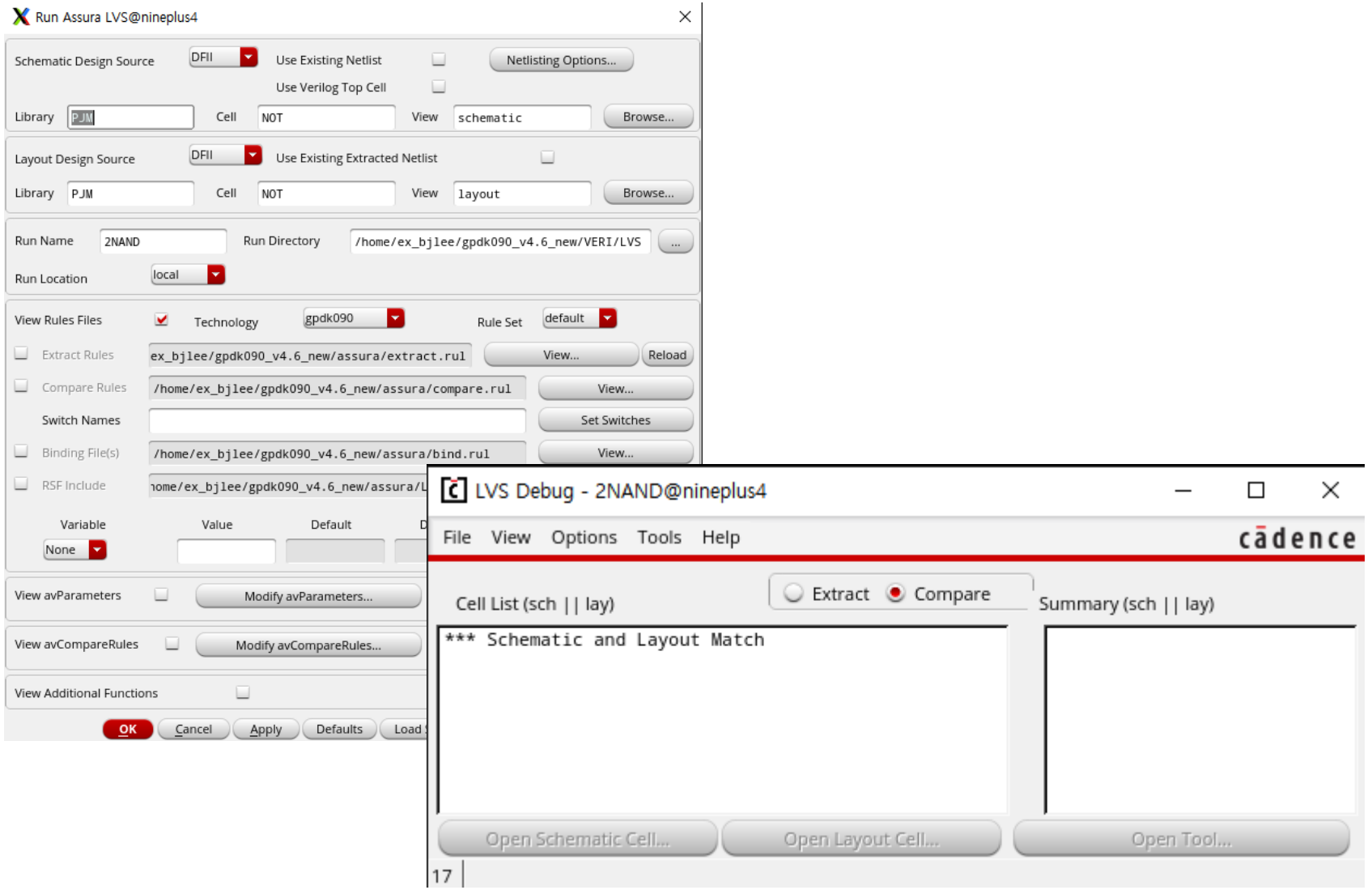


Switch (DRC)

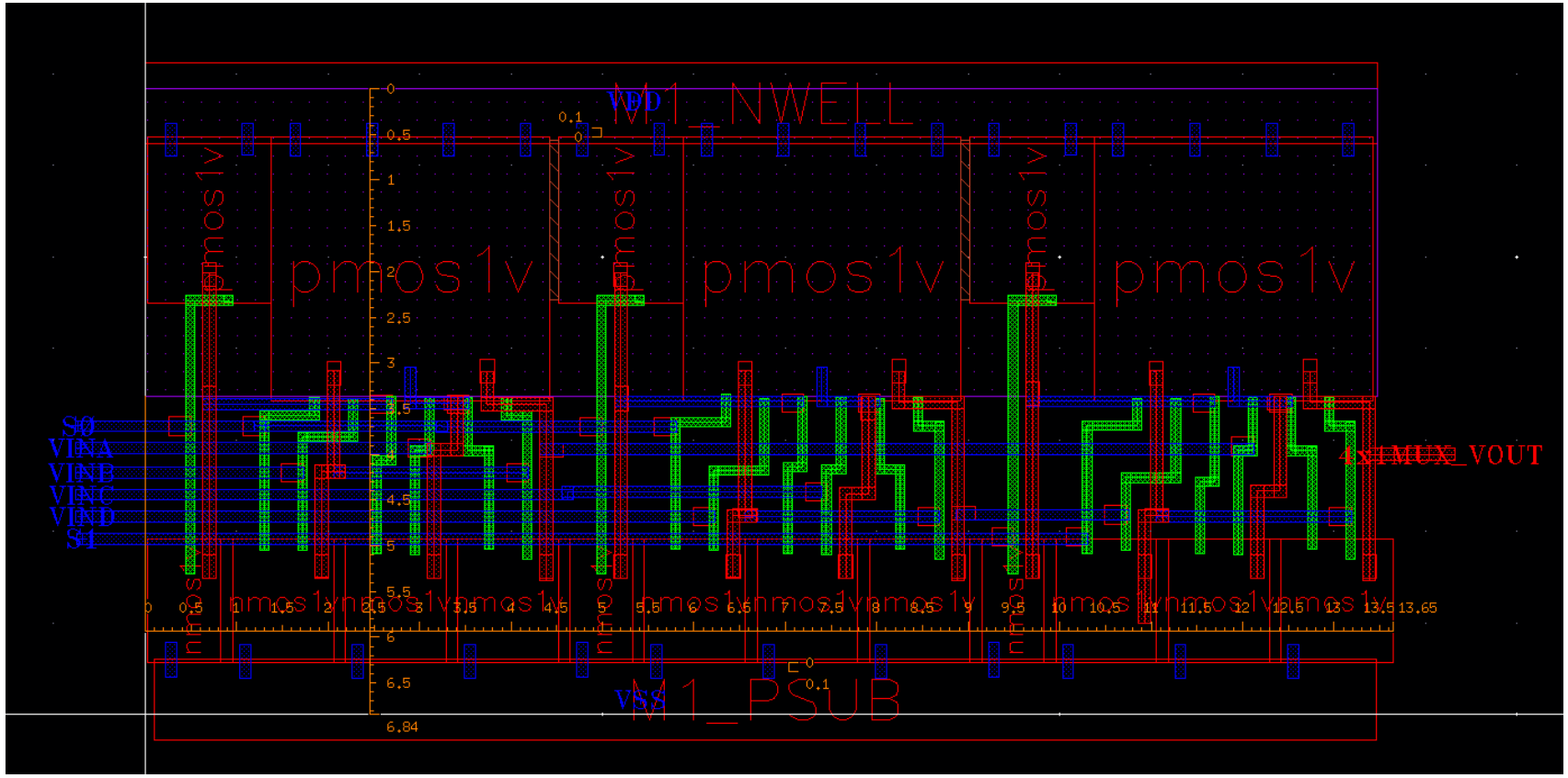

Run Assura DRC@nineplus4
Layout Design Source
DFII
Compare two layouts
Generate LvL Compare Rules...
Library
PJN
Cell
NOT
View
layout
Browse...
Save Extracted View
View Name
drc_extracted
Area To Be Checked
Full
Run Name
2NAND
Run Directory
/home/ex_bjlee/gpdk090_v4.6_new/VERI/DRC
Run Location
local
View Rules Files
Technology
gpdk090
Rule Set
default
Rules File
me/ex_bjlee/gpdk090_v4.6_new/assura/drc.rul
View...
Reload
Switch Names
Set Switches
RSF Include
View...
Variable
Value
Default
Description
None
View avParameters
Modify avParameters...
8 avParameters are set.
View Additional Functions
No additional functions are set.
Use avFlattenCell Function
Use joinableNet Function
Create New Layout Database
Use changeLabel Function
Enable limitDrcCheck
OK
Cancel
Apply
Defaults
Load State
Save State
View RSF
Help


@nineplus4
No DRC errors found.
Close

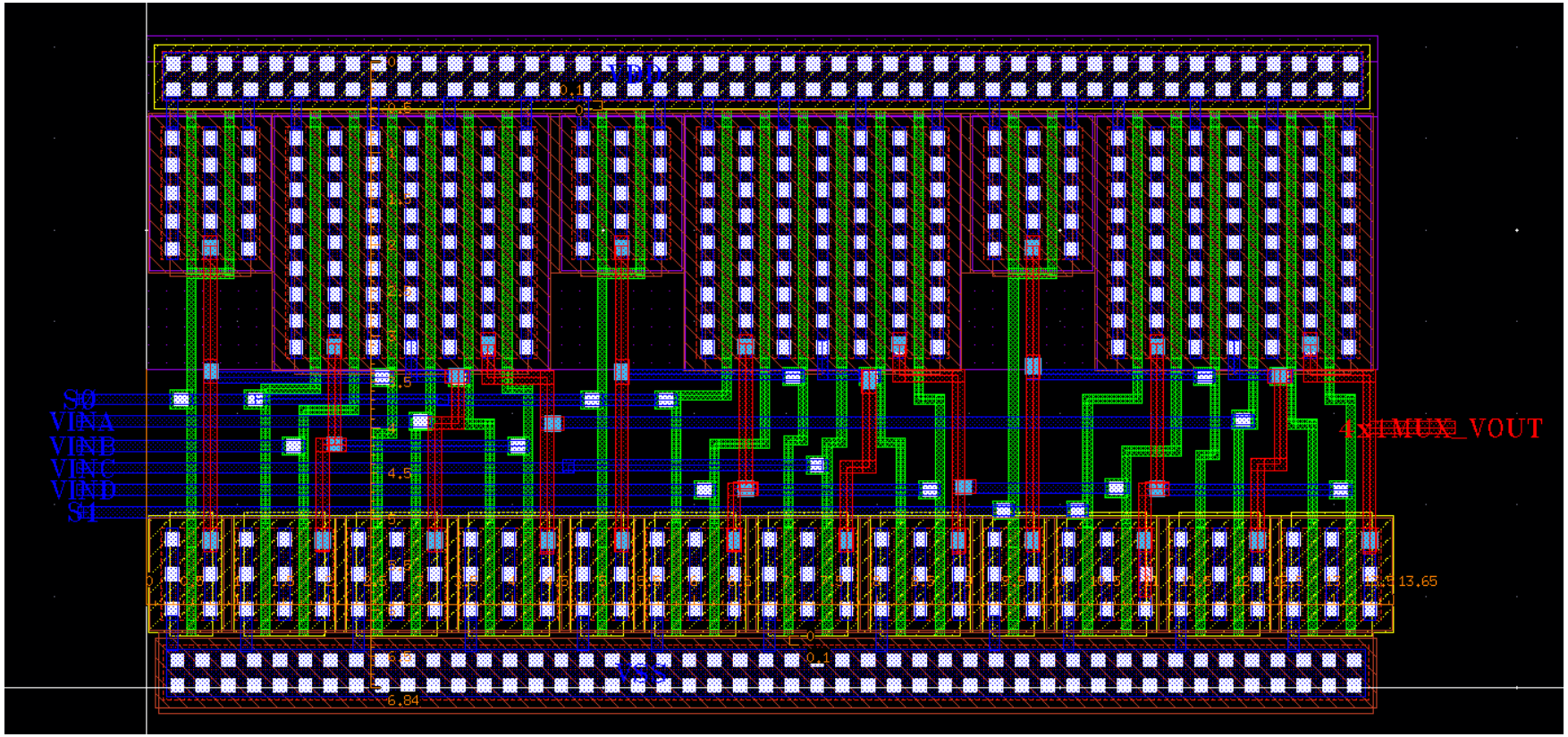
Switch (LVS)


Run Assura LVS@nineplus4
Schematic Design Source
DFII
Use Existing Netlist
Netlisting Options...
Use Verilog Top Cell
Library
PJM
Cell
NOT
View
schematic
Browse...
Layout Design Source
DFII
Use Existing Extracted Netlist
Library
PJM
Cell
NOT
View
layout
Browse...
Run Name
2NAND
Run Directory
/home/ex_bjlee/gpdk090_v4.6_new/VERI/LVS
Run Location
local
View Rules Files
Technology
gpdk090
Rule Set
default
Extract Rules
ex_bjlee/gpdk090_v4.6_new/assura/extract.rul
View...
Reload
Compare Rules
/home/ex_bjlee/gpdk090_v4.6_new/assura/compare.rul
View...
Switch Names
Set Switches
Binding File(s)
/home/ex_bjlee/gpdk090_v4.6_new/assura/bind.rul
View...
RSF Include
Variable
Value
Default
None
View avParameters
Modify avParameters...
View avCompareRules
Modify avCompareRules...
View Additional Functions
OK
Cancel
Apply
Defaults
LVS Debug - 2NAND@nineplus4
File
View
Options
Tools
Help
cadence
Extract
Compare
Cell List (sch || lay)
Summary (sch || lay)
*** Schematic and Layout Match
Open Schematic Cell...
Open Layout Cell...
Open Tool...
17

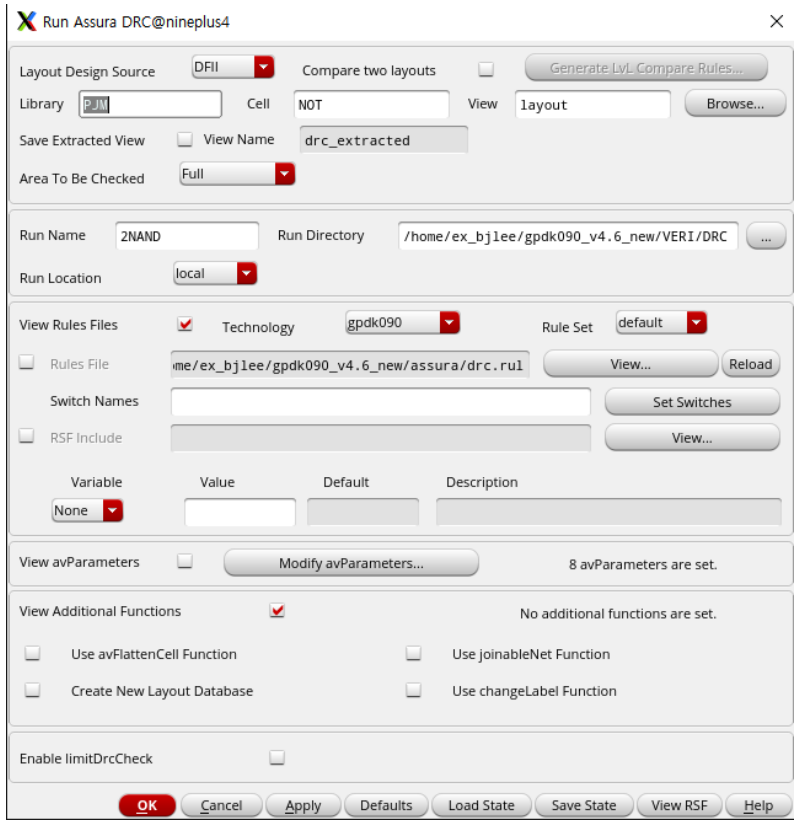
4*1 MUX Layout(logic gate)

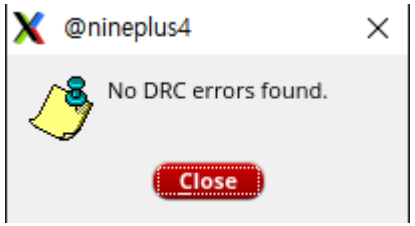


4*1 MUX Layout

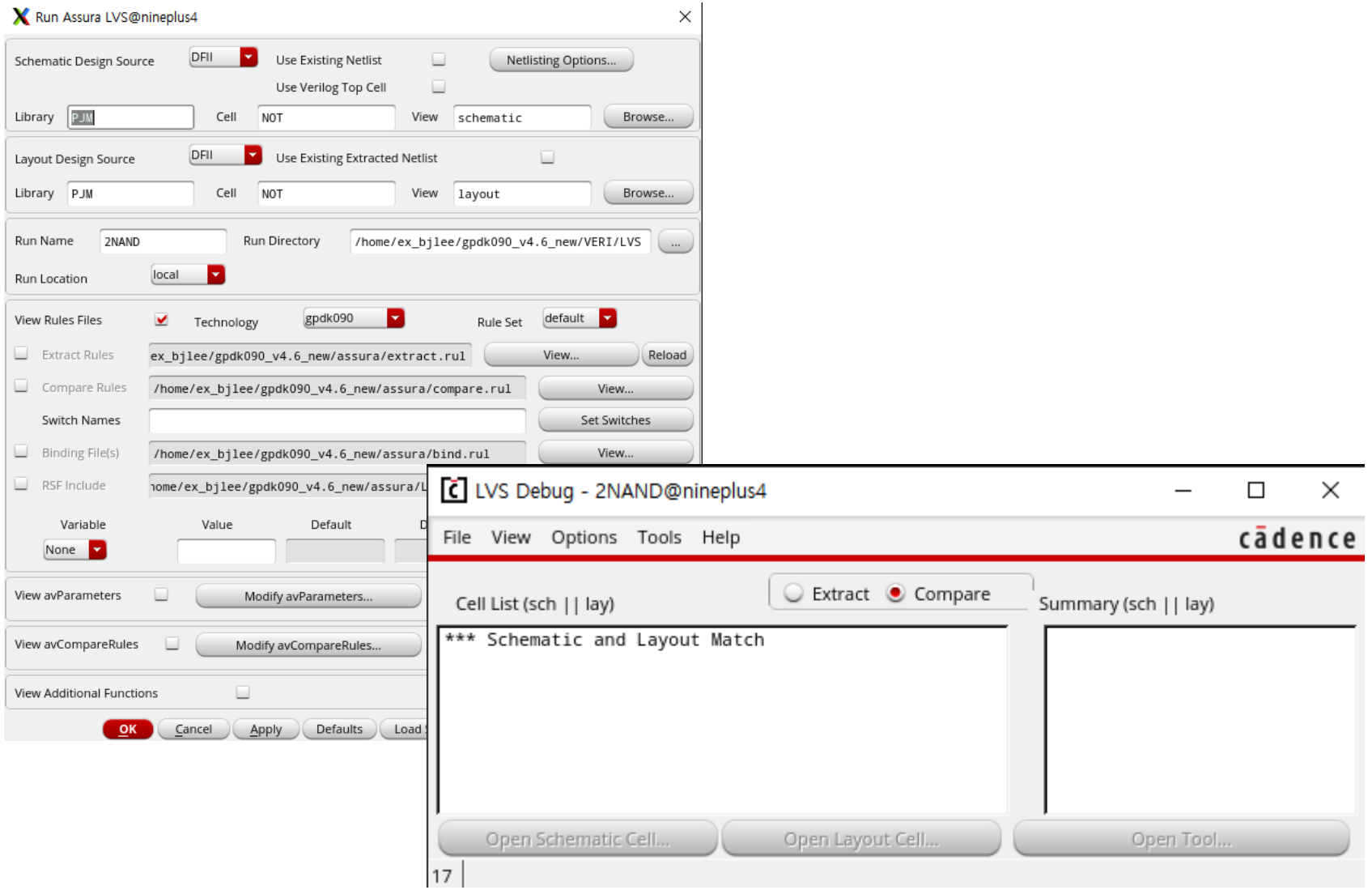


4*1 MUX DRC(logic gate)

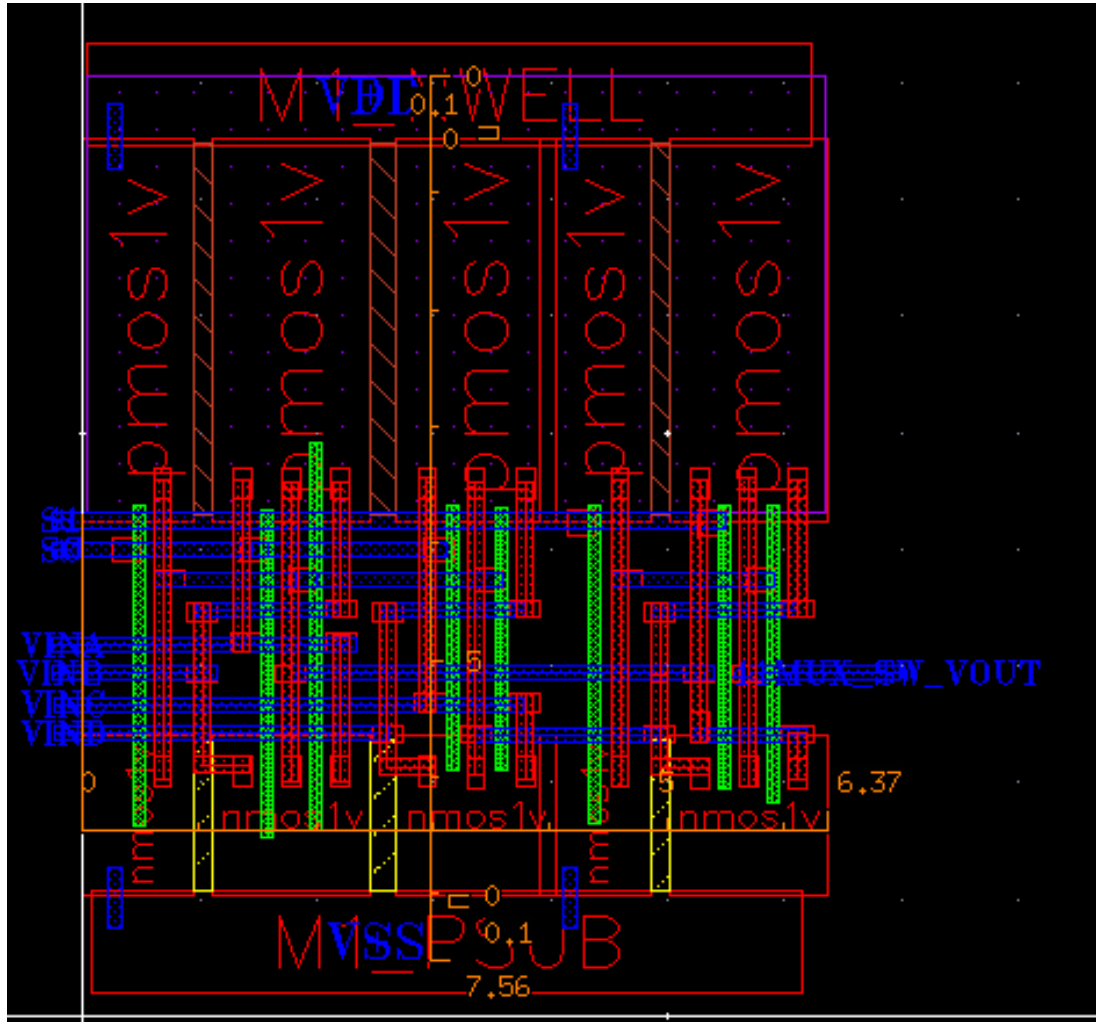




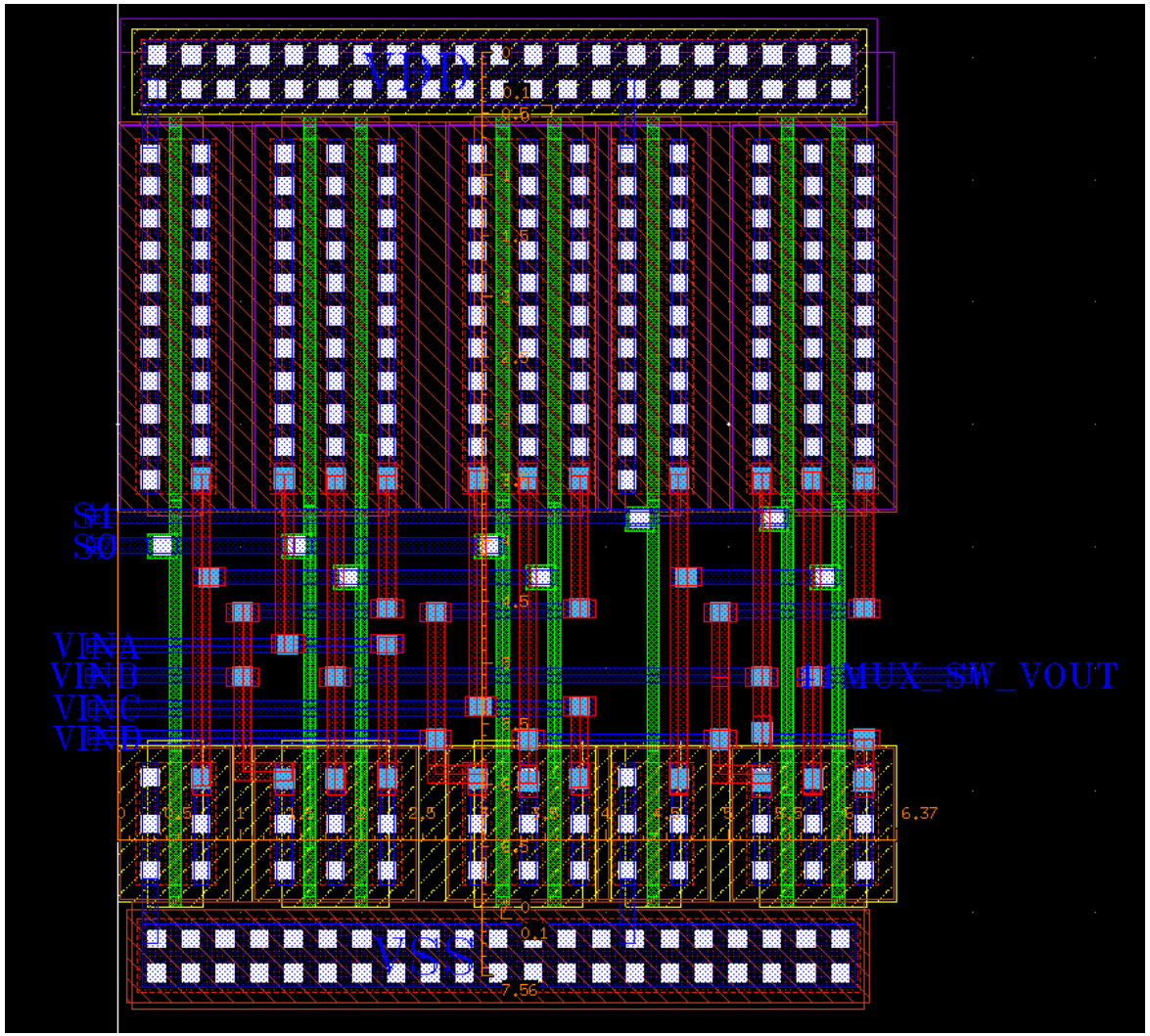
4*1 MUX LVS(logic gate)



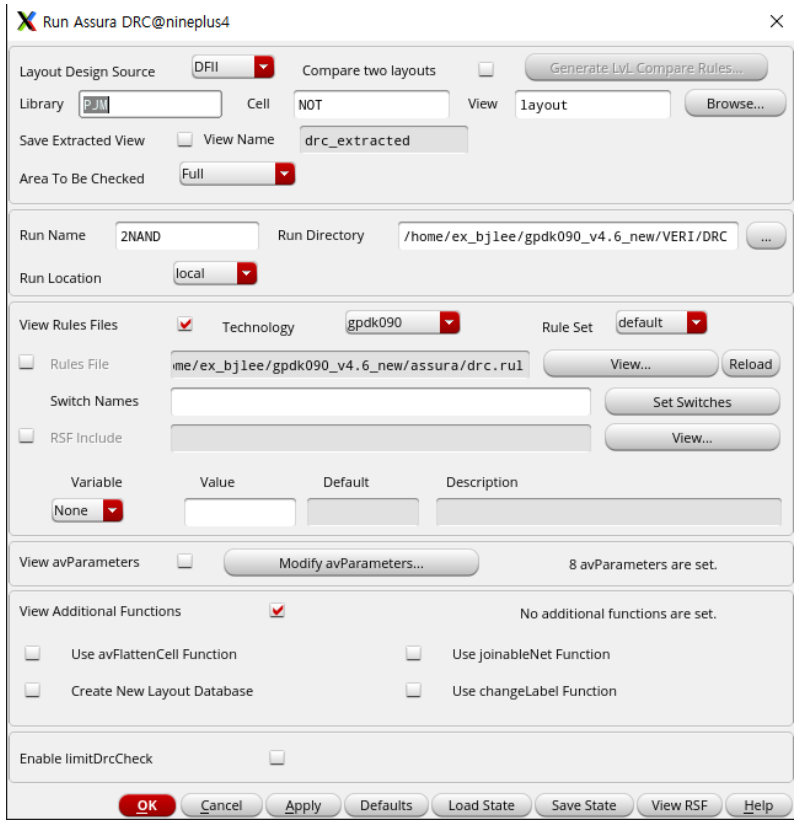
4*1 MUX Layout(Switch)

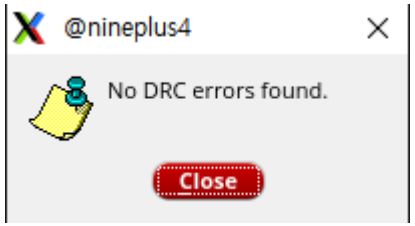


4*1 MUX Layout(Switch)

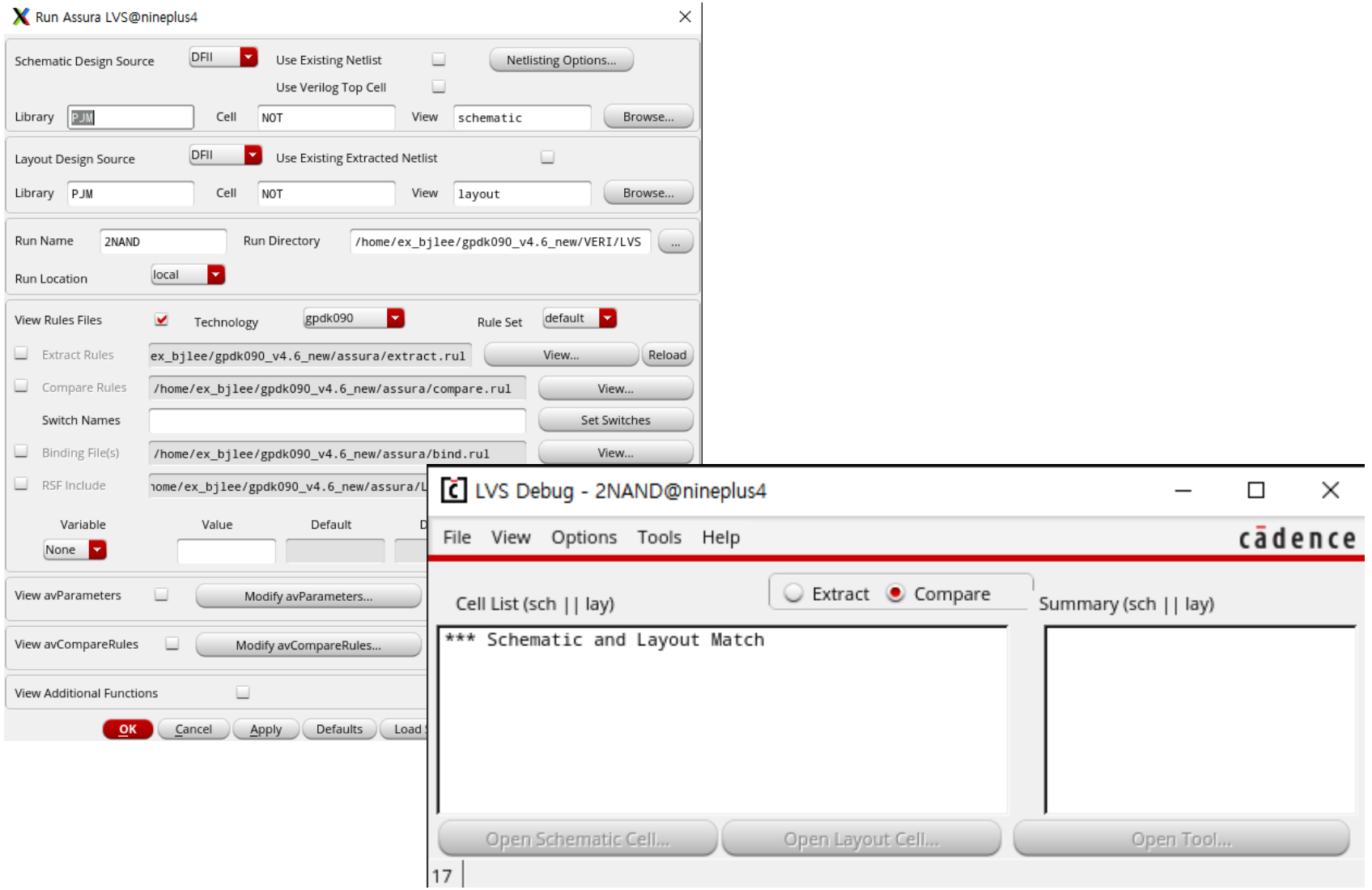


4*1 MUX DRC(Switch)





4*1 MUX LVS(Switch)



크기비교

	Logic gate	Switch
가로(um)	13.38	6.37
세로(um)	7.4	7.56

	Logic gate	Switch
Tr. 수	36	16
Tr. 수		20개 감소

Thank You

Q & A