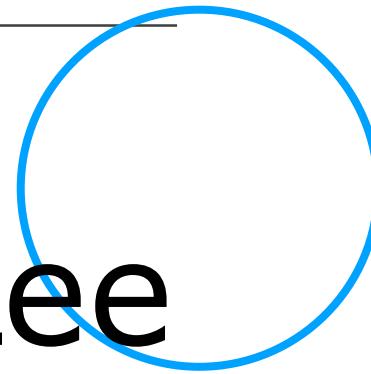


Cadence
Full-Custom IC Design

One Chip Design



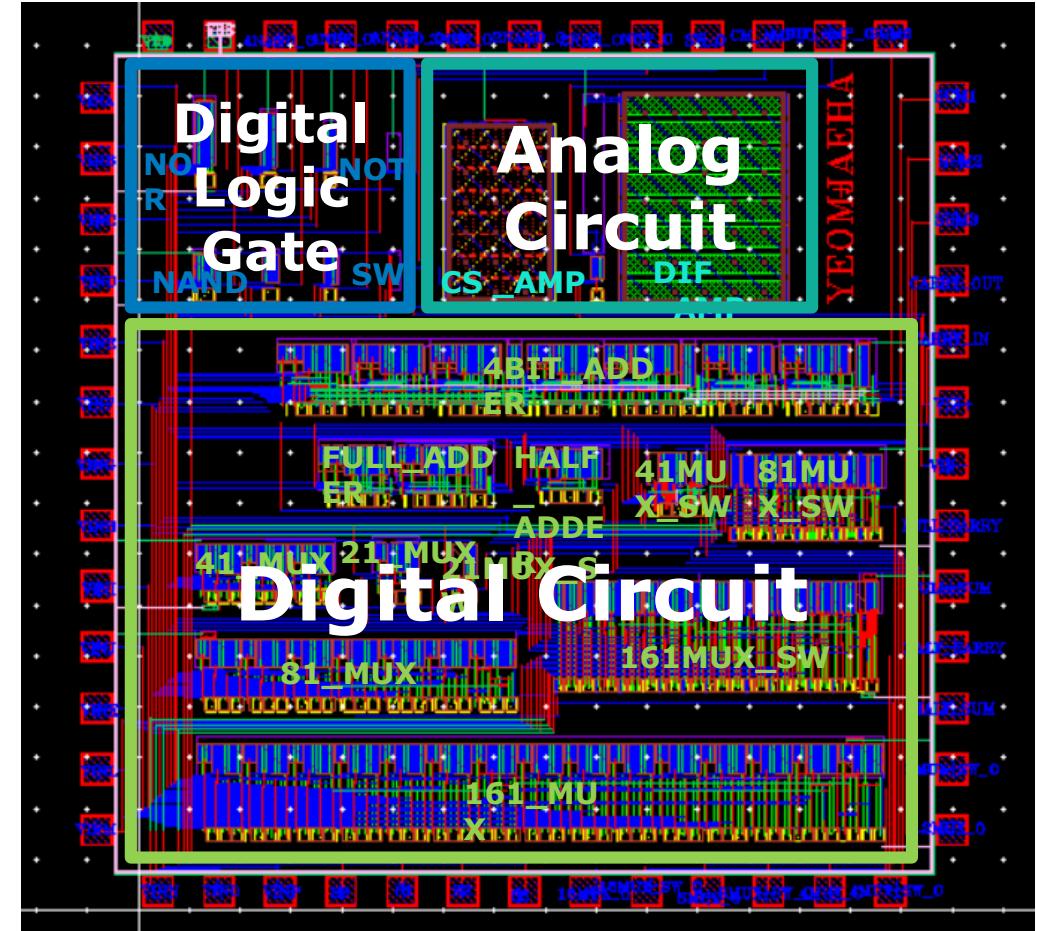
Ph. D. ByoungJin Lee

INDEX

Program & Tool

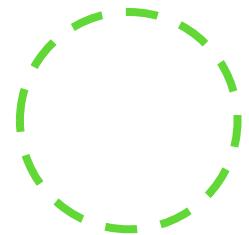
Digital Circuits & Analog Circuits
Schematic / Simulation / Layout / DRC/ LVS

One Chip





PROGRAM & TOOL



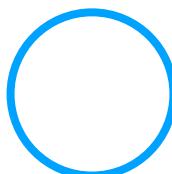
Cadence Virtuoso Schematic Editor/Layout Editor

Cadence Virtuoso Spectre/ADE

Assura(LVS & DRC)

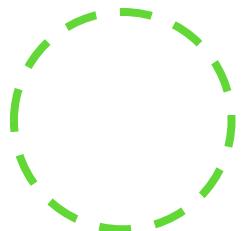


GPKD090





DIGITAL CIRCUITS & ANALOG CIRCUITS



Digital Logic Gates

- NOT / SWITCH
- 2NAND / 3NAND / 4NAND
- 2NOR / 3NOR / 4NOR

Digital Circuits

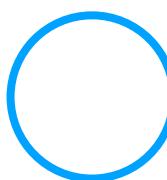
- 2x1 MUX / 4x1 MUX / 8x1 MUX / 16x1 MUX (Difference Logic & Switch)
- HALF_ADDER / FULL_ADDER / 4BIT_ADDER

Analog Circuits

- Common Source Amp / Differential Amp (Single-ended Output)

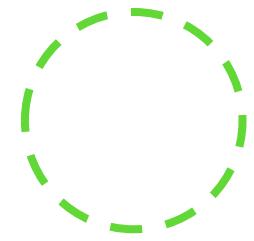


One Chip





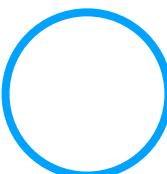
DIGITAL LOGIC GATE



-NOT / SWITCH

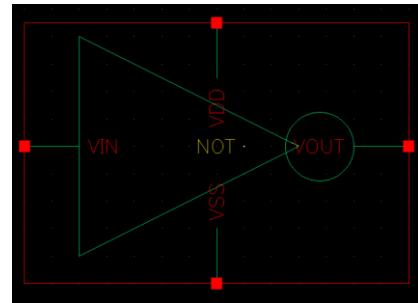
-2NAND / 3NAND / 4NAND

-2NOR / 3NOR / 4NOR





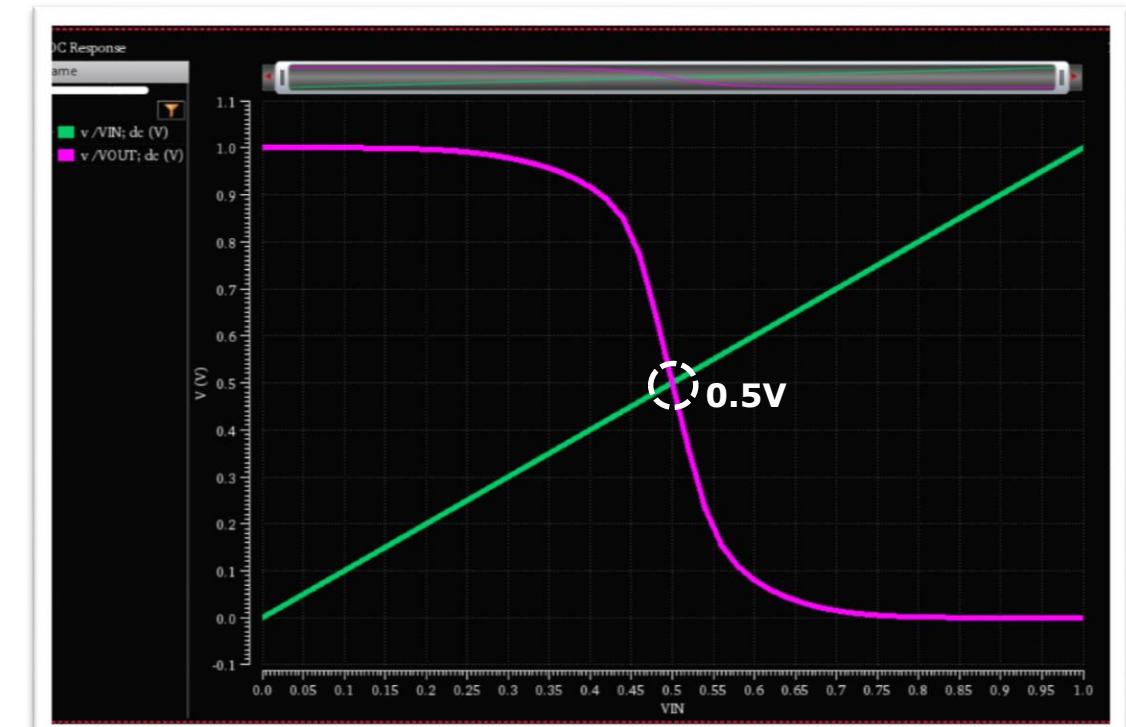
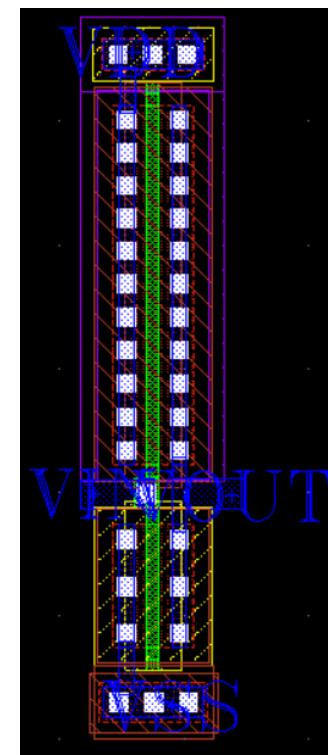
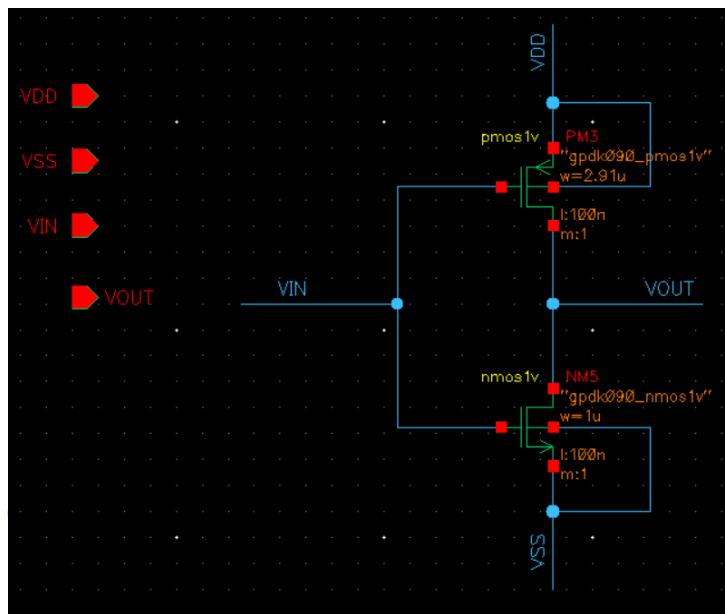
NOT



Schematic

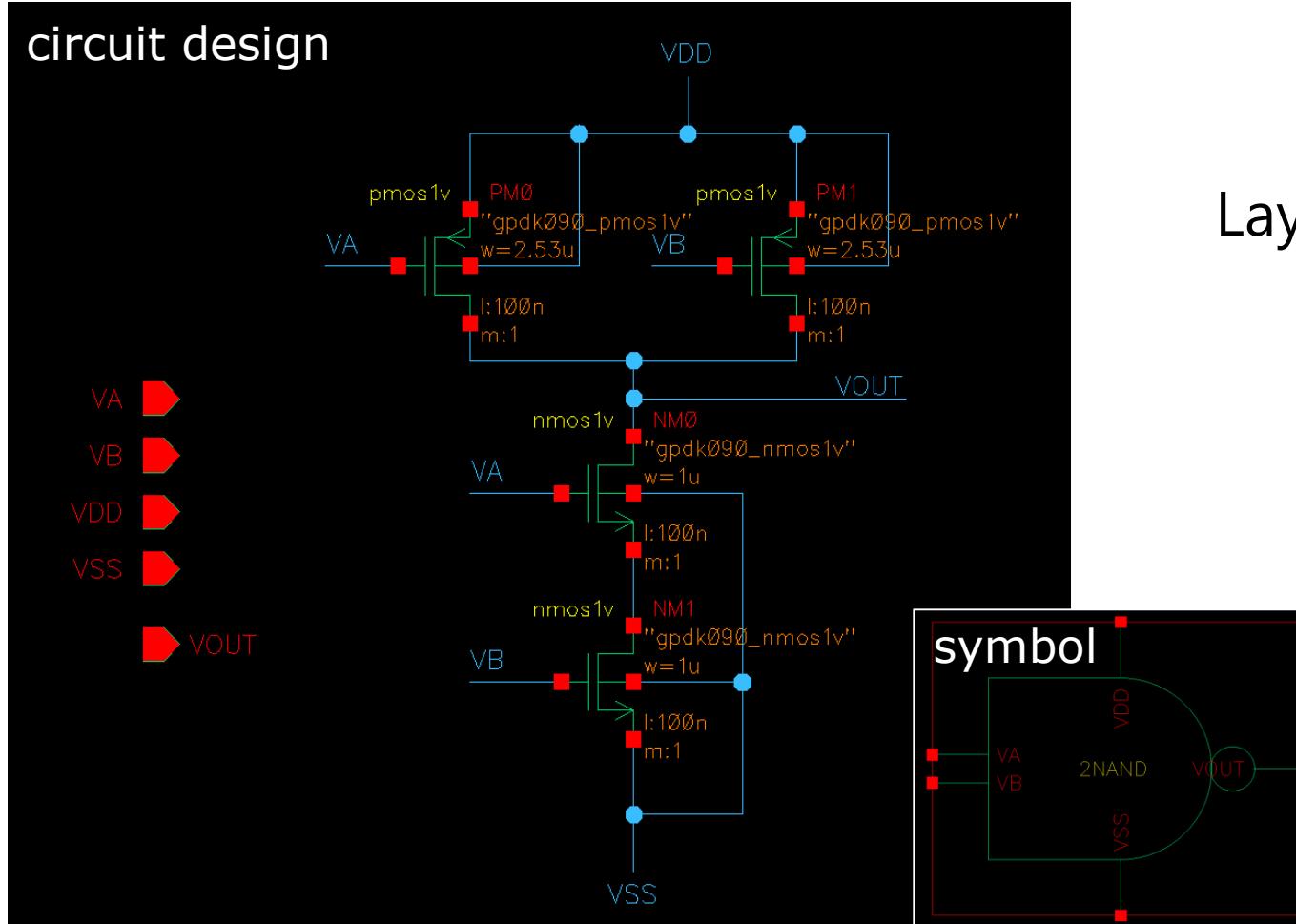
Layout

Simulation

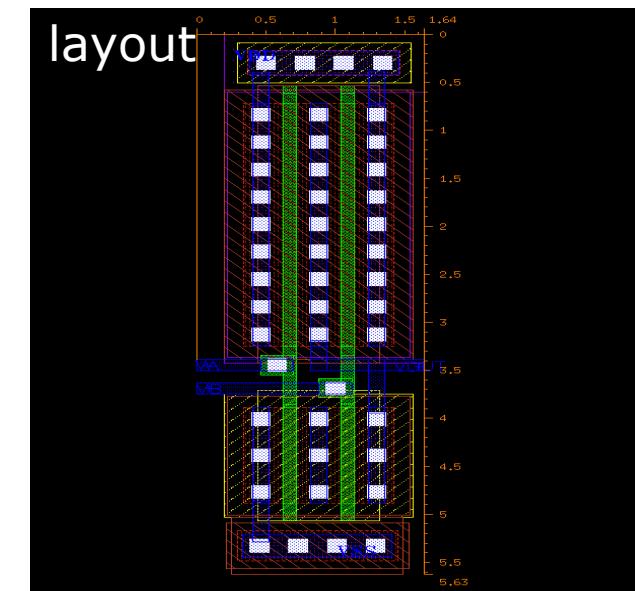


2NAND

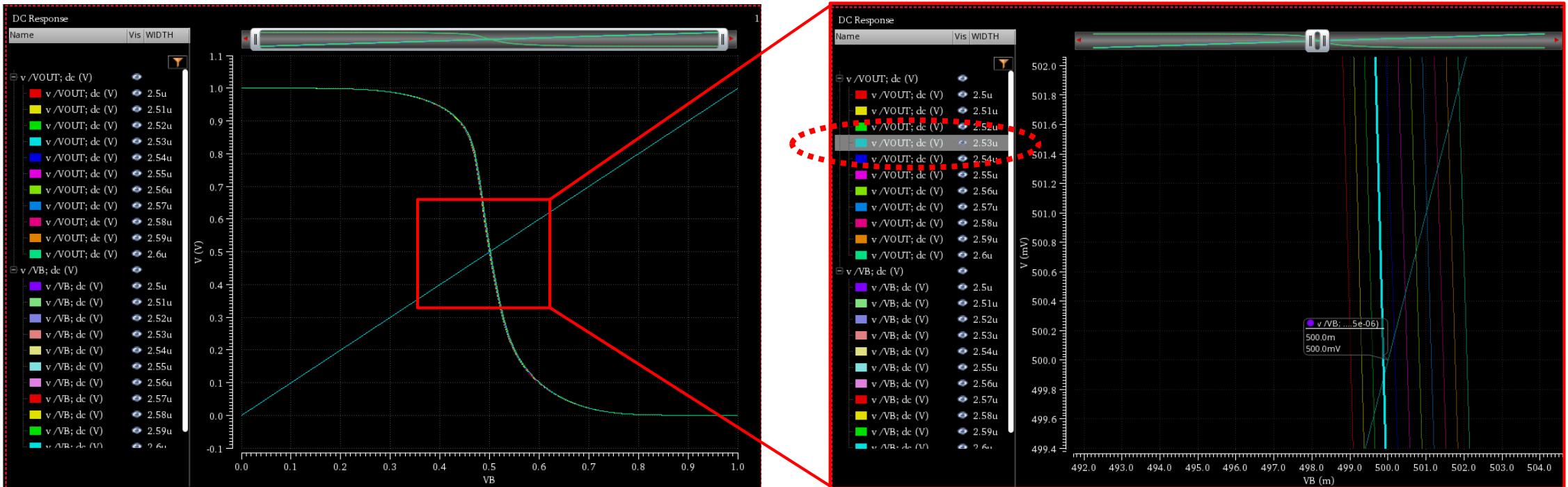
circuit design



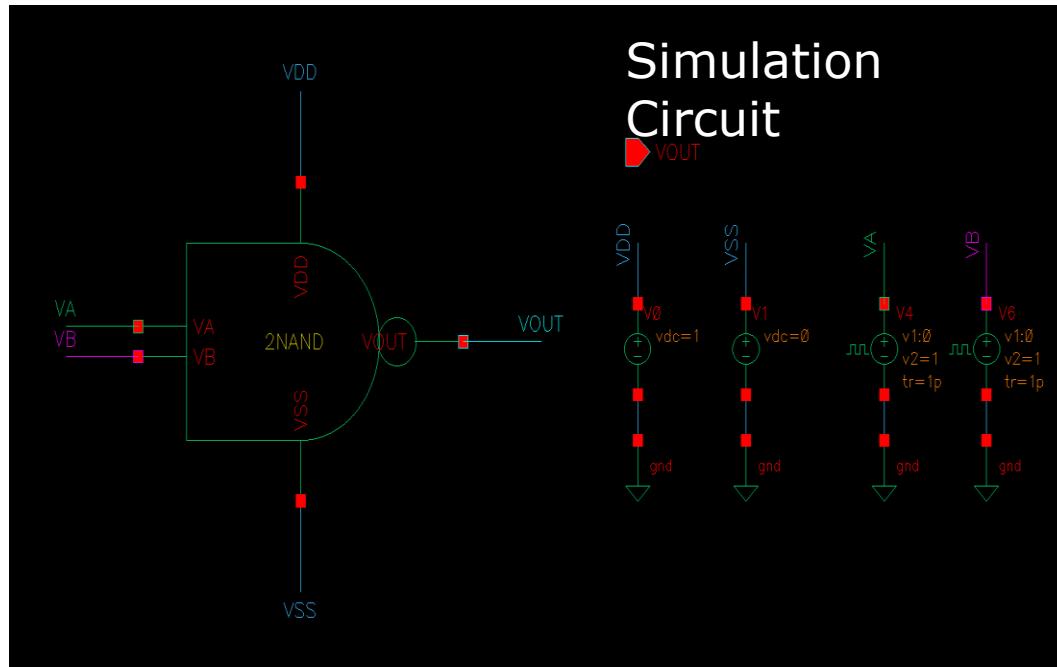
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2NAND Simulation

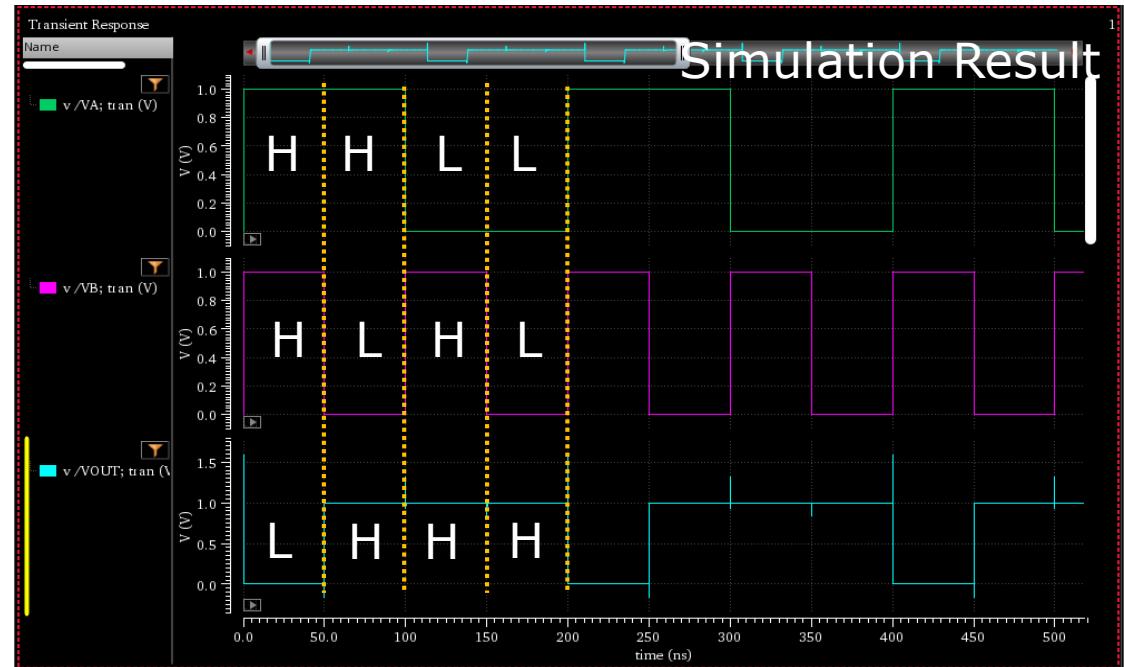


2NAND Simulation



Truth table

V _A	V _B	V _{OUT}
L	L	H
L	H	H
H	L	H
H	H	L

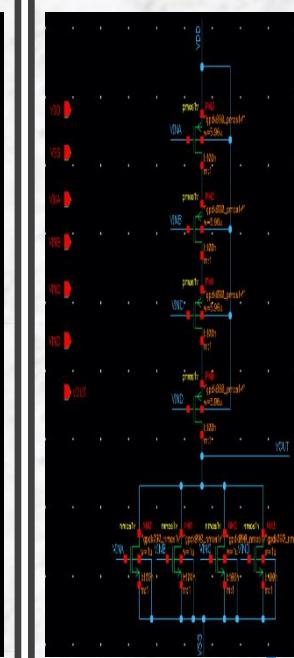
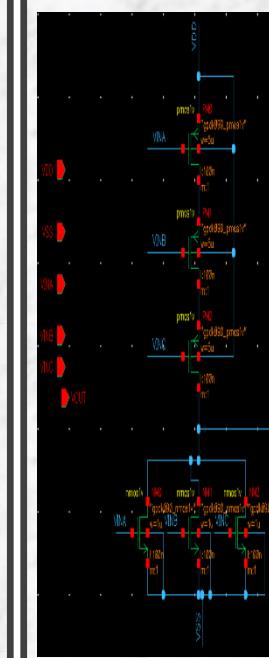
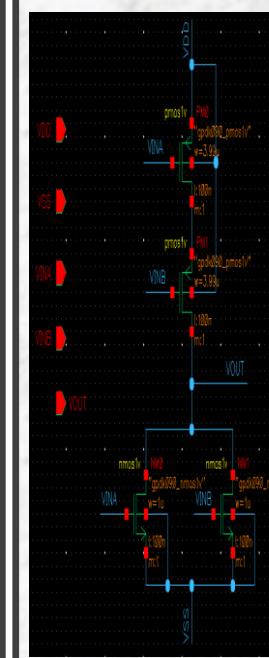
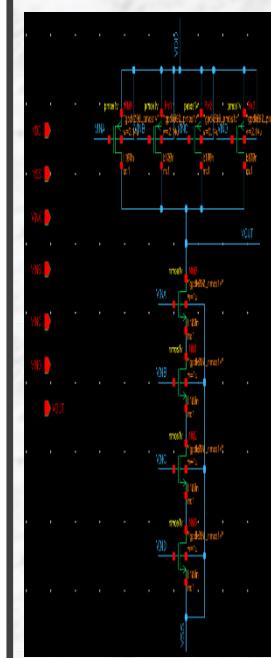
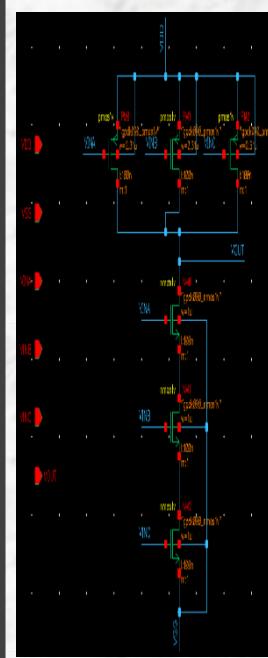
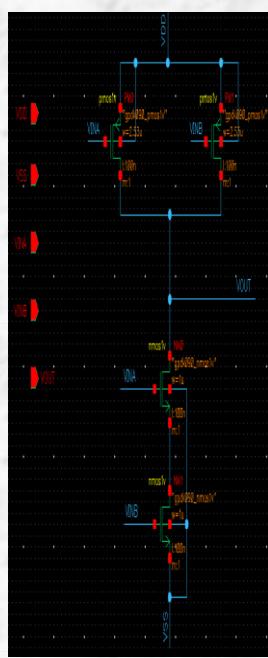
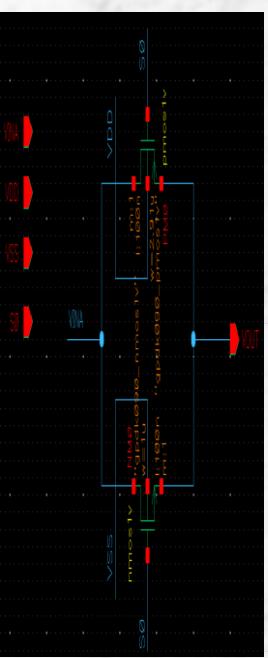
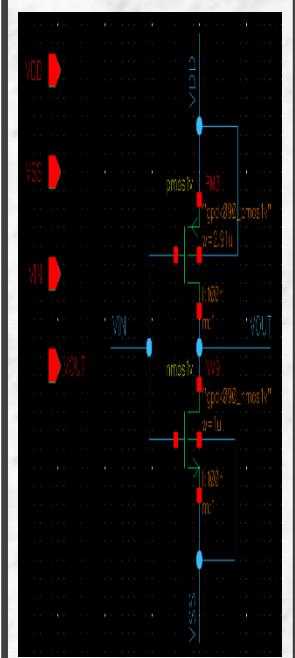


Digital Logic Gate Schematic

● ● ● ● ●

	NOT	SWITCH	2NAND	3NAND	4NAND	2NOR	3NOR	4NOR
NMOS L=100nm	1um	1um	1um	1um	1um	1um	1um	1um
PMOS L=100nm	2.91um	2.91um	2.53um	2.31um	2.14um	3.99um	5um	5.96um

NOT SWITCH 2NAND 3NAND 4NAND 2NOR 3NOR 4NOR



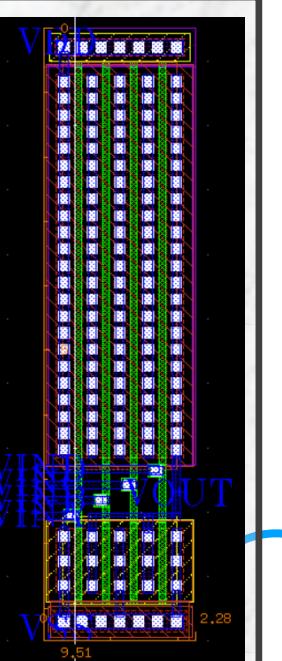
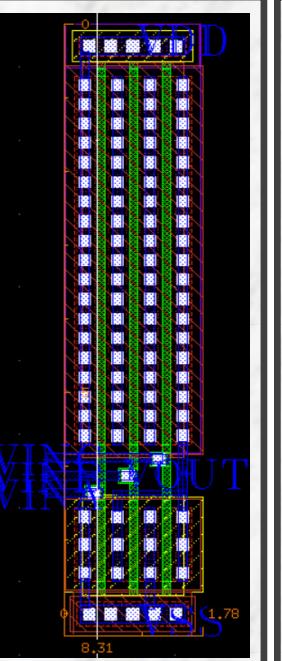
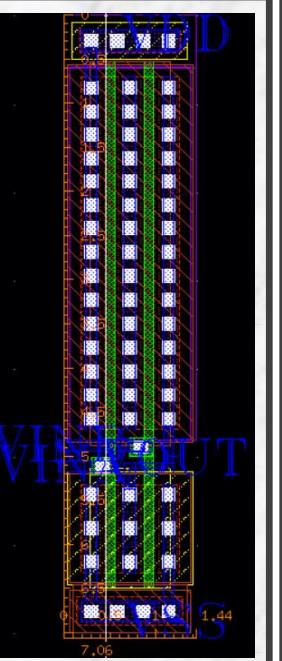
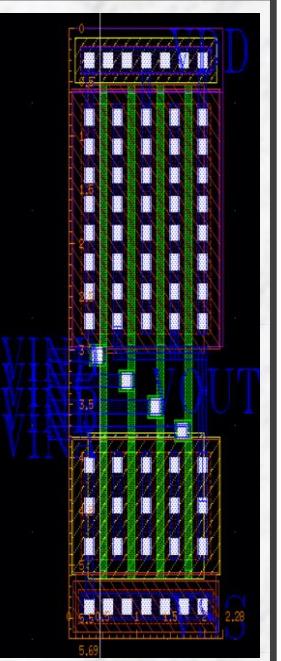
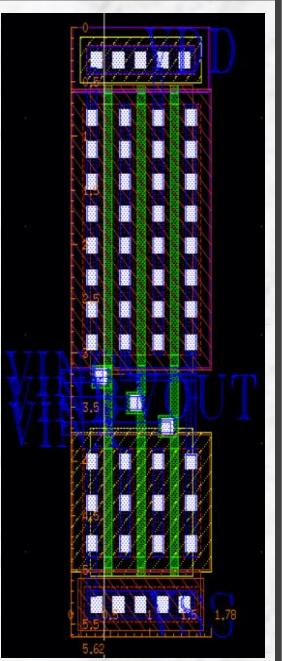
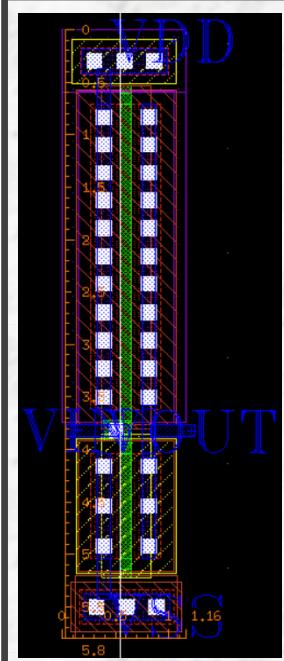
Digital Logic Gate Layout

● ● ● ● ●

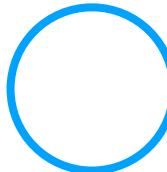
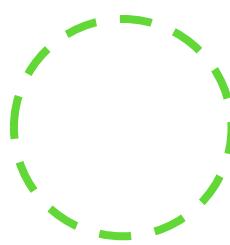
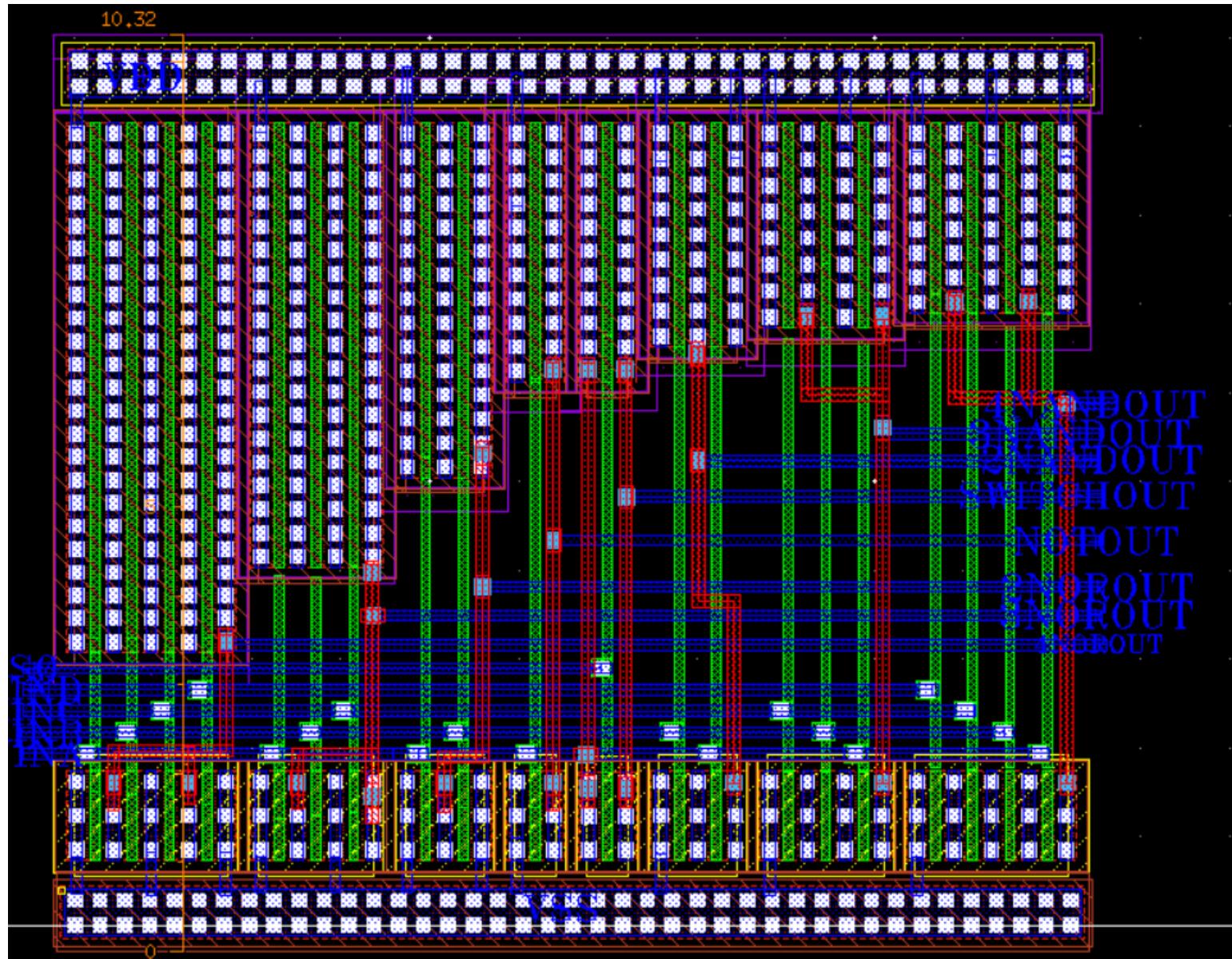


	NOT	SWITCH	2NAND	3NAND	4NAND	2NOR	3NOR	4NOR
Area(μm^2)	6.728	6.9832	8.0928	10.0036	12.9732	10.1664	14.7918	21.6828

NOT SWITCH 2NAND 3NAND 4NAND 2NOR 3NOR 4NOR

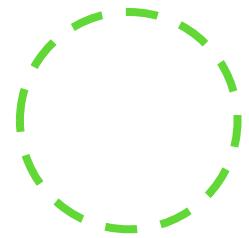


Digital Logic Gate Layout



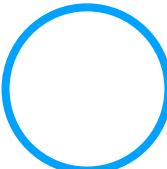


DIGITAL CIRCUIT



- 2x1 MUX / 4x1 MUX / 8x1 MUX / 16x1 MUX (Logic & Switch)

- HALF_ADDER / FULL_ADDER / 4BIT_ADDER

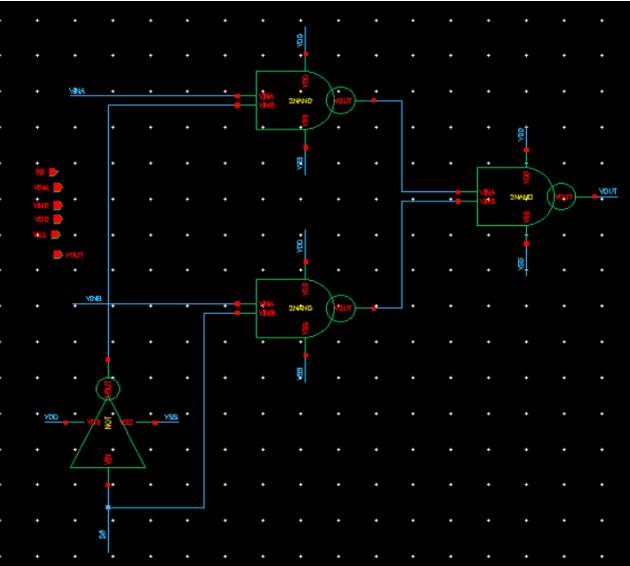


2X1 MUX (LOGIC & SWITCH)

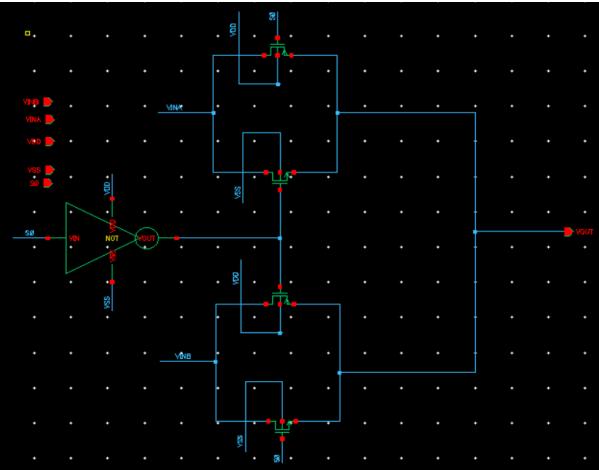


Logic

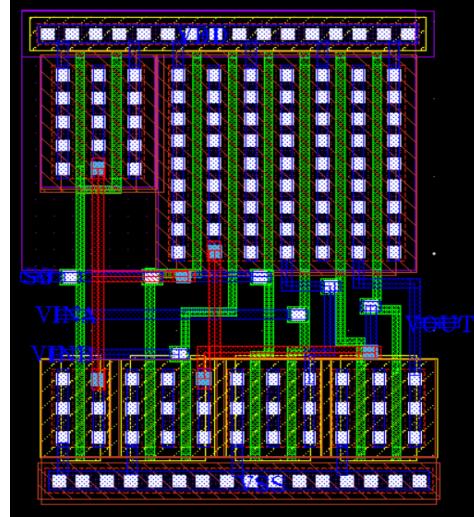
Schematic



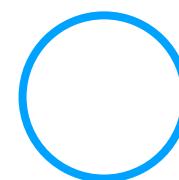
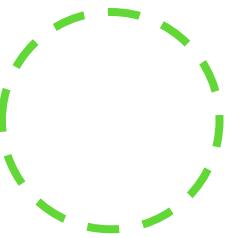
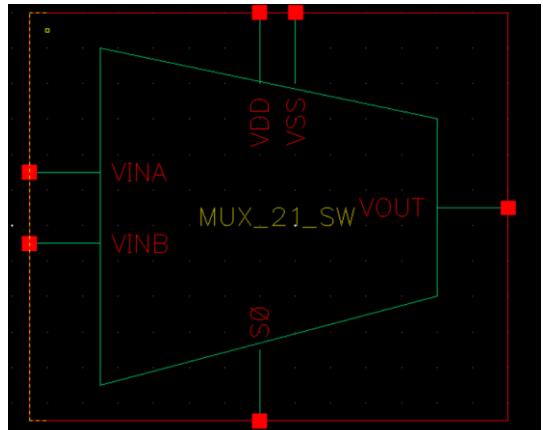
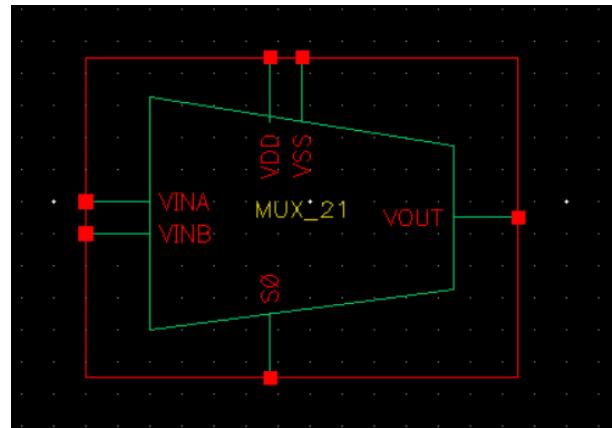
Switch



Layout



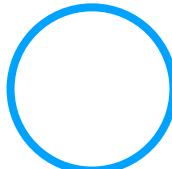
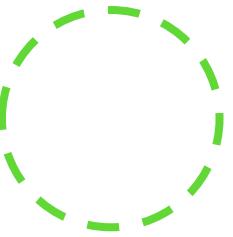
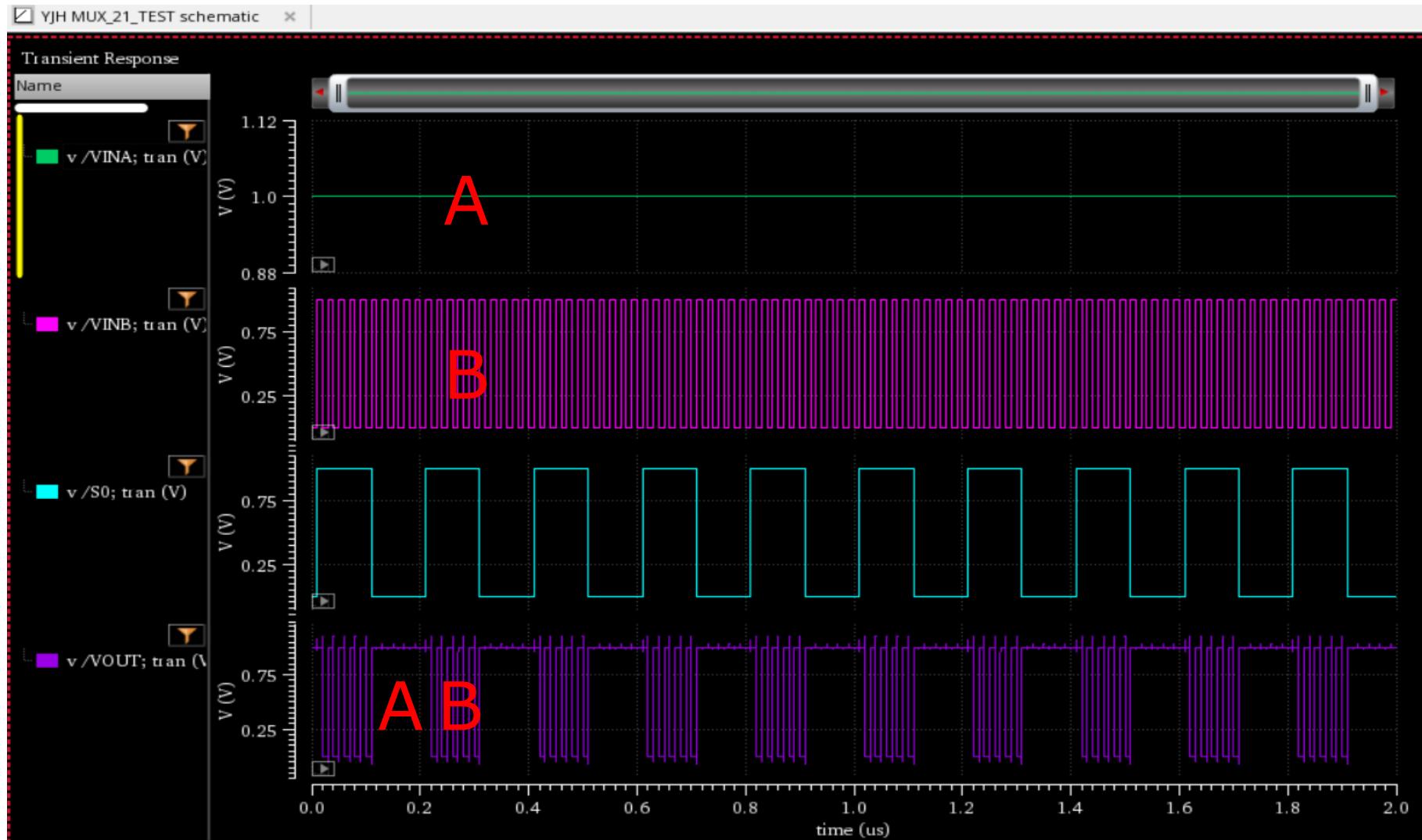
Symbol



2X1 MUX (LOGIC & SWITCH)

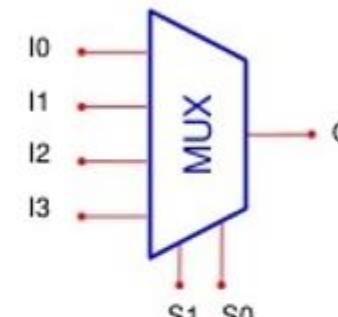
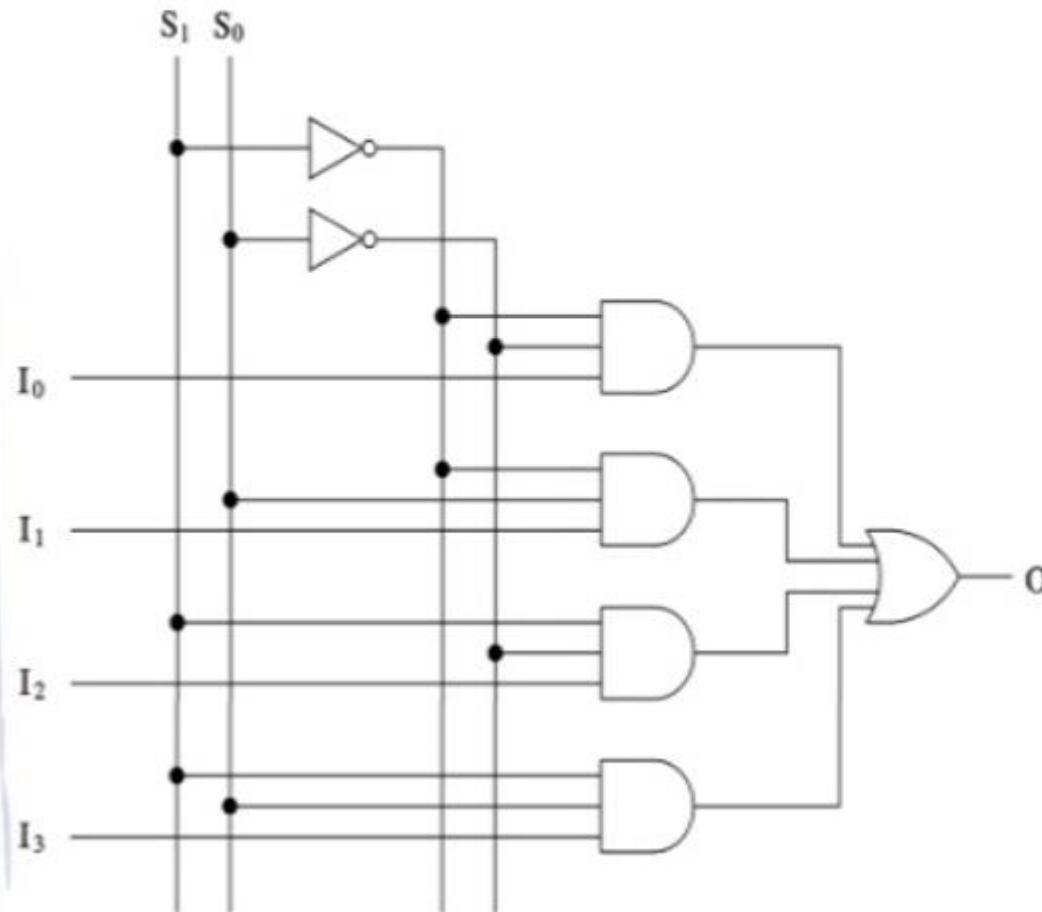
Logic
&
Switch

Simulation



4 X 1 MUX

Multiplexer (MUX)

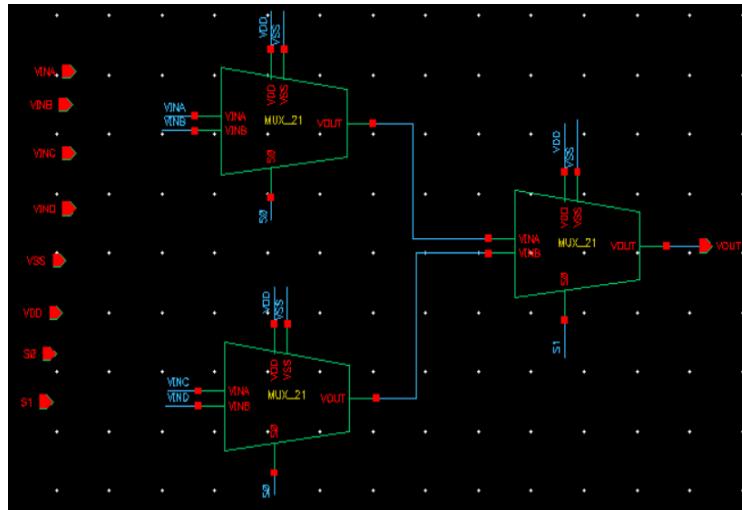


S_1	S_0	O
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

4X1 MUX (LOGIC & SWITCH)

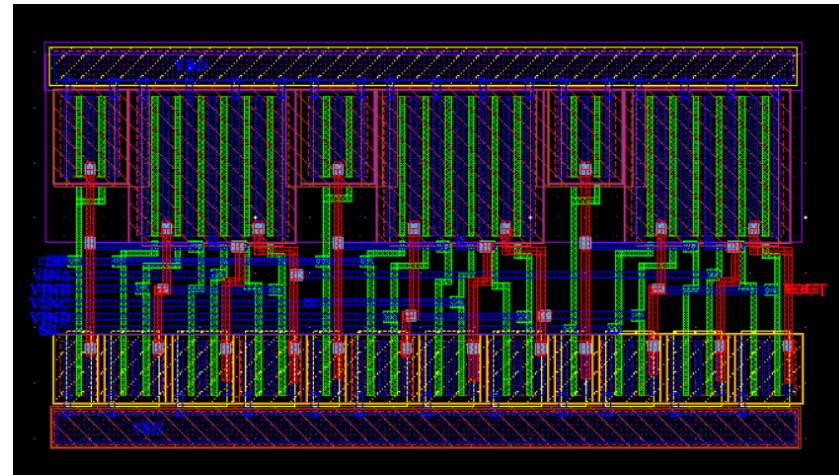
● ● ● ● ●

Logic

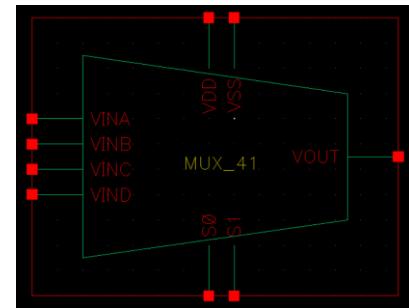


Schematic

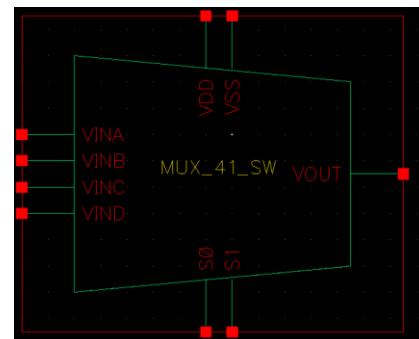
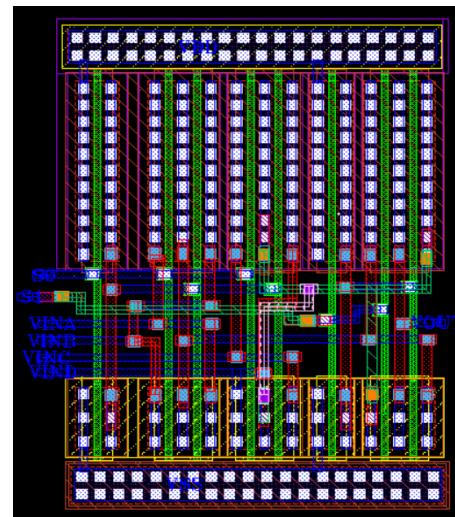
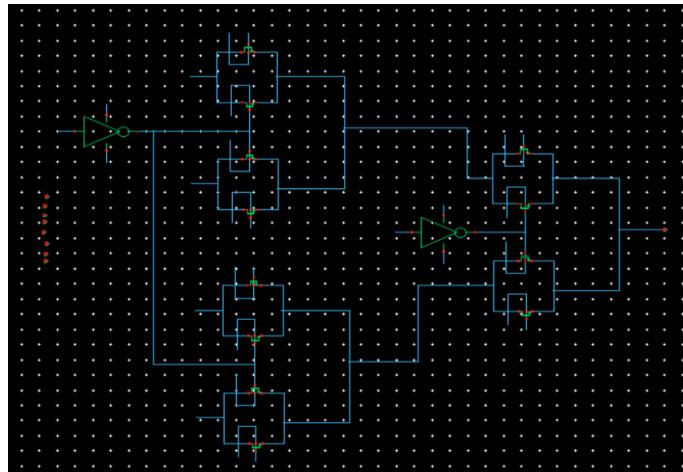
Layout



Symbol



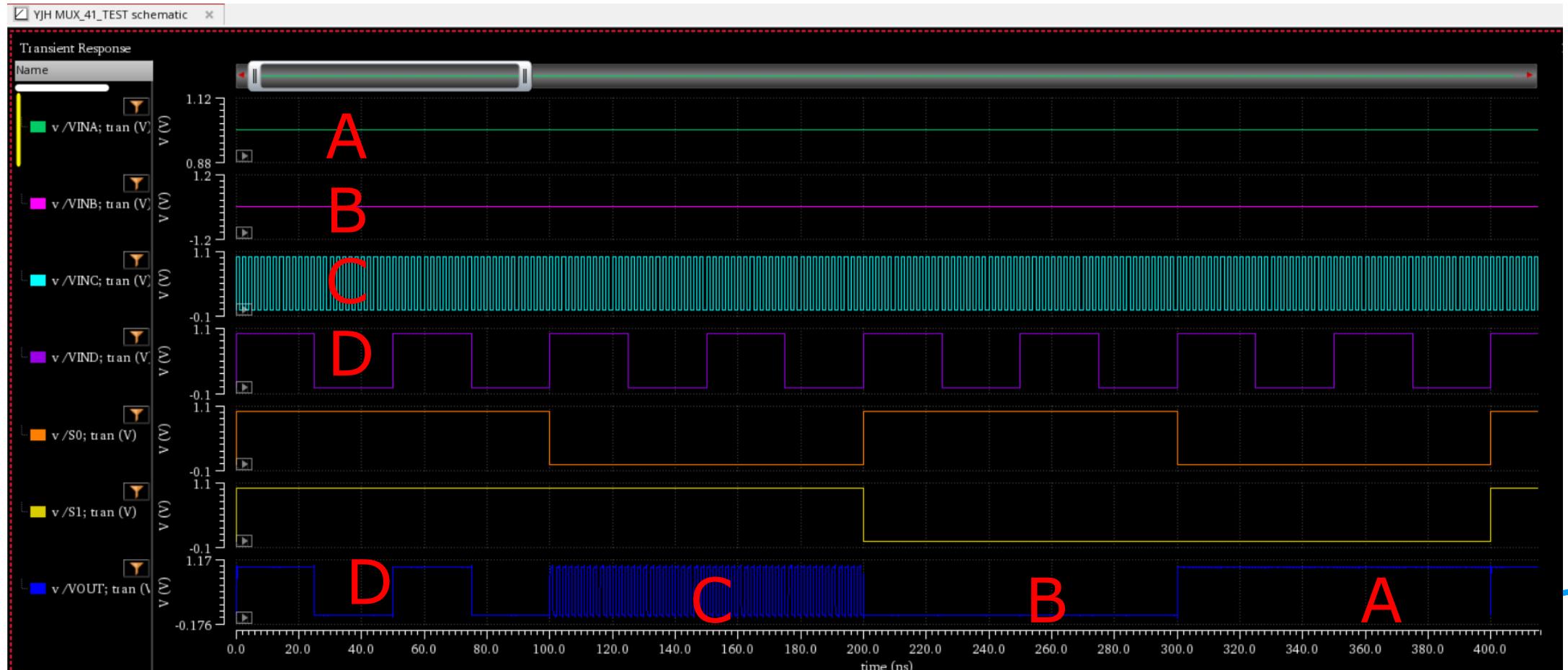
Switch



4X1 MUX (LOGIC & SWITCH)

Simulation

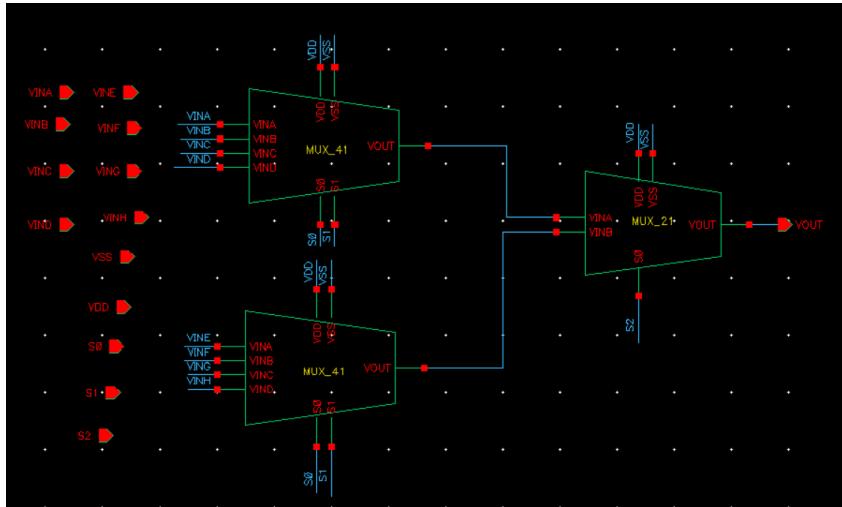
Logic
&
Switch



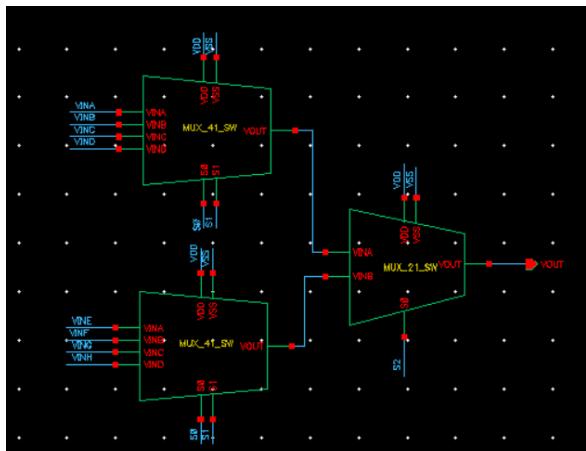
8X1 MUX (LOGIC & SWITCH)



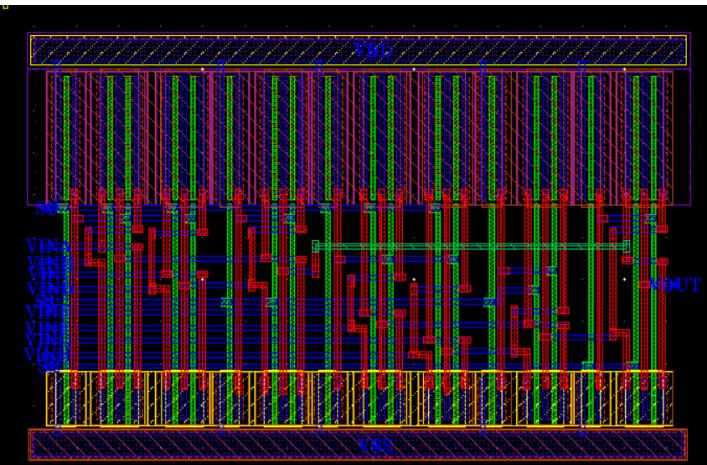
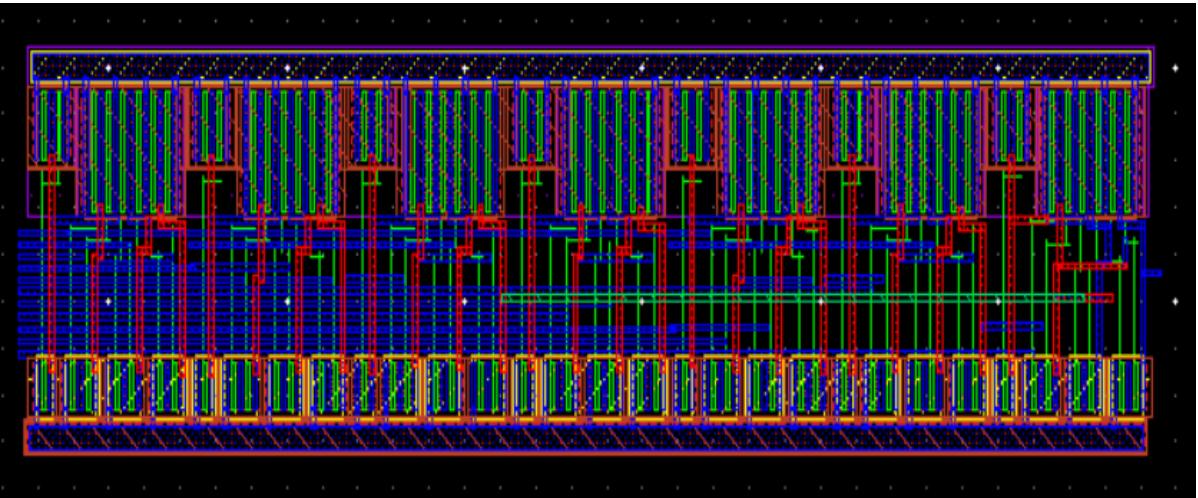
Logic



Switch



Layout

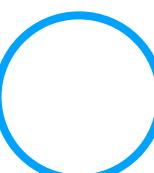
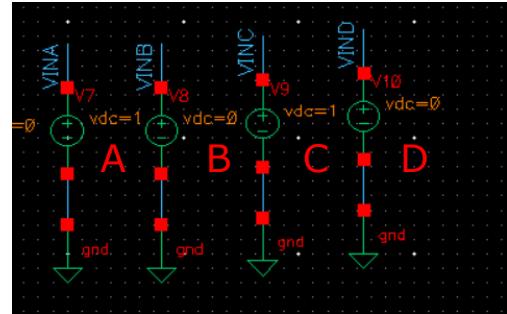
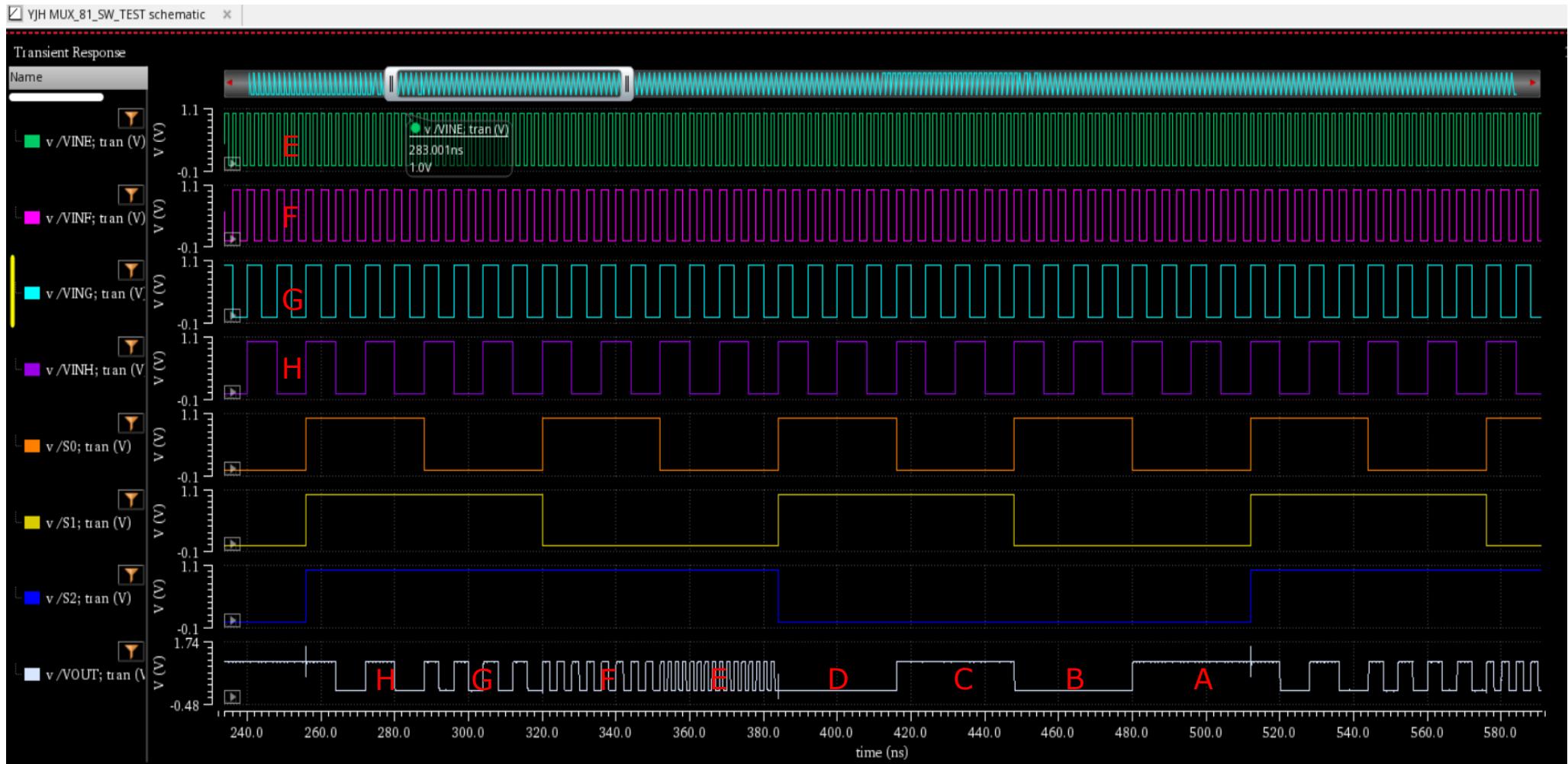


8X1 MUX (LOGIC & SWITCH)



Simulation

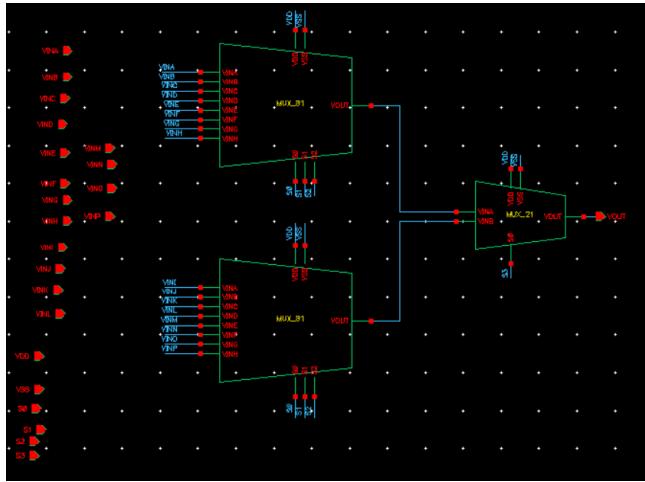
Logic
&
Switch



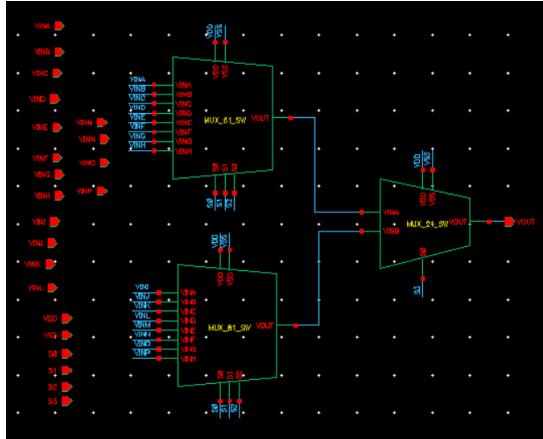
16X1 MUX (LOGIC & SWITCH)



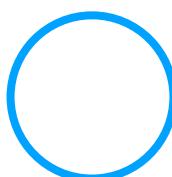
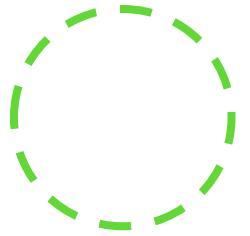
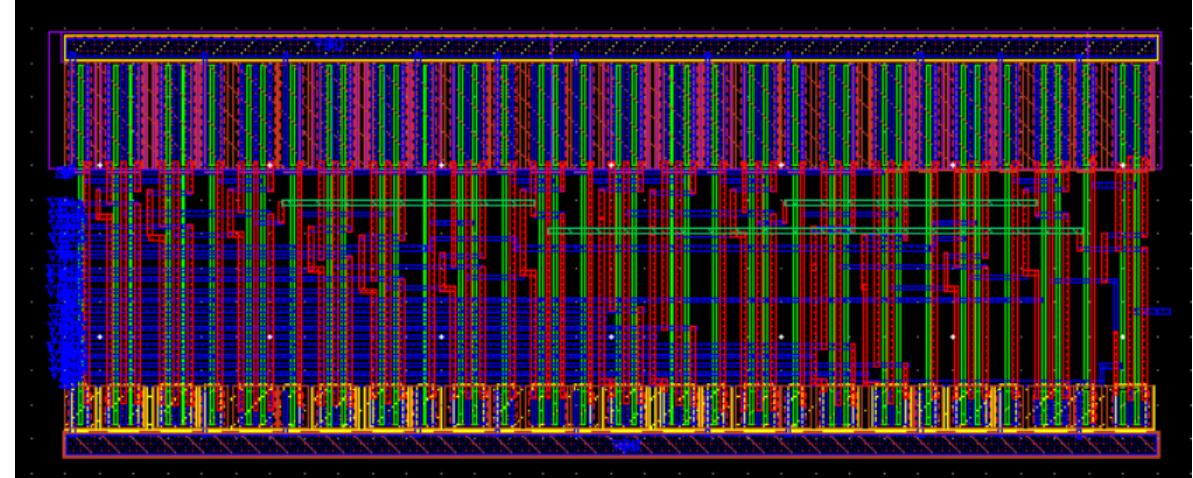
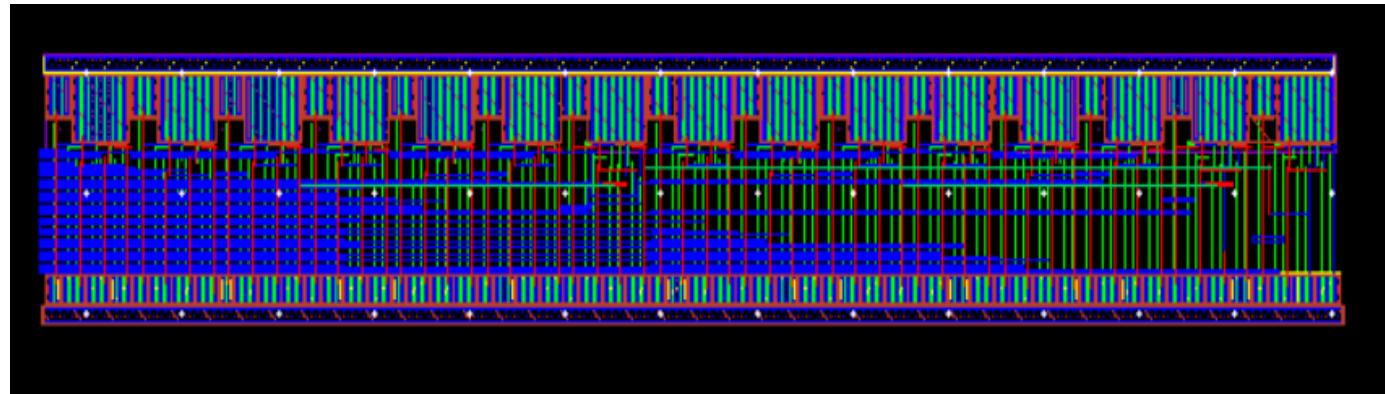
Logic



Switch



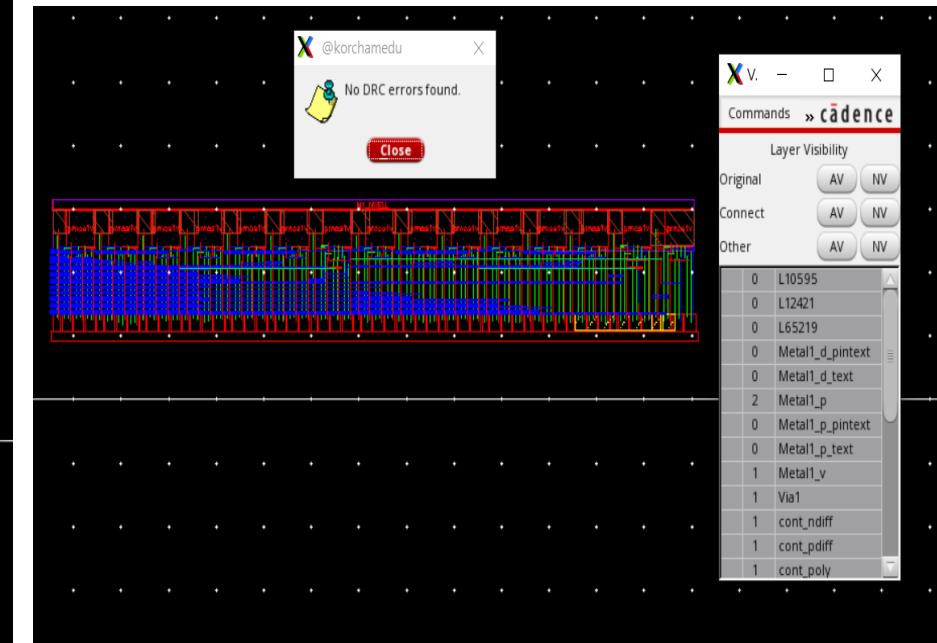
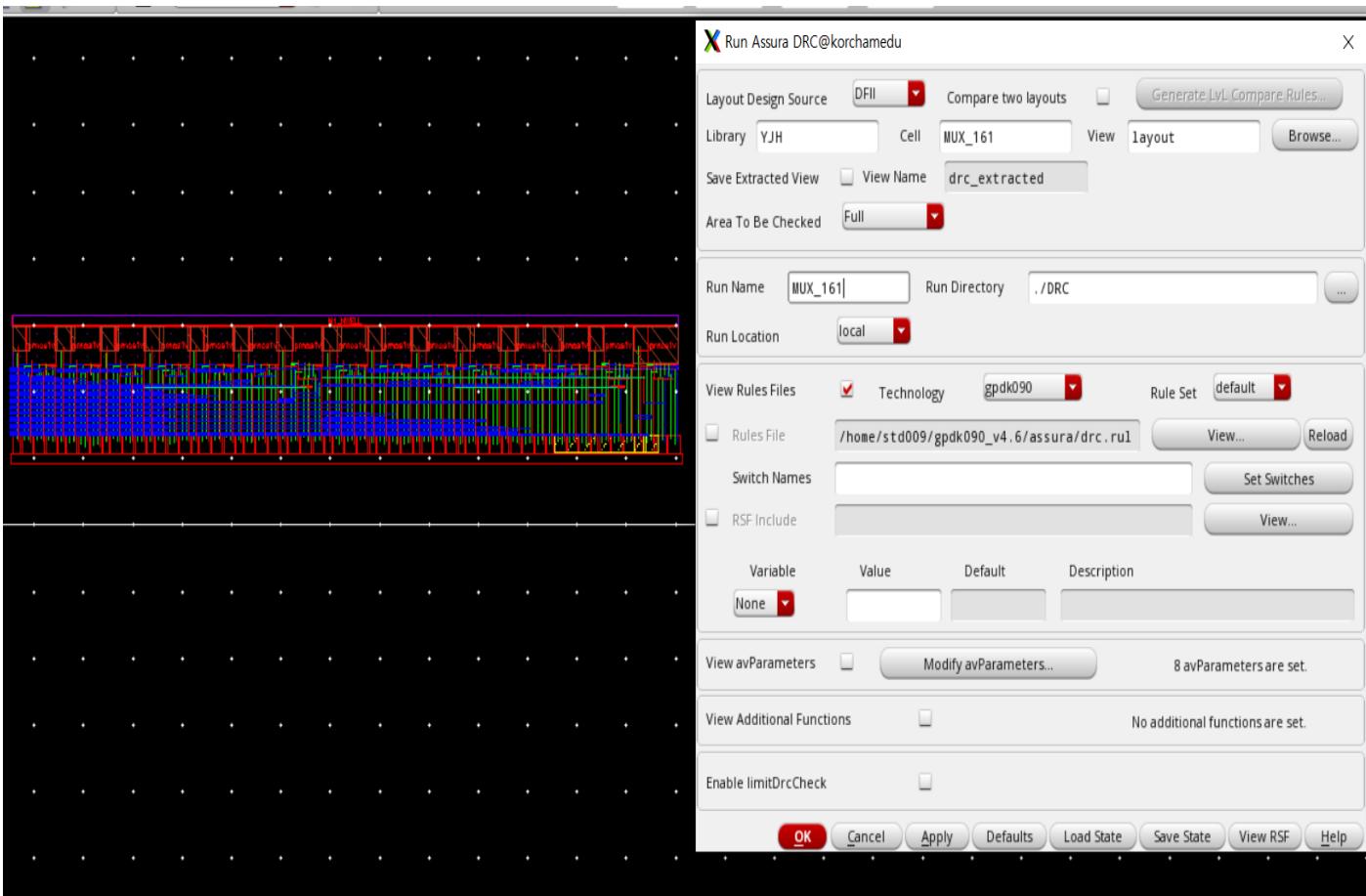
Layout



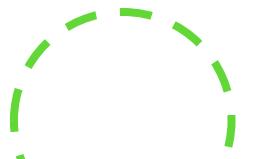
16X1 MUX (LOGIC & SWITCH)

DRC

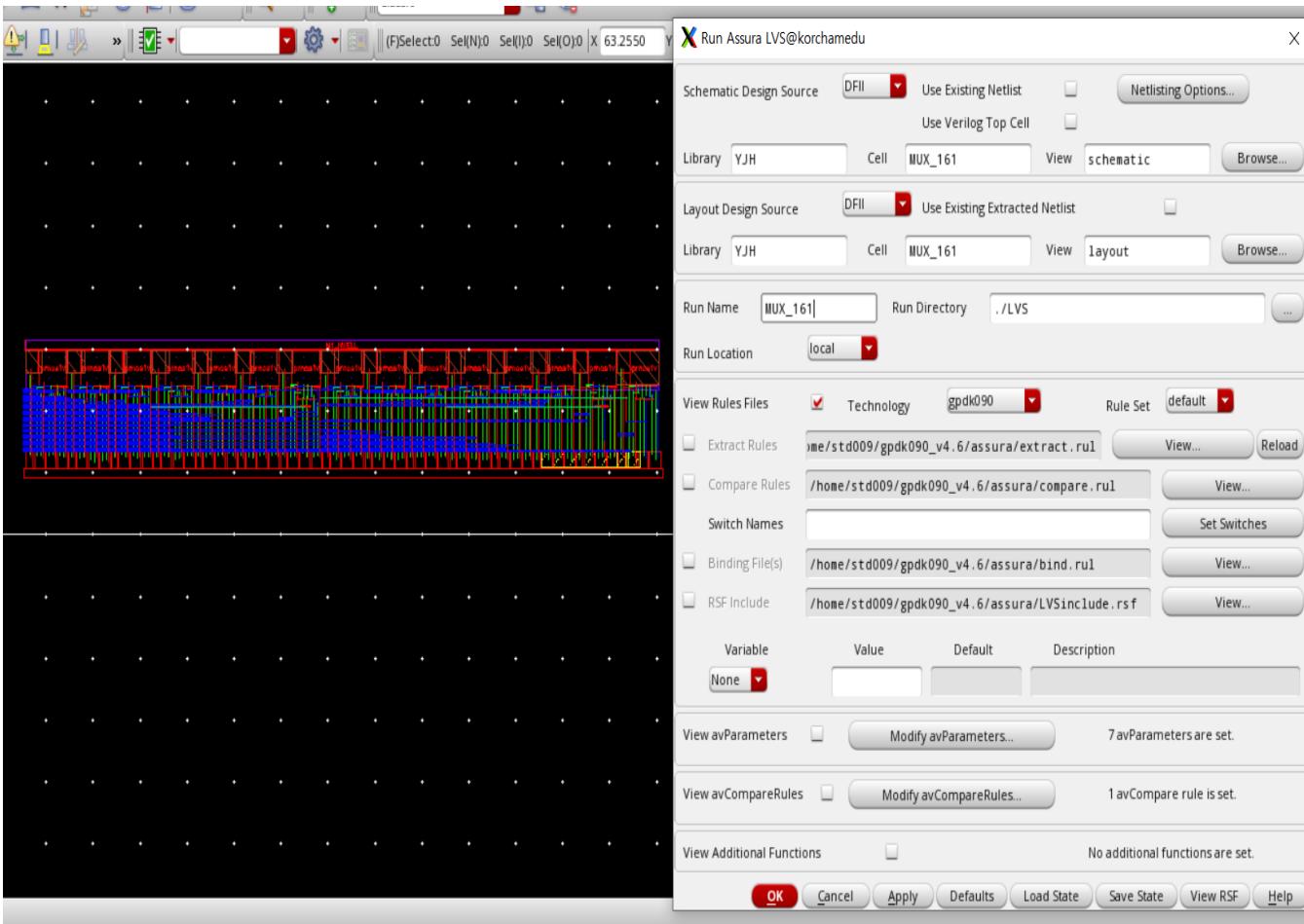
Logic



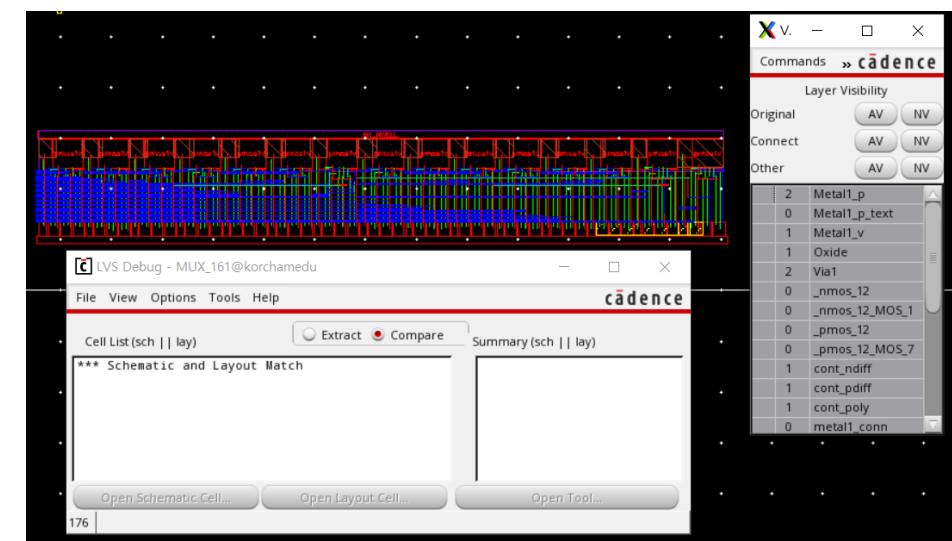
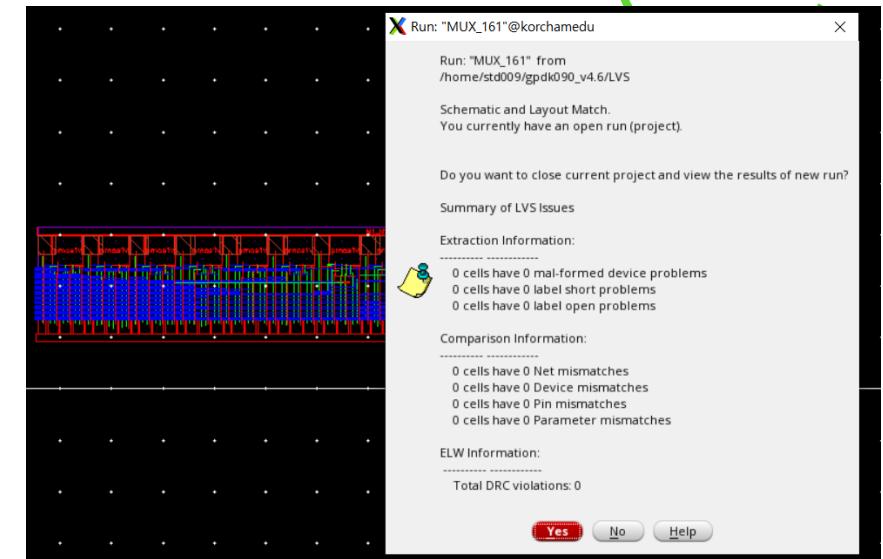
16X1 MUX (LOGIC & SWITCH)



LVS



Logic

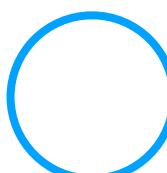
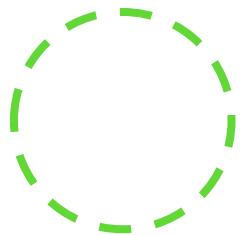


MUX (LOGIC & SWITCH)

Area	2X1 MUX	4X1 MUX	8X1 MUX	16X1 MUX
LOGIC (μm^2)	30.9353	101.7603	276.3482	758.5501
SWITCH (μm^2)	20.8030	46.7775	159.951	405.1853
Ratio	1.4871	2.1754	1.7277	1.8721

TR	31 / 5000 2X1 MUX	4X1 MUX	8X1 MUX	16X1 MUX
LOGIC (unit)	14	42	98	210
SWITCH (unit)	6	16	38	78

It can be used efficiently due to its small area and number of transistors.



ADDER

HALF_ADDER

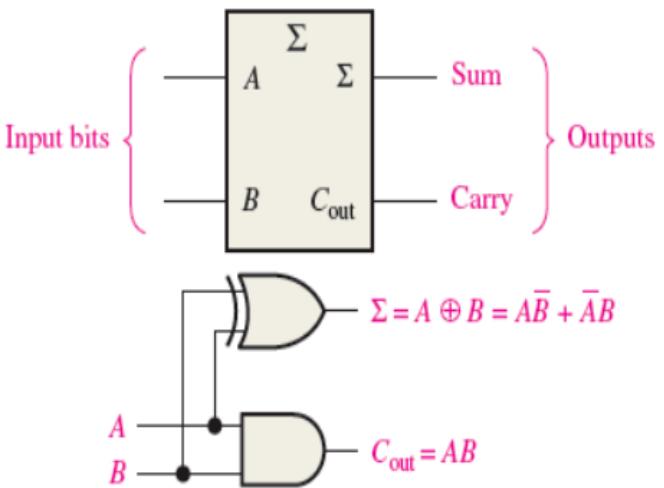
Half-adder truth table.

A	B	C_{out}	Σ
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

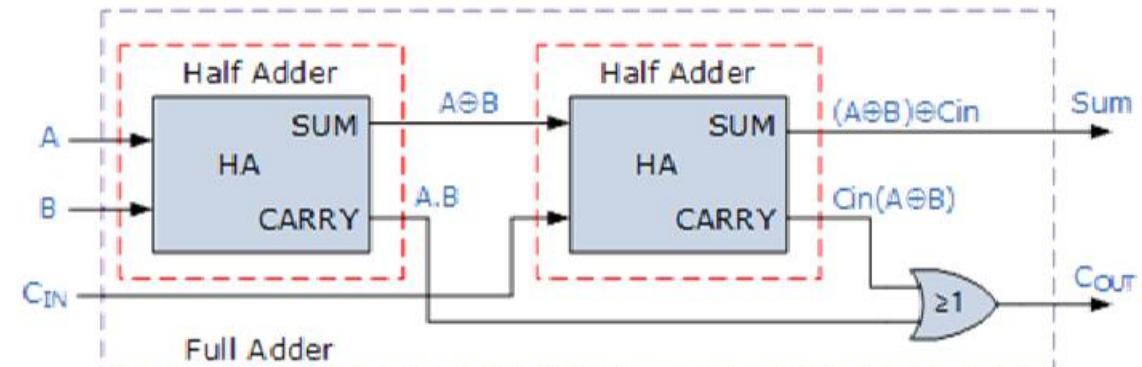
Σ = sum

C_{out} = output carry

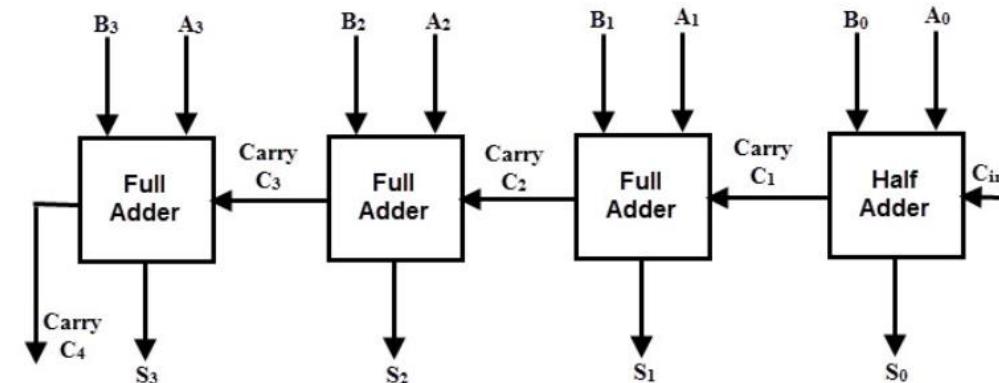
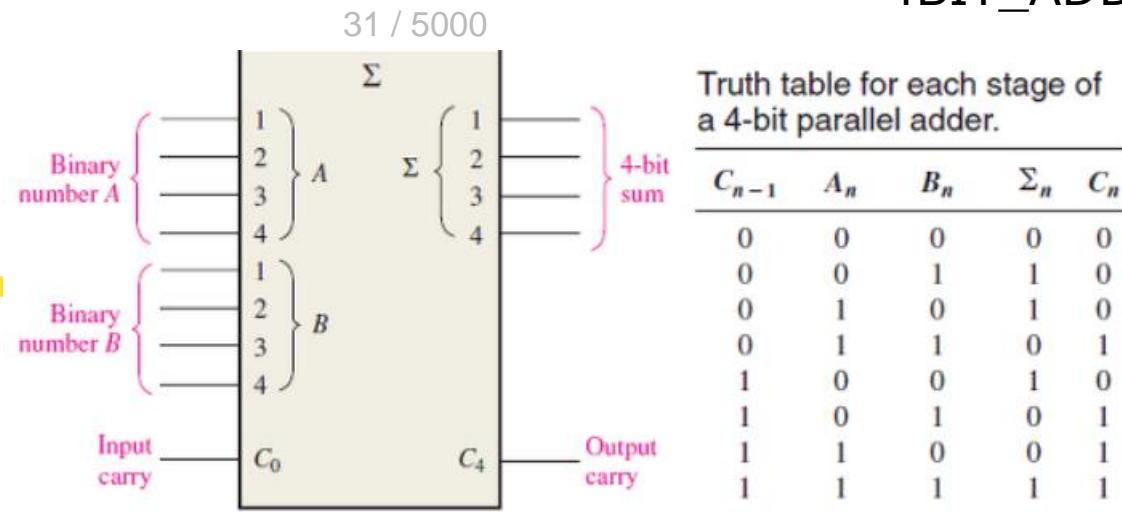
A and B = input variables (operands)



FULL_ADDER

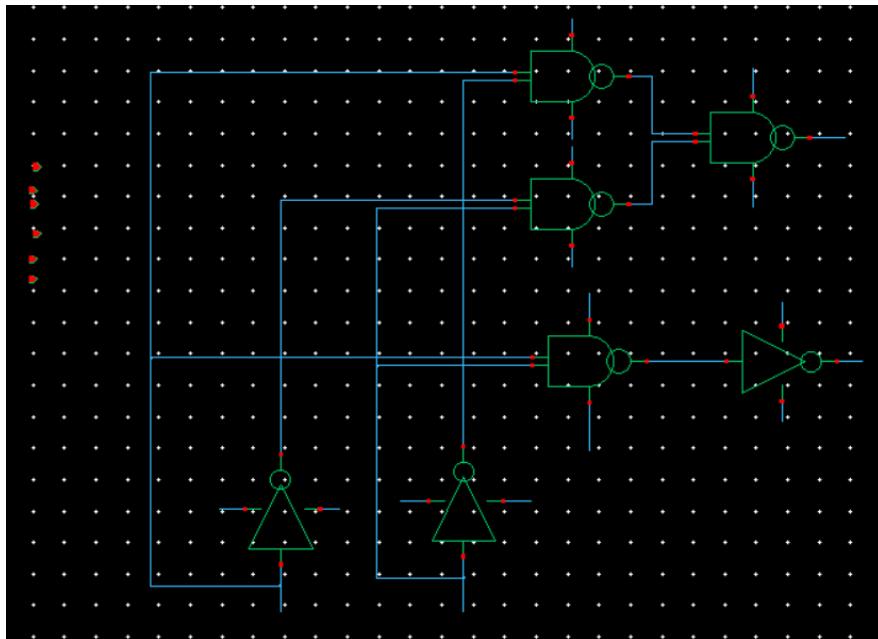


4BIT_ADDER

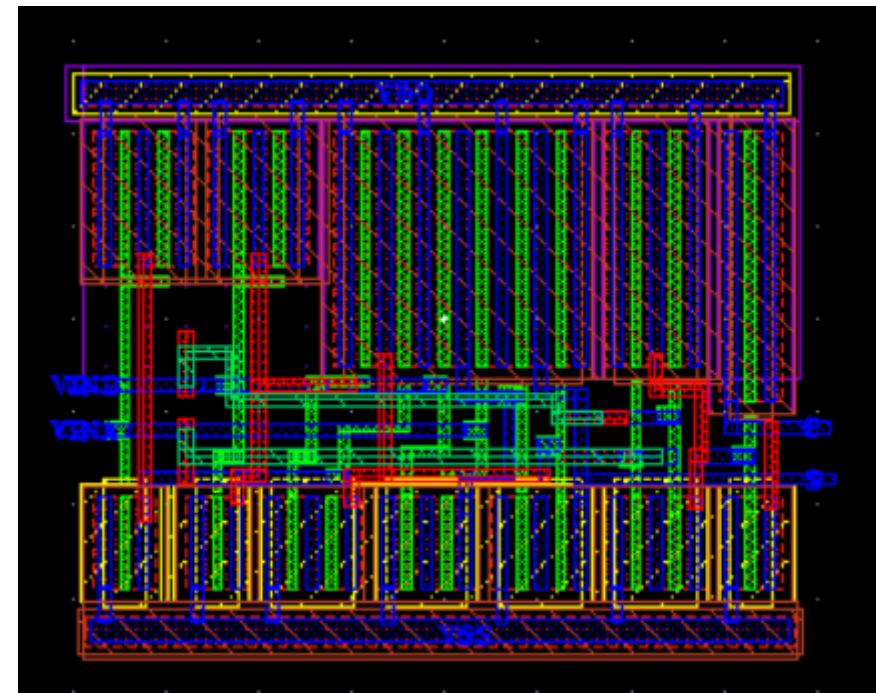


HALF_ADDER

Schematic



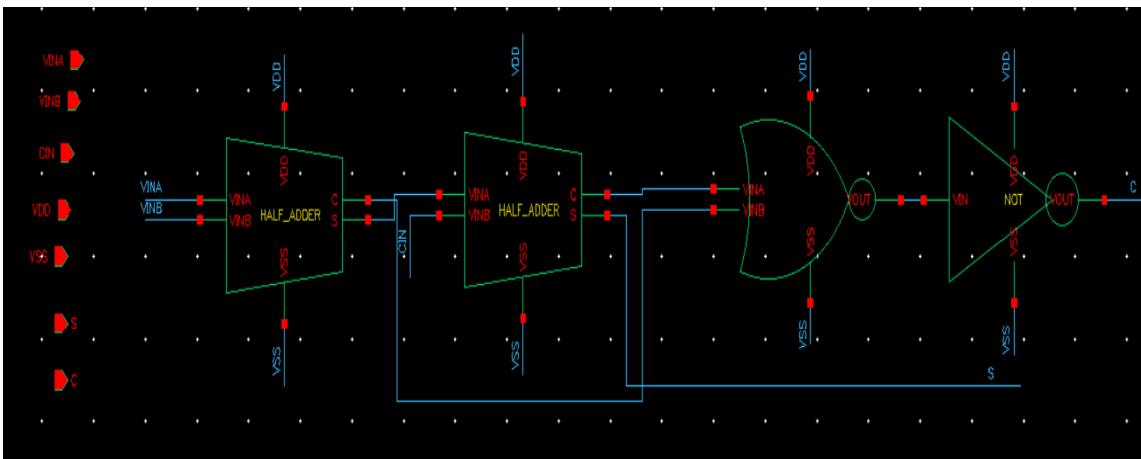
Layout



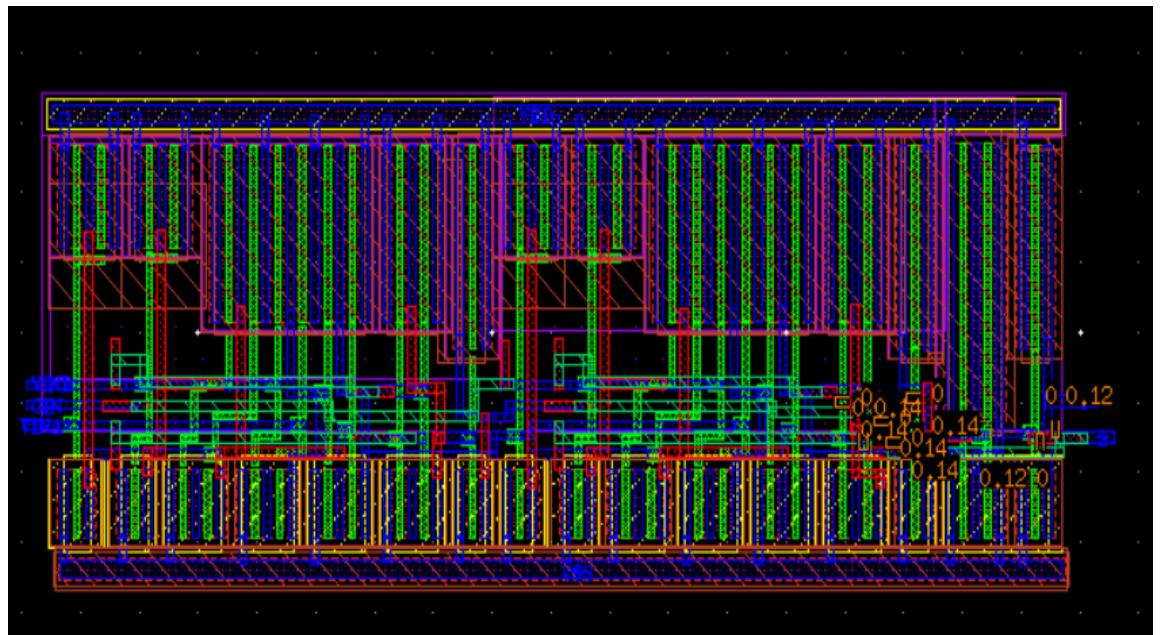
$$\text{Area}(\mu\text{m}^2) = 7.91 \times 6.38 = 50.4658$$

FULL_ADDER

Schematic

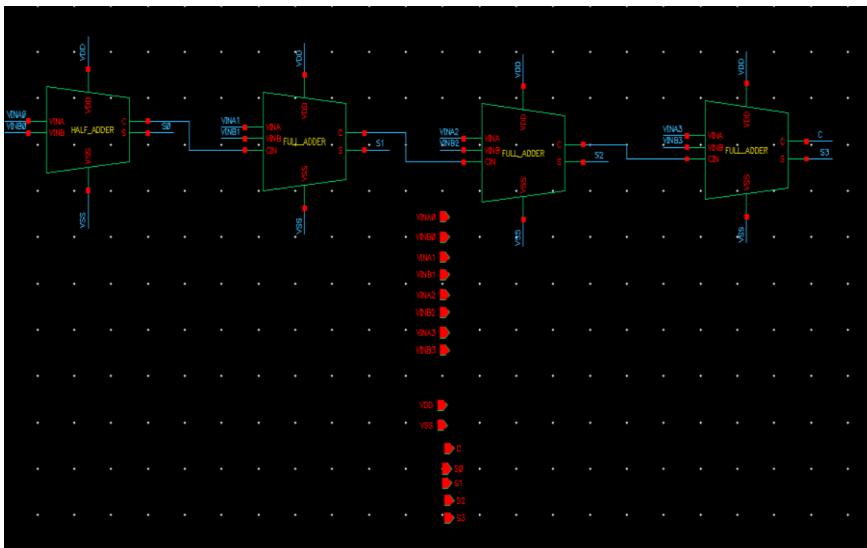


Layout



$$\text{Area}(\mu\text{m}^2) = 17.48 \times 7.105 = 124.1954$$

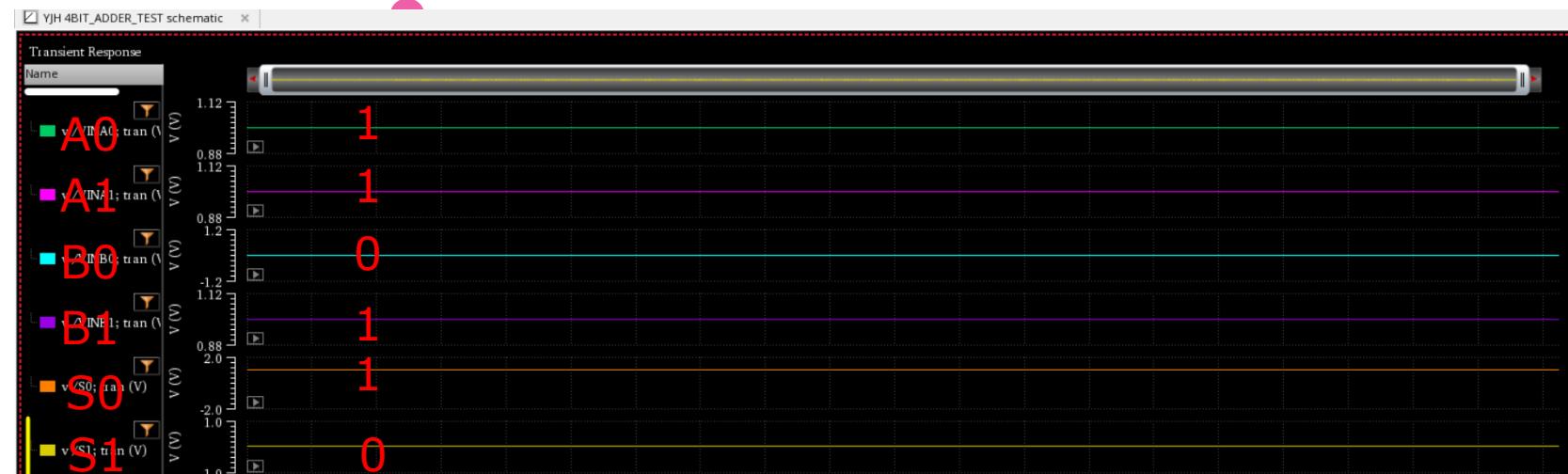
4BIT_ADDER



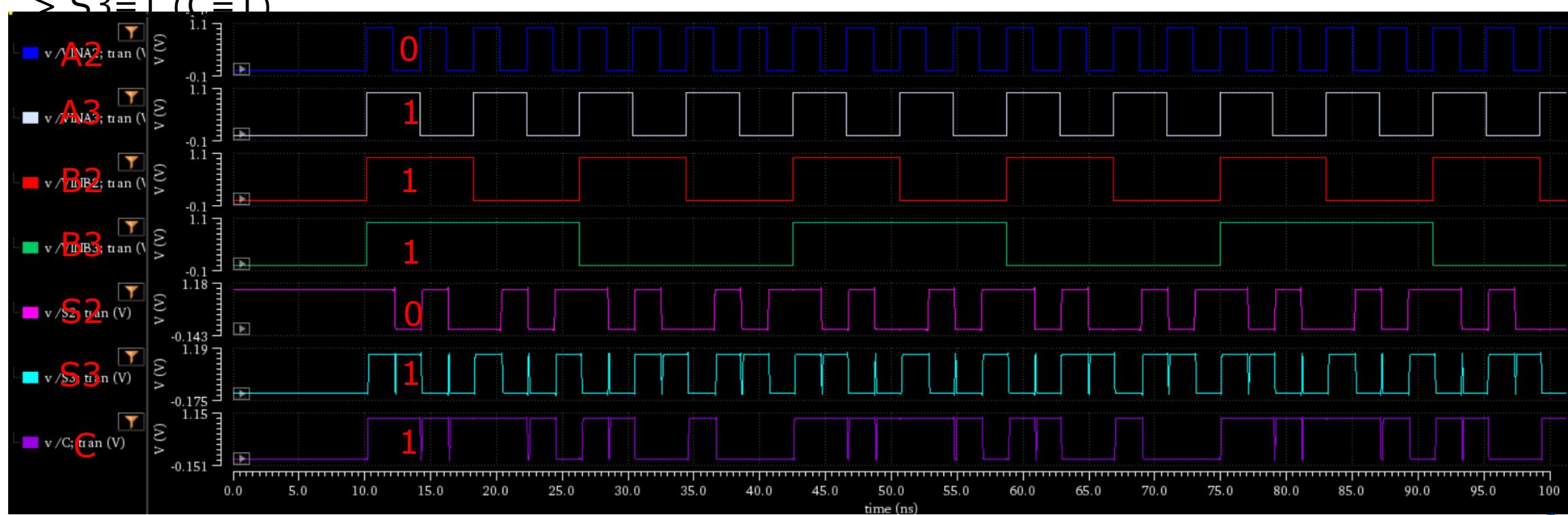
Schematic

4BIT_ADDER

Simulation

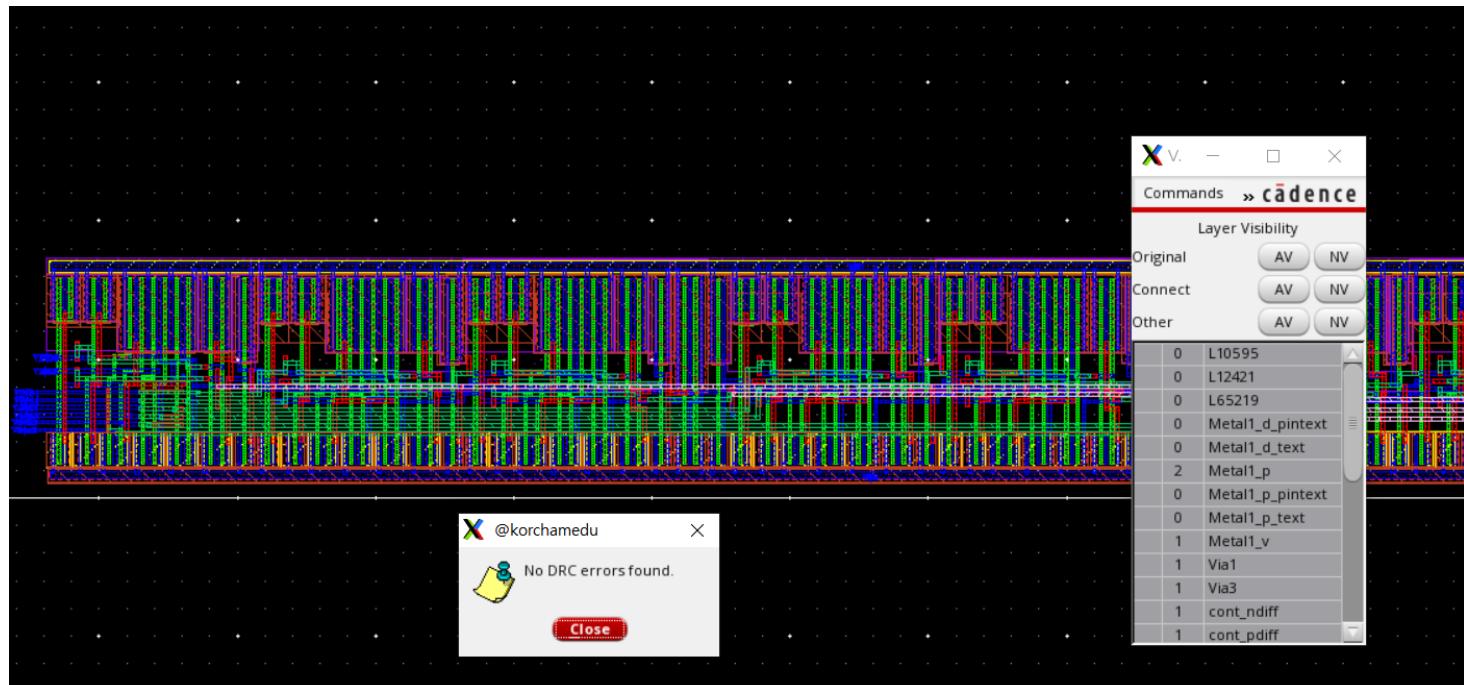
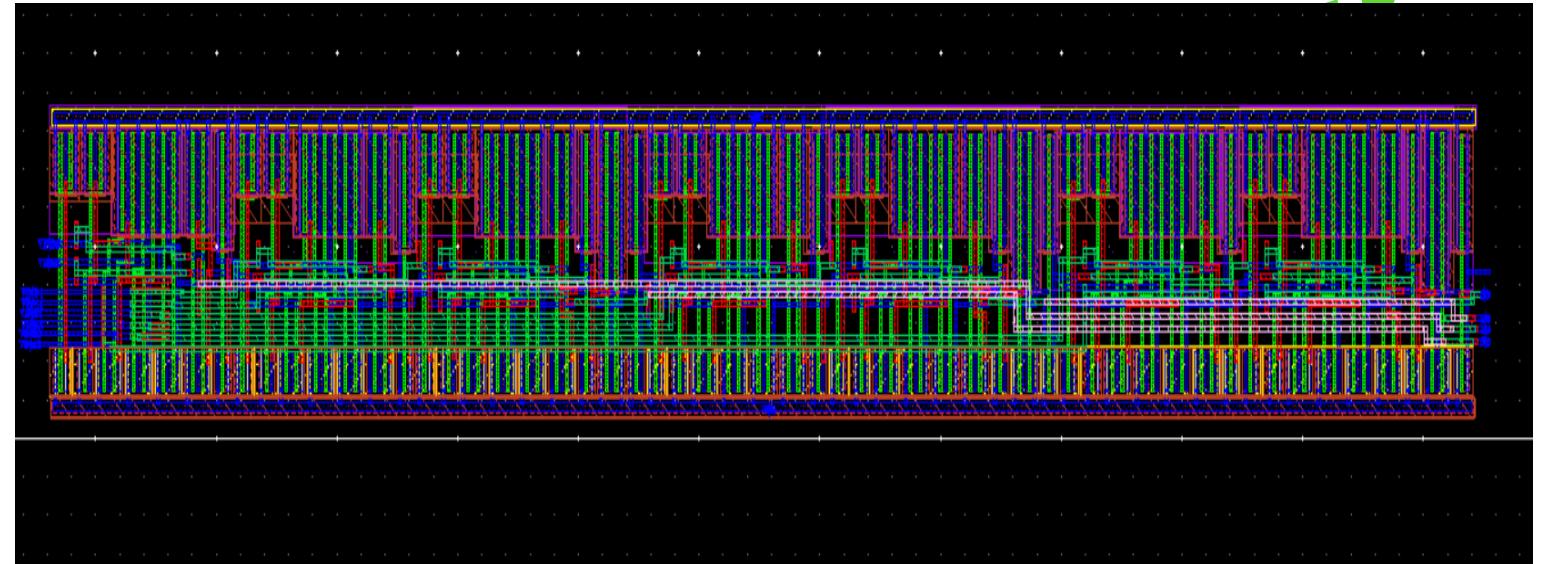


$A_0 + B_0 \rightarrow S_0 = 1$ $A_1 + B_1 \rightarrow S_1 = 0$ ($C_1 = 1$) $A_2 + B_2 + (C_1) \rightarrow S_2 = 0$ ($C_2 = 1$) $A_3 + B_3 + (C_2) \rightarrow S_3 = 1$ ($C = 1$)



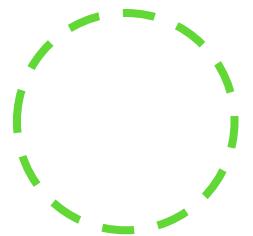
4BIT_ADDER

Layout/DRC

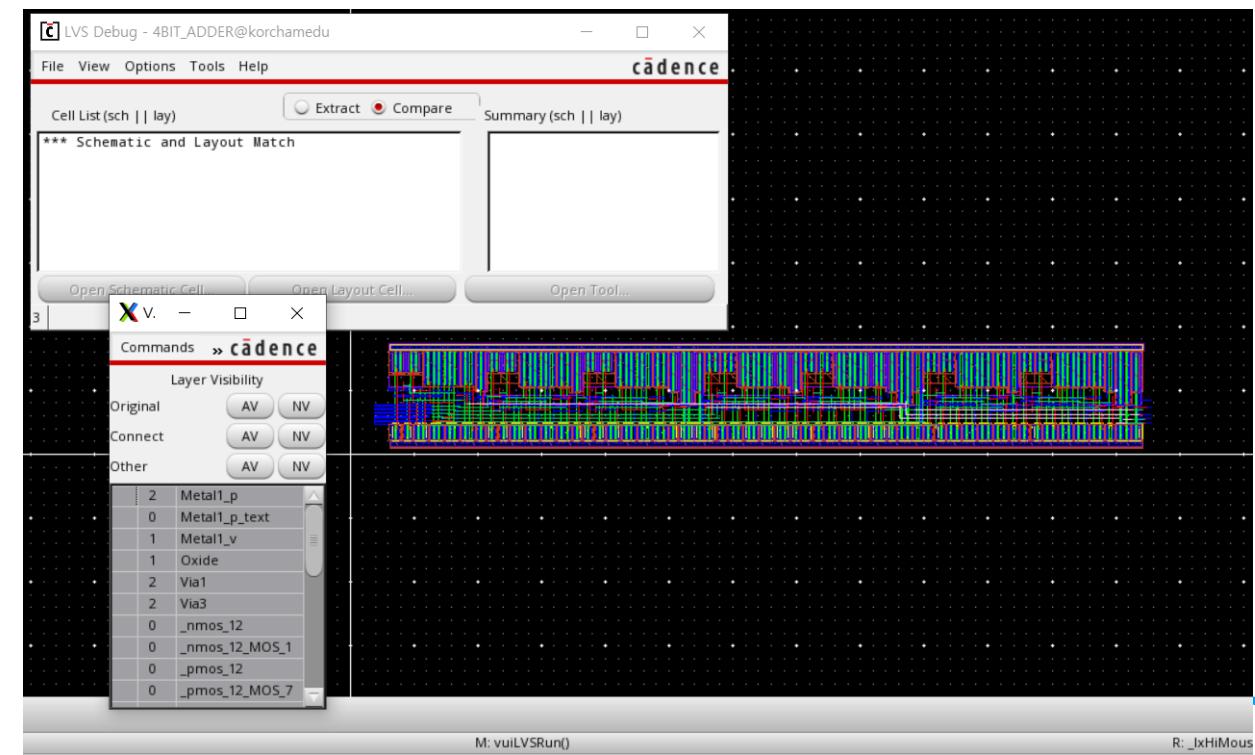
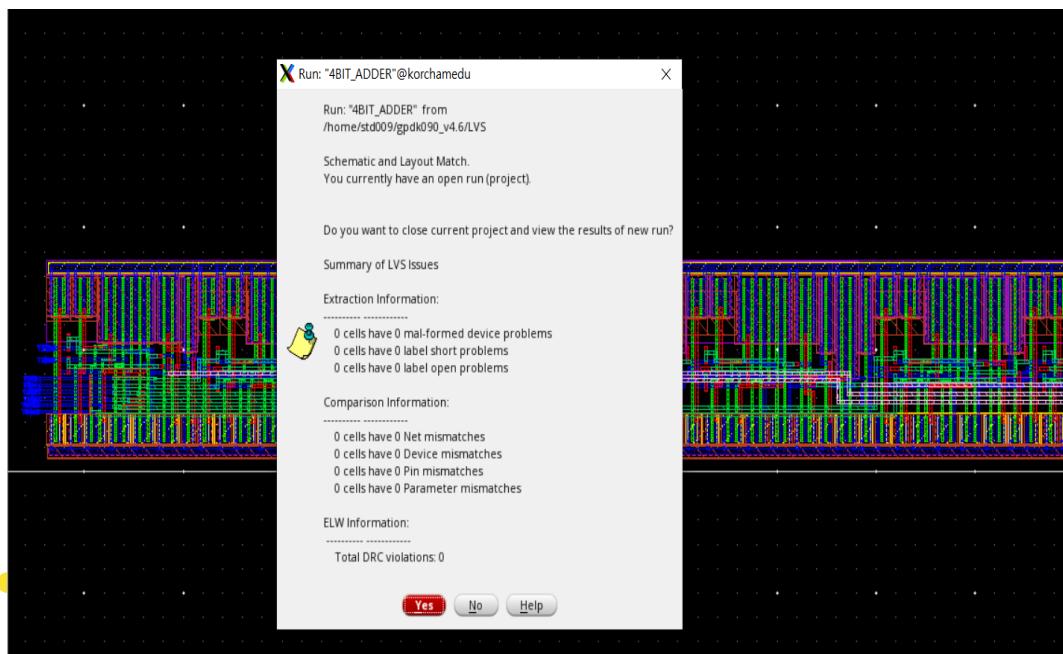


$$\text{Area}(\mu\text{m}^2) = 59.14 \times 8.165 = 482.8781$$

4BIT_ADDER



LVS

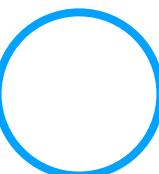
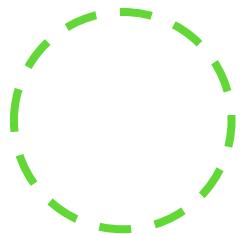


R: JxHiMous



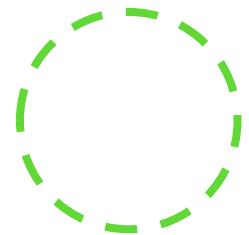
ANALOG CIRCUIT

- Common Source Amp / Differential Amp (Single-ended Output)



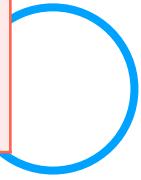


ANALOG CIRCUIT SPEC

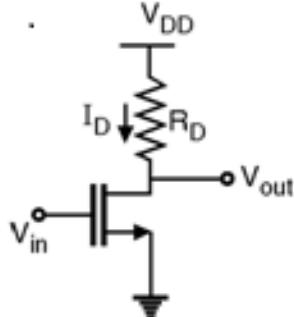
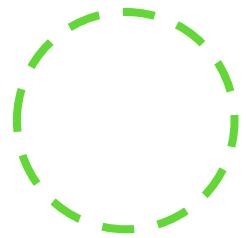


	Res	Nmos0	Nmos1	Nmos2	Nmos3	Pmos0	Pmos1
CS_Amp	4k	1um	x	x	x	x	x
Diff_Amp	25k	2um	2um	800nm	800nm	250nm	250nm

	gm	Gain (Av)	Bandwidth	Power Consumption
CS_Amp	~754.59[uA/V]	6.334[dB]	3.04[GHz]	123.153[uW]
Diff_Amp	~189.955[uA/V]	13.448[dB]	262.271[MHz]	43.469[uW]



COMMON SOURCE AMP



CS stage with resistive load

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2$$

$$\text{i.e. } I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{in} - V_{TH})^2$$

But by KVL,

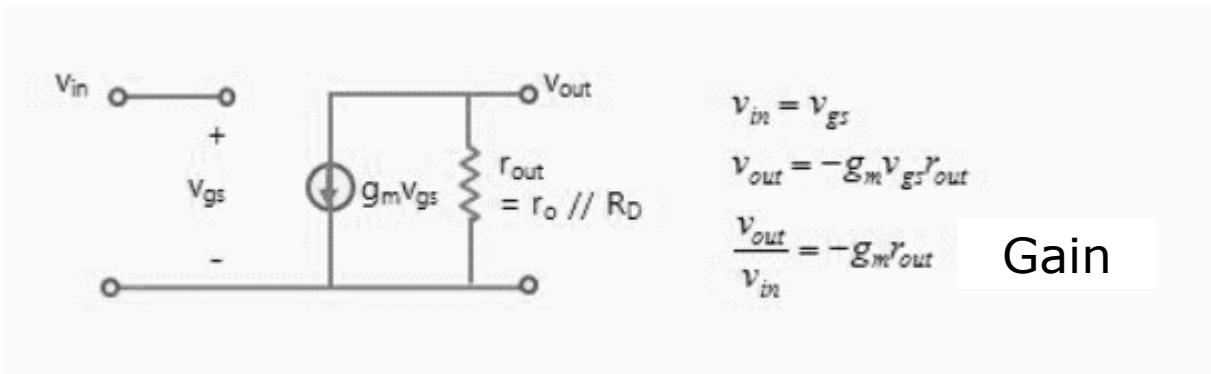
$$V_{DD} - I_D R_D = V_{out}$$

$$\therefore V_{out} = V_{DD} - \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{in} - V_{TH})^2 R_D$$

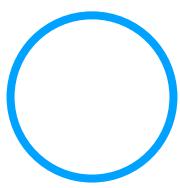
Differentiating this equation with respect to V_{in}

$$\frac{dV_{out}}{dV_{in}} = -\mu_n C_{ox} \frac{W}{L} (V_{in} - V_{TH}) R_D$$

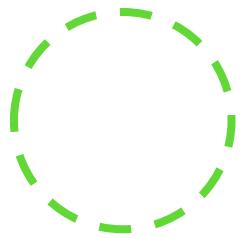
$$\text{Hence, The voltage gain } A_v = -g_m R_D \quad \left[\because g_m = \mu_n C_{ox} \frac{W}{L} (V_{in} - V_{TH}) \right]$$



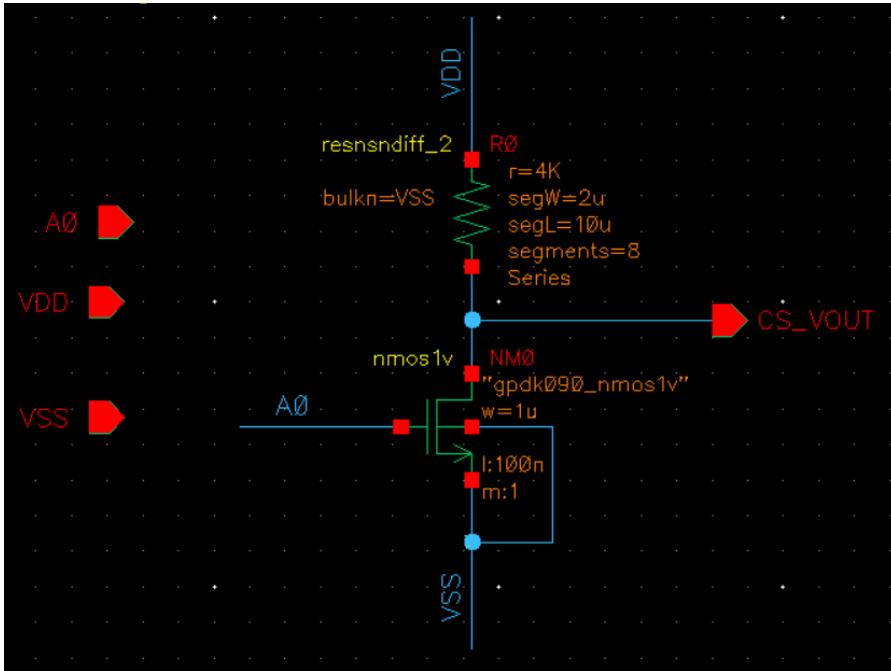
common-source amplifier is one of three basic single-stage field-effect transistor (FET) amplifier topologies, typically used as a voltage or transconductance amplifier.



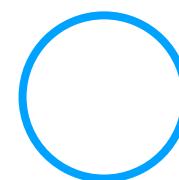
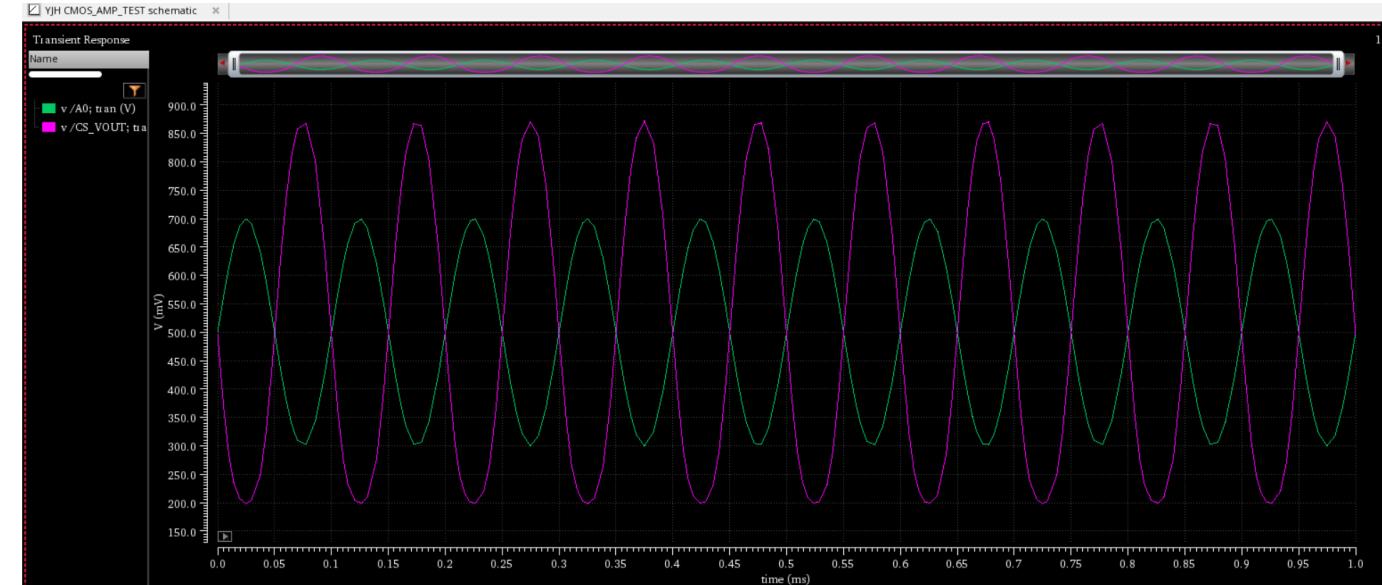
COMMON SOURCE AMP



Schematic

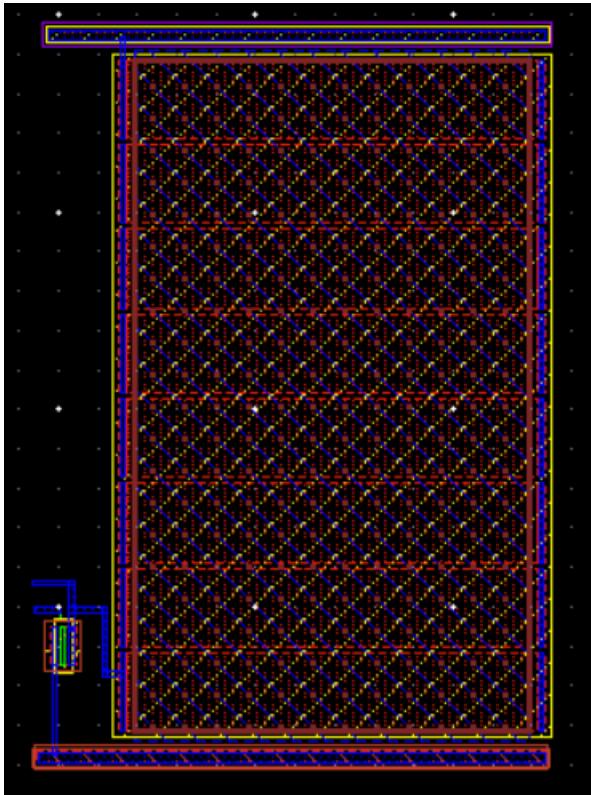


Simulation

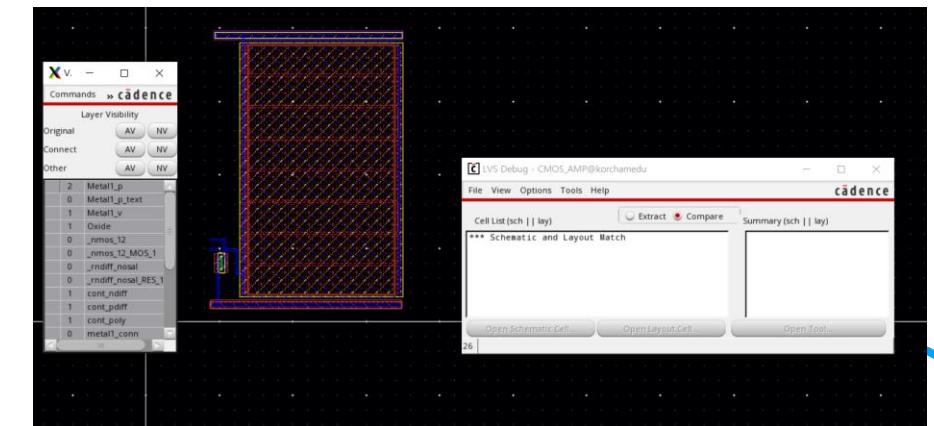
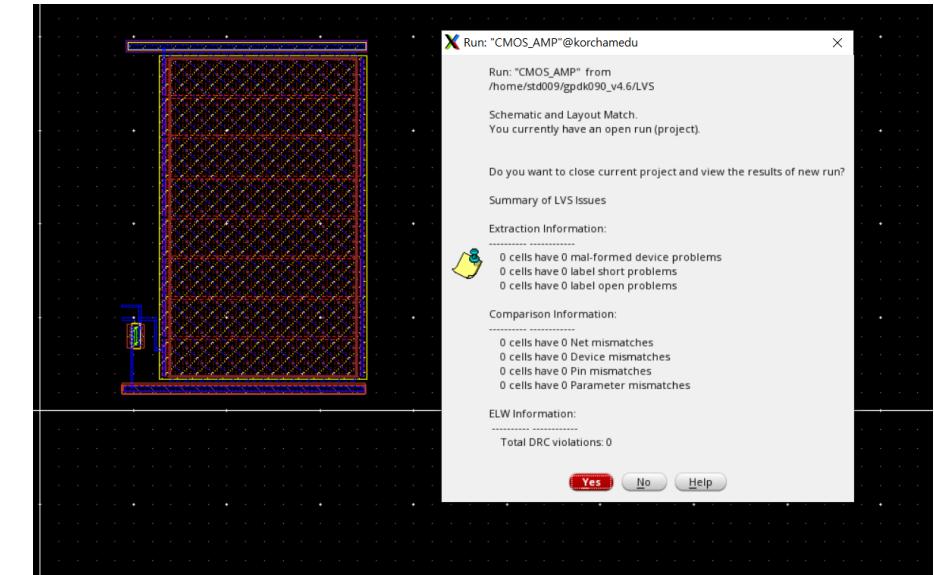
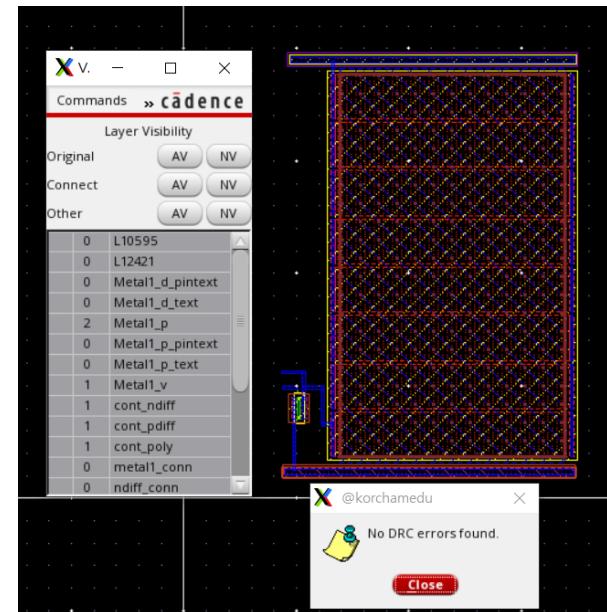


COMMON SOURCE AMP

Layout

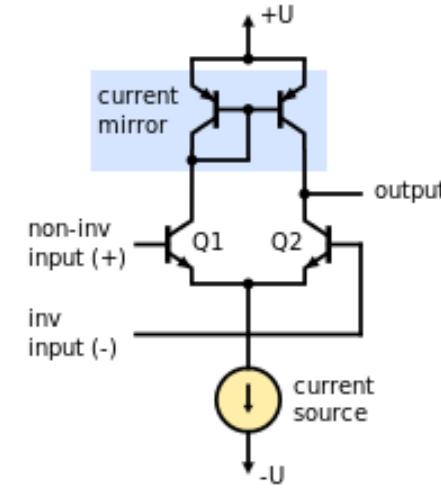
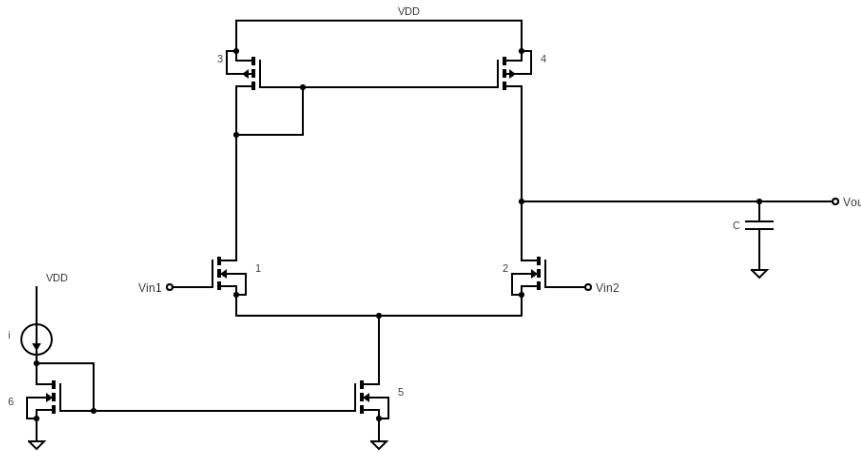
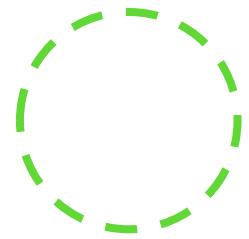


DRC/LVS



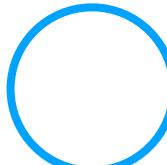


DIFFERENTIAL AMP



- If the differential output is not desired, then only one output can be used (taken from just one of the collectors (or anodes or drains), disregarding the other output; this configuration is referred to as *single-ended output*).

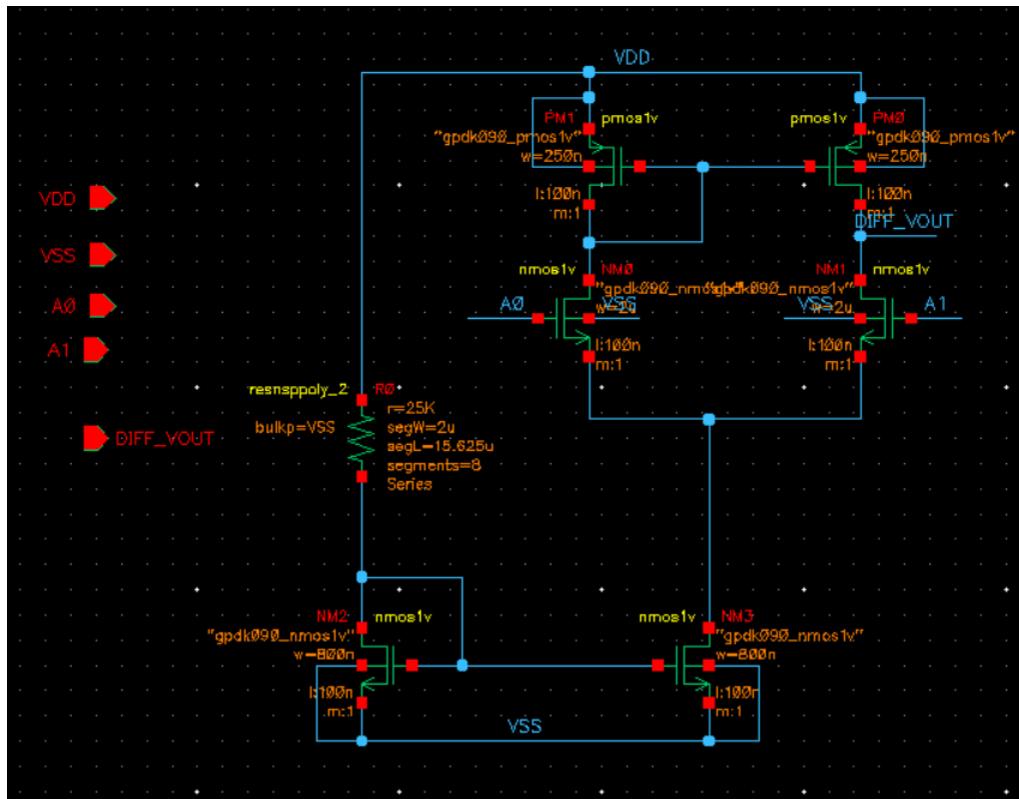
The gain is half that of the stage with differential output.



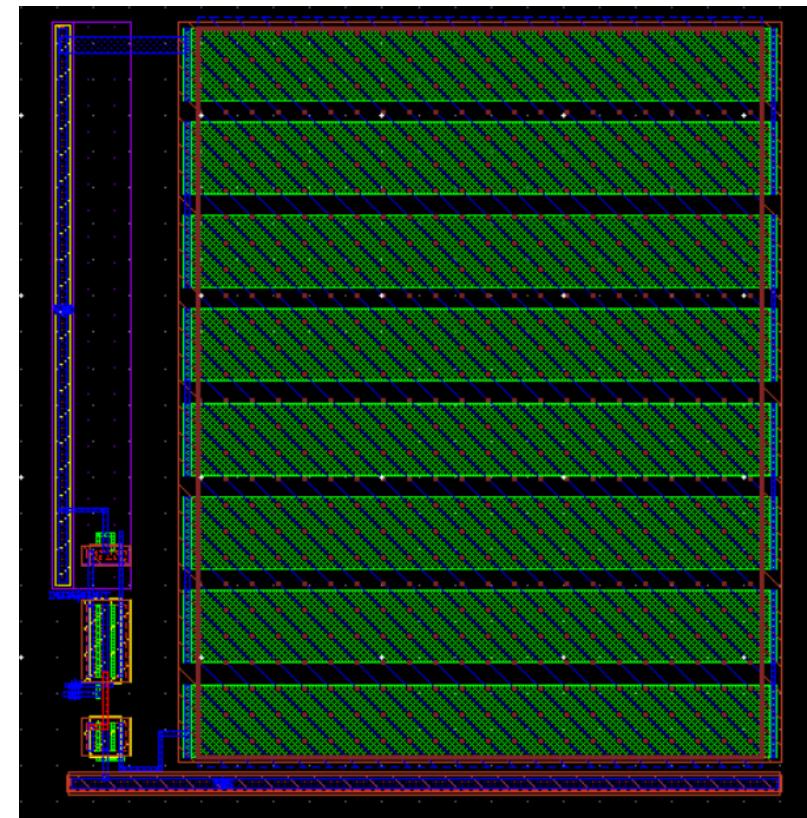
DIFFERENTIAL AMP



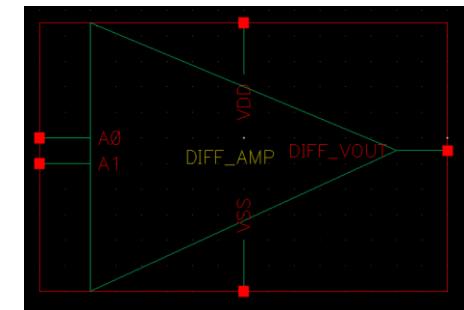
Schematic



Layout

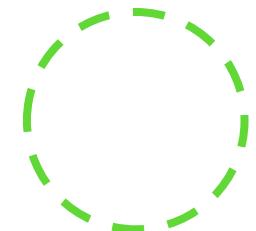


Symbol

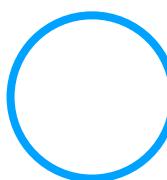
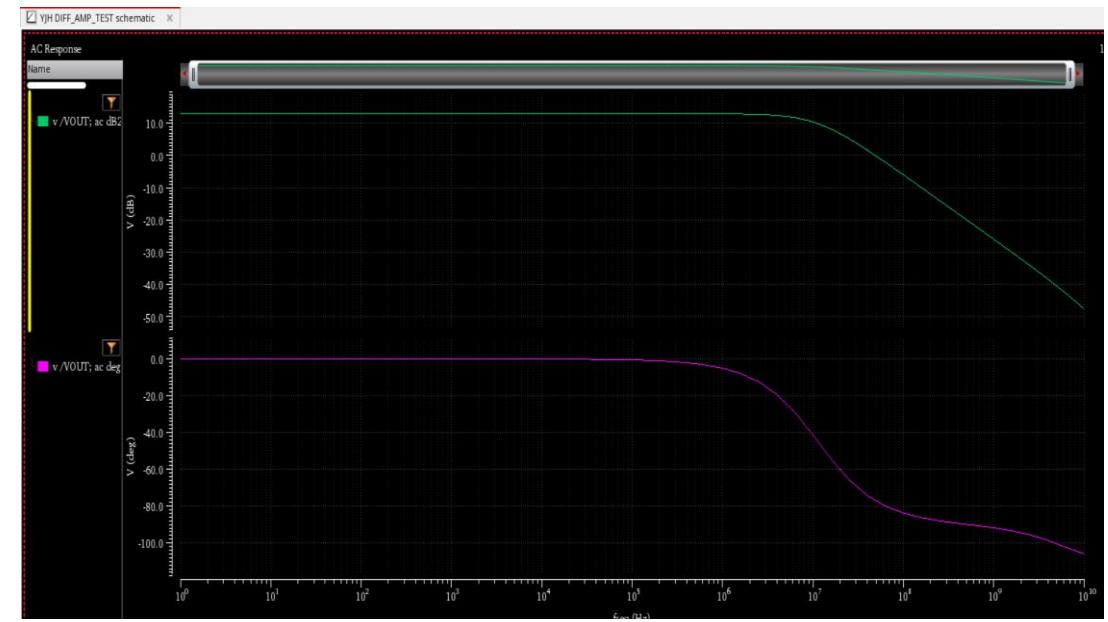
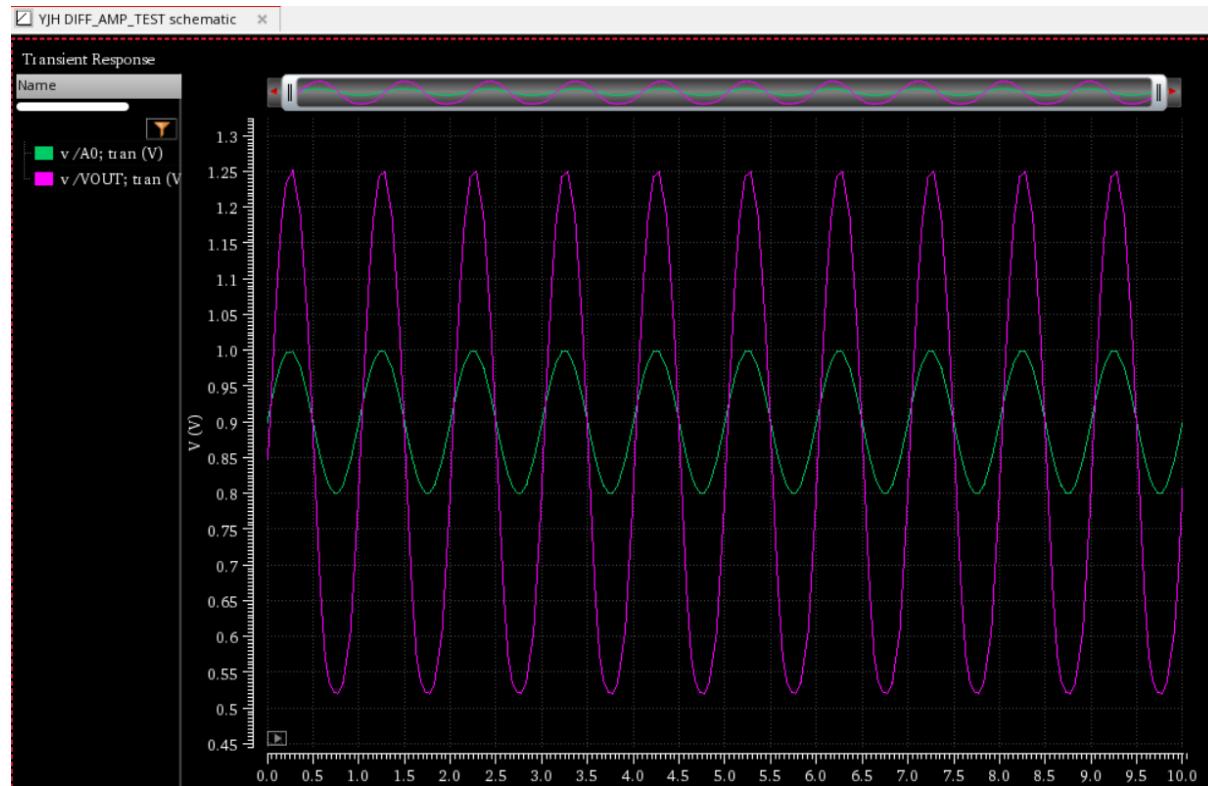




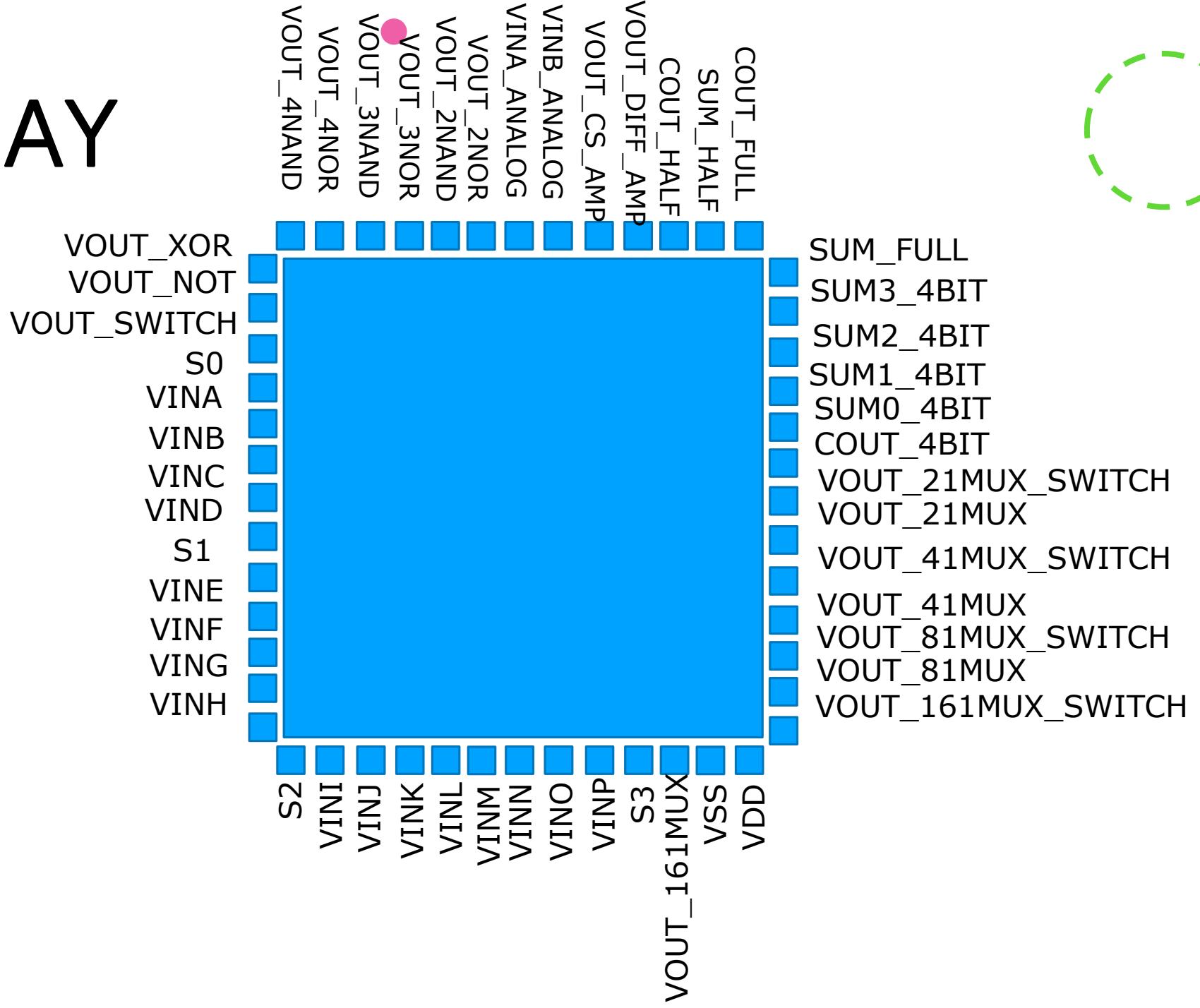
DIFFERENTIAL AMP



Simulation (TRAN./AC)

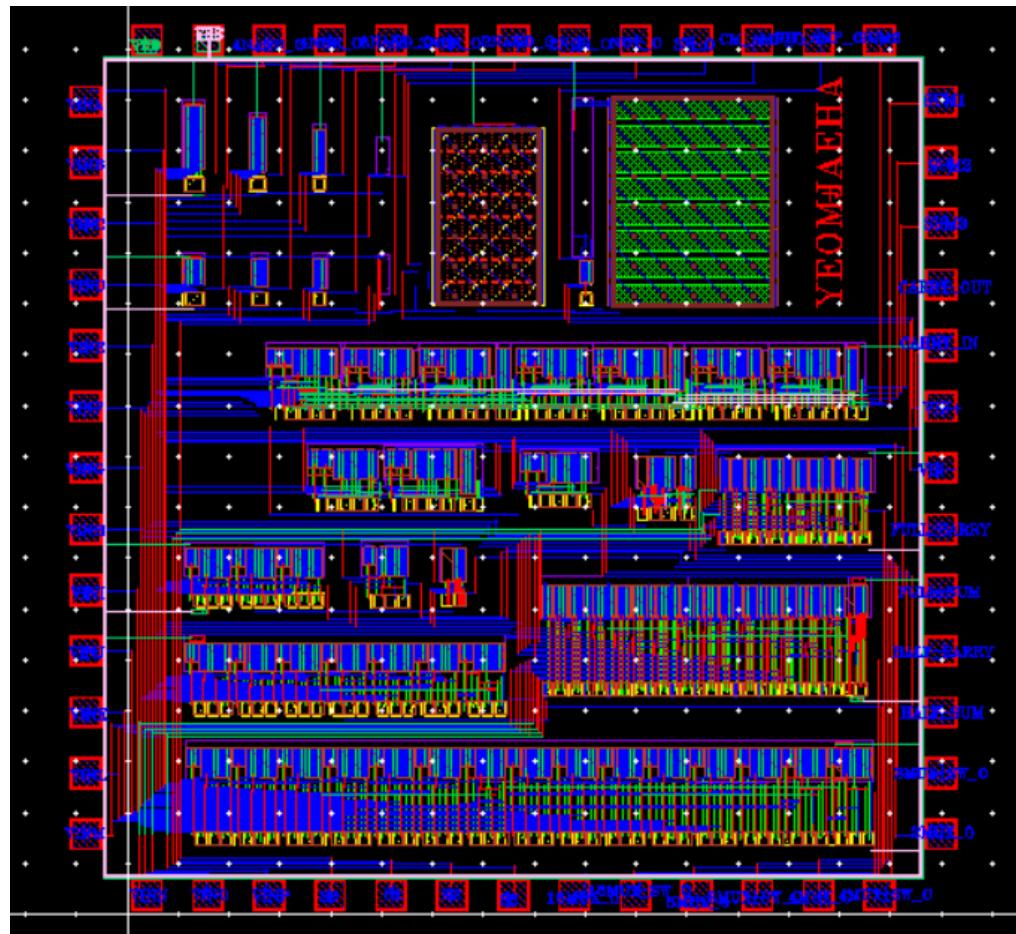


PIN ARRAY

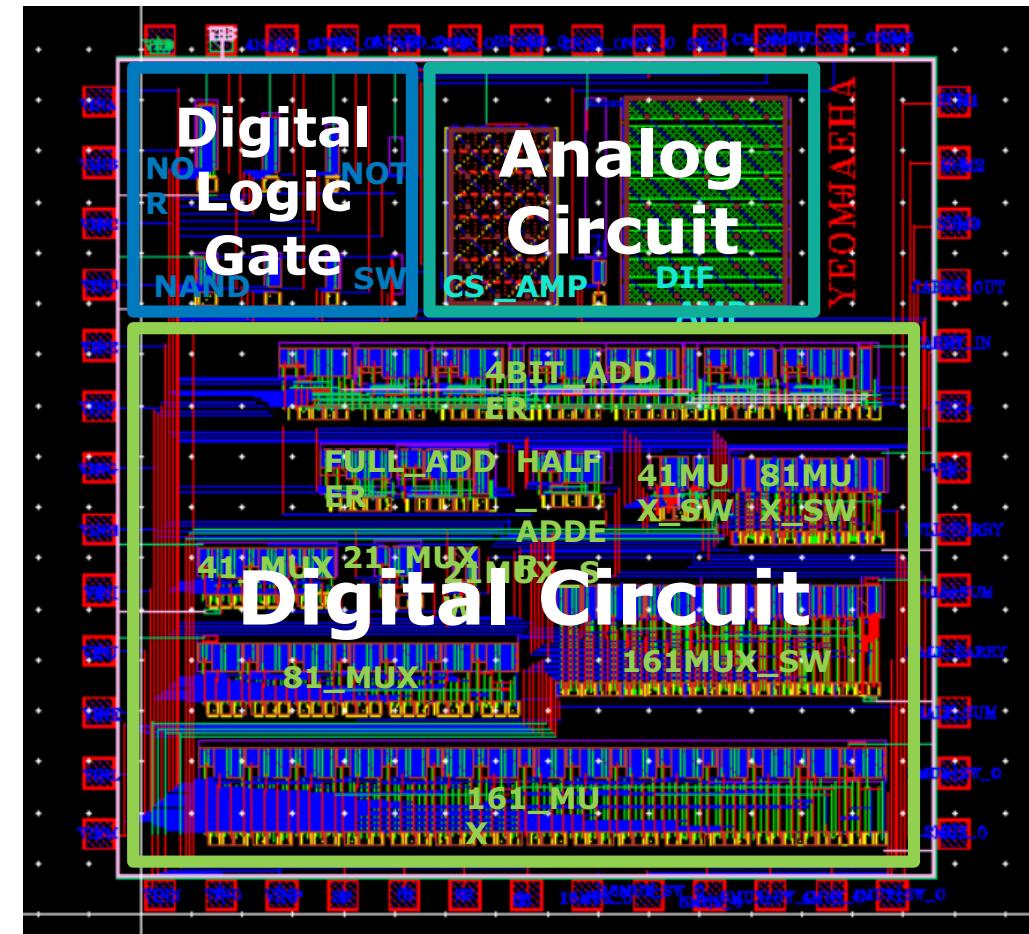
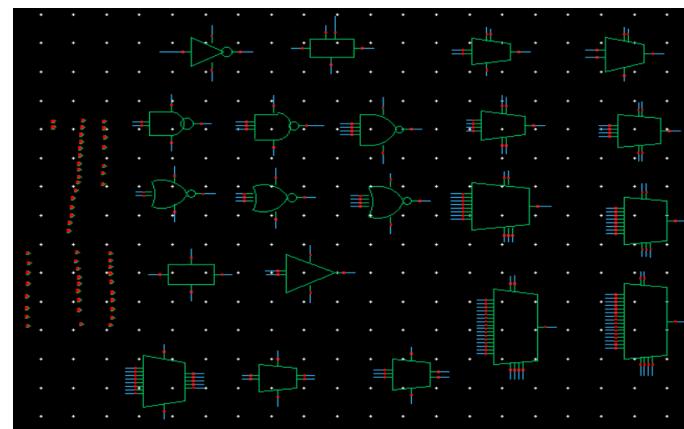


ONE CHIP

Layout



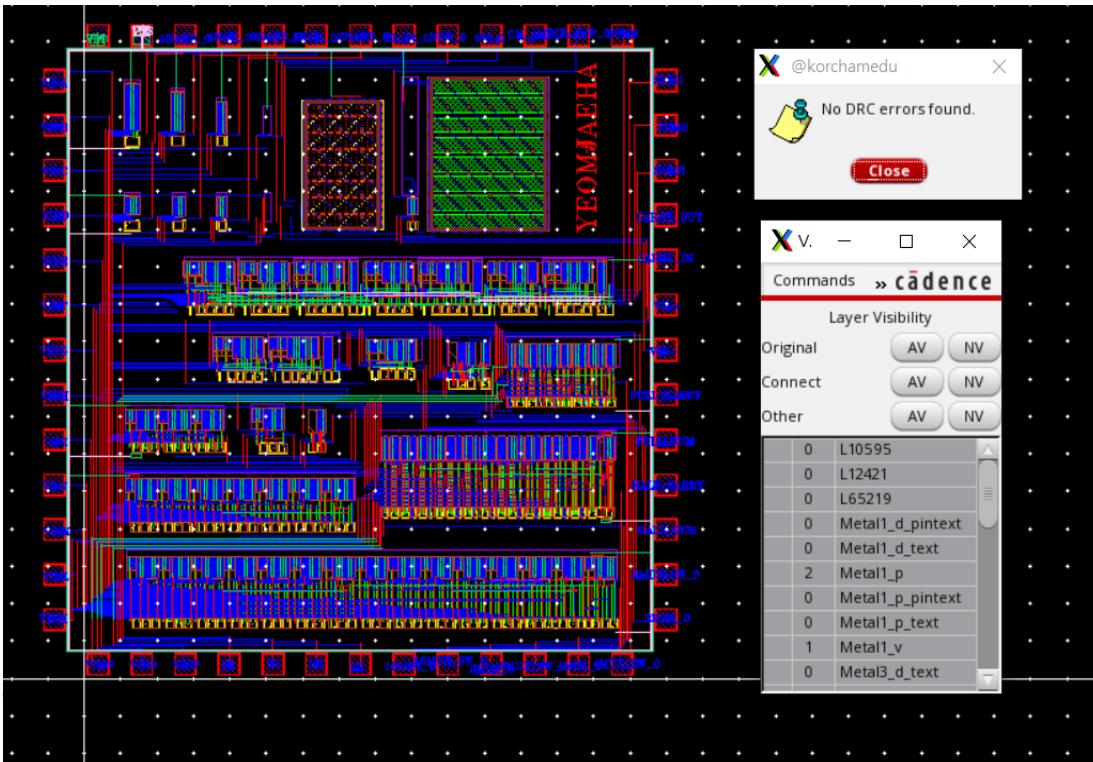
Schematic



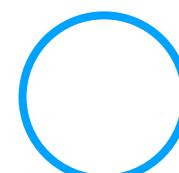
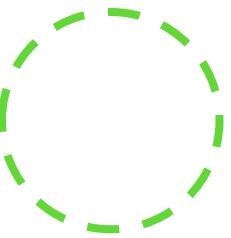
ONE CHIP



DRC

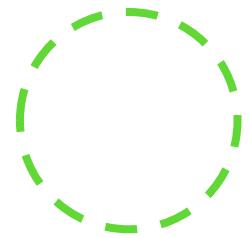


LVS





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