
Cadence
Full-Custom IC Design

One chip Design

BS. Junho PARK

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Program & Tool

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Digital Circuits & Analog Circuits
Schematic/Simulation/Layout/DRC/LVS

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One Chip

PROGRAM & TOOL

1

Cadence Virtuoso Schematic Editor / Layout Editor

2

Cadence Virtuoso Spectre / ADE

3

Assura (DRC & LVS)

3

GPDK090

DIGITAL CIRCUITS & ANALOG CIRCUITS

001

- NOT / SWITCH / XOR
- 2NAND / 3NAND / 4NAND
- 2NOR / 3NOR / 4NOR

Digital Logic Gates

002

- 2x1, 4x1, 8x1, 16x1 MUX (Difference Logic & Switch)
- HALF_ADDER / FULL_ADDER / 4BIT_ADDER / 4BIT_SUBTRACTOR

Digital Circuits

003

- Common Source Amp / Differential Amp (Single-ended Output)

Analog Circuits

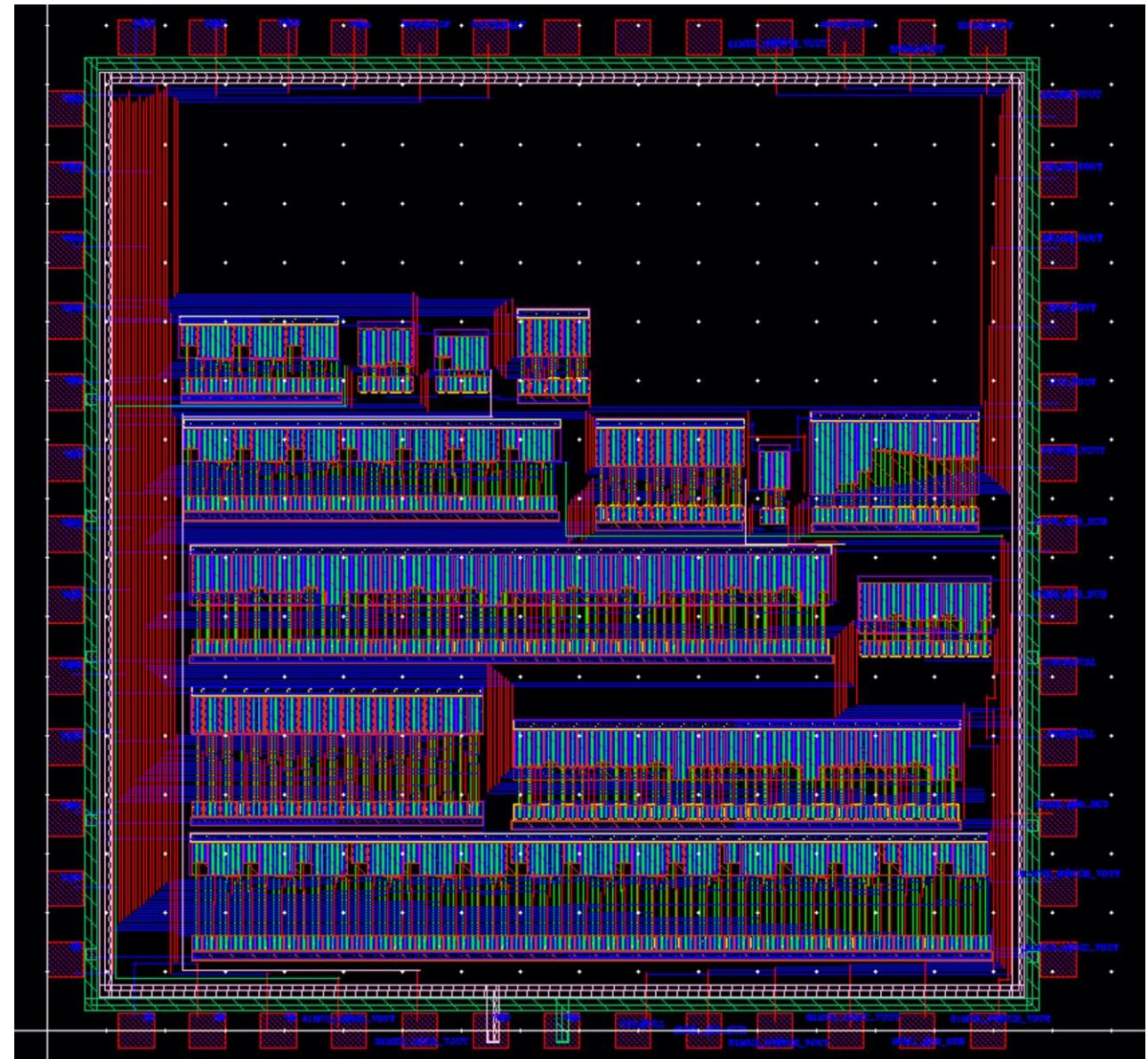
004

- Digital Logic Gates + Digital Circuits + Analog Circuits + PAD Frame

One Chip

ONE CHIP

One Chip Design



DITIGAL LOGIC GATE

1

NOT/SWITCH

2

2NAND/3NAND/4NAND

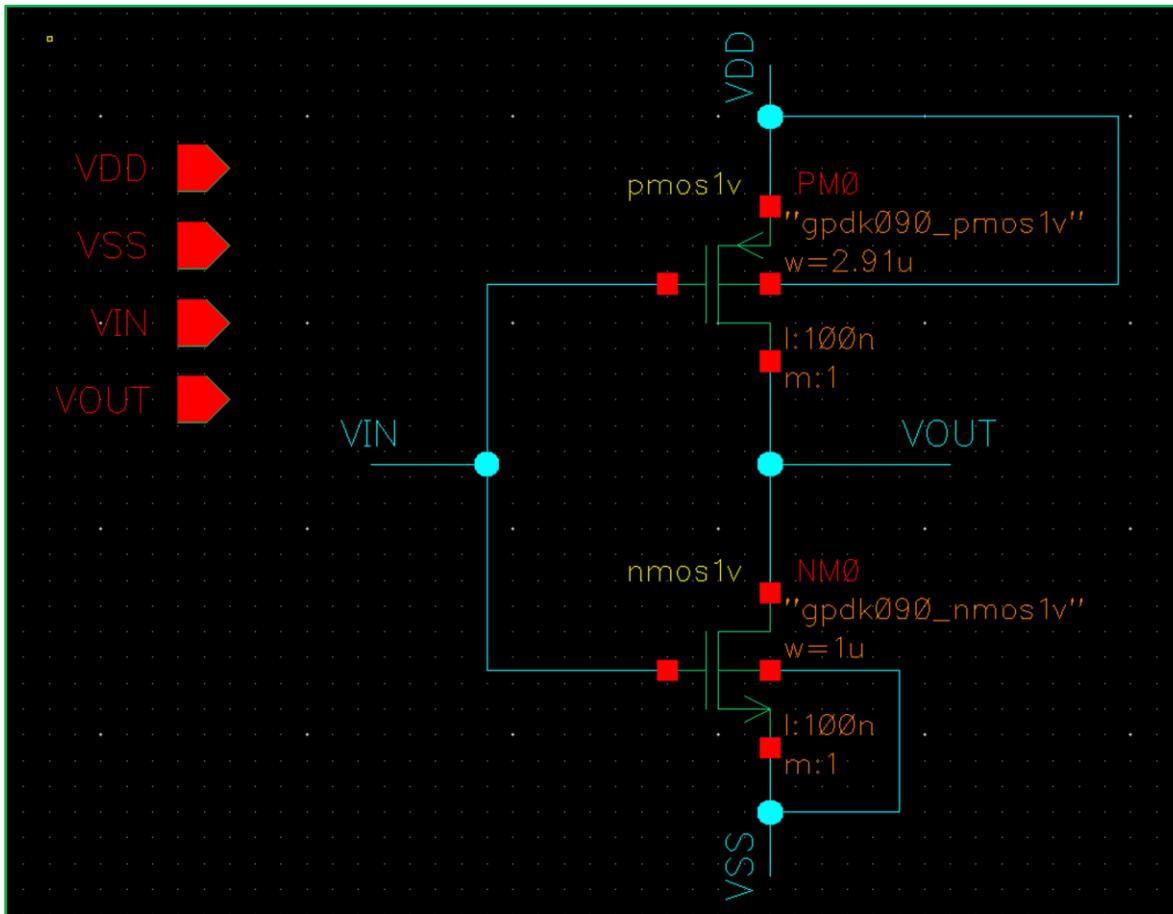
3

2NOR/3NOR/4NOR

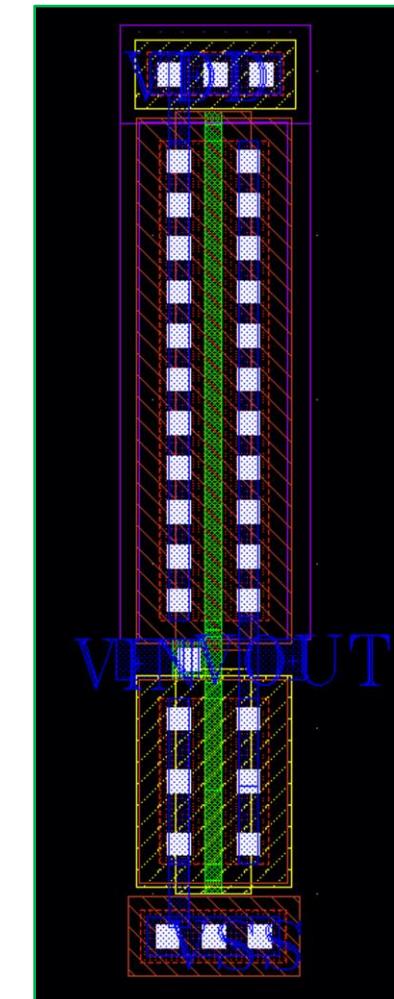
DITIGAL LOGIC GATE

NOT

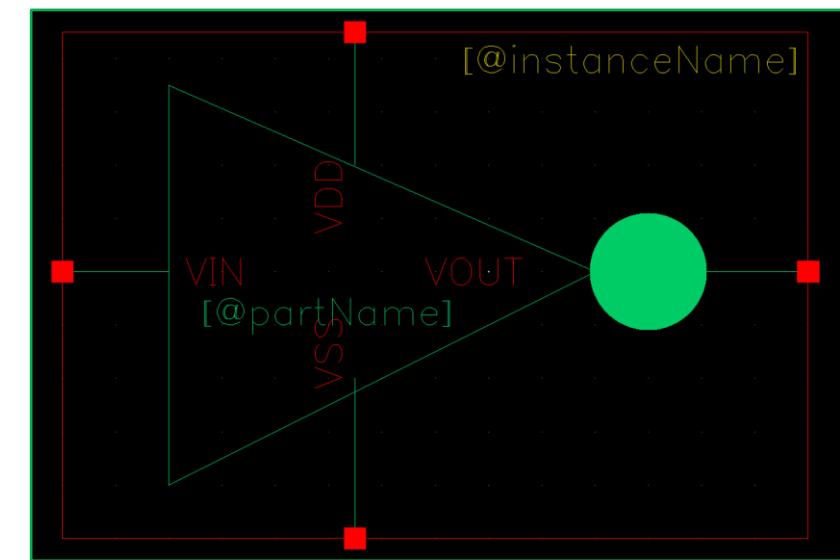
Schematic



Layout



Symbol



DITIGAL LOGIC GATE

NOT

Simulation

DC Response

Name WID

v/VIN; dc (V)

v/VIN; dc (V) 1.0u

v/VIN; dc (V) 2.0u

v/VIN; dc (V) 3.0u

v/VIN; dc (V) 4.0u

v/VIN; dc (V) 5.0u

v/VIN; dc (V) 6.0u

v/VIN; dc (V) 7.0u

v/VIN; dc (V) 8.0u

v/VIN; dc (V) 9.0u

v/VIN; dc (V) 10.0u

v/VOUT; dc (V)

v/VOUT; dc (V) 1.0u

v/VOUT; dc (V) 2.0u

v/VOUT; dc (V) 3.0u

v/VOUT; dc (V) 4.0u

v/VOUT; dc (V) 5.0u

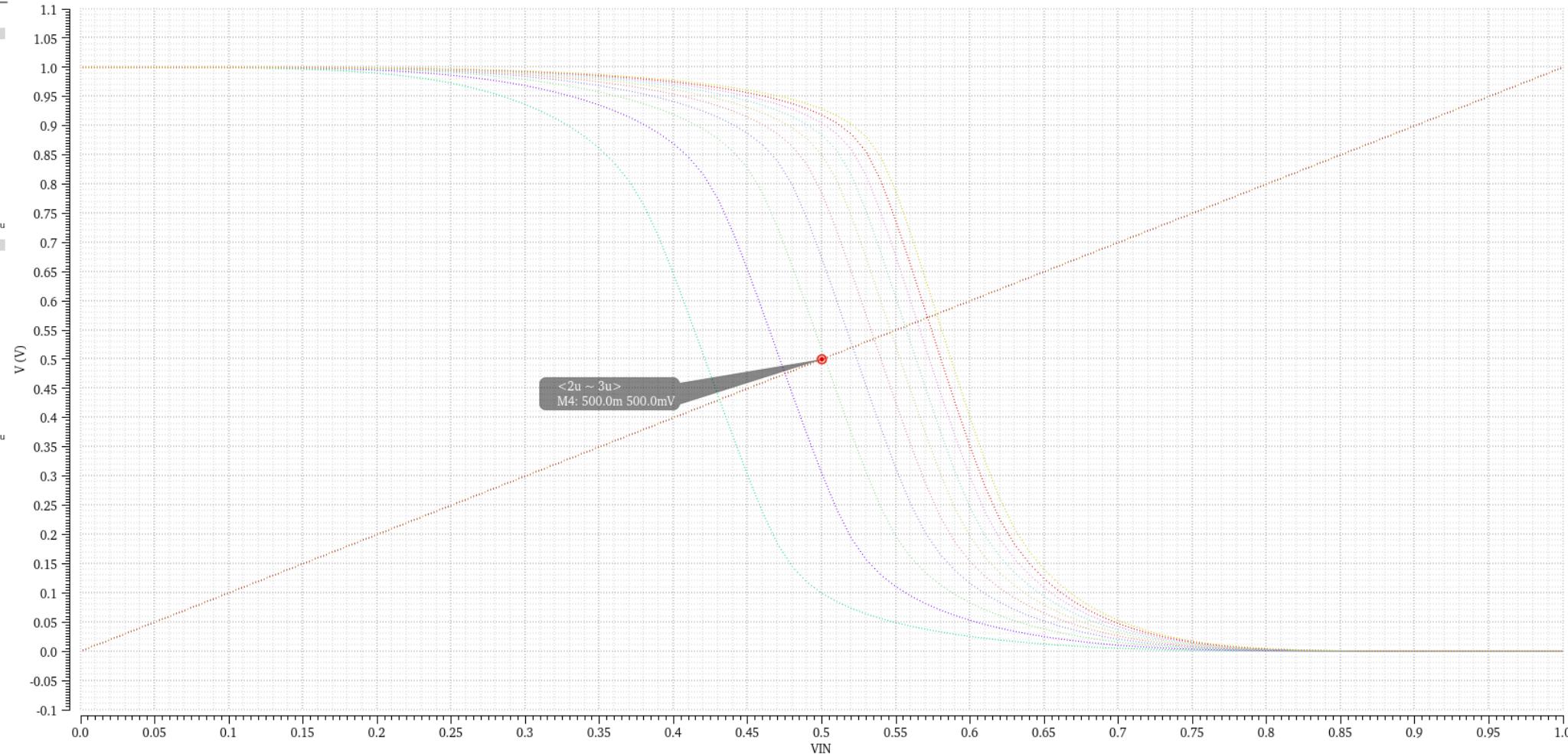
v/VOUT; dc (V) 6.0u

v/VOUT; dc (V) 7.0u

v/VOUT; dc (V) 8.0u

v/VOUT; dc (V) 9.0u

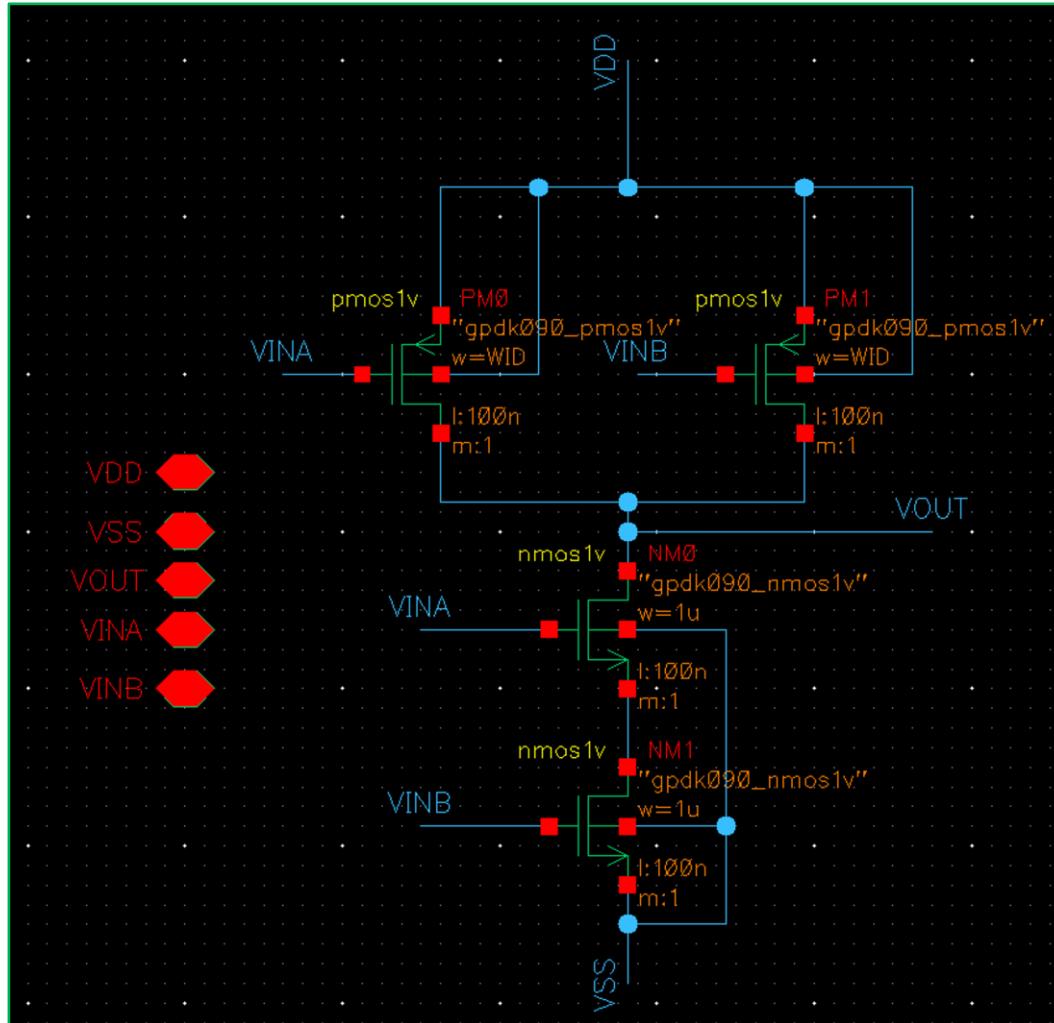
v/VOUT; dc (V) 10.0u



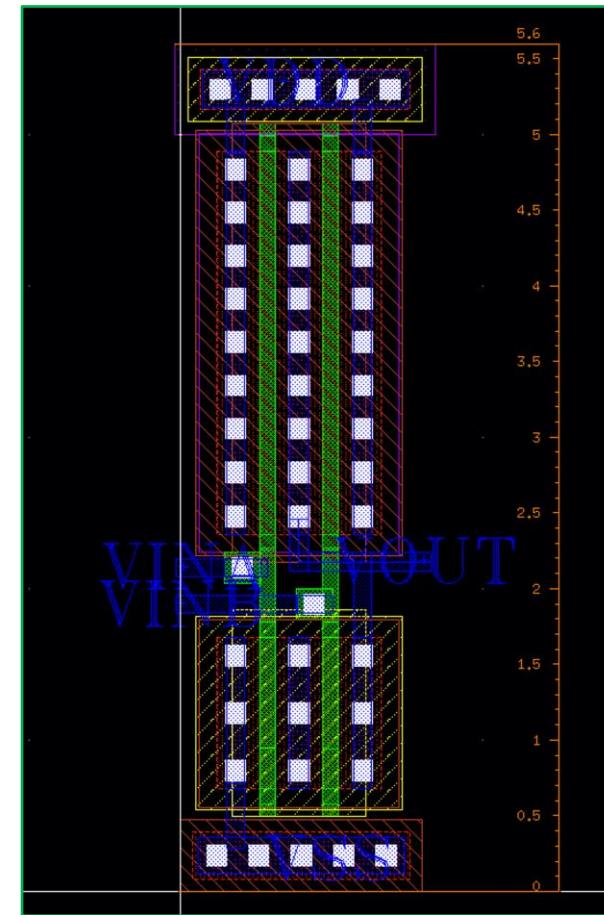
DITIGAL LOGIC GATE

2NAND

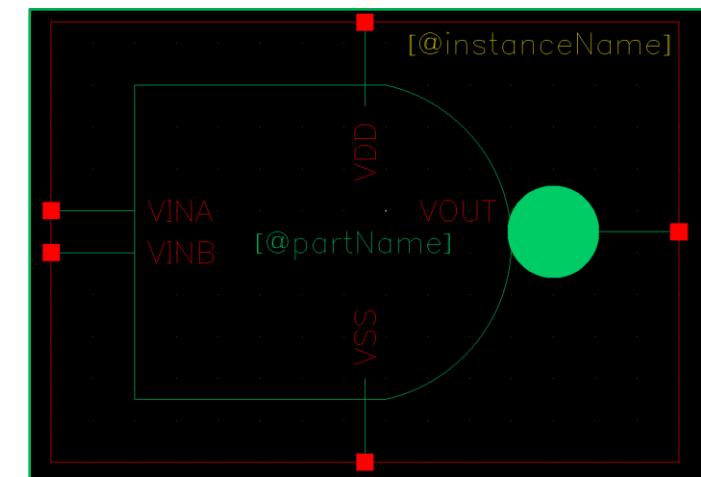
Schematic



Layout



Symbol



DITIGAL LOGIC GATE

2NAND

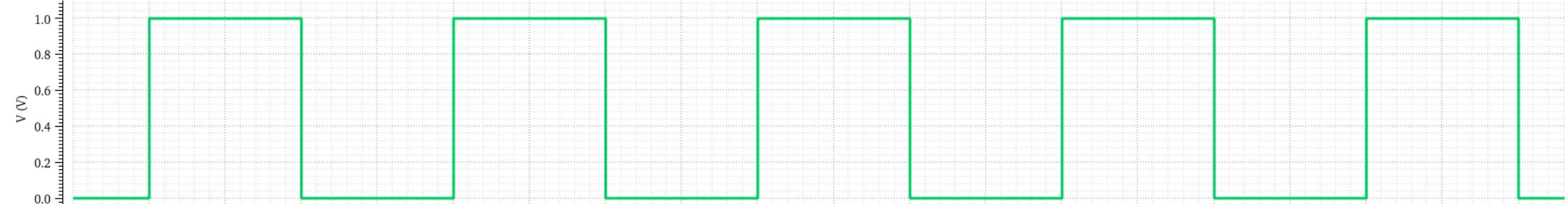
Simulation

Transient Response

Name

1

v /VINA; tran (V)



v /VINB; tran (V)



v /VOUT; tran (V)



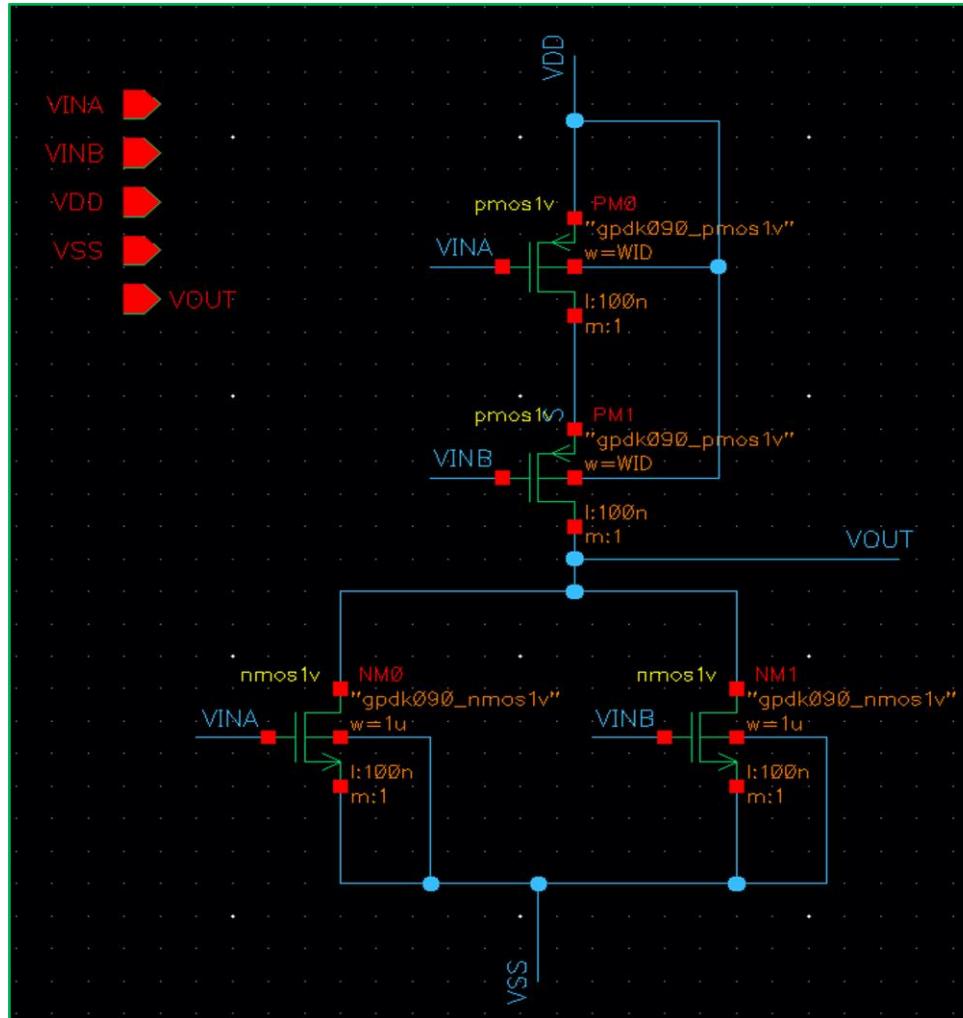
| X1 | X2 | Y |
|----|----|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

10

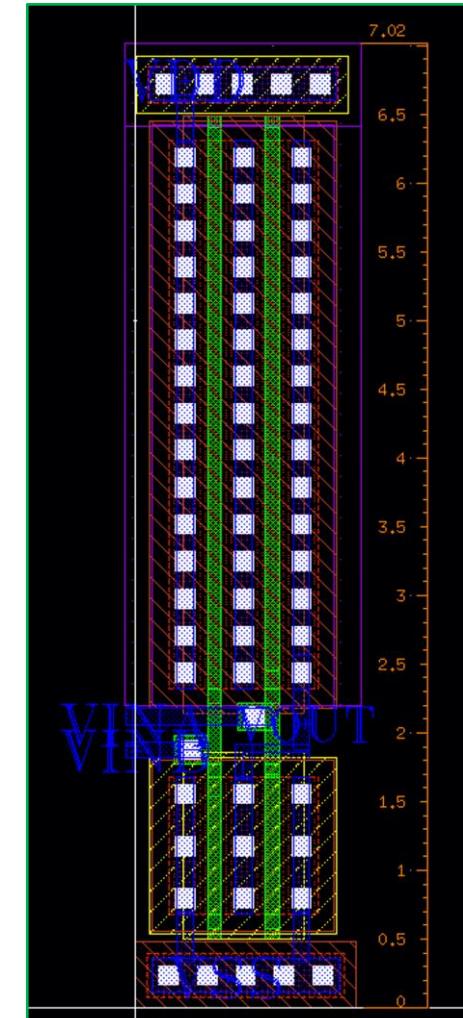
DITIGAL LOGIC GATE

2NOR

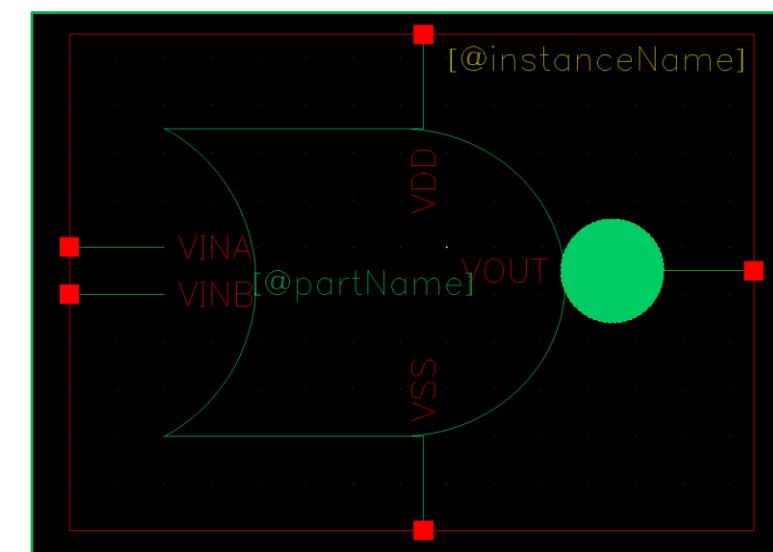
Schematic



Layout



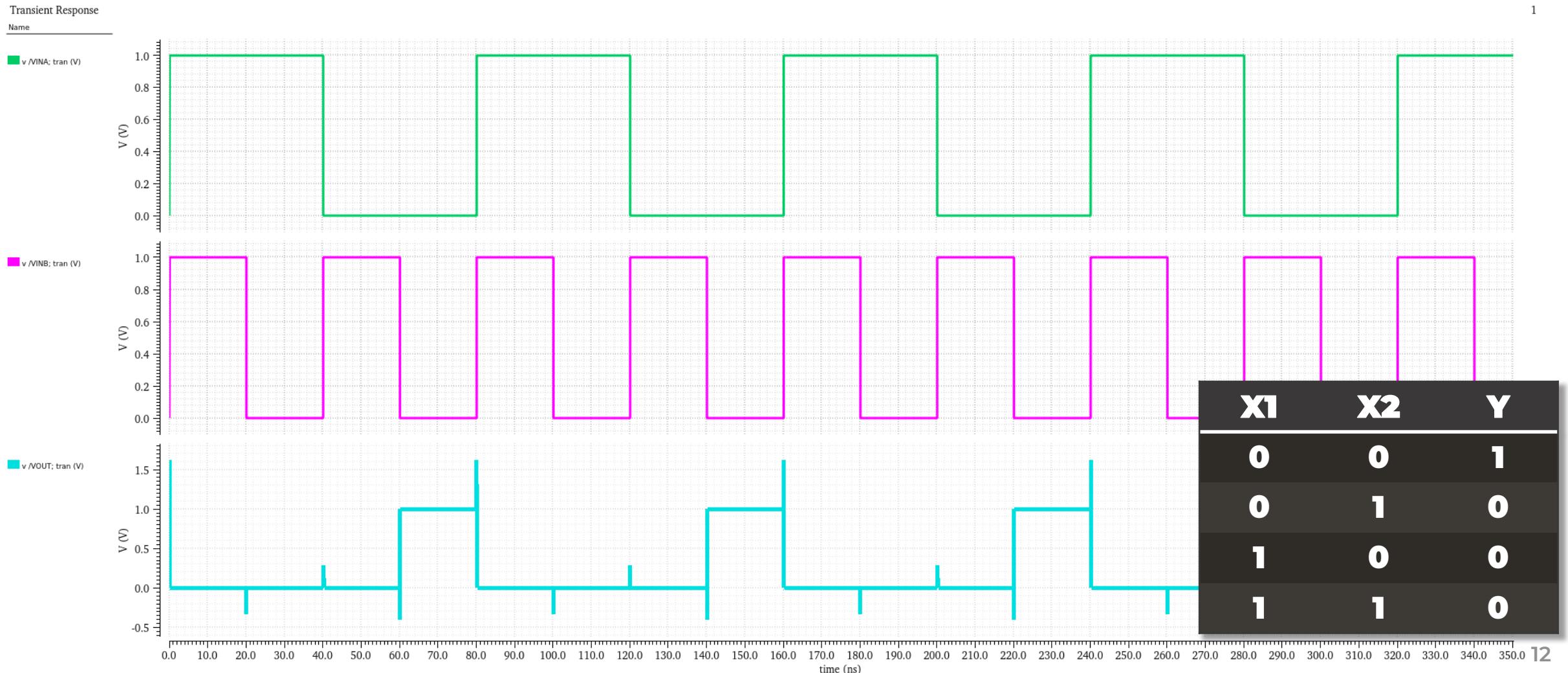
Symbol



DITIGAL LOGIC GATE

2NOR

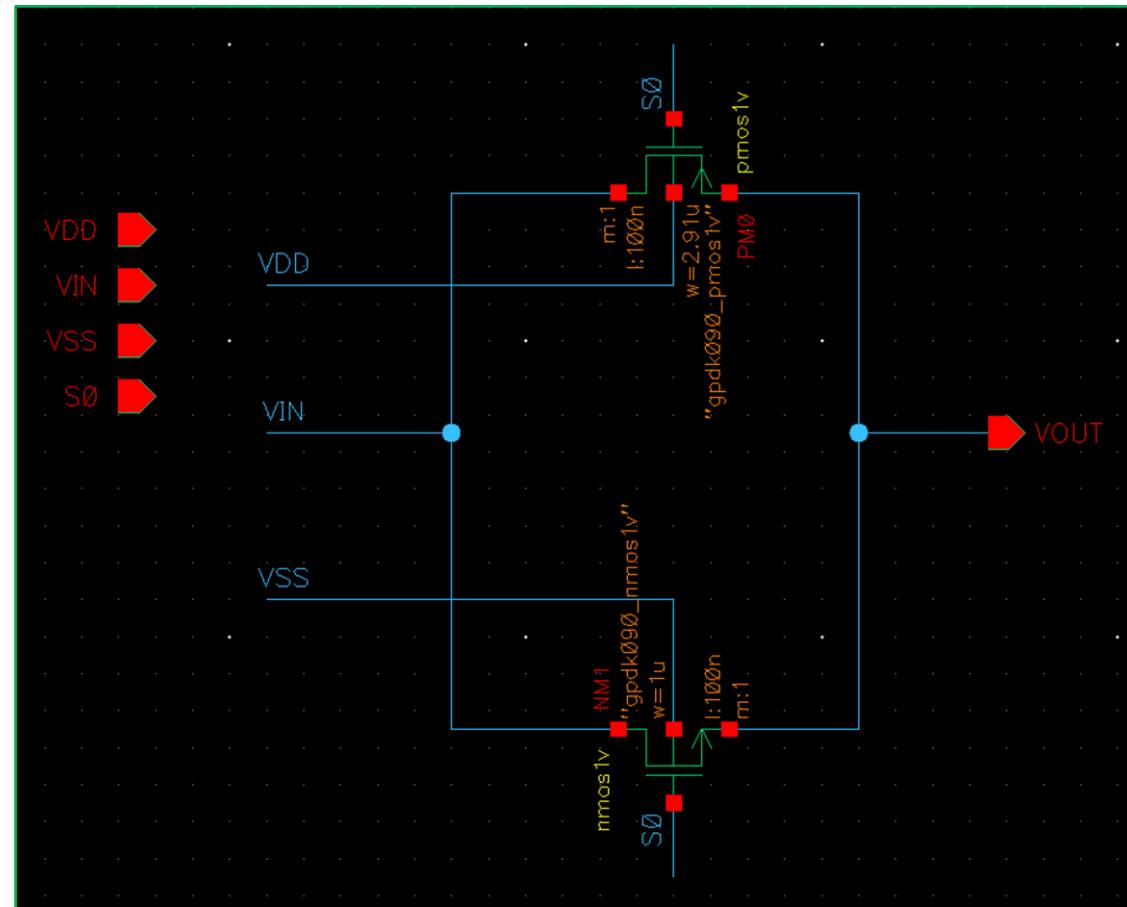
Simulation



DITIGAL LOGIC GATE

SWITCH

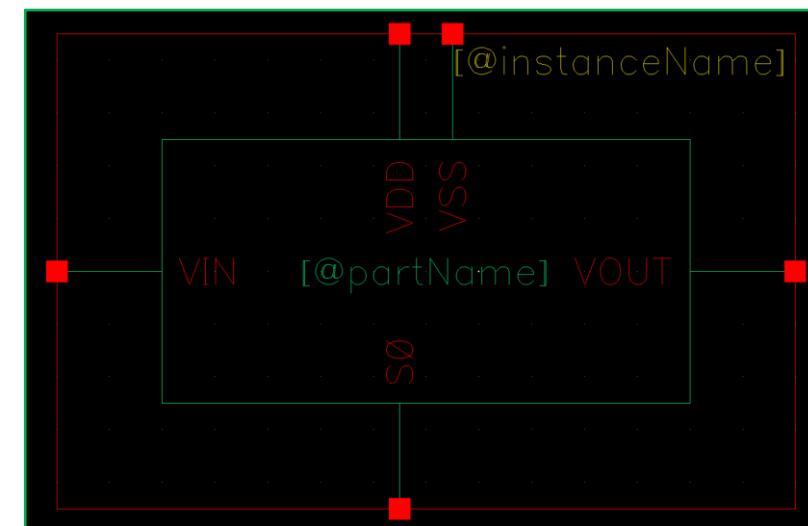
Schematic



Layout



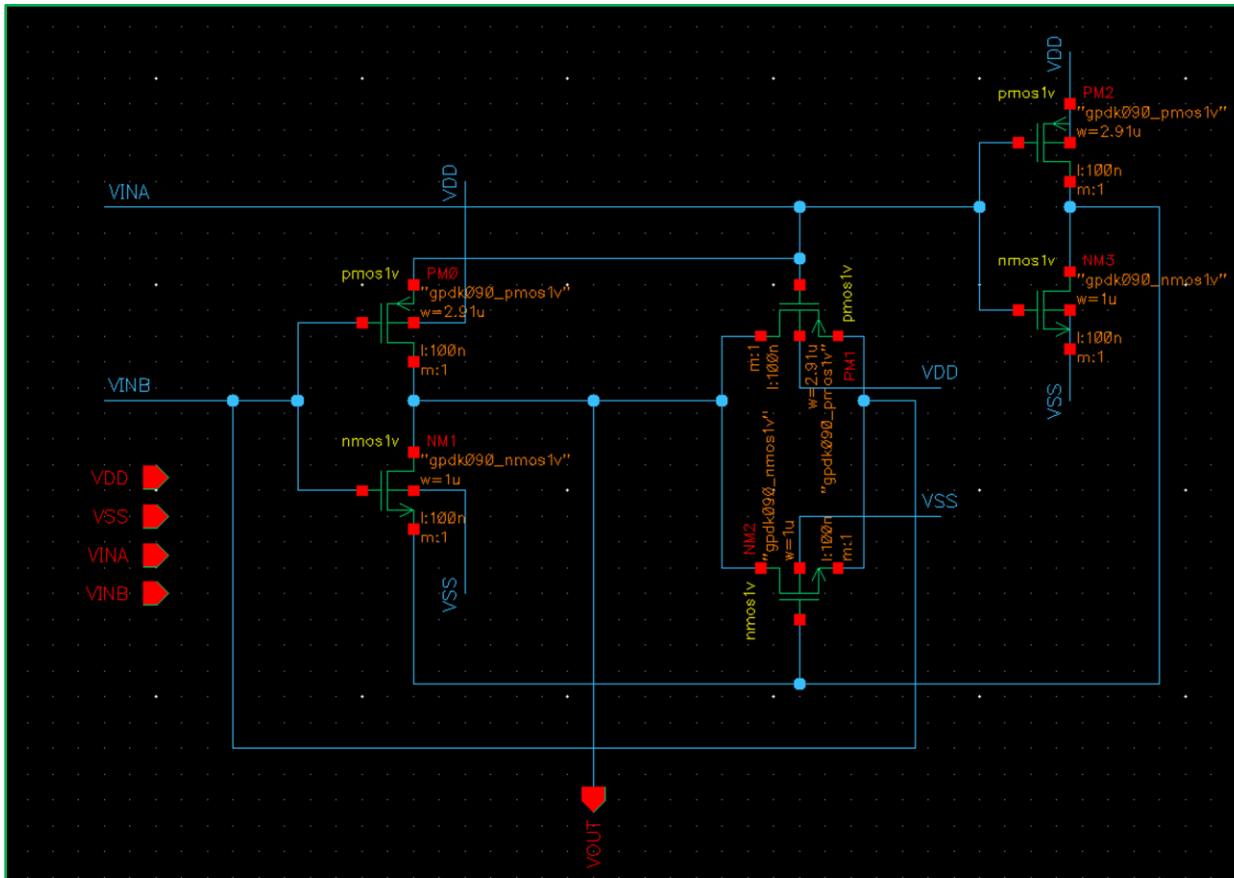
Symbol



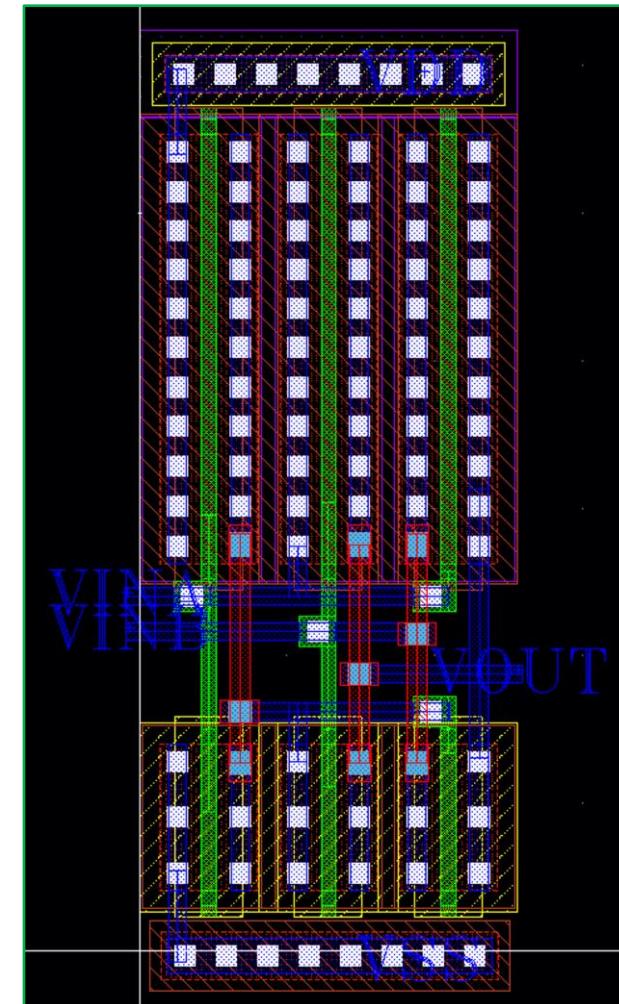
DITIGAL LOGIC GATE

XOR

Schematic



Layout



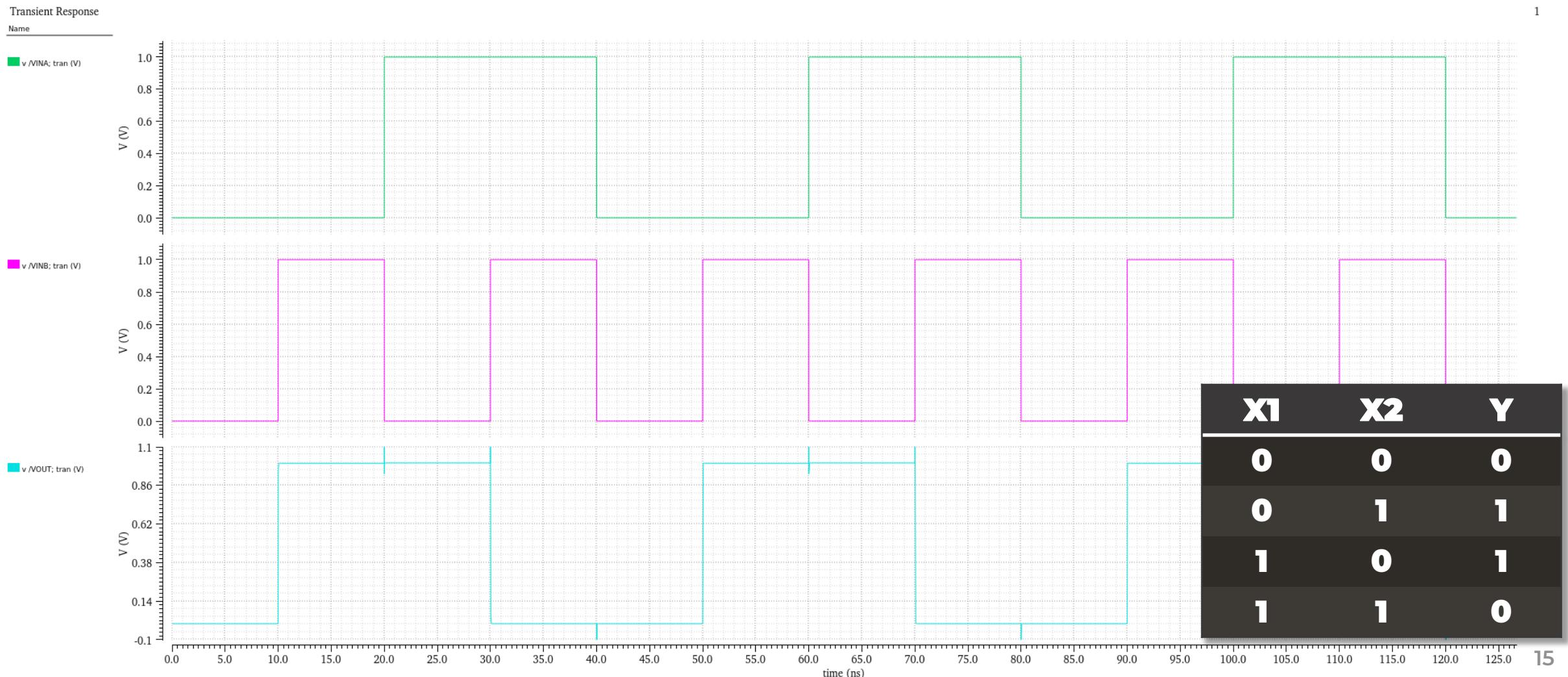
Symbol



DITIGAL LOGIC GATE

XOR

Simulation

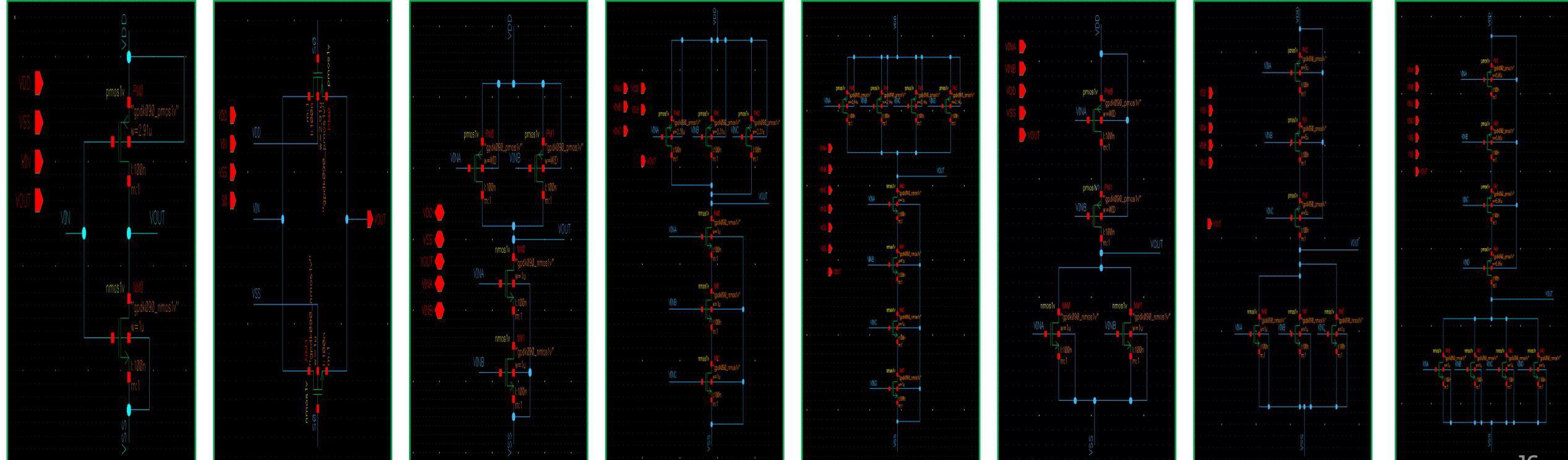


DITIGAL LOGIC GATE

Schematic

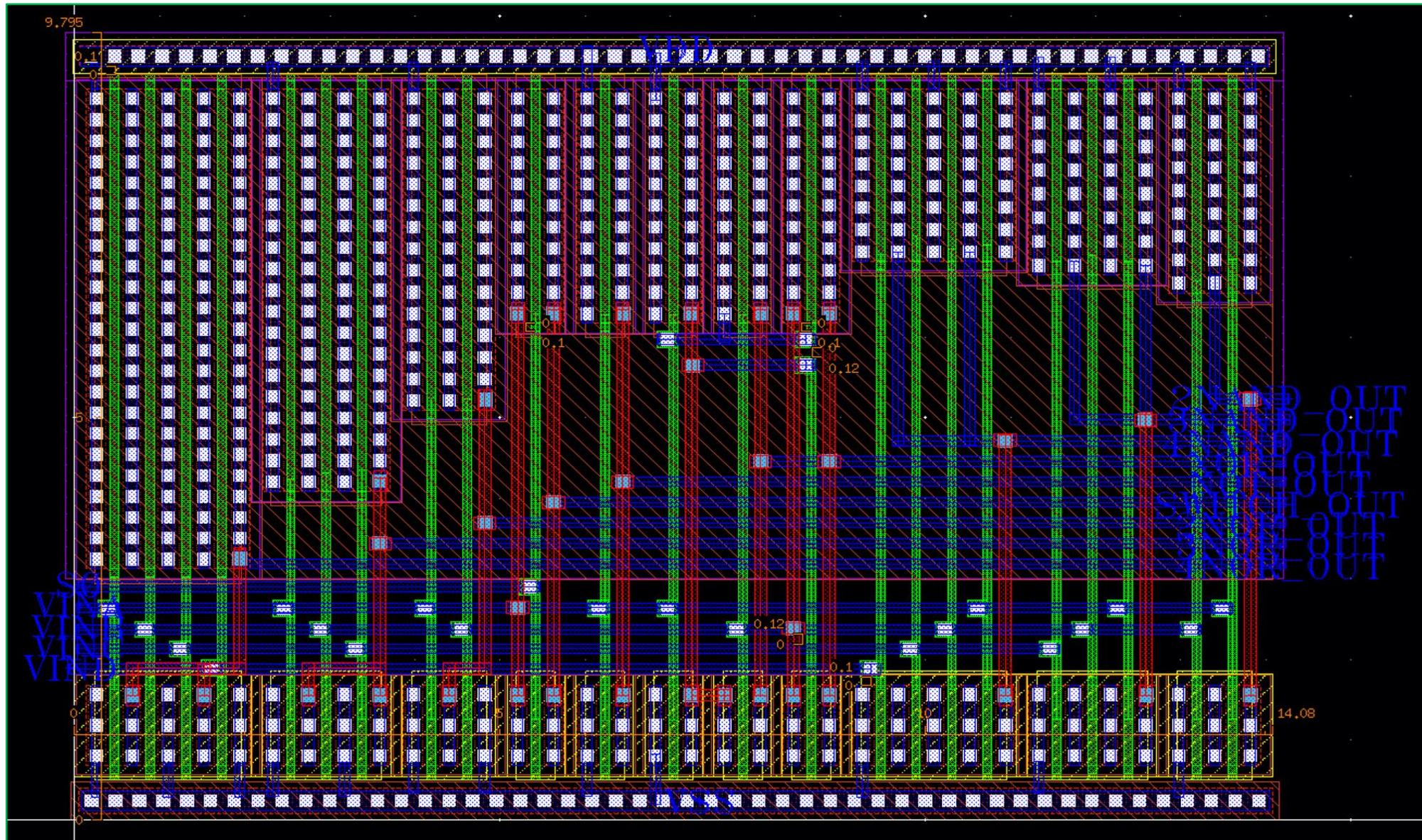
| NOT | SWITCH | 2NAND | 3NAND | 4NAND | 2NOR | 3NOR | 4NOR |
|-----------------------------------|--------|--------|--------|--------|--------|--------|------|
| NMOS $L = 100\text{nm}$ | 1um | 1um | 1um | 1um | 1um | 1um | 1um |
| PMOS $L = 100\text{nm}$ | 2.91um | 2.91um | 2.53um | 2.31um | 2.14um | 3.99um | 5um |

<NOT> <SWITCH> <2NAND> <3NAND> <4NAND> <2NOR> <3NOR> <4NOR>



DITIGAL LOGIC GATE

Layout



DITIGAL CIRCUIT

1

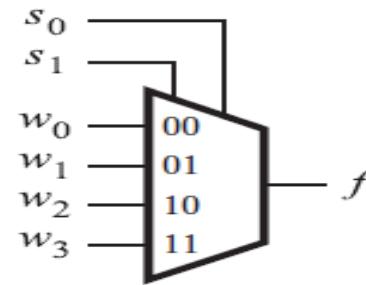
2x1 MUX, 4x1, 8x1, 16x1 MUX (Logic & Switch)

2

HALF_ADDER/FULL_ADDER/4BIT_ADDER/4BIT_SUBTRACTOR

DITIGAL CIRCUIT

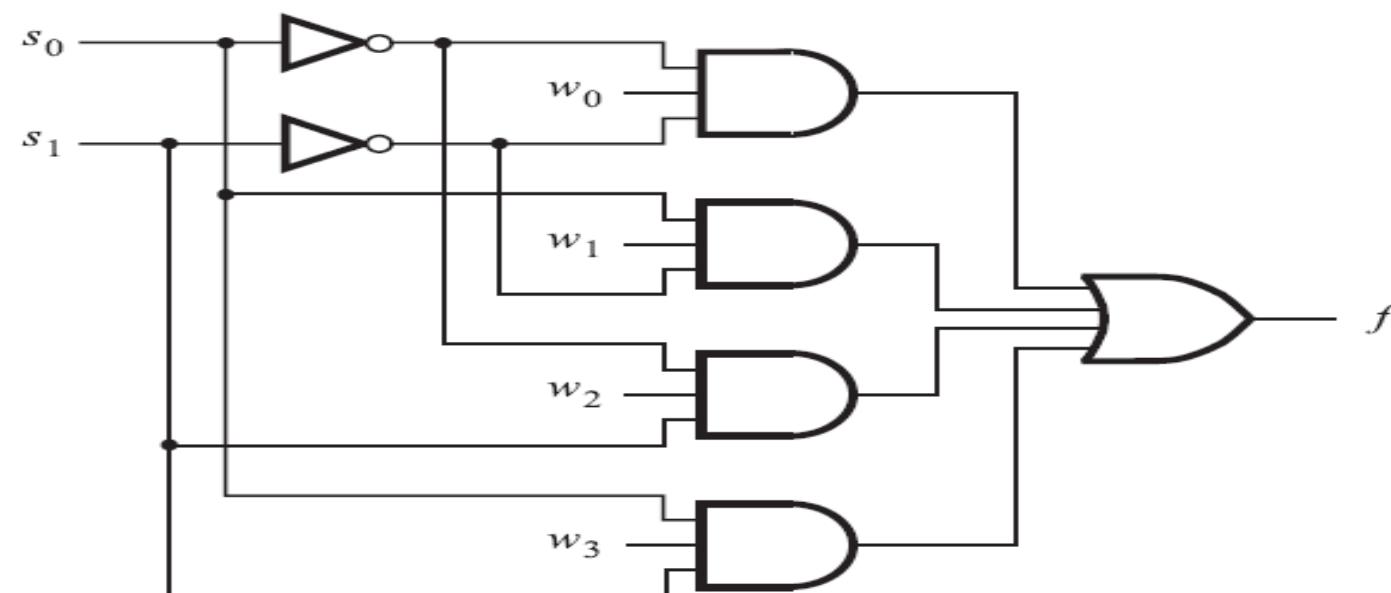
MUX



(a) Graphical symbol

| s_1 | s_0 | f |
|-------|-------|-------|
| 0 | 0 | w_0 |
| 0 | 1 | w_1 |
| 1 | 0 | w_2 |
| 1 | 1 | w_3 |

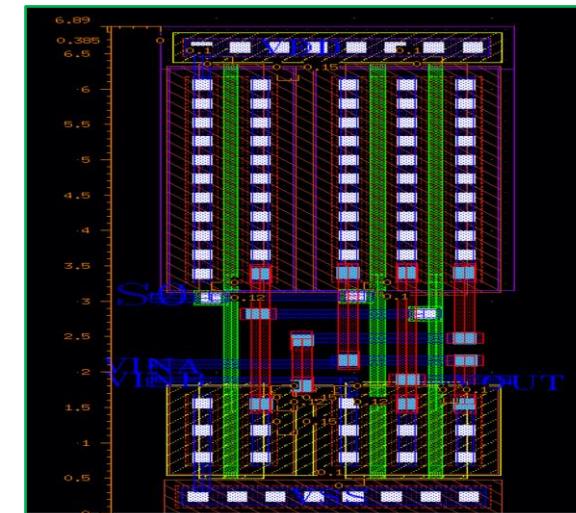
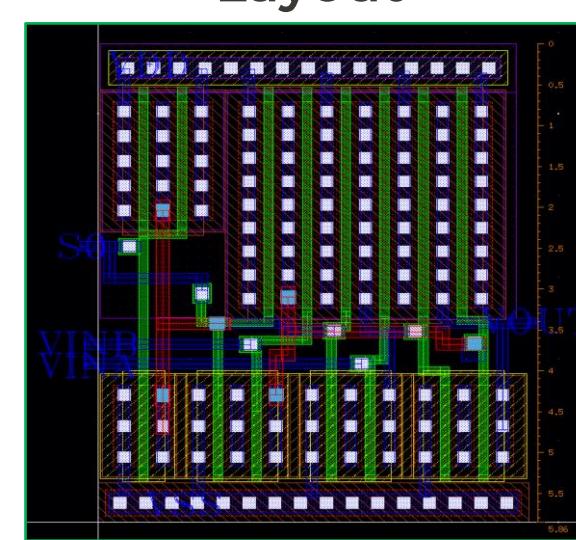
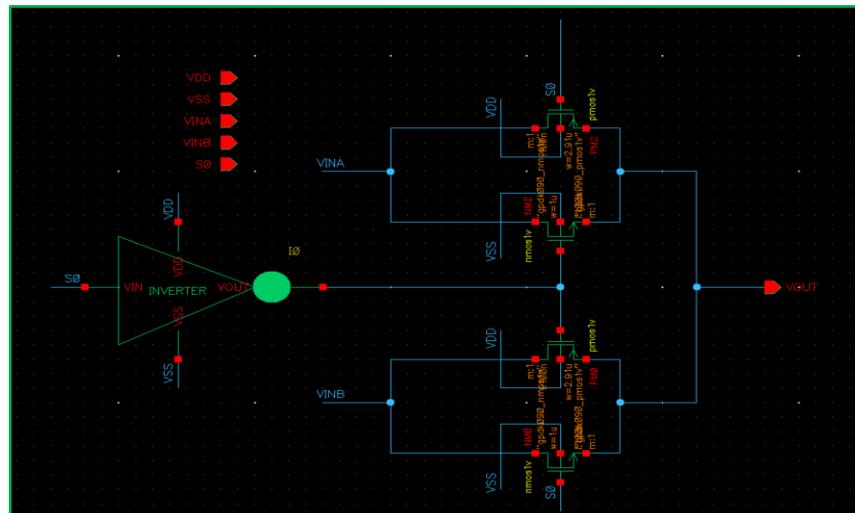
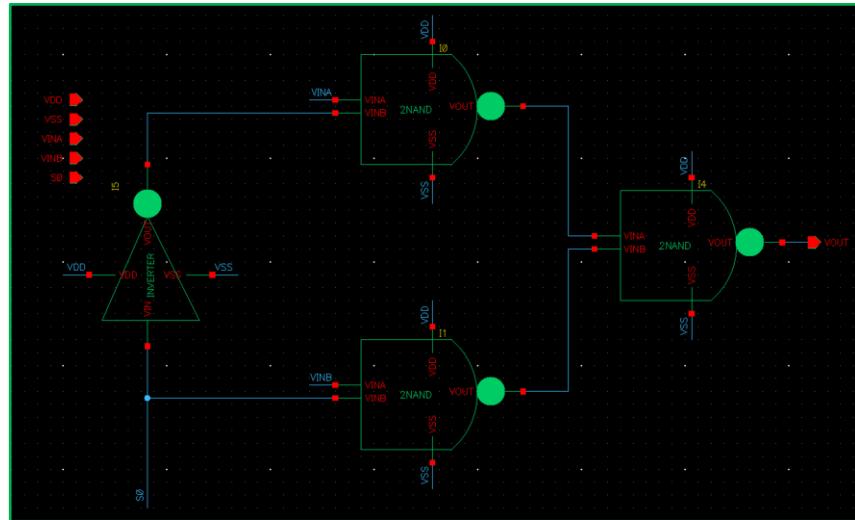
(b) Truth table



(c) Circuit

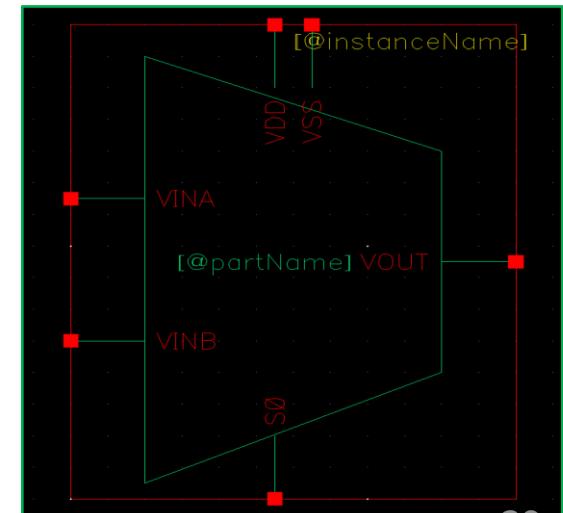
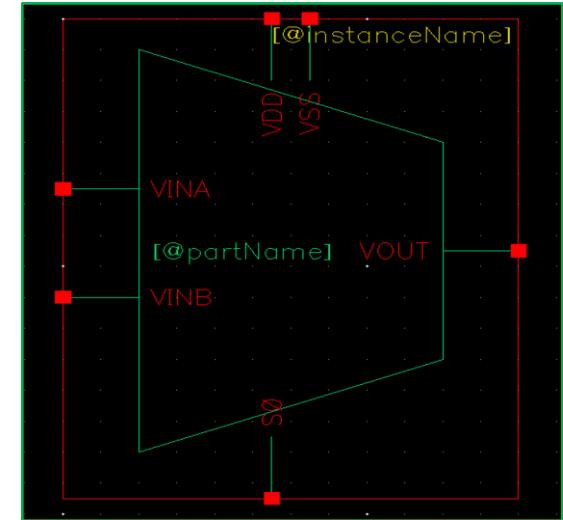
DITIGAL CIRCUIT

Logic
Focus



2x1 MUX

Symbol



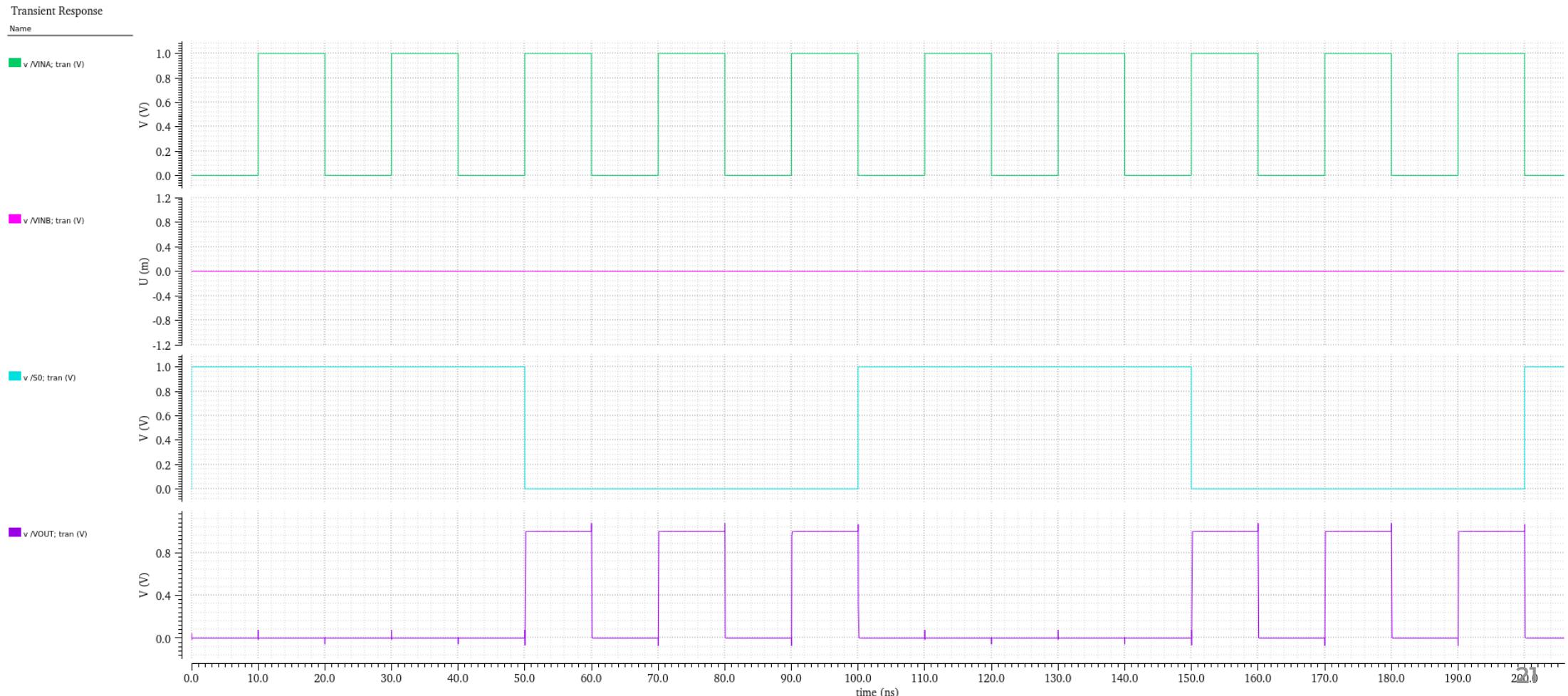
DITIGAL CIRCUIT

2x1 MUX

Logic
&
Switch

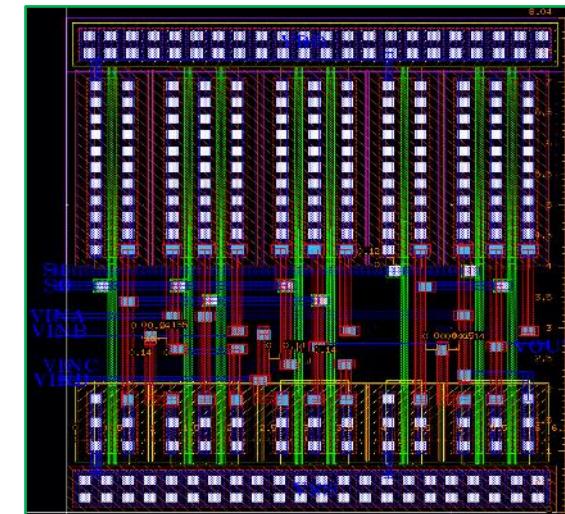
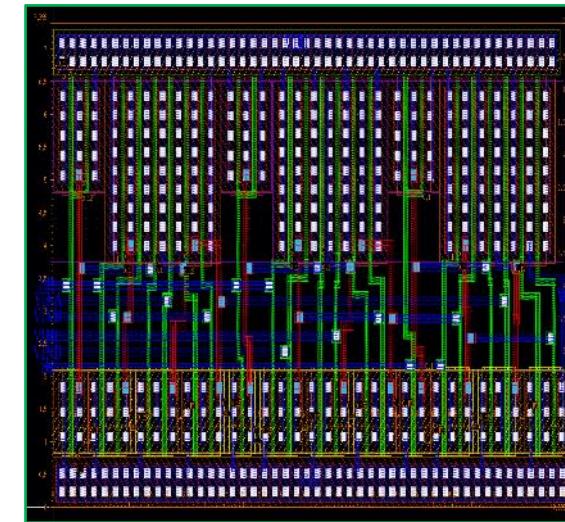
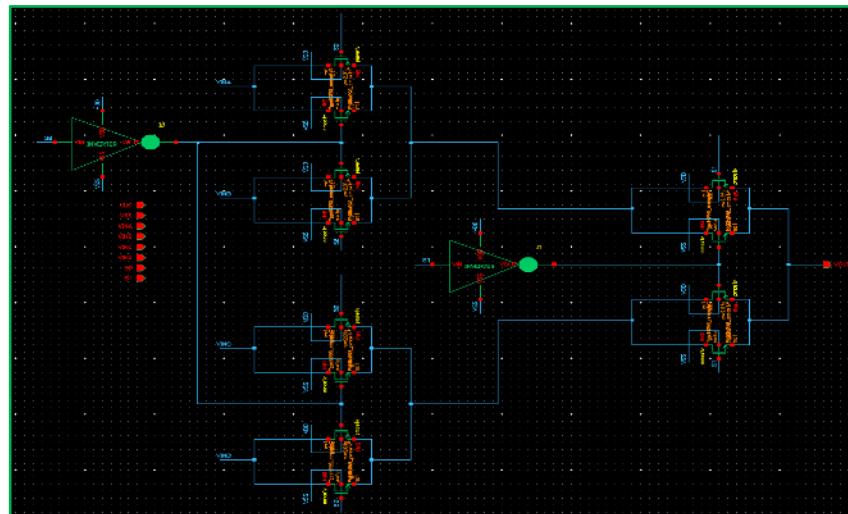
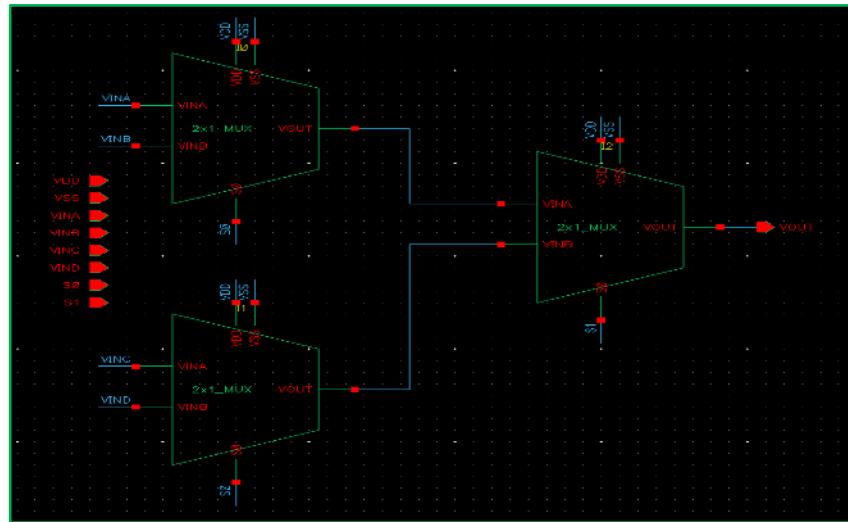
SWITCH

Simulation



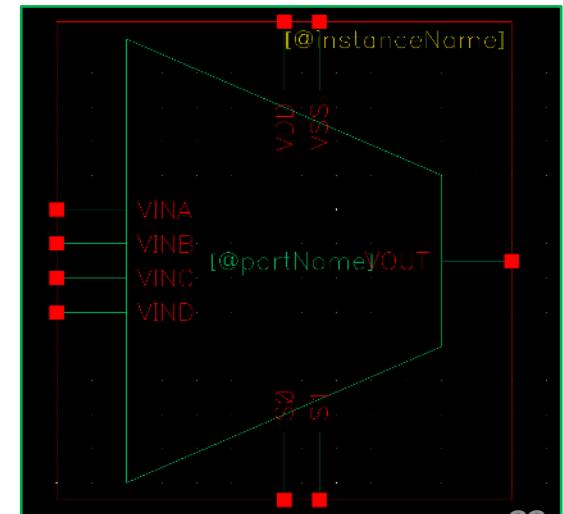
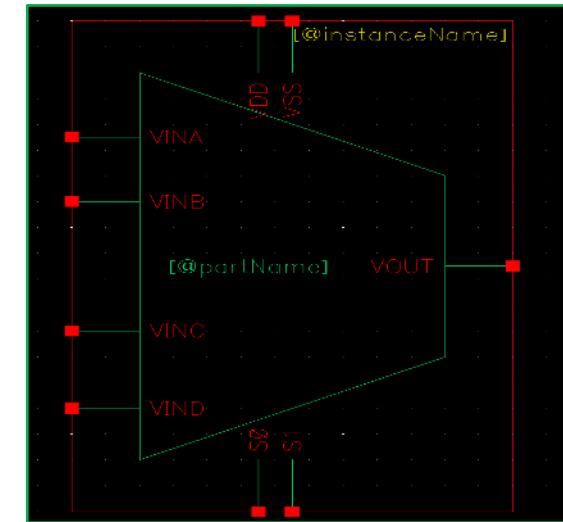
DITIGAL CIRCUIT

Logic
Focus



4x1 MUX

Symbol



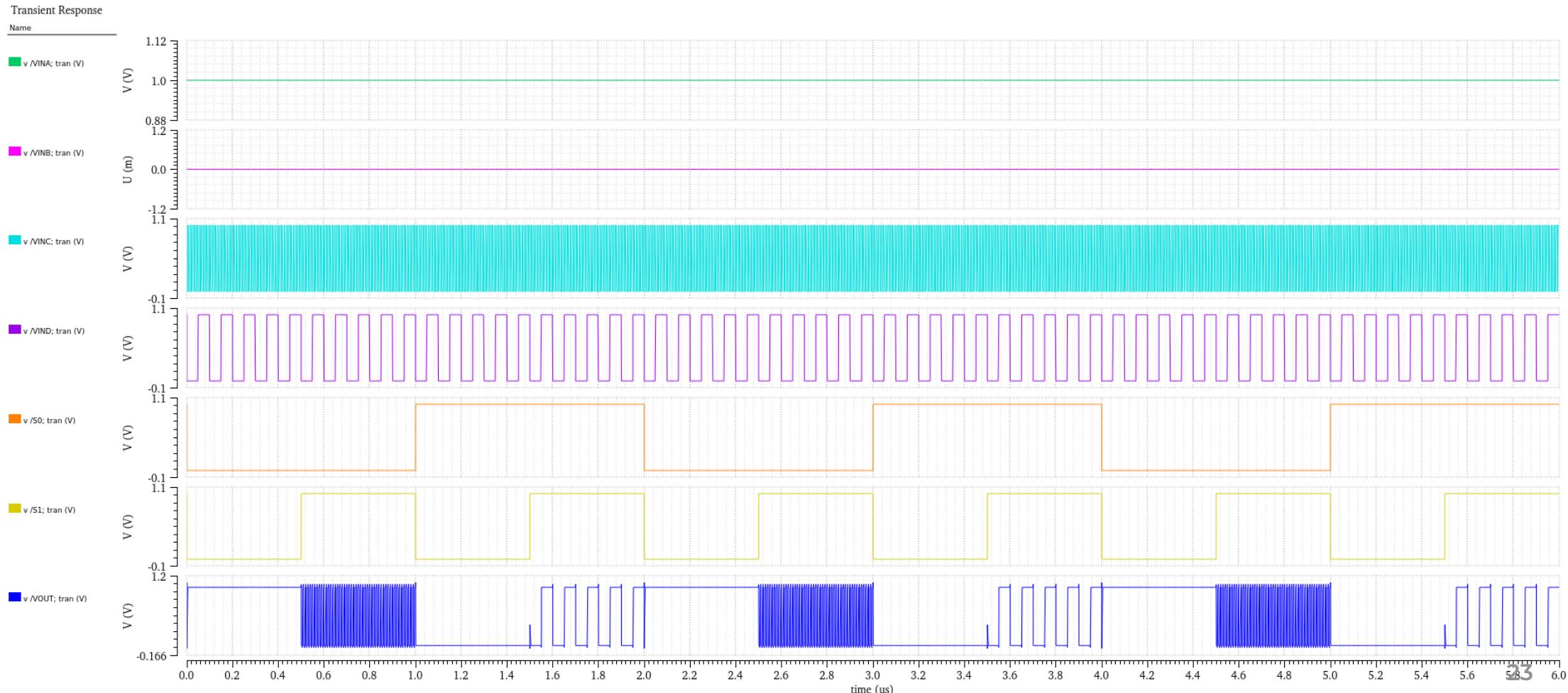
DITIGAL CIRCUIT

4x1 MUX

Logic
&
Switch

switch

Simulation

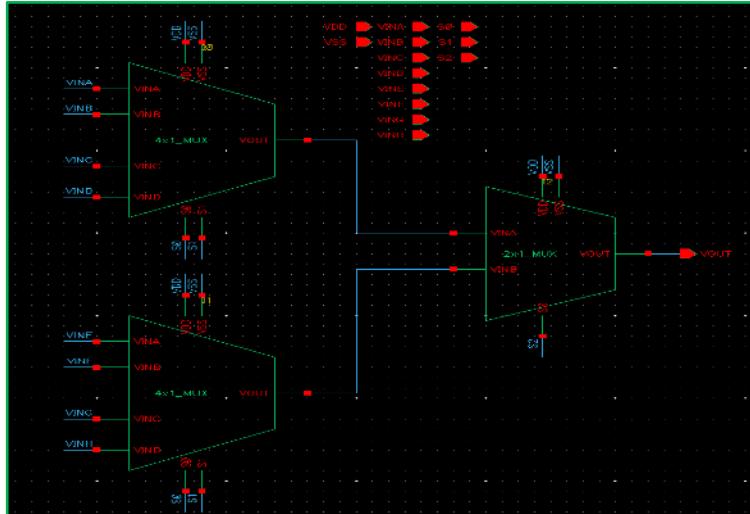


DITIGAL CIRCUIT

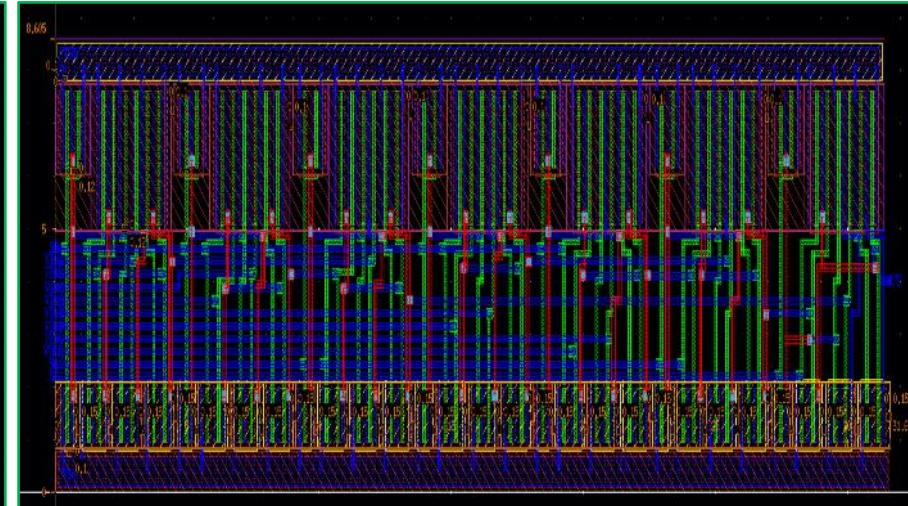
8x1 MUX

Logic
FPGA

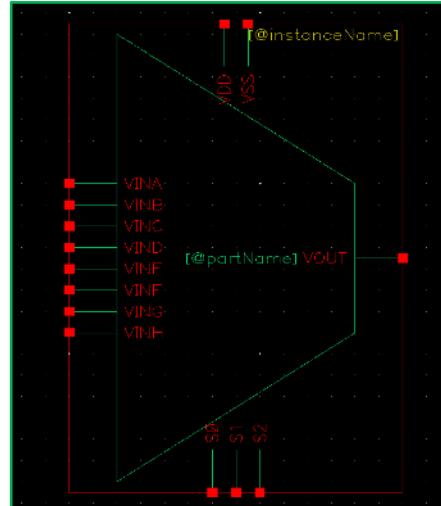
Schematic



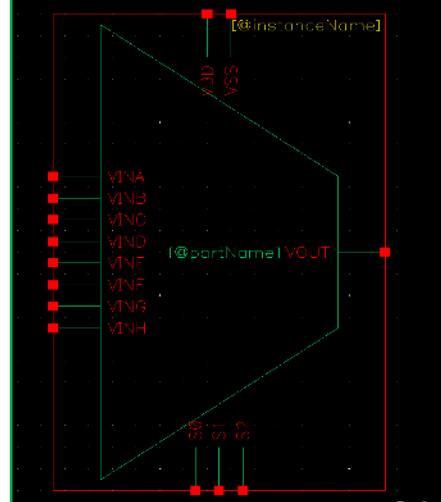
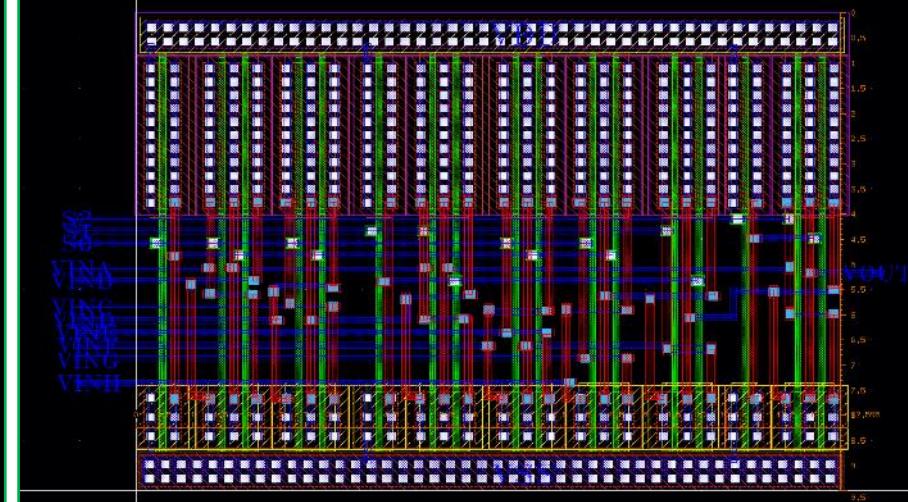
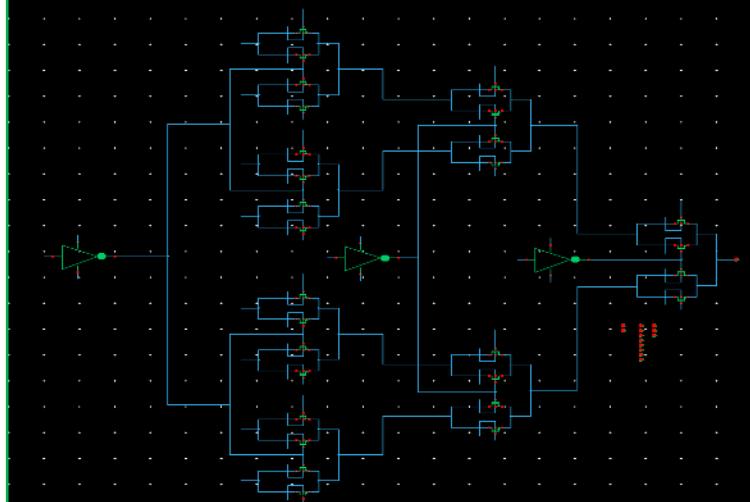
Layout



Symbol



Switch
FABRIC



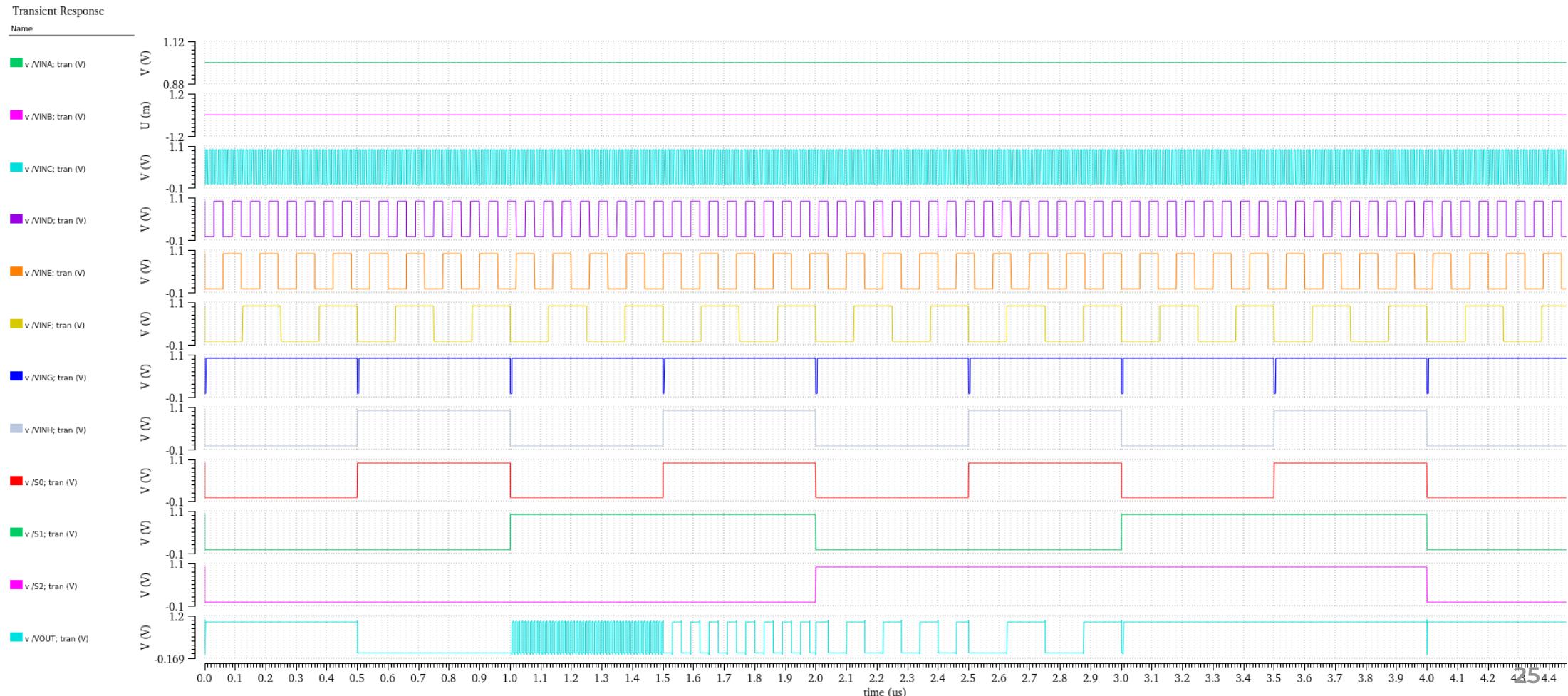
DITIGAL CIRCUIT

8x1 MUX

Logic
&
Switch

MUX

Simulation

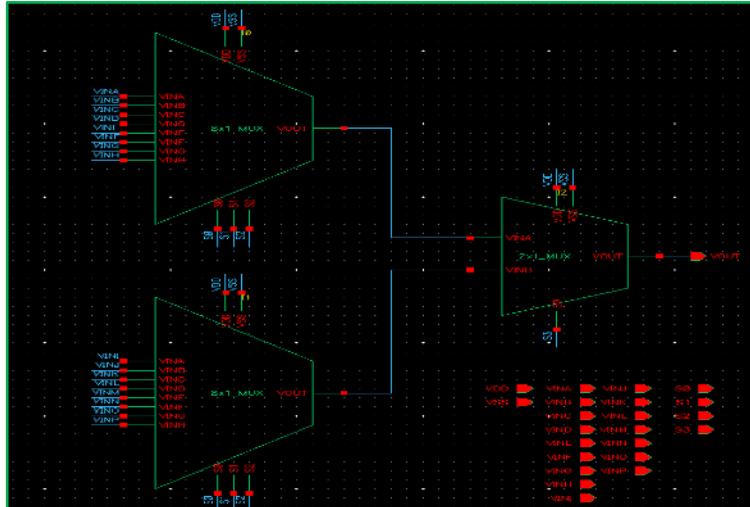


DITIGAL CIRCUIT

16x1 MUX

Logic
editor

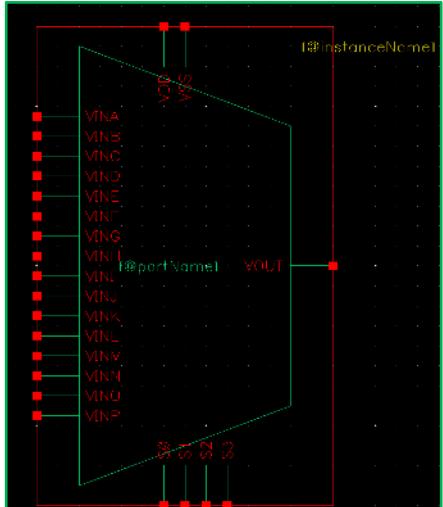
Schematic



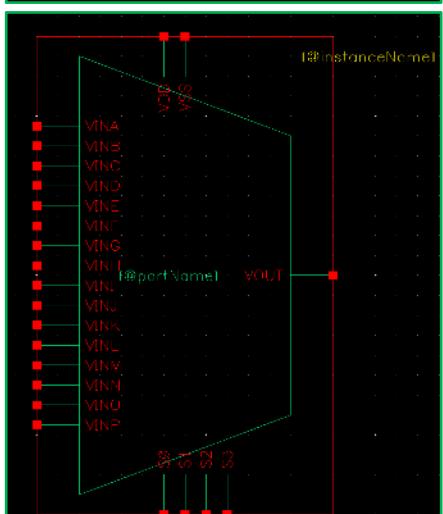
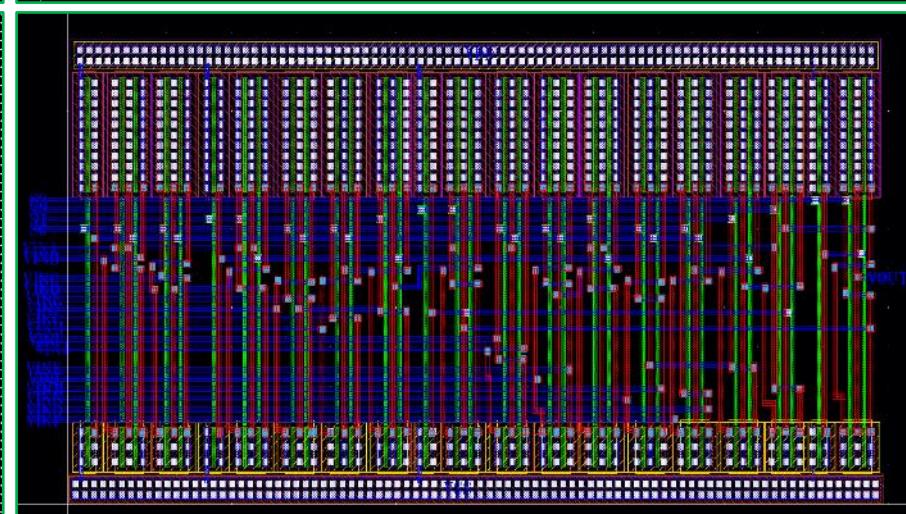
Layout



Symbol



Switch
editor



DITIGAL CIRCUIT

16x1 MUX

Logic
&
Switch

SWITCH

Simulation



DITIGAL CIRCUIT

MUX

| Area | 2x1 MUX | 4x1 MUX | 8x1 MUX | 16x1 MUX |
|----------------------|---------|----------|----------|----------|
| Logic (μm^2) | 30.9353 | 101.7603 | 276.3482 | 758.5501 |
| Switch (μm^2) | 20.8030 | 46.7775 | 159.951 | 405.1853 |
| Ratio | 1.4871 | 2.1754 | 1.7277 | 1.8721 |

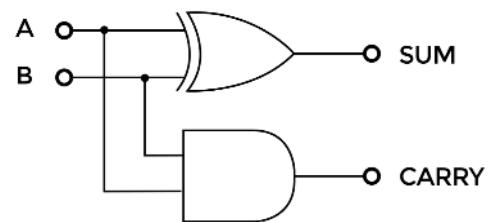
| TR | 2x1 MUX | 4x1 MUX | 8x1 MUX | 16x1 MUX |
|---------------|---------|---------|---------|----------|
| Logic (unit) | 14 | 42 | 98 | 210 |
| Switch (unit) | 6 | 16 | 38 | 78 |

It can be used
efficiently due to its
*small area and
number of transistors.*

DITIGAL CIRCUIT

ADDER

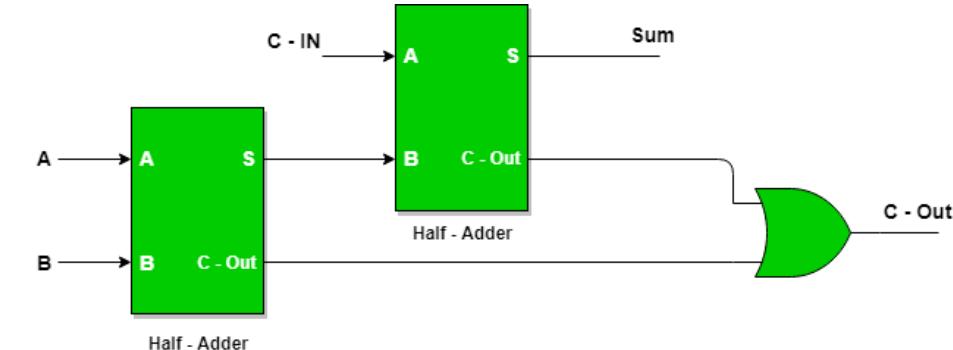
Half Adder



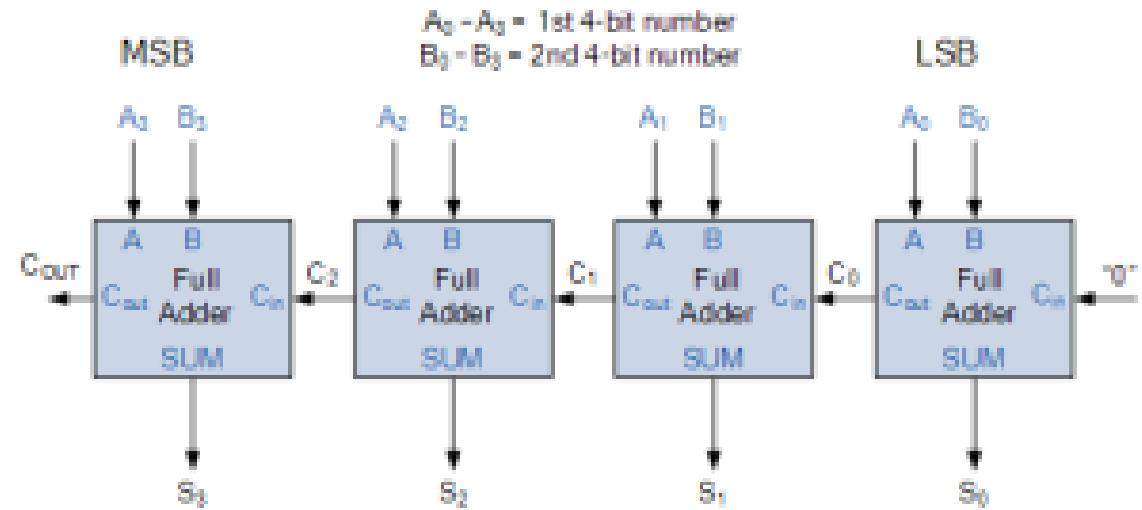
| A | B | Sum | Carry |
|---|---|-----|-------|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |



Full Adder



4Bit Adder



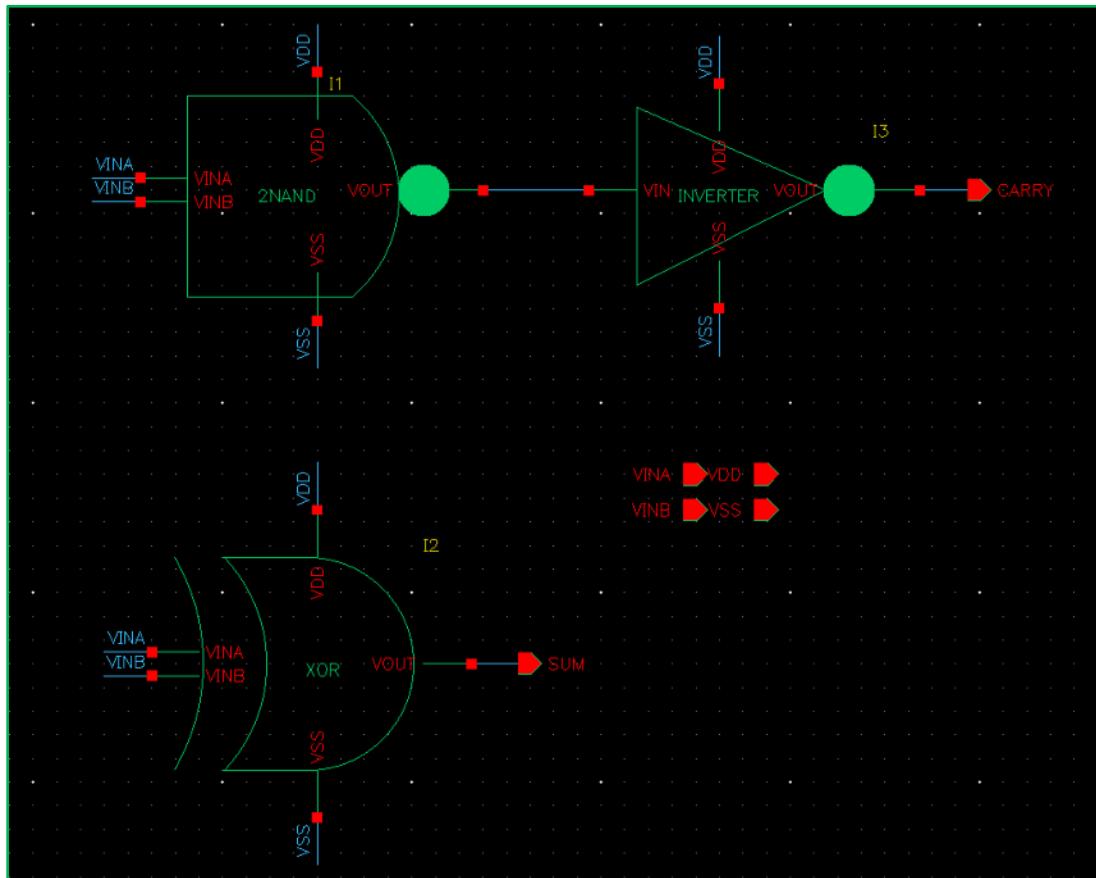
| A_1 | B_1 | C_{in} | Σ_1 | C_{out} |
|-------|-------|----------|------------|-----------|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

| Inputs | | | Outputs | |
|--------|---|----------|---------|-----------|
| A | B | C_{in} | Sum | C_{out} |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

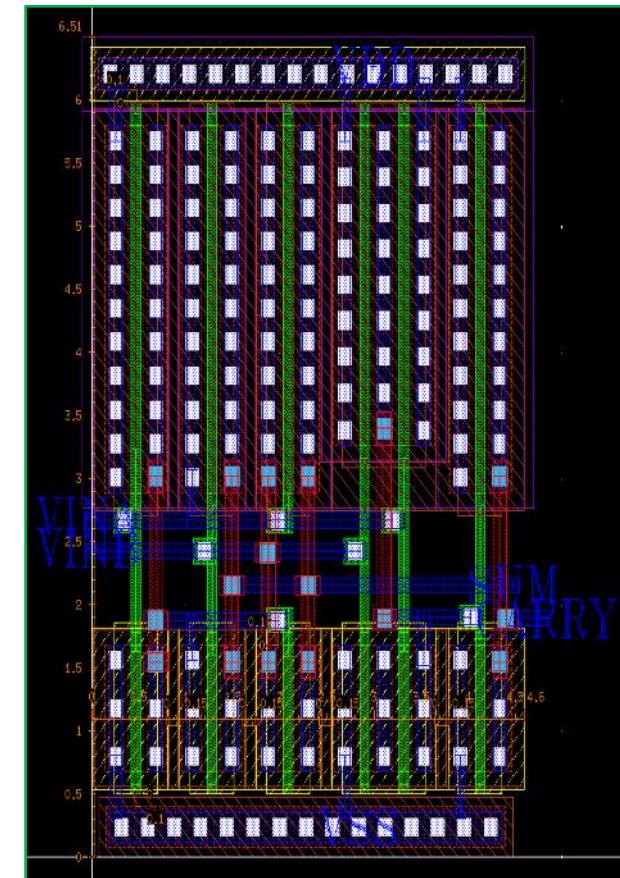
DITIGAL CIRCUIT

HALF_ADDER

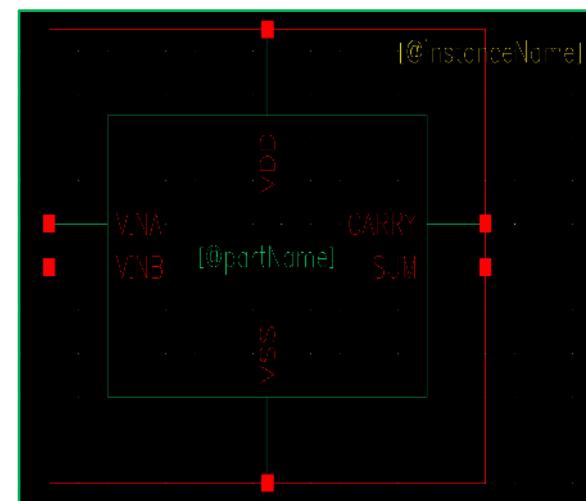
Schematic



Layout



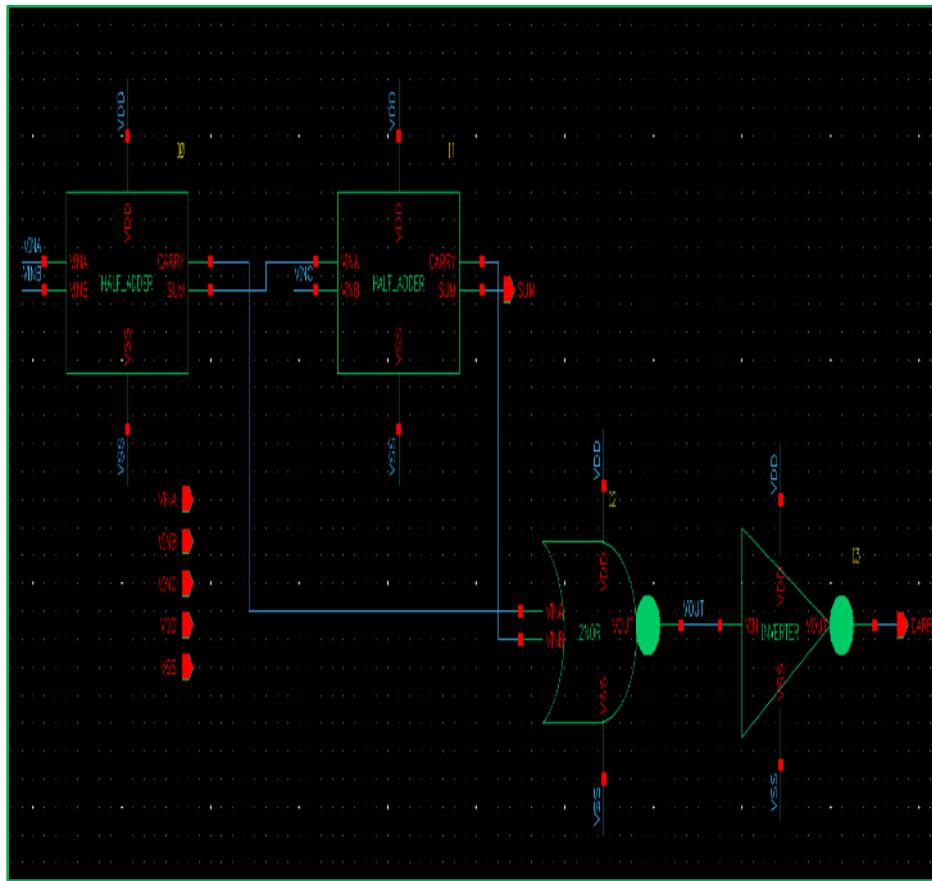
Symbol



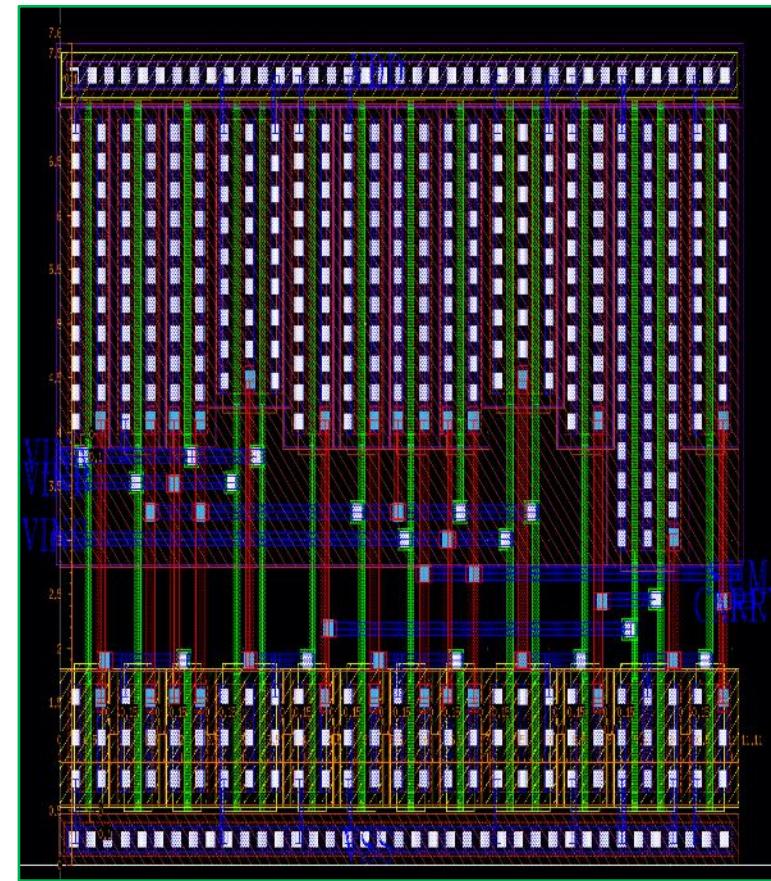
DITIGAL CIRCUIT

FULL_ADDER

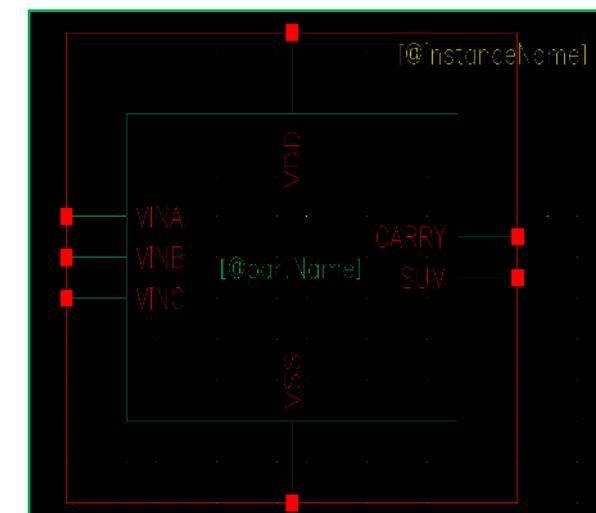
Schematic



Layout



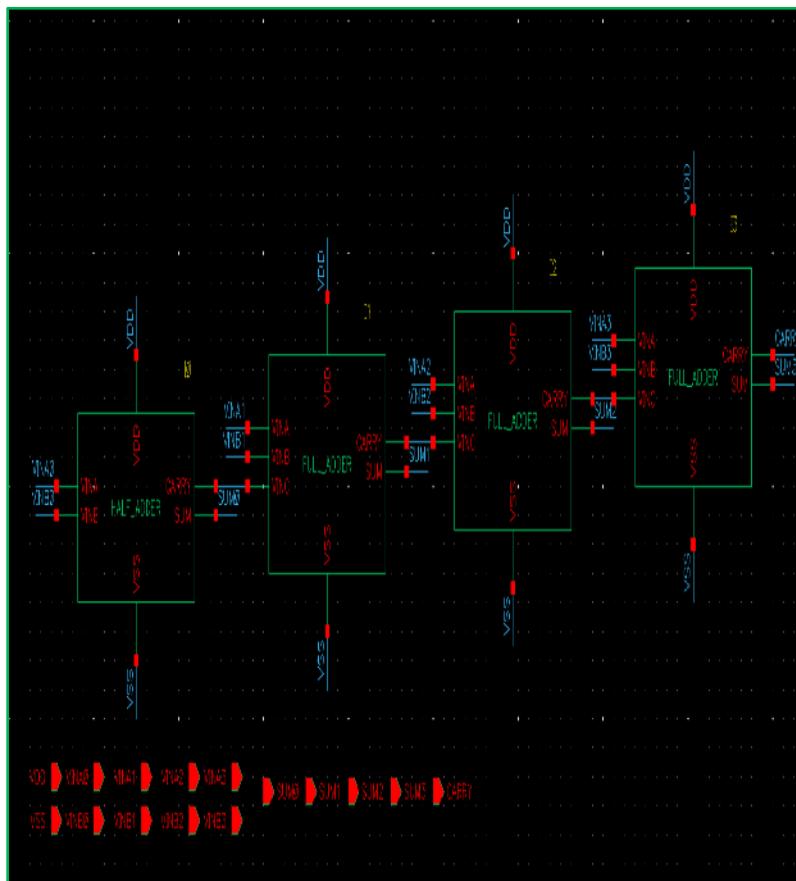
Symbol



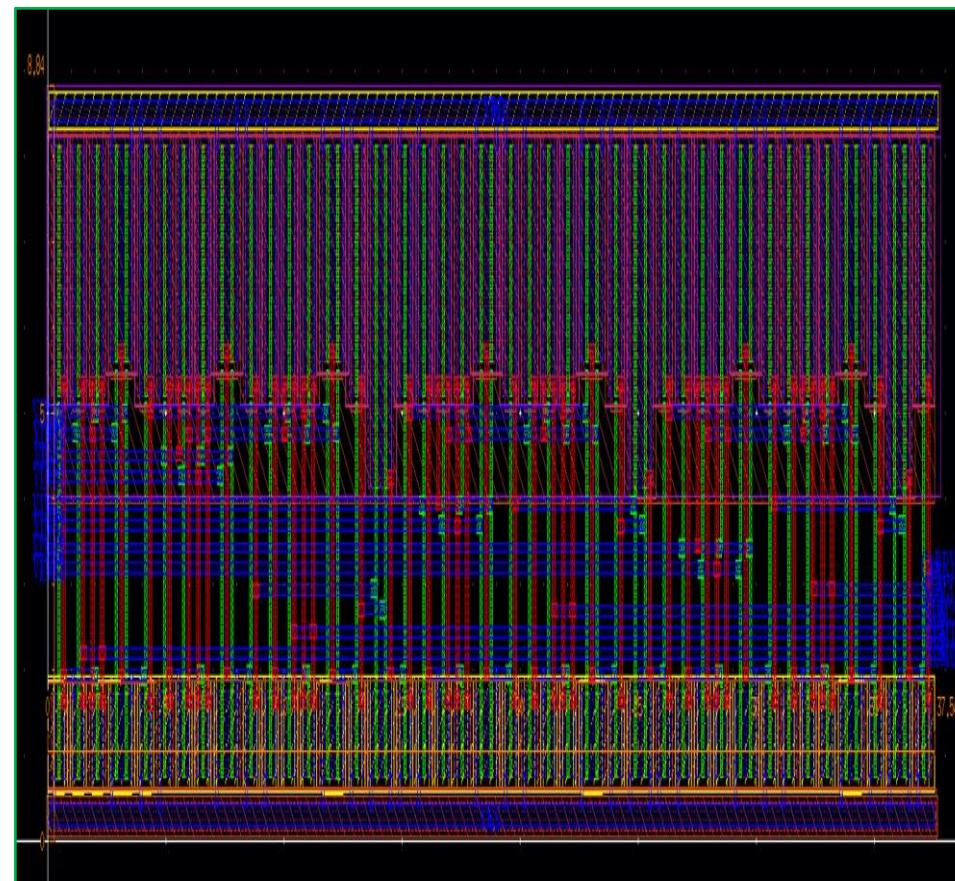
DITIGAL CIRCUIT

4BIT_ADDER

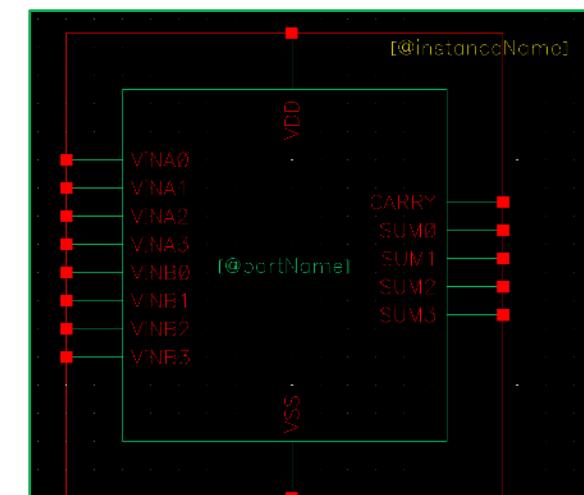
Schematic



Layout



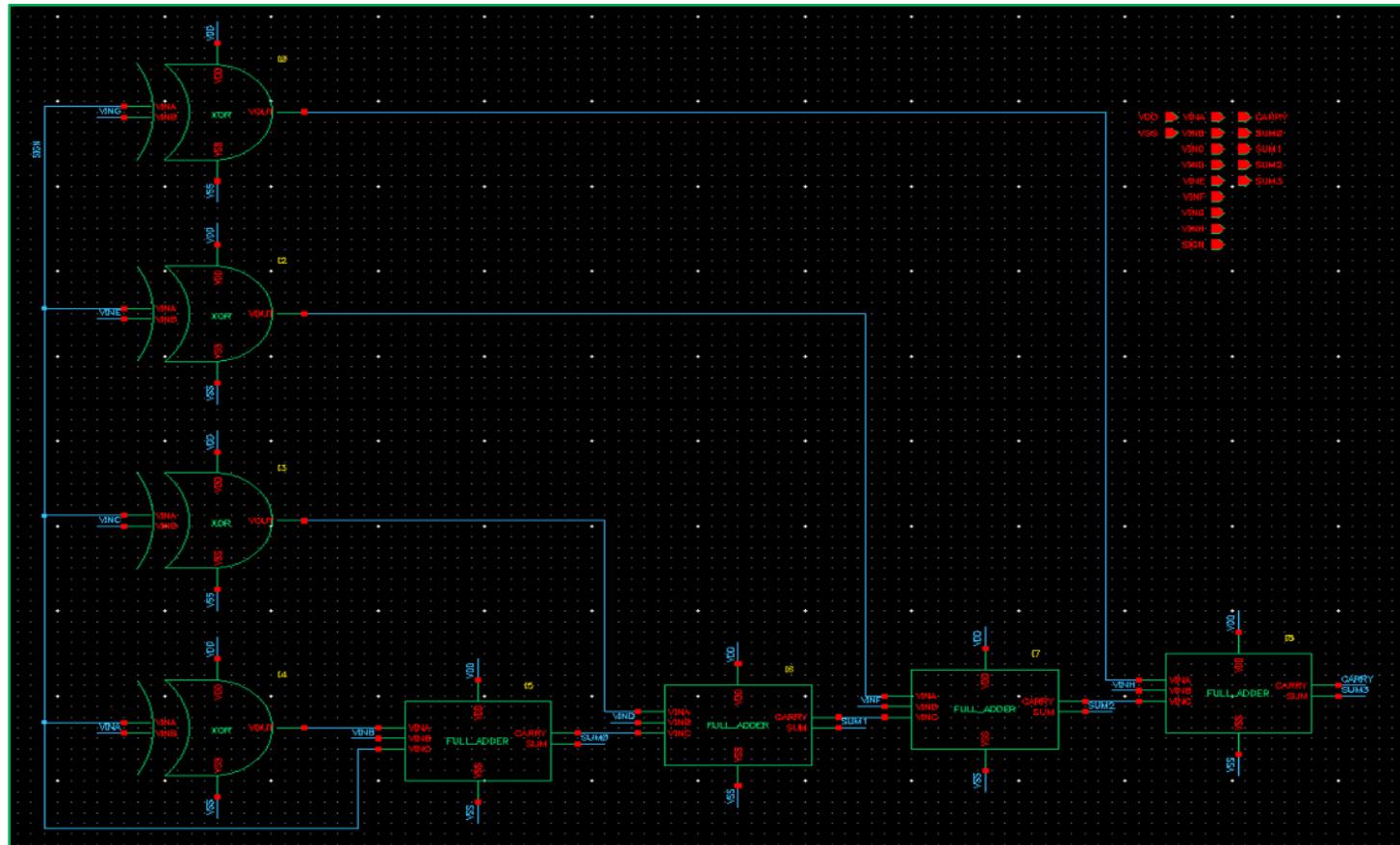
Symbol



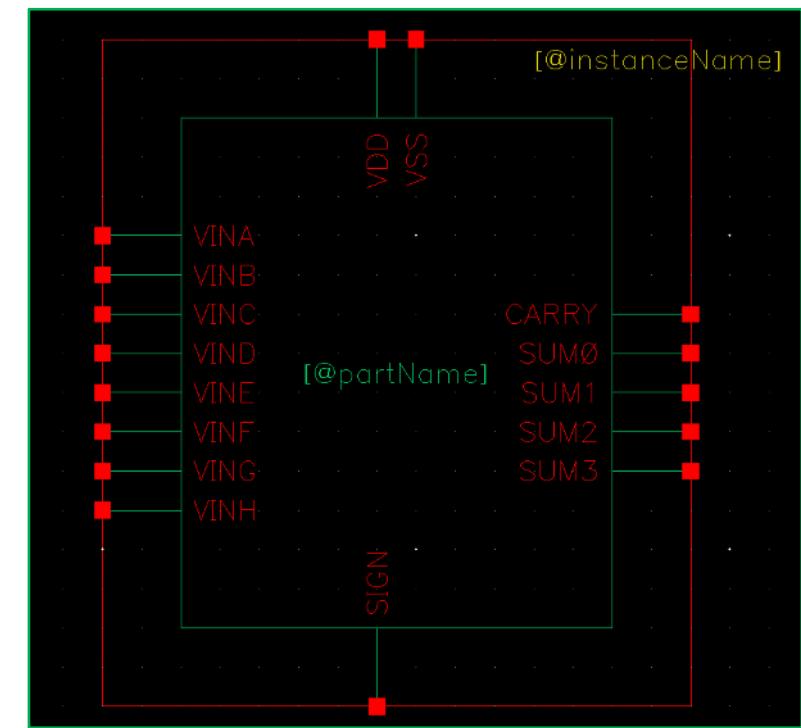
DITIGAL CIRCUIT

4BIT_SUBTRACTOR

Schematic



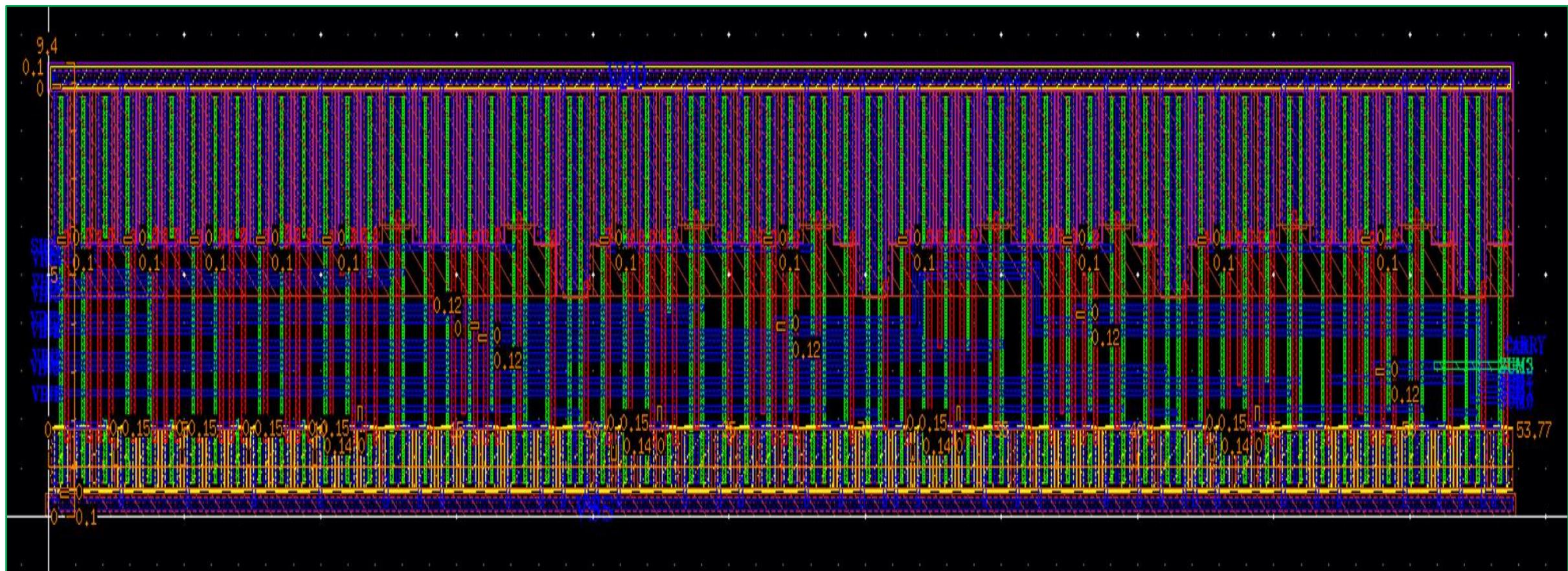
Symbol



DITIGAL CIRCUIT

4BIT_SUBTRACTOR

Layout



DITIGAL CIRCUIT

ADDER

| | Half_Adder | Full_Adder | 4Bit_Adder | 4Bit_Subtractor |
|----------------------------|-------------------|-------------------|-------------------|------------------------|
| Width (μm) | 7.91 | 17.48 | 37.54 | 53.77 |
| Length (μm) | 6.38 | 7.105 | 8.84 | 9.4 |
| Area (μm^2) | 50.4658 | 124.1954 | 331.5884 | 505.438 |

ANALOG CIRCUIT

1

Common Source Amp

2

Differential Amp (Single-ended Output)

ANALOG CIRCUIT

AMP

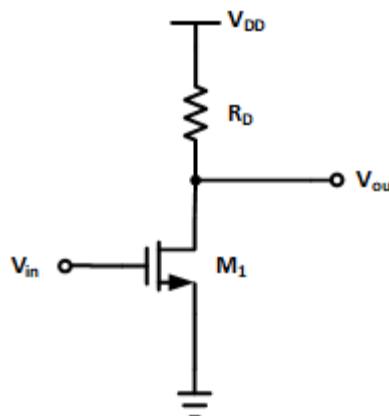
Spec

| | Res | NMOS0 | NMOS1 | NMOS2 | NMOS3 | PMOS0 | PMOS1 |
|-----------------|---------|-------|-------|-------|-------|-------|-------|
| CS_Amp | 4k ohm | 1um | X | X | X | X | X |
| Diff_Amp | 25k ohm | 2um | 2um | 800nm | 800nm | 250nm | 250nm |

| | gm | Gain (Av) | Bandwidth | Power Consumption |
|-----------------|----------------|------------|--------------|-------------------|
| CS_Amp | ~754.59[uA/V] | 6.334[dB] | 3.01[GHz] | 123.153[uW] |
| Diff_Amp | ~189.955[uA/V] | 13.448[dB] | 262.271[MHz] | 43.469[uW] |

ANALOG CIRCUIT

CS_AMP



Large-Signal Analysis

Case 1) M1 off

$$V_{out} = V_{DD} - I_D \cdot R_D$$

Cuz M1's MOSFET is off, Drain Current (I_d) = 0.
So $V_{out} = V_{DD}$.

<Common-Source Stage Basic Circuit>

Case 2) $V_{in} > M1$'s threshold Voltage (V_{th})

$$V_{out} = V_{DD} - \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L} \right) (V_{GS} - V_{TH})^2 \cdot R_D$$

Case 2) $V_{in} > M1$'s threshold Voltage (V_{th})

MOSFET Condition

V_{in} Condition

M1 State & V_{out} Condition

$$V_{GS} < V_{TH}$$

$$0 < V_{in} < V_{TH}$$

M1 Off, $V_{out} = V_{DD}$

$$V_{GS} - V_{TH} < V_{DS}$$

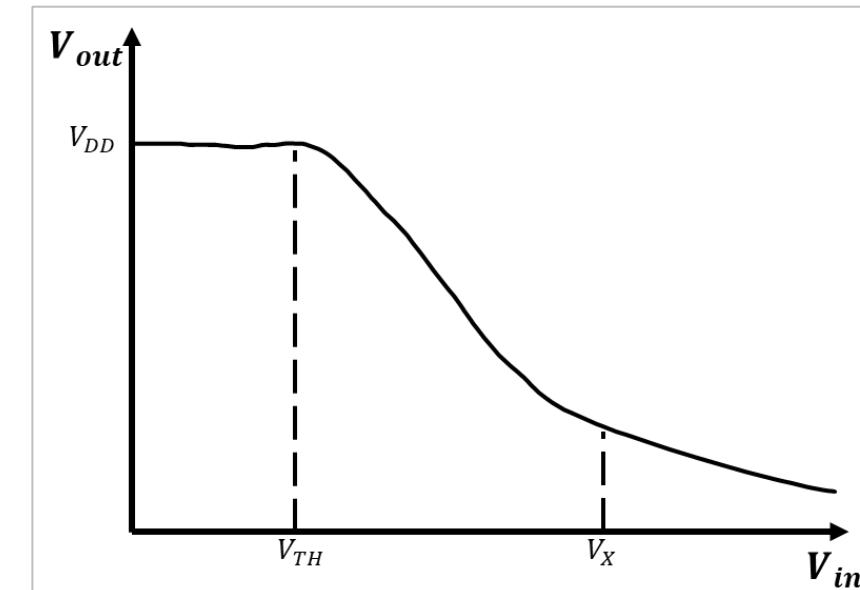
$$V_{TH} < V_{in} < V_X$$

M1 On(Saturation), $V_{out} = V_{DD} - \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L} \right) (V_{GS} - V_{TH})^2 \cdot R_D$

$$V_{GS} - V_{TH} > V_{DS}$$

$$V_X < V_{in} < V_{DD}$$

M1 On(Triode)

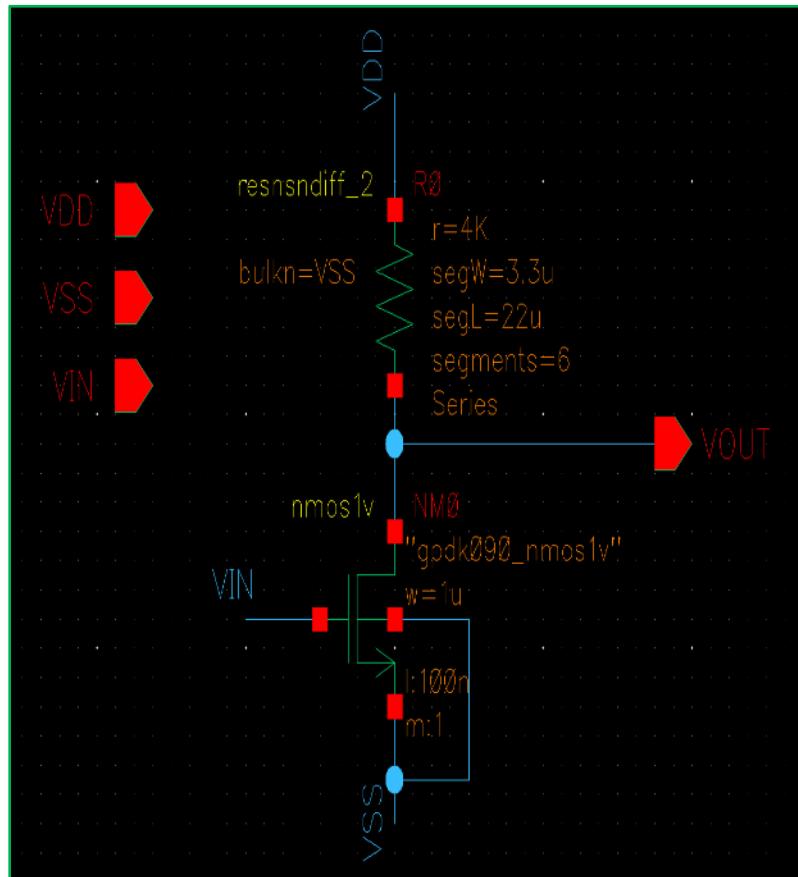


<Common-Source Stage Large-Signal Behavior>

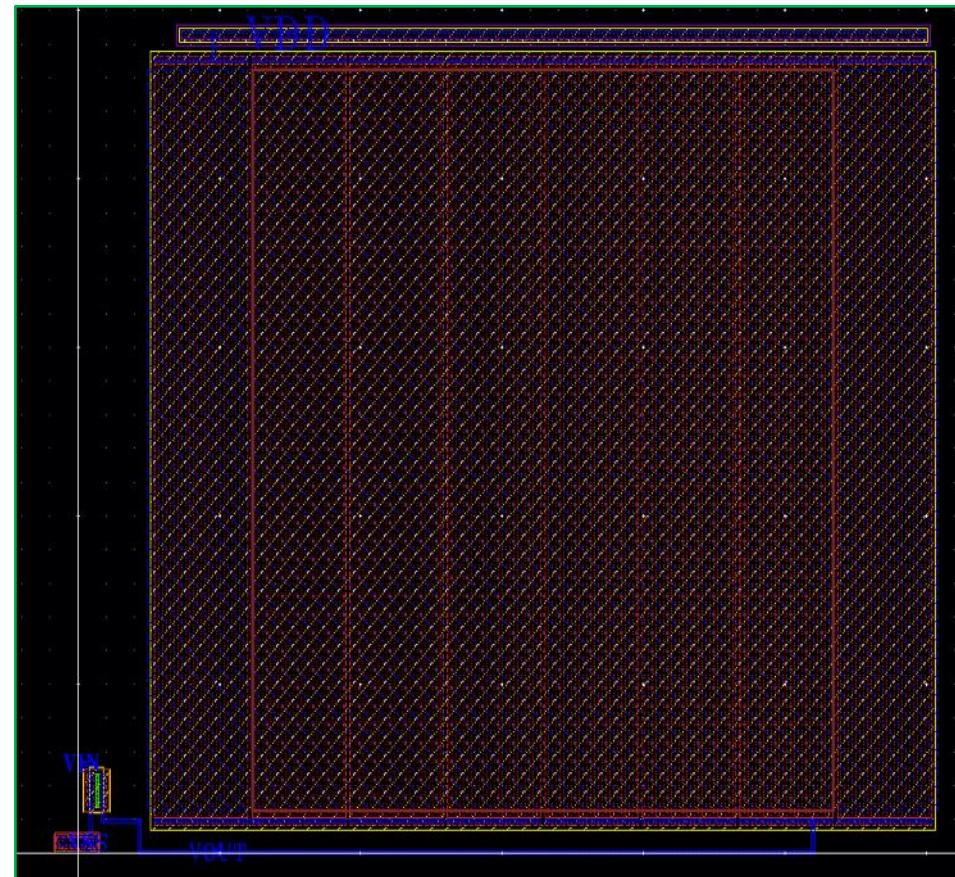
ANALOG CIRCUIT

CS_AMP

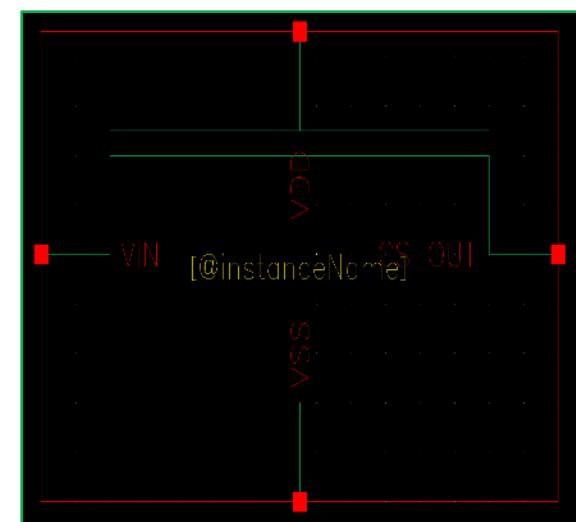
Schematic



Layout

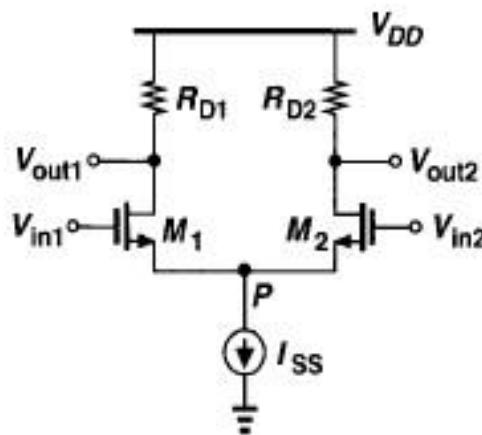


Symbol



ANALOG CIRCUIT

DIFF_AMP



<Differential Amplifier Basic Circuit>

$$v_O = A_d v_{Id} + A_{cm} v_{Icm}$$

차동모드 이득(A_{cm}), 차동모드 입력(v_{Icm})
차동 이득이 높은 값이 나오는 것이 이상적

공통모드 이득(A_{cm}), 공통모드 입력(v_{Icm})
공통 모드 이득이 0이 나오는 것이 이상적

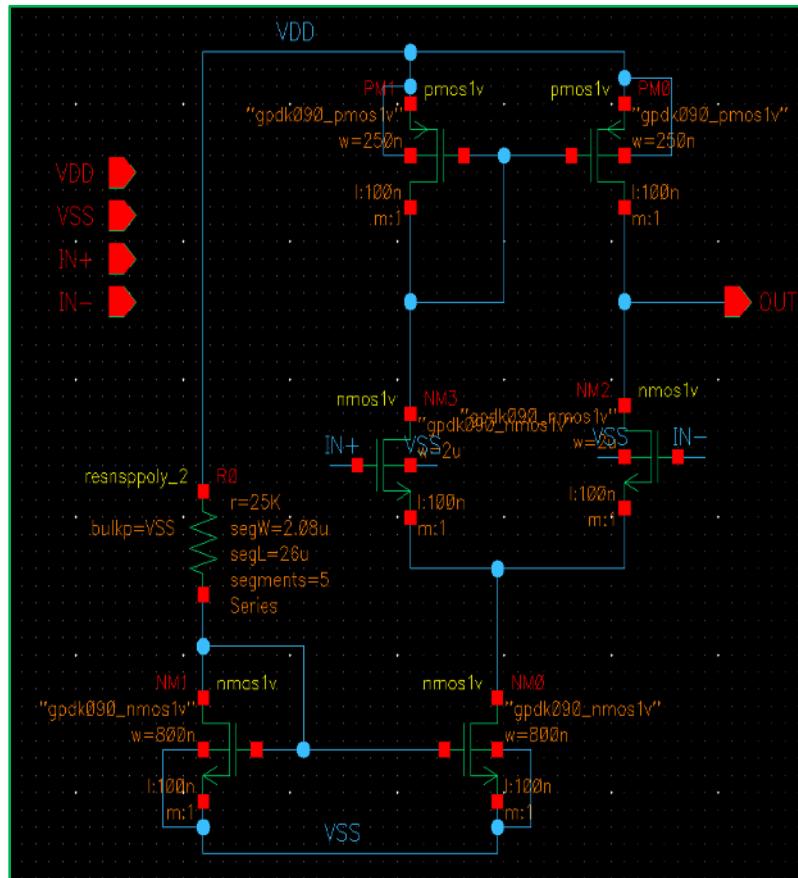
Common Mode Gain (A_{cm}) cannot be 0.
So, parameter exist. It is “Common Mode Rejection Ratio, CMRR).

$$CMRR = \left| \frac{A_{DM}}{A_{CM-DM}} \right| \quad \text{The higher CMRR, the better.}$$

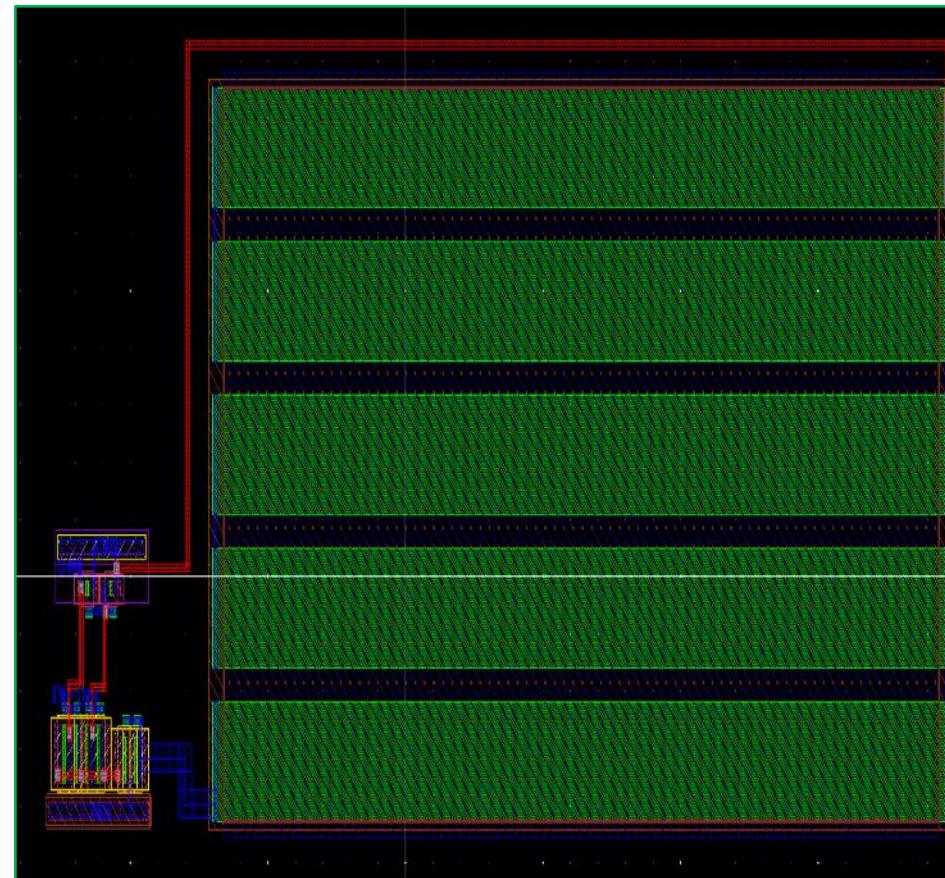
ANALOG CIRCUIT

DIFF_AMP

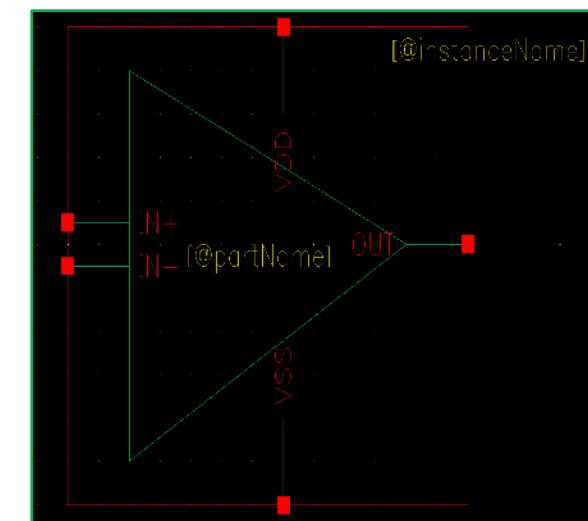
Schematic



Layout



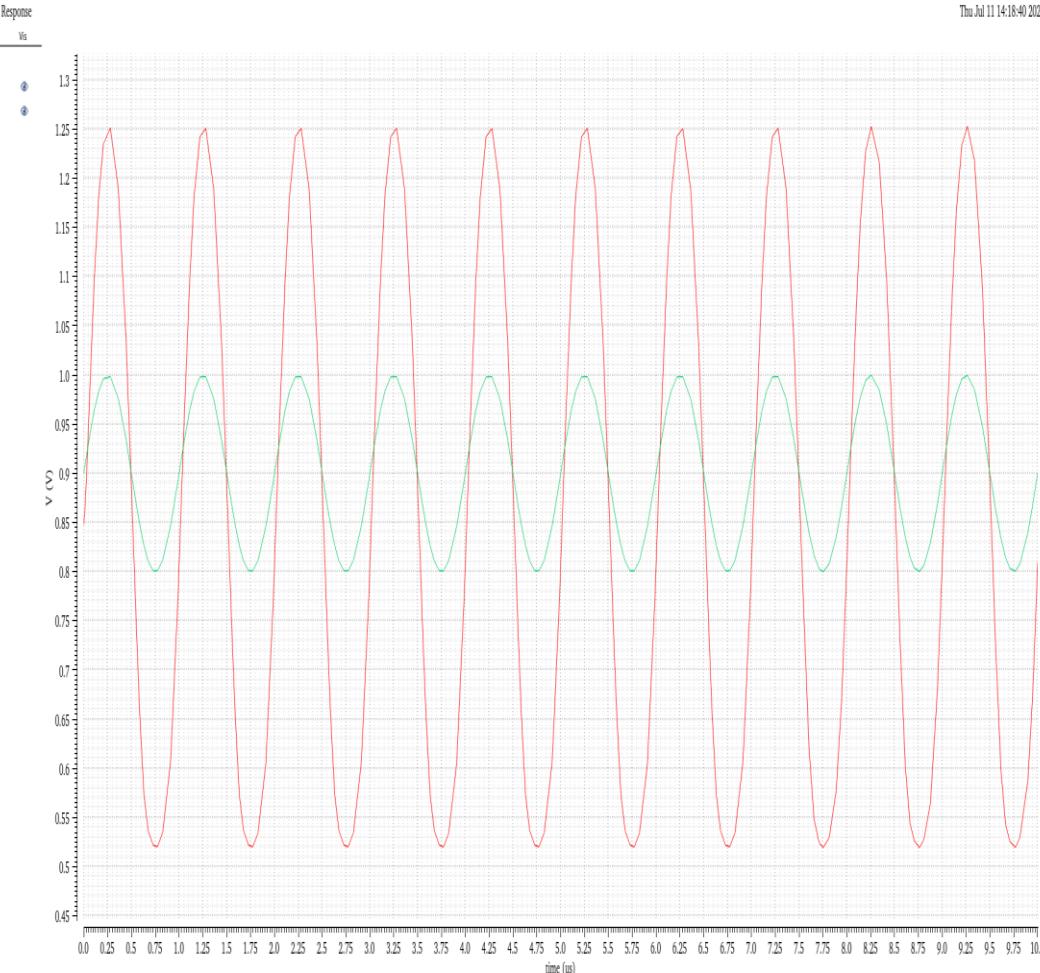
Symbol



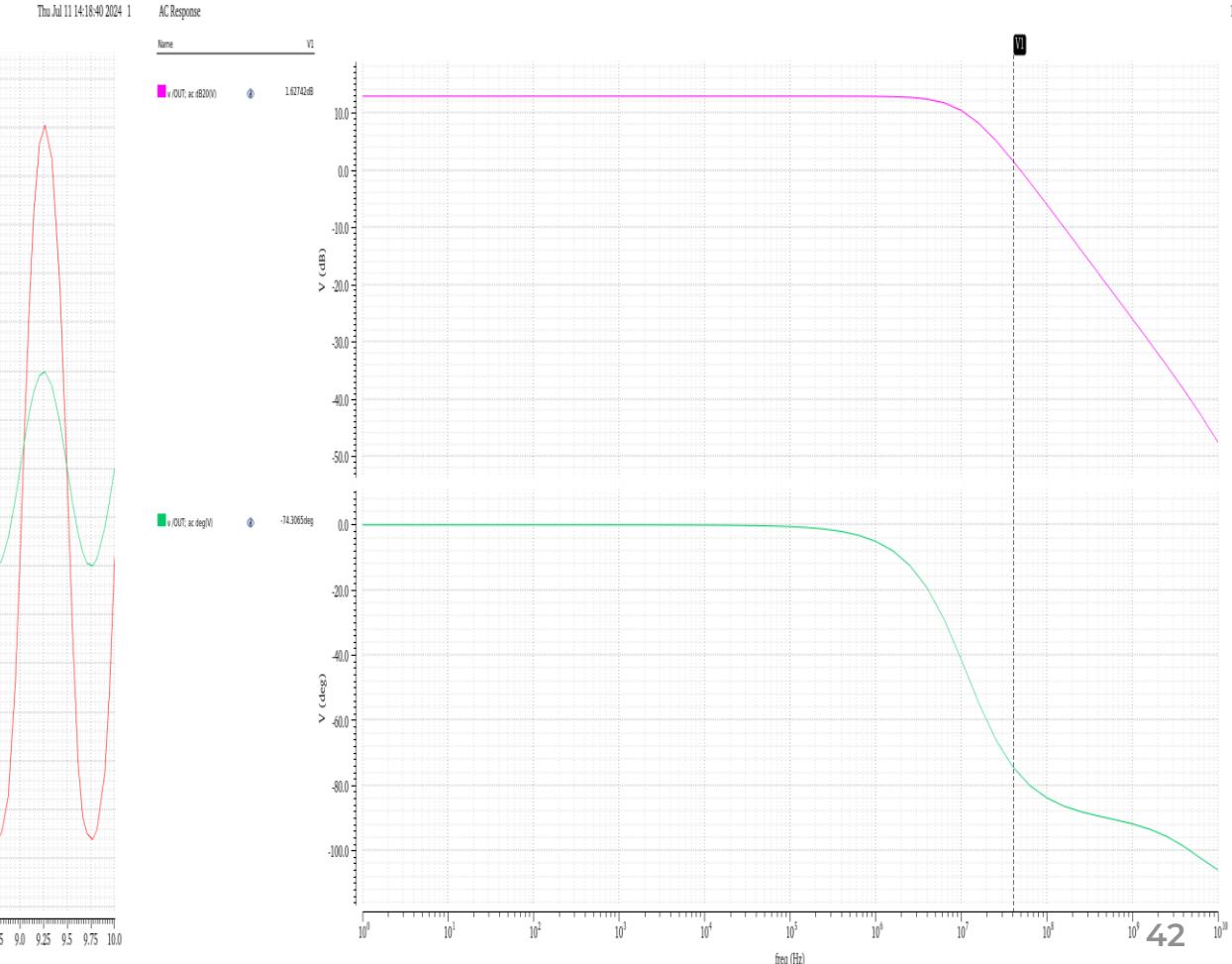
DITIGAL CIRCUIT

DIFF_AMP

Trans
&
AC
AC



Simulation



ONE CHIP

1

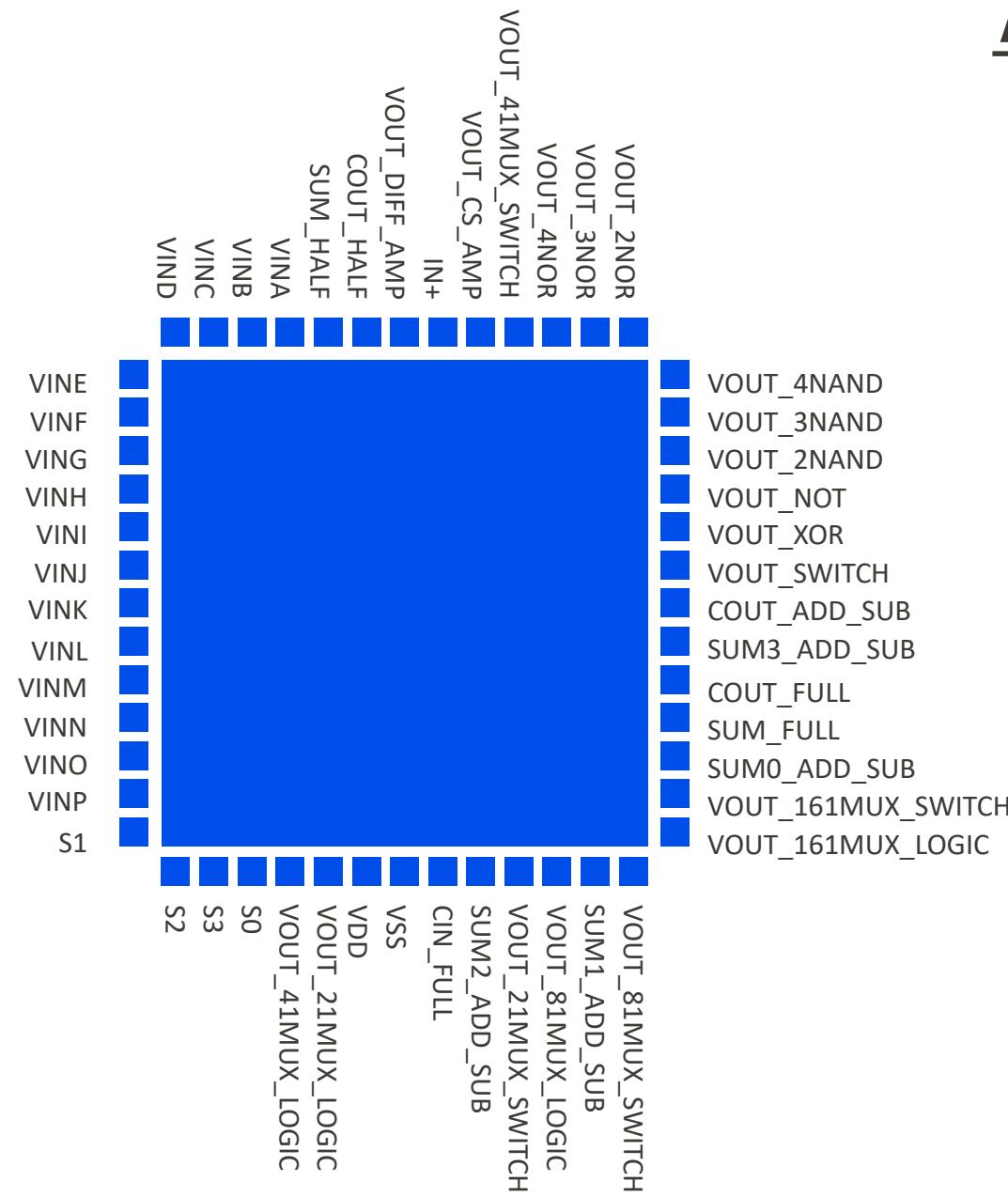
Chip's Pin Array

2

Total One Chip Design

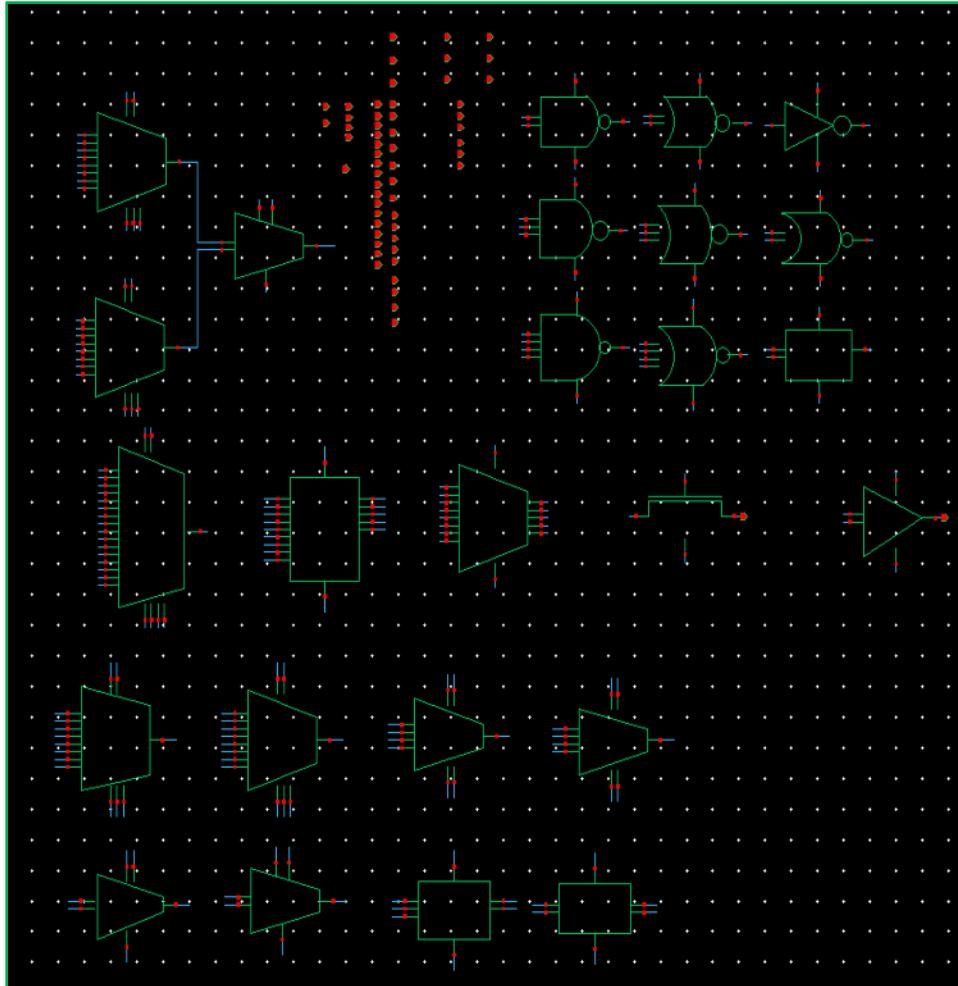
ONE CHIP

PIN MAPPING

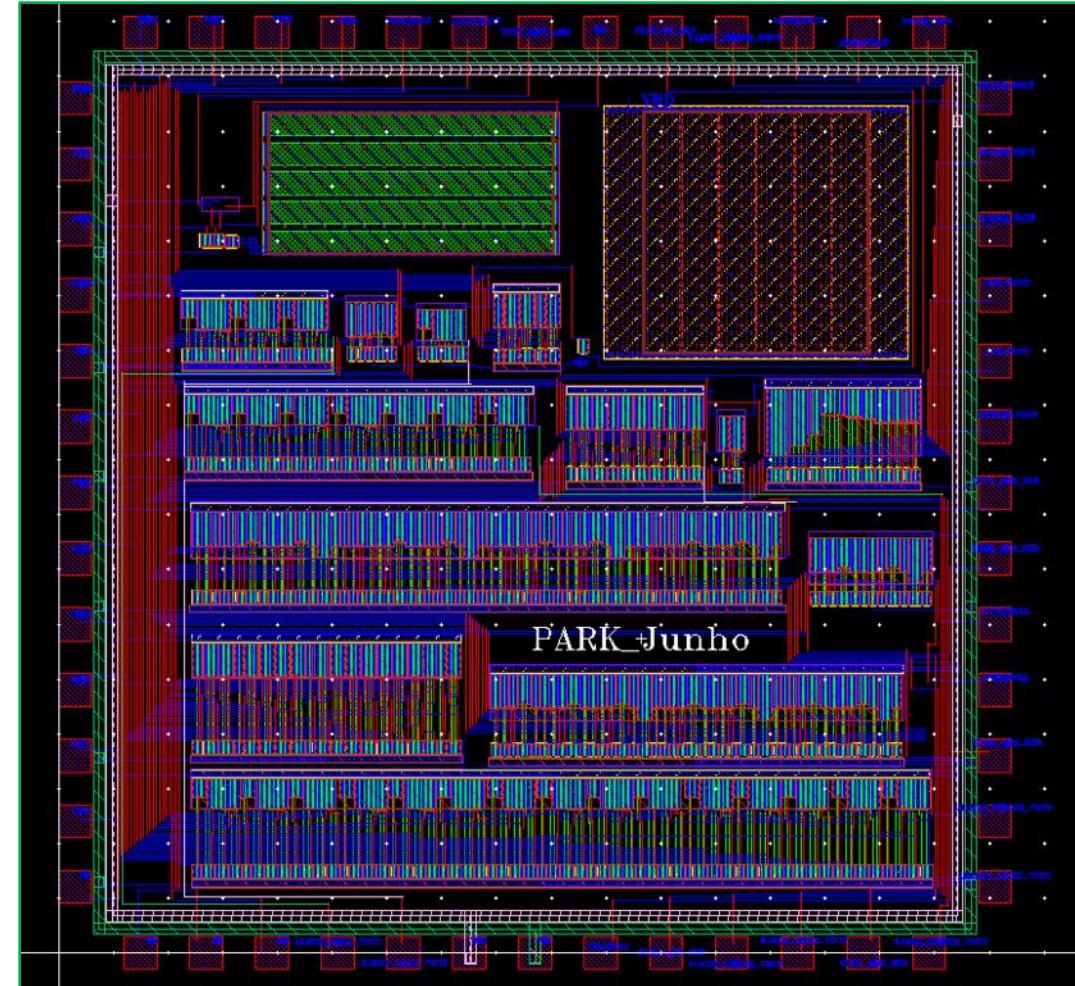


ONE CHIP

Schematic

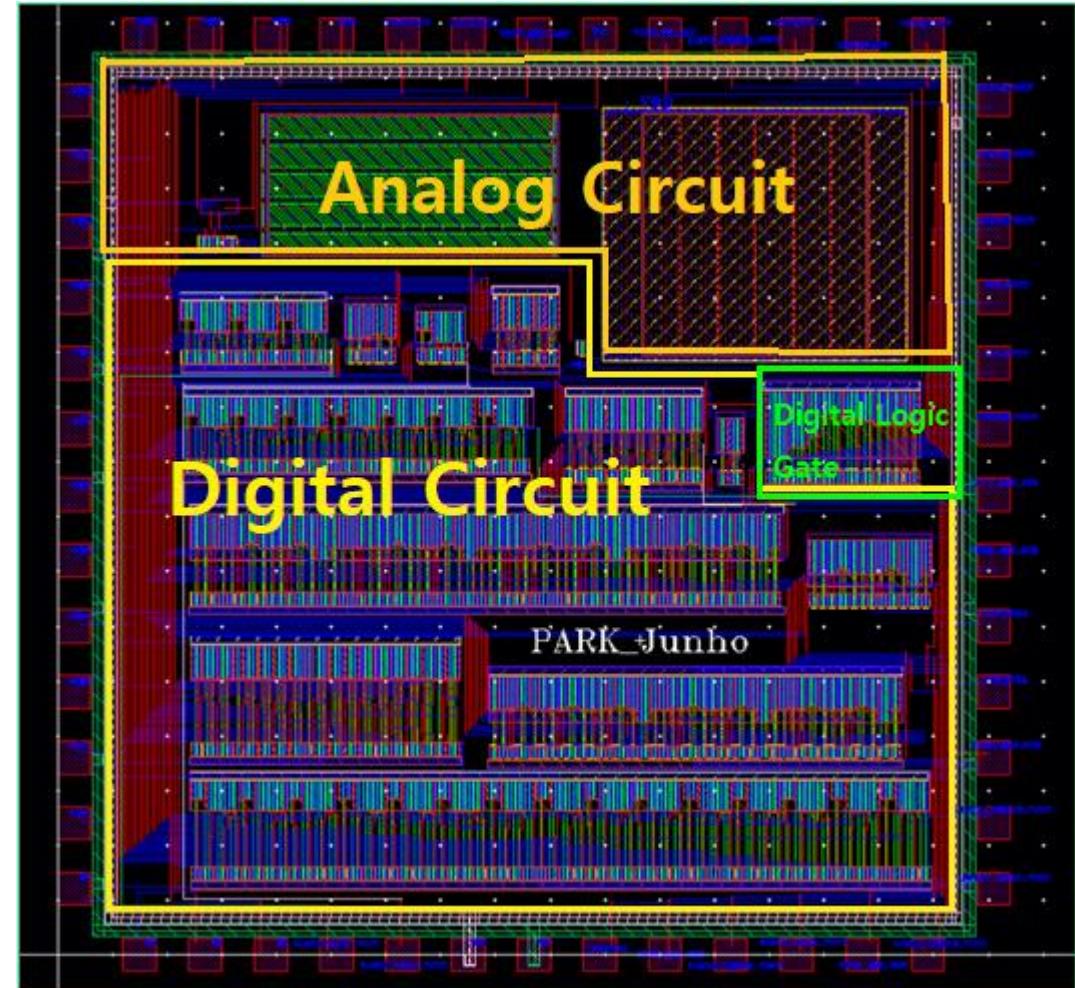
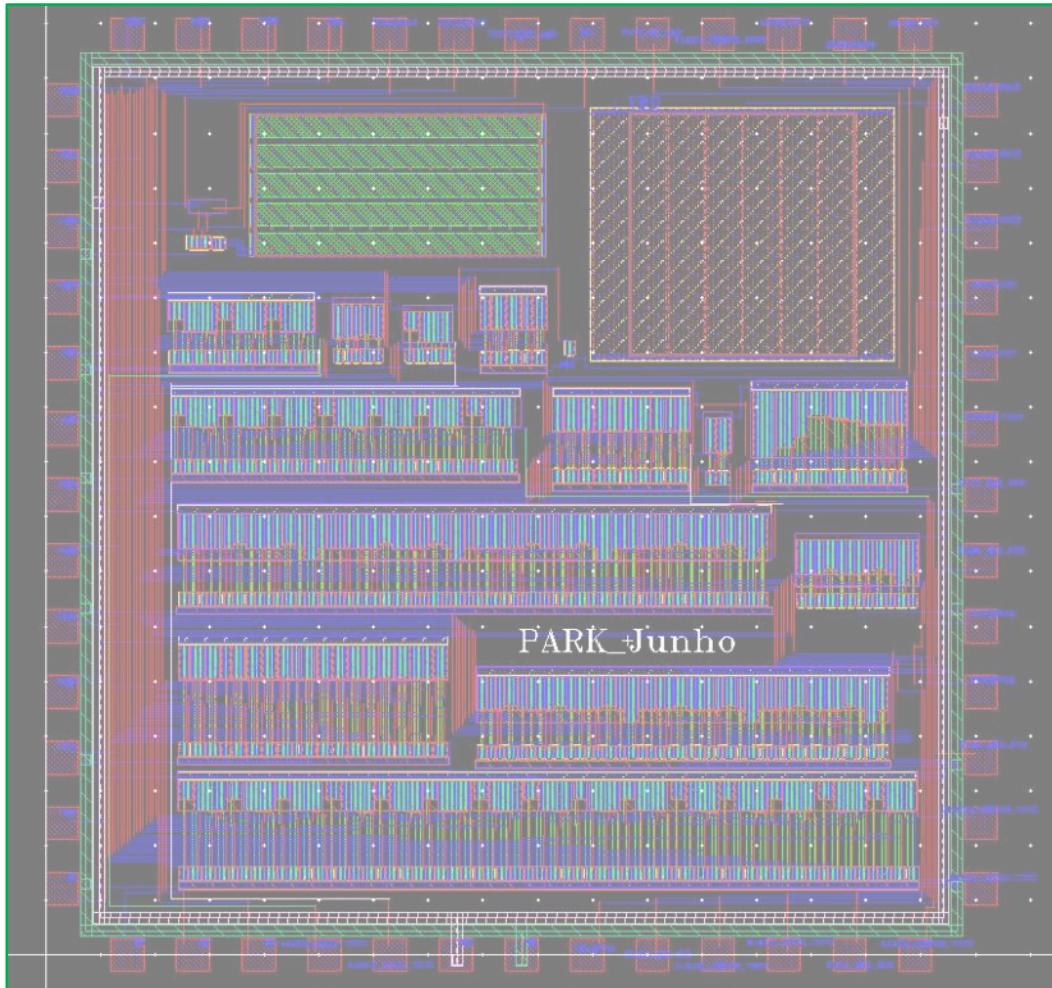


Layout



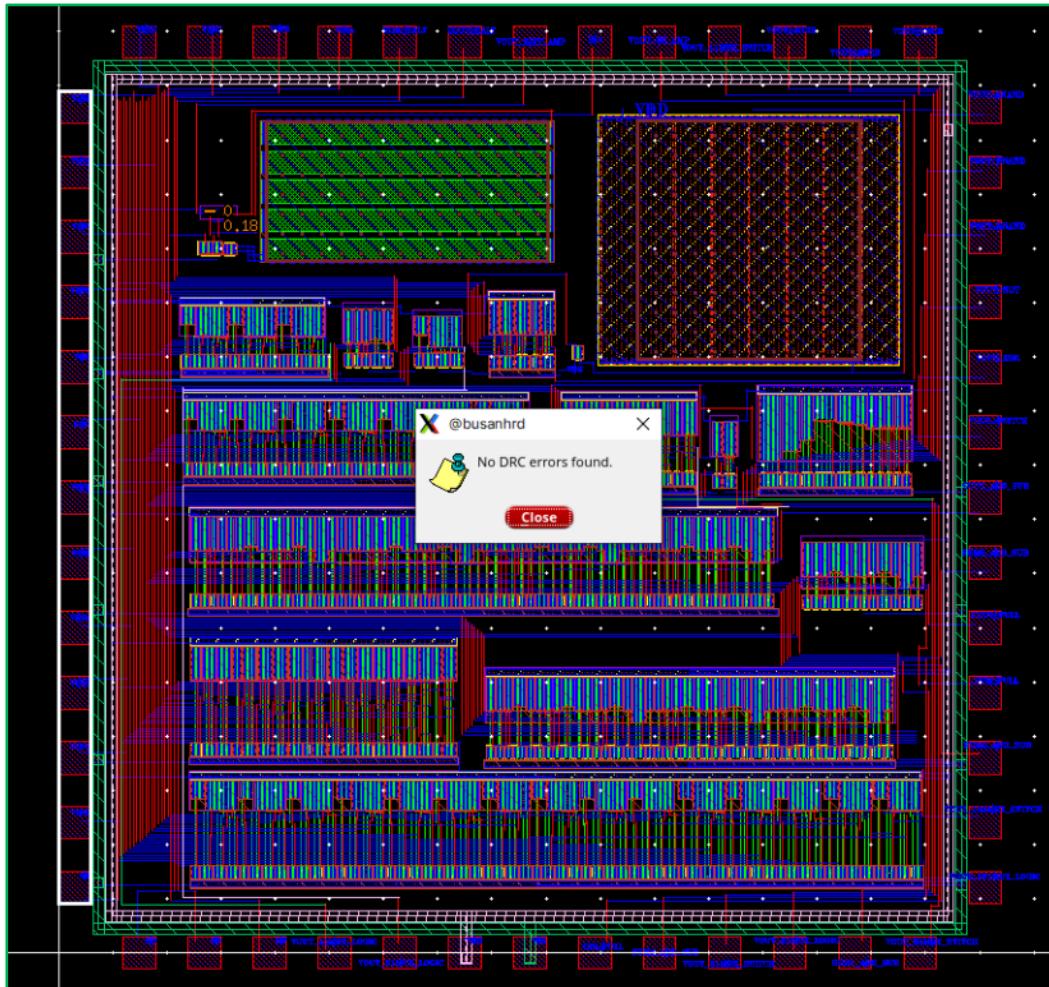
ONE CHIP

Layout

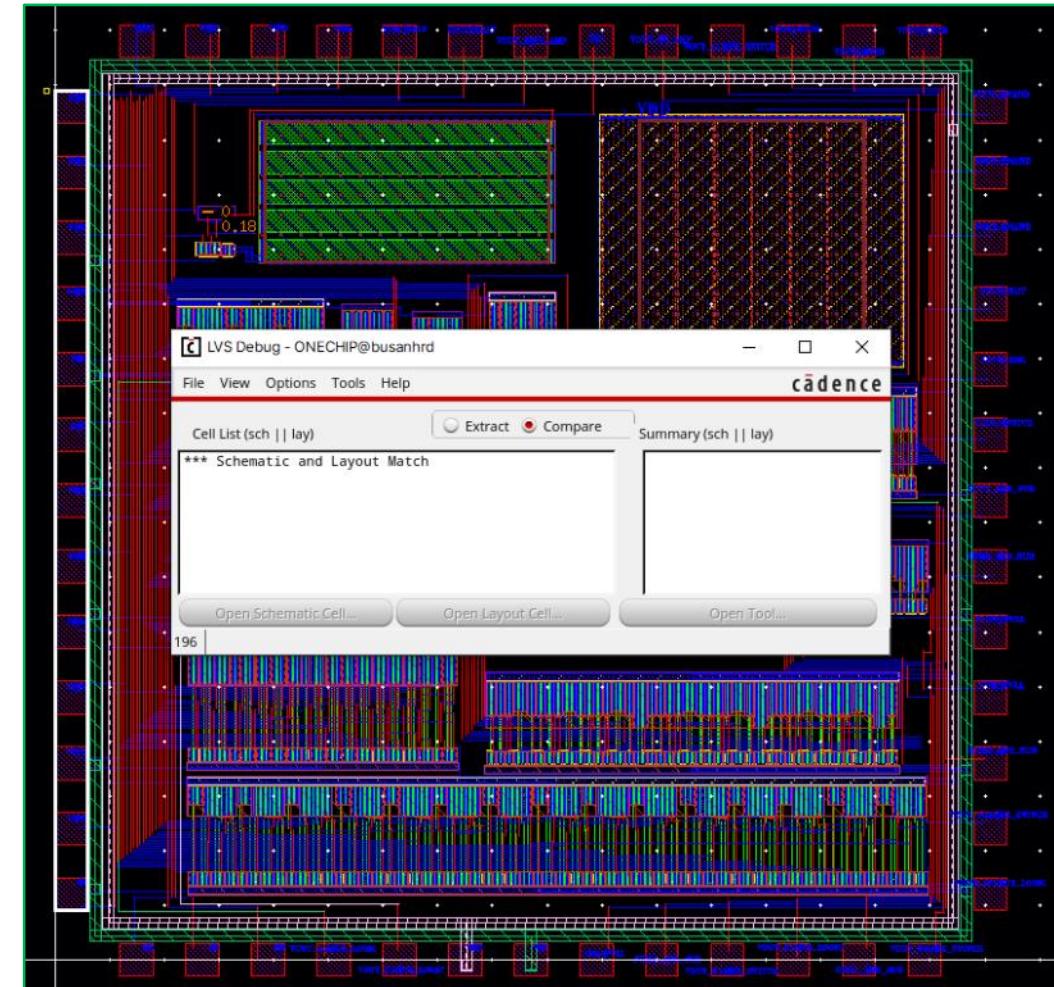


ONE CHIP

DRC Result



DRC Result



CONTACT



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010-8920-3089

hello