

Xilinx Vivado Design Suite

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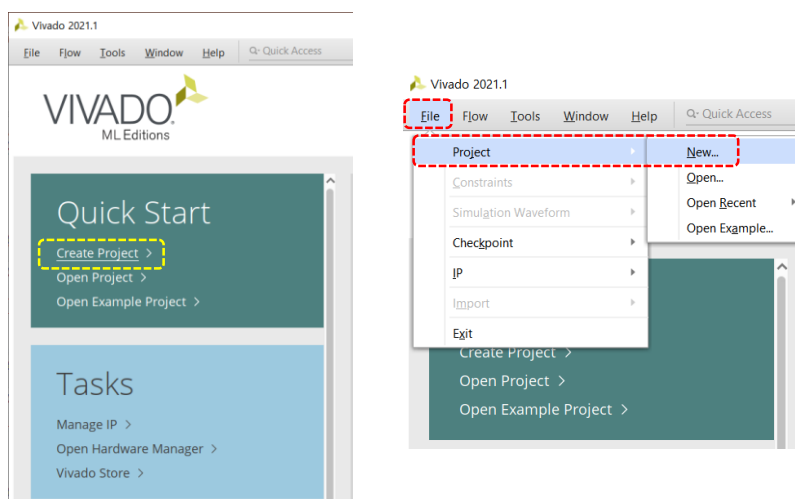
1. Vivado Design Suite
2. Vivado IDE
3. Project 생성
4. 설계 입력
5. RTL Simulation
6. Design Synthesis
7. Design Implementation
8. FPGA Device Programming

Verilog HDL

Xilinx Vivado Design Suite

3.1 Project 생성 – New Project

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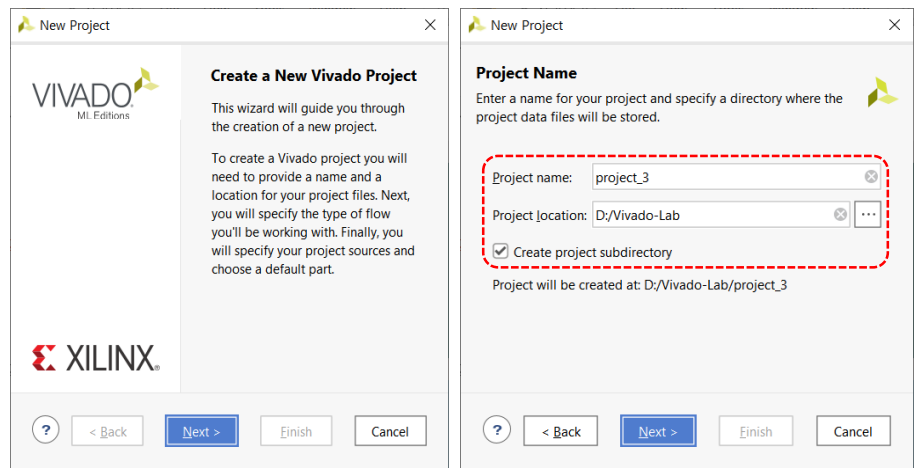
Verilog HDL

Xilinx Vivado Design Suite

3.1 Project 생성 – New Project

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Project Name, Location 설정



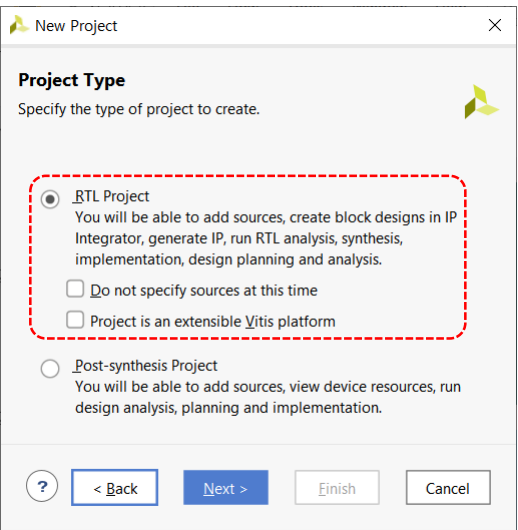
Verilog HDL

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3.1 Project 생성 – New Project

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Project Type 설정



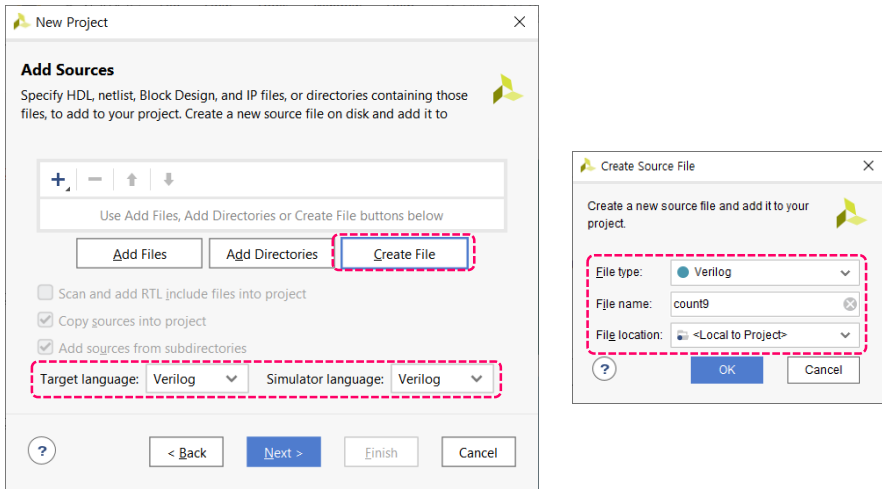
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3.2 Project 생성 – Add Sources

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■ Add or Create Sources



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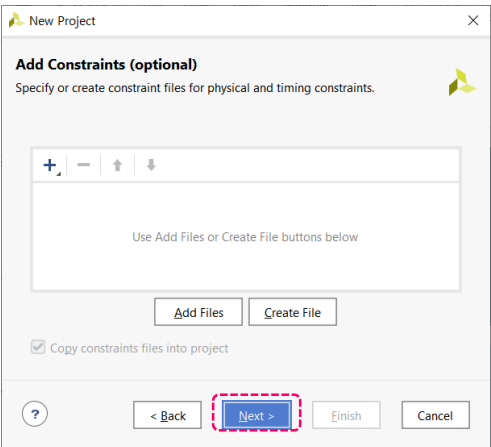
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3.3 Project 생성 – Add Constraints

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■ Add Constraints

❖ Constraint 파일(Xilinx Design Constraint; XDC) 생성 및 기존 파일 추가



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3.4 Project 생성 – Default Part

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❑ Default Part; FPGA 디바이스 및 보드 선택 (xc7s75fgga484-1)

New Project

Default Part

Choose a default Xilinx part or board for your project.

Parts

Boards

Reset All Filters

Category: General Purpose

Package: fgga484

Temperature: All Remaining

Family: Spartan-7

Speed: All Remaining

Static power: All Remaining

Search:

Part	I/O Pin Count	Available IOBs	LUT Elements	FlipFlops	Block RAMs	Ultra RAMs	DSP
xc7s50fgga484-1Q	484	250	32600	65200	75	0	120
xc7s75fgga484-2	484	338	48000	96000	90	0	140
xc7s75fgga484-1	484	338	48000	96000	90	0	140
xc7s75fgga484-1IL	484	338	48000	96000	90	0	140

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Next >

Finish

Cancel

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3.5 Project 생성 – Project Summary

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❑ New Project Summary

New Project

VIVADO
ML Editions

XILINX

To create the project, click Finish

New Project Summary

A new RTL project named 'project_3' will be created.

1 source file will be added.

No constraints files will be added. Use Add Sources to add them later.

The default part and product family for the new project:
Default Part: xc7s75fgga484-1
Product: Spartan-7
Family: Spartan-7
Package: fgga484
Speed Grade: -1

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Next >

Finish

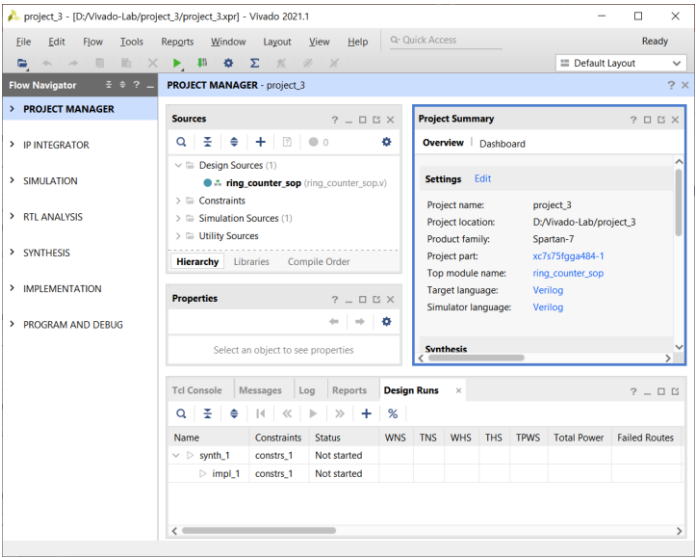
Cancel

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3.6 Project 생성 – 완료된 상태

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