Verilog HDL 개요(2)

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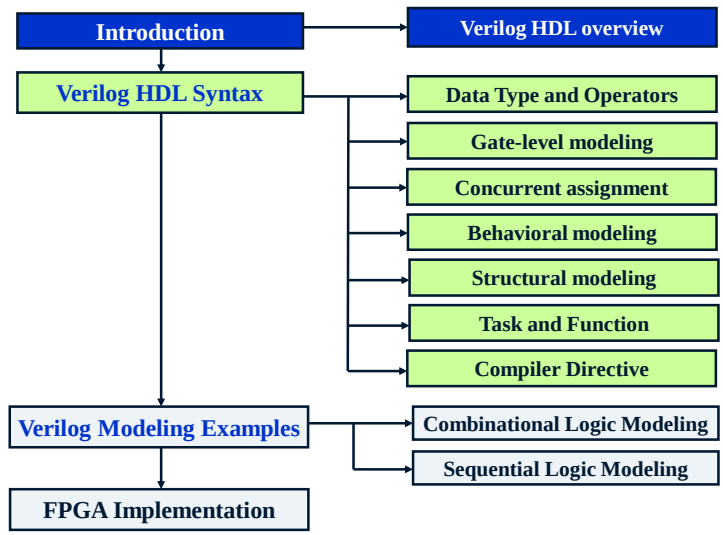
Learning Map



수박과 호박의 차이

수박? 호박?

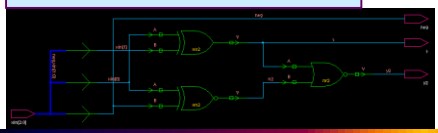
수박과 호박의 차이

HDL(Hardware Description Language)

```
module booth_enc(xin, y, y2, neg);
   input  [2:0] xin;
   output       y, y2, neg;
   reg    [2:0] tmp;

   assign   y = tmp[2];
   assign  y2 = tmp[1];
   assign neg = tmp[0];

   always @(xin) begin
      case(xin)
         0   : tmp = 3'b000;
         1,2 : tmp = 3'b100;
         3   : tmp = 3'b010;
         4   : tmp = 3'b011;
         5,6 : tmp = 3'b101;
         7   : tmp = 3'b001;
     endcase
   end
endmodule
```

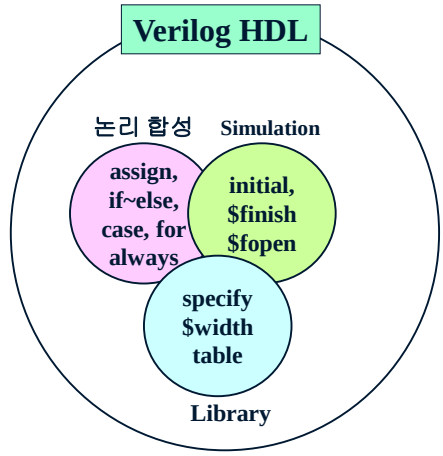
C Program

```
main() {
 int bitw_a, bitw_b, bitw_rbpp, bitw, a, b;
 int deci_a, deci_b;
 int bin_a[64], bin_b[64];
 int bin_z[128];
 int rec[32][4];
 int pp[32][65];
 int cor[32], cor_vec[32][2];
 int rbpp[32][67][2];

if(bitw_b%2 == 1)
   num_bpp = (bitw_b+1)/2;
else
   num_bpp = bitw_b/2;

Mba(bin_b,rec,cor,num_bpp,fp);

PPgen(bin_a,rec,bitw_a,num_bpp,pp,cor,fp);
```



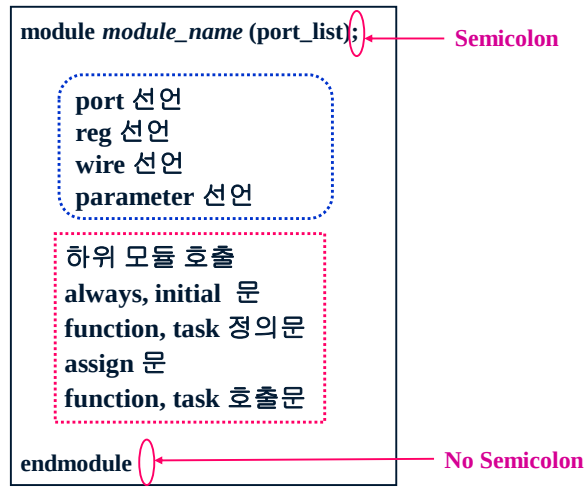
HDL is used to design hardware,
Not to program software

Verilog HDL 개요

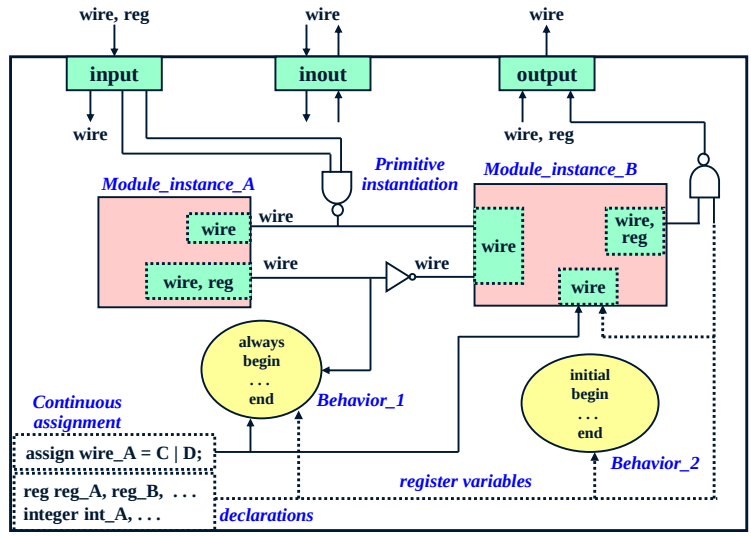


Verilog HDL 구문

Verilog HDL의 모듈

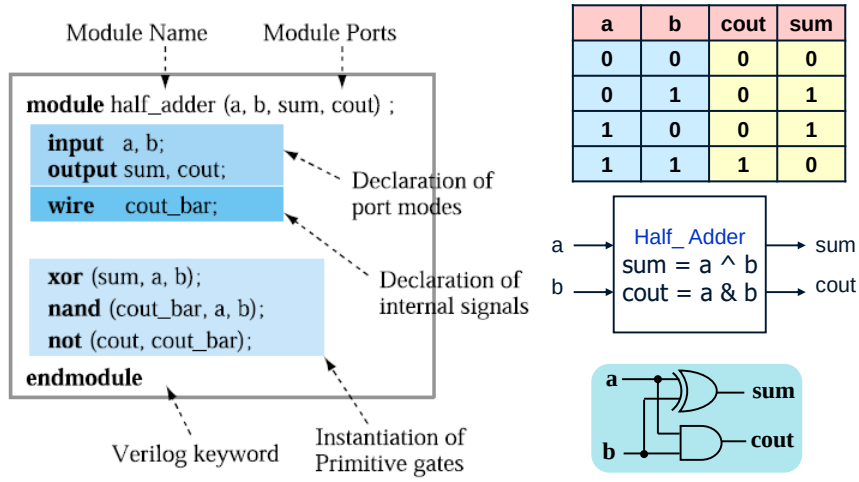


Verilog HDL의 모듈



Verilog 모델링 예

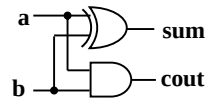
❑ 게이트 프리미티브를 이용한 모델링 예 (반가산기 회로)



a	b	cout	sum
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Verilog 모델링 예

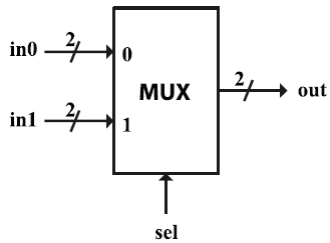
❑ 연속 할당문을 이용한 모델링




```
module half_adder2(a, b, sum,
cout);
   input a, b;
   output sum, cout;

     assign cout = a & b;
     assign sum  = a ^ b;
endmodule
```


Verilog 모델링 예

❑ 행위수준 모델링 (조합논리회로)

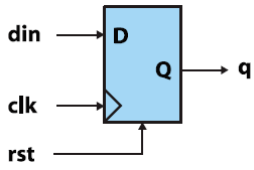



```
module mux2b_if(in0, in1, sel, out);
  input  [1:0] in0, in1;
  input        sel;
  output [1:0] out;
  reg    [1:0] out;

  always @(sel or in0 or in1) begin
    if (sel ==0)
       out = in0;
    else
       out = in1;
  end
endmodule
```

Verilog 모델링 예

❑ 행위수준 모델링 (순차회로)

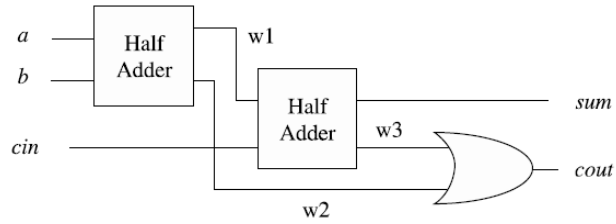
❖ 클록의 상승에지에서 동작하는 D 플립플롭




```
module D_ff (clk, din, rst, q);
   input  clk, din, rst;
   output q;
   reg    q;

always @(posedge clk or posedge rst)
begin
   if (rst == 1)
       q <= 0;
   else
       q <= din;
end

endmodule
```


Verilog 모델링 예

❑ 하위 모듈 인스턴스를 이용한 구조적 모델링




```
module full_add(a, b, cin, sum, cout);
  input   a, b, cin;
  output  sum, cout;
  wire    w1, w2, w3;                                  //1비트 wire 선언은 생략 가능

  half_adder U1(.a(a), .b(b), .sum(w1), .cout(w2)); // 이름에 의한 포트 매핑
  half_adder U2(w1, cin, sum, w3);                  // 순서에 의한 포트 매핑
  or         U3(cout, w2, w3);                      // 게이트 프리미티브 인스턴스
endmodule
```