MINI RISC Opcodes				Syntax															
Category	**TAG**	**Description**	**Mnemonic**	**15**	**14**	**13**	**12**	**11**	10	9	8	7	6	5	4	3	2	1	0
--	--	No Operation	NOP	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X
R- TYPE	ALU	Multiply 2 regs and store in 3rd	MUL	0	0	0	0	1	X	X	X	reg_1			reg2			X	X
R- TYPE	ALU	Subtract 2 regs and store in 3rd	SUB	0	0	0	1	0	res			reg_1			reg2			X	X
R- TYPE	ALU	Divide 2 regs and store in 3rd	DIV	0	0	0	1	1	X	X	X	reg_1			reg2			X	X
R- TYPE	ALU	Complement all the bits in reg	NOT	0	0	1	0	0	res			reg_1			X	X	X	X	X
R- TYPE	ALU	AND 2 regs and store in 3rd	AND	0	0	1	0	1	res			reg_1			reg_2			X	X
R- TYPE	ALU	OR 2 regs and store in 3rd	OR	0	0	1	1	0	res			reg_1			reg_2			X	X
R- TYPE	ALU	XOR 2 regs and store in 3rd	XOR	0	0	1	1	1	res			reg_1			reg_2			X	X
R- TYPE	ALU	Increment	INC	0	1	0	0	0	res			reg_1			X	X	X	X	X
R- TYPE	ALU	Compare 2 registers	CMP	0	1	0	0	1	X	X	X	reg_1			reg_2			X	X
R- TYPE	ALU	Rotate Right	RR	0	1	0	1	0	res			reg_1			X	X	X	X	X
R- TYPE	ALU	Rotate Left	RL	0	1	0	1	1	res			reg_1			X	X	X	X	X
R- TYPE	ALU BIT	Set Bit	SETB	0	1	1	0	0	reg			reg_bit_position				X	X	X	X
R- TYPE	ALU BIT	Clear Bit	CLRB	0	1	1	0	1	reg			reg_bit_position				X	X	X	X
R- TYPE	ALU BIT	Complement Bit	CPLB	0	1	1	1	0	reg			reg_bit_position				X	X	X	X
R- TYPE	ALU BIT	Set Flag	SETF	0	1	1	1	1	X	X	X	flag_bit_position				X	X	X	X
R- TYPE	ALU BIT	Clear Flag	CLRF	1	0	0	0	0	X	X	X	flag_bit_position				X	X	X	X
R- TYPE	ALU BIT	Complement Flag	CPLF	1	0	0	0	1	X	X	X	flag_bit_position				X	X	X	X
B- TYPE	BRANCH	load addr to jump to	LOADBR	1	0	0	1	0	11 bit address										
B- TYPE	BRANCH	Jump if flag it is set	JF	1	0	0	1	1	X	X	X	flag_bit_position				X	X	X	X
M- TYPE	RAM	Loads byte held at an address	LOAD	1	0	1	0	0	reg			[reg2] (has addr)			X	X	X	X	X
M- TYPE	RAM	Stores value in reg to memory	STORE	1	0	1	0	1	reg			[reg2] (has addr)			X	X	X	X	X
I- TYPE	IMMEDIATE	Loads Immediate byte to reg	LBL	1	0	1	1	0	reg			Immediate_byte							
I- TYPE	IMMEDIATE	Loads byte held at an address, to upper 16 bits	LBH	1	0	1	1	1	reg			Immediate_byte							
Uncategorized	REG	Move from reg a to reg b	MOV	1	1	0	0	0	destination			source			X	X	X	X	X
R-TYPE	ALU	ADD 2 regs and store in 3rd	ADD	1	1	0	0	1	res			reg_1			reg2			X	X
Uncategorized				1	1	0	1	0	X	X	X	reg							
Uncategorized				1	1	0	1	1	X	X	X	Port_bit_position							
Uncategorized				1	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X
Uncategorized	INPUT	Move to registers from I/O pins	MOVIN	1	1	1	0	1	X	X	X	X	X	X	X	X	X	X	X
Uncategorized	INPUT	Mov IO Bit to IO flag	MOVB	1	1	1	1	0	X	X	X	X	X	X	X	X	X	X	X
Uncategorized	MISC	Halt or Stop execution	HALT	1	1	1	1	1	X	X	X	X	X	X	X	X	X	X	X