



EXPERIMENT NO: 4

AIM:- Verification of truth table for positive edge triggered, negative edge triggered, level triggered IC flip-flops (At least one IC each of D latch, D flip-flop, JK flip-flops).

APPARATUS REQUIRED: - IC' S 7400, 7402 Digital Trainer & Connecting leads.

BRIEF THEORY:

RS FLIP-FLOP: There are two inputs to the flip-flop defined as R and S. When I/Ps $R = 0$ and $S = 0$ then O/P remains unchanged. When I/Ps $R = 0$ and $S = 1$ the flip-flop is switched to the stable state where O/P is 1 i.e. SET. The I/P condition is $R = 1$ and $S = 0$ the flip-flop is switched to the stable state where O/P is 0 i.e. RESET. The I/P condition is $R = 1$ and $S = 1$ the flip-flop is switched to the stable state where O/P is forbidden.

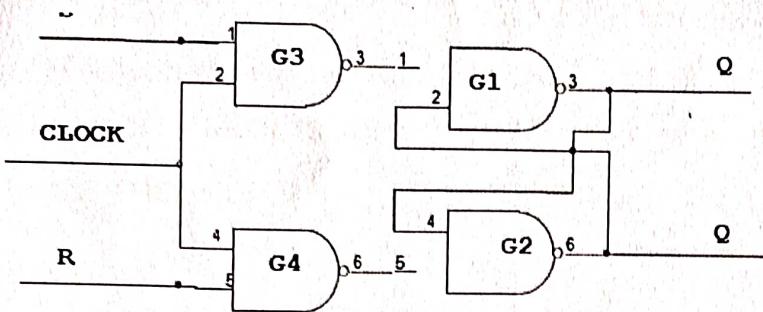
JK FLIP-FLOP: For purpose of counting, the JK flip-flop is the ideal element to use. The variable J and K are called control I/Ps because they determine what the flip-flop does when a positive edge arrives. When J and K are both 0s, both AND gates are disabled and Q retains its last value.

D FLIP –FLOP: This kind of flip flop prevents the value of D from reaching the Q output until a clock pulse occurs. When the clock is low, both AND gates are disabled D can change value without affecting the value of Q. On the other hand, when the clock is high, both AND gates are enabled. In this case, Q is forced to equal the value of D. When the clock again goes low, Q retains or stores the last value of D. a D flip flop is a bistable circuit whose D input is transferred to the output after a clock pulse is received.

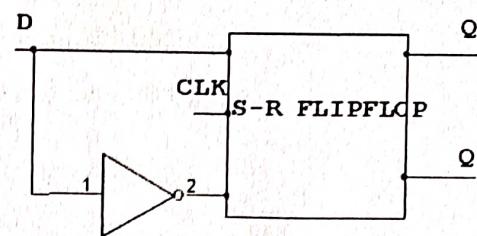
T FLIP-FLOP: The T or "toggle" flip-flop changes its output on each clock edge, giving an output which is half the frequency of the signal to the T input. It is useful for constructing binary counters, frequency dividers, and general binary addition devices. It can be made from a J-K flip-flop by tying both of its inputs high.



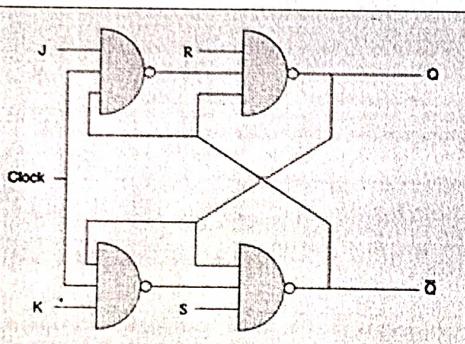
CIRCUIT DIAGRAM:-



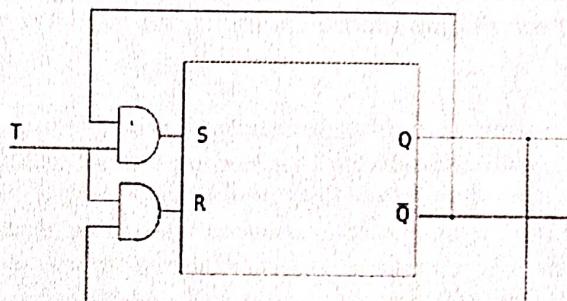
SR FLIPFLOP



D FLIPFLOP



JK FLIPFLOP



T FLIPFLOP

Activa
Go to S-

JK FLIPFLOP

CLOCK	S	R	Q_{n+1}
1	0	0	NO CHANGE
1	0	1	0
1	1	0	1
1	1	1	Q_n'

PRECAUTIONS:

- 1) Make the connections according to the IC pin diagram.
- 2) The connections should be tight.
- 3) The V_{cc} and ground should be applied carefully at the specified pin only.

RESULT: Truth table of JK-Flip flop is verified on digital trainer kit.



EXPERIMENT NO: 5

AIM: - Verification of truth table for encoder and decoder ICs, Mux and De-Mux.

APPARATUS REQUIRED: IC 7447, 7-segment display, IC 74139 and connecting leads.

BRIEF THEORY:

DECODER:

A decoder is a device which does the reverse of an encoder, undoing the encoding so that the original information can be retrieved. The same method used to encode is usually just reversed in order to decode. In digital electronics, a decoder can take the form of a multiple-input, multiple-output logic circuit that converts coded inputs into coded outputs, where the input and output codes are different. e.g. n-to-2n, binary-coded decimal decoders. Enable inputs must be on for the decoder to function, otherwise its outputs assume a single "disabled" output code word. In case of decoding all combinations of three bits eight ($2^3=8$) decoding gates are required. This type of decoder is called 3-8 decoder because 3 inputs and 8 outputs . For any input combination decoder outputs are 1 .

ENCODER :

An encoder is a device, circuit, transducer, software program, algorithm or person that converts information from one format or code to another, for the purposes of standardization, speed, secrecy, security, or saving space by shrinking size. An encoder has M input and N output lines. Out of M input lines only one is activated at a time and produces equivalent code on output N lines. If a device output code has fewer bits than the input code has, the device is usually called an encoder. For example Octal-to-Binary Encoder take 8 inputs and provides 3 outputs, thus doing the opposite of what the 3-to-8 decoder does. At any one time, only one input line has a value of 1. The figure below shows the truth table of an Octal-to-binary encoder.

For an 8-to-3 binary encoder with inputs I₀-I₇ the logic expressions of the outputs Y₀-Y₂ are:

$$Y_0 = I_1 + I_3 + I_5 +$$

$$I_7 \quad Y_1 = I_2 + I_3 + I_6 +$$

$$I_7 \quad Y_2 = I_4 + I_5 + I_6$$

$$+ I_7$$

DEMULTIPLEXER:

Demultiplexer means generally one into many. A demultiplexer is a logic circuit with one input and many output. By applying control signals, We can steer the input signal to one of the output lines. The ckt. has one input signal, m control signal and n output signals. Where $2^n = m$. It functions as an electronic switch to route an incoming data signal to one of several outputs.

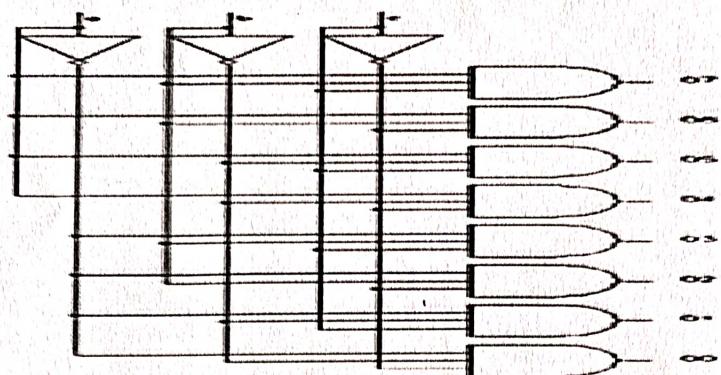


Figure 3:8 Decoder

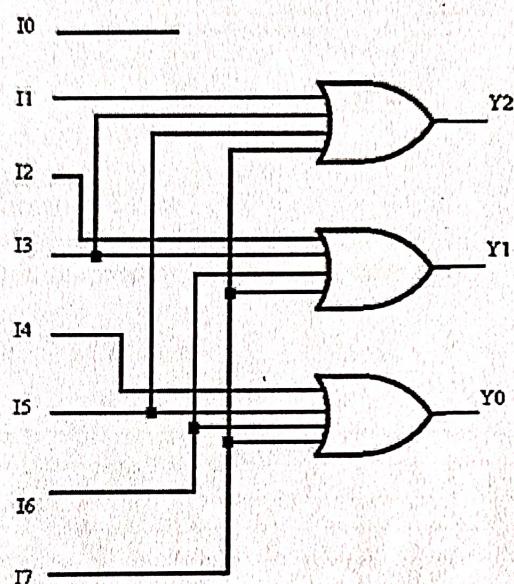


Figure 3:8 Encoder

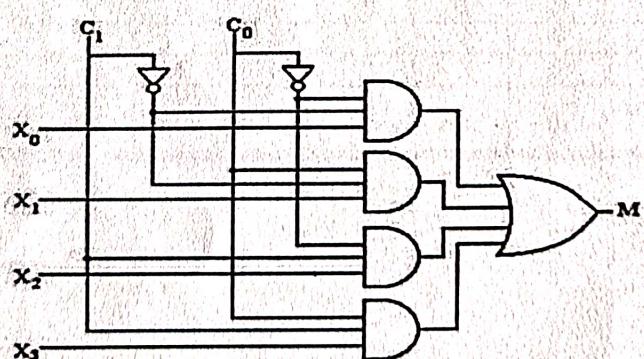


Figure 4: 1mux

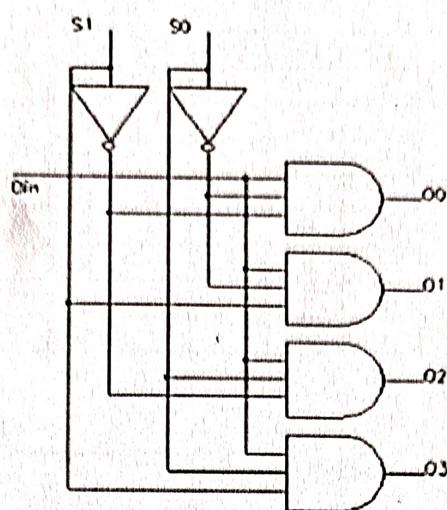


Figure 1:4 Demux

PROCEDURE:

- 1) Connect the circuit as shown in figure.
- 2) Apply Vcc & ground signal to every IC.
- 3) Observe the input & output according to the truth table.

OBSERVATION TABLE:

Truth table for Decoder

Inputs			Outputs								
a	b	c	D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇	
0	0	0	1	0	0	0	0	0	0	0	
0	0	1	0	1	0	0	0	0	0	0	
0	1	0	0	0	1	0	0	0	0	0	
0	1	1	0	0	0	1	0	0	0	0	
1	0	0	0	0	0	0	1	0	0	0	
1	0	1	0	0	0	0	0	1	0	0	
1	1	0	0	0	0	0	0	0	1	0	
1	1	1	0	0	0	0	0	0	0	1	
Output function			$\bar{a}\bar{b}c$	$\bar{a}bc$	$\bar{ab}\bar{c}$	\bar{abc}	$a\bar{b}\bar{c}$	$a\bar{bc}$	$a\bar{b}\bar{c}$	abc	



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Truth table for Encoder

I ₀	I ₁	I ₂	I ₃	I ₄	I ₅	I ₆	I ₇	Y ₂	Y ₁	Y ₀
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1

Truth table for Demux

Output select Lines		Output selected
S ₁	S ₀	
0	0	O ₀
0	1	O ₁
1	0	O ₂
1	1	O ₃

PRECAUTIONS:

- 1) Make the connections according to the IC pin diagram.
- 2) The connections should be tight.
- 3) The V_{cc} and ground should be applied carefully at the specified pin only.

RESULT: Encoder/ decoder Multiplexer and demultiplexer have been studied and verified.



EXPERIMENT NO: 6

OBJECTIVE: - Design shift Register & verify truth table. Used as a serial/parallel shift. Resistor.

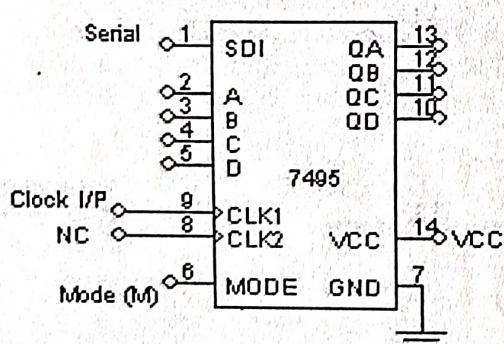
Apparatus Required: - IC 7495, 7-segment display, IC 74139 and connecting leads etc.

Procedure: -

Serial In Parallel Out:-

1. Connections are made as per circuit diagram.
2. Apply the data at serial i/p
3. Apply one clock pulse at clock 1 (Right Shift) observe this data at QA.
4. Apply the next data at serial i/p.
5. Apply one clock pulse at clock 2, observe that the data on QA will shift to QB and the new data applied will appear at QA.
6. Repeat steps 2 and 3 till all the 4 bits data are entered one by one into the shift register.

Pin diagram:



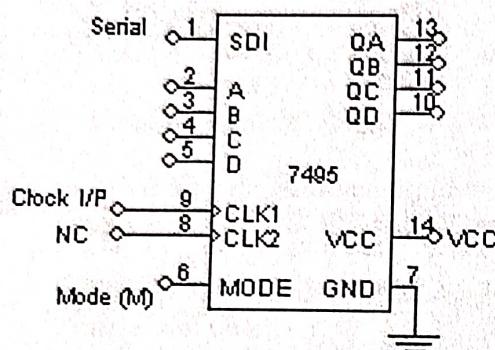
Truth Table:-

Clock	Serial i/p	QA	QB	QD	
1	0	0	X	X	X
2	1	1	0	X	X
3	1	1	1	0	X
4	1	1	1	1	0



Serial In Serial Out:-

1. Connections are made as per circuit diagram.
2. Load the shift register with 4 bits of data one by one serially.
3. At the end of 4th clock pulse the first data „d0“ appears at QD.
4. Apply another clock pulse; the second data „d1“ appears at QD.
5. Apply another clock pulse; the third data appears at QD.
6. Application of next clock pulse will enable the 4th data „d3“ to appear at QD. Thus the data applied serially at the input comes out serially at QD



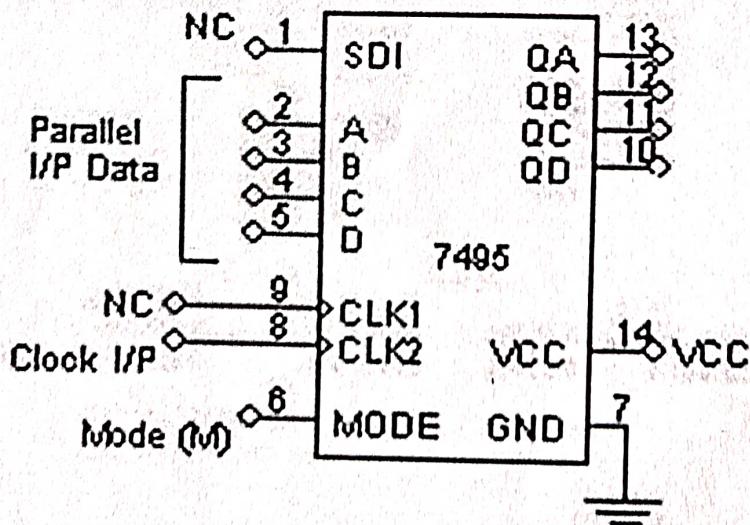
Pin Diagram:

Clock	Serial i/p	QA	QB	QC	QD
1	d0=0	0	X	X	X
2	d1=1	1	0	X	X
3	d2=1	1	1	0	X
4	d3=1	1	1	1	0=d0
5	X	X	1	1	1=d1
6	X	X	X	1	1=d2
7	X	X	X	X	1=d3

Truth Table:-

Parallel In Parallel Out:-

1. Connections are made as per circuit diagram.
2. Apply the 4 bit data at A, B, C and D.
3. Apply one clock pulse at Clock 2 (Note: Mode control M=1).The 4 bit data at A, B, C and D appears at QA, QB, QC and QD respectively.



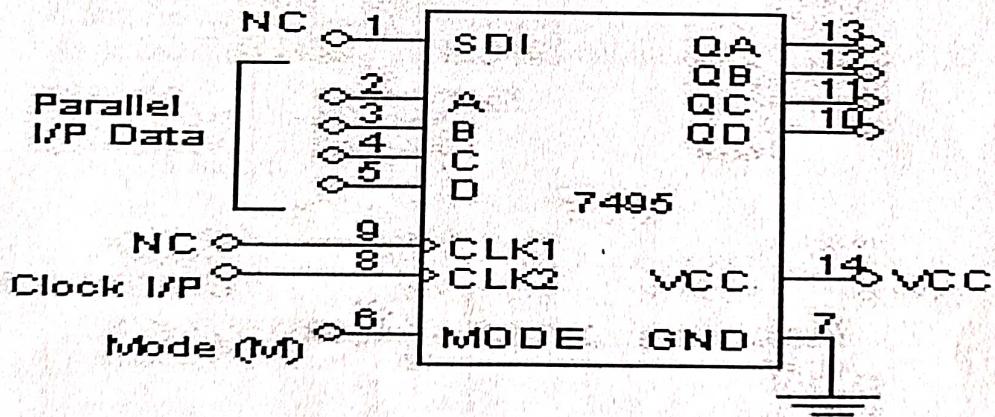


Truth Table:-

Clock	Parallel i/p				Parallel o/p			
	A	B	C	D	QA	QB	QD	
1	1	0	1	1	1	0	1	1

Parallel In Serial Out:-

1. Connections are made as per circuit diagram.
2. Apply the desired 4 bit data at A, B, C and D.
3. Keeping the mode control M=1 apply one clock pulse. The data applied at A, B, C and D will appear at QA, QB, QC and QD respectively.
4. Now mode control M=0. Apply clock pulses one by one and observe the data coming out serially at QD.





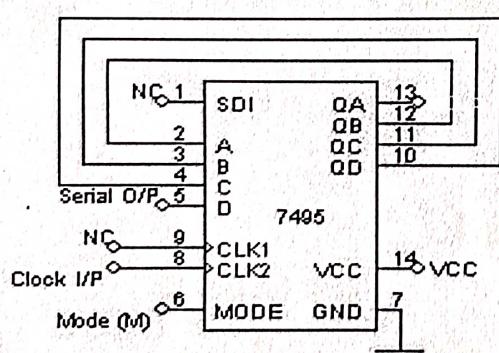
Truth Table:-

Mode	Clock	Parallel i/p				Parallel o/p			
		A	B	C	D	QA	QB	QD	
1	1	1	0	1	1	1	0	1	1
0	2	X	X	X	X	X	1	0	1
0	3	X	X	X	X	X	X	1	0
0	4	X	X	X	X	X	X	X	1

Left Shift:-

1. Connections are made as per circuit diagram
2. Apply the first data at D and apply one clock pulse. This data appears at QD.
3. Now the second data is made available at D and one clock pulse applied. The data appears at QD to QC and the new data appears at QD.
4. Step 3 is repeated until all the 4 bits are entered one by one
At the end 4th clock pulse the 4 bits are available at QA, QB, QC and QD.

Pin diagram: -



Truth Table:-

Clock	Serial i/p	QA	QB	QC	QD
1	1	X	X	X	1
2	0	X	X	1	0
3	1	X	1	0	1
4	1	1	0	1	1



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RESULT:- We successfully verify the designing of shift resistors.

PRECAUTIONS: -

- 1) The continuity of the connecting terminals should be checked before going.
- 2) It should be care that the values of the components of the circuit is does not exceed to their ratings (maximum value).
- 3) Before the circuit connection it should be check out working condition of all the Component.



EXPERIMENT NO: 7

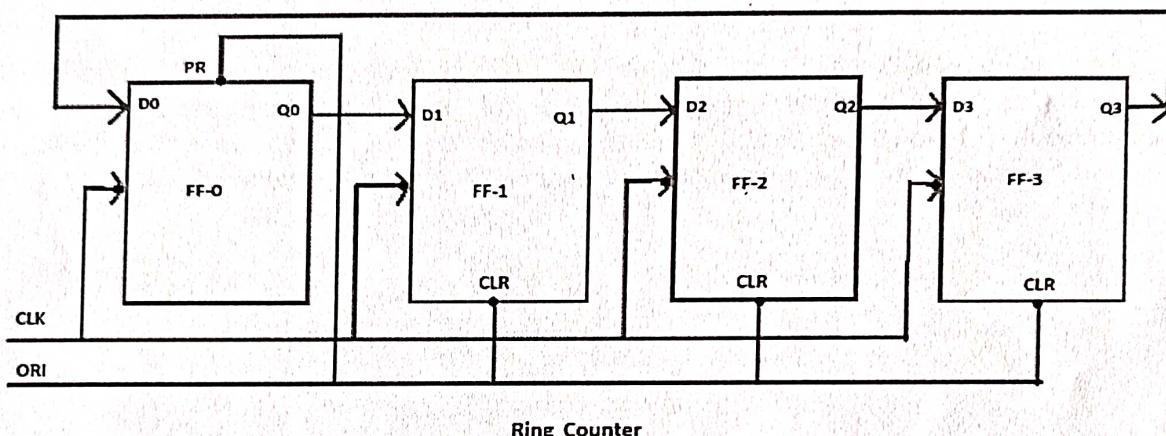
AIM: - To design a 4 bit ring counter and verify its operation.

Apparatus required: - Asynchronous Counter IC 7490, IC 74193, power supply, connecting wires etc.

Theory:

A ring counter is a typical application of the Shift register. The ring counter is almost the same as the shift counter. The only change is that the output of the last flip-flop is connected to the input of the first flip-flop in the case of the ring counter but in the case of the shift register it is taken as output. Except for this, all the other things are the same.

Circuit Diagram for Ring Counter:-



In this diagram, we can see that the clock pulse (CLK) is applied to all the flip-flops simultaneously. Therefore, it is a Synchronous Counter. Also, here we use Overriding input (ORI) for each flip-flop. Preset (PR) and Clear (CLR) are used as ORI. When PR is 0, then the output is 1. And when CLR is 0, then the output is 0. Both PR and CLR are active low signal that always works in value 0.

$$PR = 0, Q = 1$$

$$CLR = 0, Q = 0$$

These two values are always fixed. They are independent of the value of input D and the Clock pulse (CLK). Working – Here, ORI is connected to Preset (PR) in FF-0 and it is connected to Clear (CLR) in FF-1, FF-2, and FF-3. Thus, output $Q = 1$ is generated at FF-0, and the rest of the flip-flop generates output $Q = 0$. This output $Q = 1$ at FF-0 is known as Pre-set 1 which is used to form the ring in the Ring Counter.



Truth Table for Ring Counter:-

ORI	CLK	Q0	Q1	Q2	Q3
low	X	1	0	0	0
high	low	0	1	0	0
high	low	0	0	1	0
high	low	0	0	0	1
high	low	1	0	0	0

This Preseted 1 is generated by making ORI low and that time Clock (CLK) becomes don't care. After that ORI is made to high and apply low clock pulse signal as the Clock (CLK) is negative edge triggered. After that, at each clock pulse, the preset 1 is shifted to the next flip-flop and thus forms a Ring. From the above table, we can say that there are 4 states in a 4-bit Ring Counter.

4 states are:

1 0 0 0

0 1 0 0

0 0 1 0

0 0 0 1

In this way can design a 4-bit Ring Counter using four D flip-flops.

PRECAUTIONS: -

- 1) The continuity of the connecting terminals should be checked before going .
- 2) It should be care that the values of the components of the circuit is does not exceed to their ratings (maximum value).
- 3) Before the circuit connection it should be check out working condition of all the Component.

RESULT: - design and verification of 4 - bit ring counter is done.



EXPERIMENT NO: 8

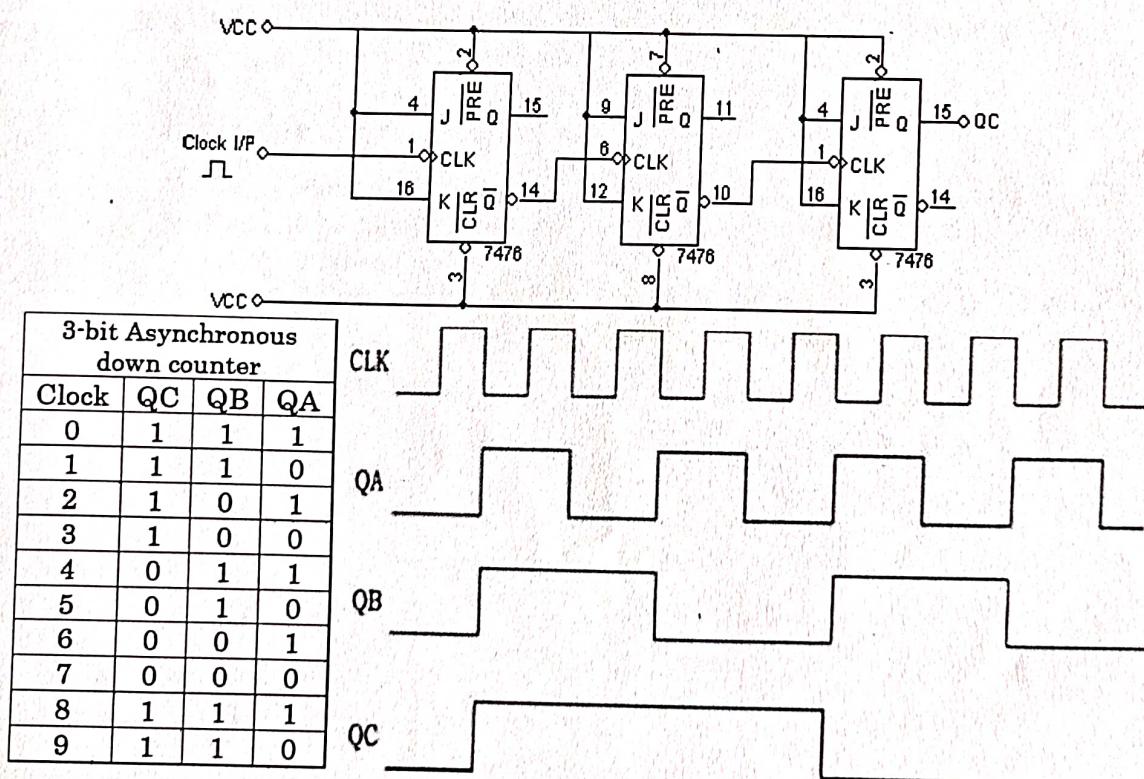
AIM - Construction and testing of any counter (Asynchronous up-counter, Asynchronous Down-counter).

Apparatus required: - Asynchronous Counter IC 7490, IC 74193, power supply, connecting wires etc.

Procedure: - Connections are made as per the circuit diagram except the connection from output of NAND gate to the load input

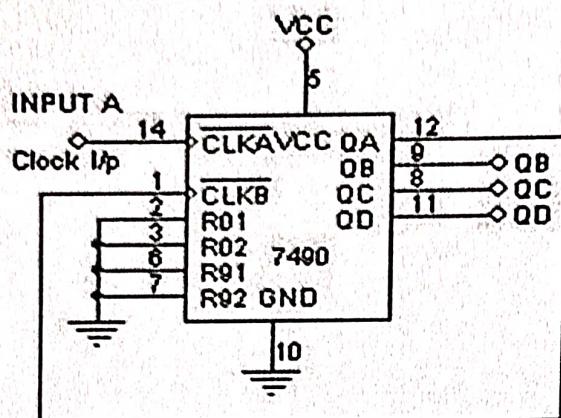
1. The data (0011) = 3 is made available at the data i/p's A, B, C & D respectively.
2. The load pin made low so that the data 0011 appears at QD, QC, QB & QA respectively.
3. Now connect the output of the NAND gate to the load input
4. Clock pulses are applied to "count up" pin and the truth table is verified
5. Now apply (1100) = 12 for 12 to 5 counter and remaining is same as for 3 to 8 counter.
6. The pin diagram of IC 74192 is same as that of 74193. 74192 can be configured to count between 0 and 9 in either direction. The starting value can be any number between 0 and 9

3-Bit Asynchronous Down Counter :-





3-bit Synchronous up Counter:-



Clock	QD	QC	QB	QA
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	0	0	0	0

RESULT: - Use of Asynchronous Counter IC's (7490 or 7493) is completed.

PRECAUTIONS: -

- 4) The continuity of the connecting terminals should be checked before going.
- 5) It should be care that the values of the components of the circuit is does not exceed to their ratings (maximum value).
- 6) Before the circuit connection it should be check out working condition of the entire Component.