Ambekeshwar Group Of Institutions

Technology & Management,
Lucknow

Session: 2023-24

PRACTICAL FILE

Branch:- CSE 2nd Year | 3rd Sem

Subject:- Digital Electronic

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2.	Realization of logic functions with the help of NAND gate.			
3.	Design of a half adder using XOR and NAND gates and verification of its operation, Construction of a full adder circuit using XOR and NAND gates and verify its operation.			
4.	Verification of truth table for positive edge triggered, negative edge triggered, level triggered IC flip- flops (At least one IC each of D latch, D flip-flop, JK flip-flops).			
5.	Verification of truth table for encoder and decoder ICs, Mux and De-Mux.			
6.	To design a 4-bit ring counter and verify it's operation.			

Practical No: 1

AIM : To Study about logic gates and verify their truth tables.

Apparatus required –

Sl. No.	Component	Specification	Qty
1.	AND Gate	IC 7408	1
2.	OR Gate	IC 7432	1
3.	NOT Gate	IC 7404	1
4.	NAND Gate 2 I/P	IC 7400	1
5.	NOR Gate	IC 7402	1
6.	X-OR Gate	IC 7486	1
7.	NAND Gate 3 I/P	IC 7410	1
8.	IC Trainer Kit	-	1
9.	Patch Cord	-	14

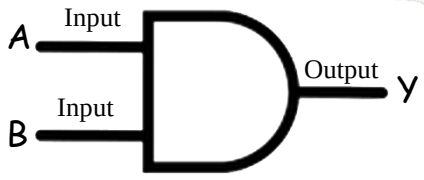
Theory :-

Circuit that takes the logical decision and the process are called logic gates. Each gate has one of more input and only one output. OR, AND and NOT are basic gates. NAND, NOR, X-OR are known as Universal gates. Basic gates form these gates.

- **AND Gate:**

The AND Gate performs a logical multiplication commonly known as AND function. The Output is high when both the inputs are high. The output is low level when any one of the inputs is low.

Symbol:-



Input		*Output*
A	*B*	*Y*
0	*0*	*0*
0	*1*	*0*
1	*0*	*0*
1	*1*	*1*

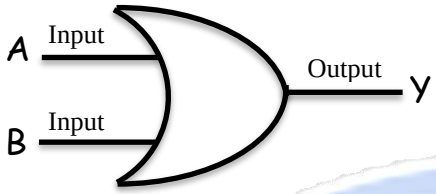
Boolean Expression:

$$Y=A.B$$

➢ OR Gate:

The OR Gate perform a logical addition commonly known as OR Function. The output is high when any one of the inputs is high. The Output is low when both the inputs are low.

Symbol:-



Input		Output
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

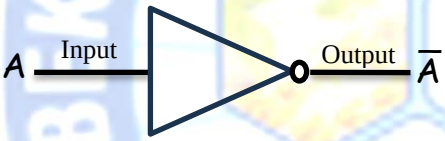
Boolean Expression:

$$Y=A+B$$

➢ NOT Gate:

The NOT Gate is called inverter. The Output is high when the input is low. The output is low when the input is high.

Symbol:-



Input	Output
A	$\bar{A}$
0	1
1	0

Boolean Expression:

$$A=\bar{A}$$

➢ NAND Gate:

The NAND Gate is a Concraction of AND-NOT. The output is high when both inputs are low and any one of the input is low. The output is low level when both inputs are high.

Symbol:-

Input		Output
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

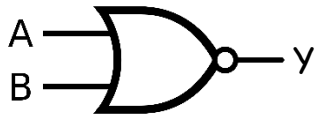
Boolean Expression:

$$Y=\overline{A.B}$$

➢ **NOR Gate:**

The NOR Gate is a contraction of OR-NOT. The output is high when both inputs are low. The output is low when one a both are high.

Symbol:-



Boolean Expression:

$$Y=\overline{A+B}$$

Input		Output
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

➢ **X-OR Gate:**

The output is high when any one of the inputs is high. The output is low when both the inputs are low and both the inputs are high.

Symbol:-

Boolean Expression:

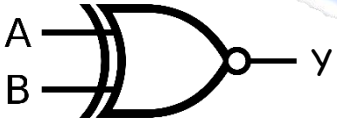
$$Y=A\oplus B$$

Input		Output
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

➢ **X-NOR Gate:**

The output is low when any one of the inputs is high. The output is high when both the inputs are low and both the inputs are high.

Symbol:-



Boolean Expression:

$$Y=A\odot B$$

Input		Output
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

Procedure:

- Connections are given as for circuit diagram.
- Logic inputs are given as per circuit diagram.
- Observe the output and verify the truth table.

Result:

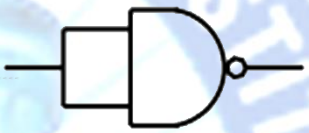
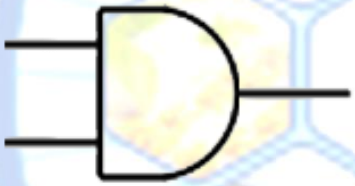
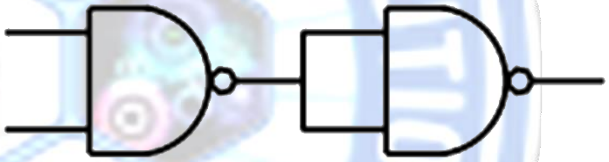
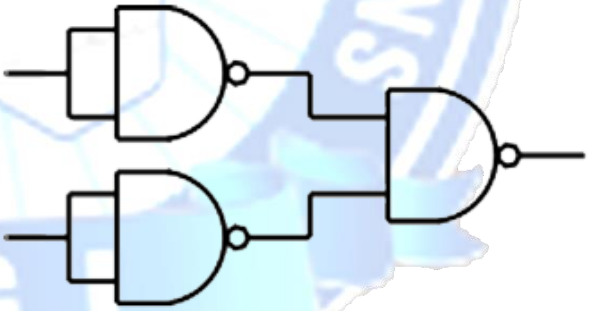
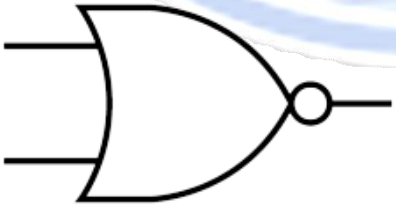
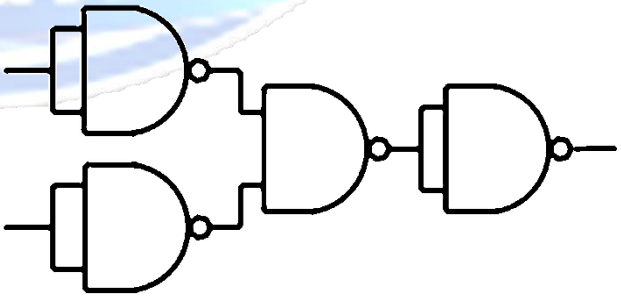
Study and verification of logic gates have been done.

Practical No: 2

AIM : Realization of logic functions with the help of NAND gate.

Equipment Required:- NAND gate, connecting wires etc.

THEORY:- NAND GATE and NOR GATE is universal gate. It is so called as because by using of this gate we can make any gate like NOT, OR, AND etc. by help of this gate we can also make multiplexers and de mux. We can realize logic function by the help of Universal Gates (NAND, NOR).

	Gate	**Equivalent in NAND gates**
NOT		
AND		
OR		
NOR		

PROCEDURE:-

1. Place the IC on IC Trainer Kit.
2. Connect Vcc and ground to respective pins of IC Trainer Kit.
3. Connect the inputs to the input switches provided in the IC Trainer Kit.
4. Connect the outputs to the switches of O/P LEDs,
5. Apply various combinations of inputs according to the truth table and observe condition of LEDs.
6. Disconnect output from the LEDs and note down the corresponding multimeter voltage readings for various combinations of inputs.

PRECAUTIONS:

1) All the connection should be tight.
2) It should be care that the values of the components of the circuit is does not exceed to their ratings (maximum value).
3) Before the circuit connection it should be check out working condition of all the Component.

RESULT: - Realization of logic functions with the help of NAND gate is done.

Practical No: 3

AIM : Design of a half adder using XOR and NAND gates and verification of its operation, Construction of a full adder circuit using XOR and NAND gates and verify its operation.

APPARATUS REQUIRED: Power supply, IC's, Digital Trainer, Connecting leads.

BRIEF THEORY: We are familiar with ALU, which performs all arithmetic and logic operation but ALU doesn't perform/ process decimal no's. They process binary no's.

Half Adder: It is a logic circuit that adds two bits. It produces the O/P, sum & carry. The Boolean equation for sum & carry are:

SUM = A + B

CARRY = A.B

Therefore, sum produces 1 when A&B are different and carry is 1when A&B are 1. Application of Half adder is limited.

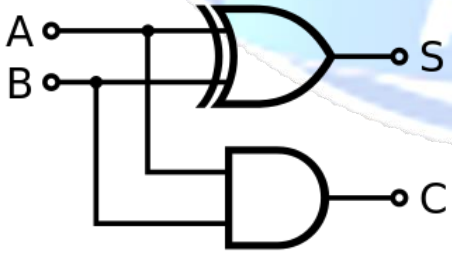
Full Adder: It is a logic circuit that can add three bits. It produces two O/P sum & carry. The Boolean Equation for sum & carry are

SUM A+B+C

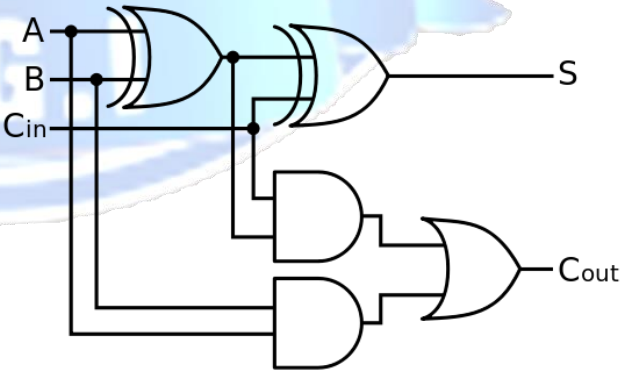
CARRY=A.B+ (A+B)

Therefore, sum produces one when I/P is containing odd no's of one & carry is one when there are two or more one in I/P.

CIRCUIT DAIGRAM:



HALF ADDER



FULL ADDER

Procedure:-

(a) Connect the ckt. as shown in fig. For half adder.
(b) Apply diff. Combination of inputs to the I/P terminal.
(c) Note O/P for Half adder.
(d) Repeat procedure for Full wave.
(e) The result should be in accordance with truth table.

OBSERVATION TABLE:

HALF ADDER:

INPUTS		OUTPUT	
A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

FULL ADDER:

INPUTS			OUTPUT	
A	B	C	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

PRECAUTIONS:

1) Make the connections according to the IC pin diagram.
2) The connections should be tight.
3) The Vcc and ground should be applied carefully at the specified pin only.

RESULT: Design of a half adder using XOR and NAND gates and verification of its operation, Construction of a full adder circuit using XOR and NAND gates and verification of its operation is done.

Practical No: 4

AIM:-Verification of truth table for positive edge triggered, negative edge triggered, level triggered IC flip- flops (At least one IC each of D latch, D flip-flop, JK flip-flops).

APPARATUS REQUIRED: - IC' S 7400, 7402 Digital Trainer & Connecting leads.

BRIEF THEORY:

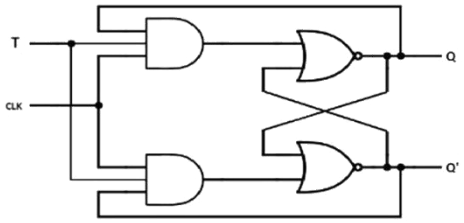
RS FLIP-FLOP: There are two inputs to the flip-flop defined as R and S. When I/Ps R = 0 and S = 0 then O/P remains unchanged. When I/Ps R = 0 and S = 1 the flip-flop is switches to the stable state where O/P is 1 i.e. SET. The I/P condition is R= 1 and S = 0 the flip-flop is switched to the stable state where O/P is 0 i.e. RESET. The I/P condition is R = 1 and S = 1 the flip-flop is switched to the stable state where O/P is forbidden.

JK FLIP-FLOP: For purpose of counting, the JK flip-flop is the ideal element to use. The variable J and K are called control I/Ps because they determine what the flip-flop does when a positive edge arrives. When J and K are both Os, both AND gates are disabled and Q retains its last value.

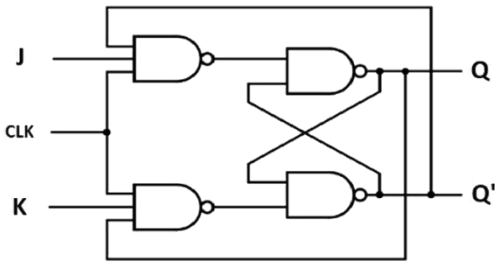
D FLIP-FLOP: This kind of flip flop prevents the value of D from reaching the Q output until a clock pulse occurs. When the clock is low, both AND gates are disabled D can change value without affecting the value of Q. On the other hand, when the clock is high, both AND gates are enabled. In this case, Q is forced to equal the value of D. When the clock again goes low, Q retains or stores the last value of D. a D flip flop is a bistable circuit whose D input is transferred to the output after a clock pulse is received.

T FLIP-FLOP: The T or "toggle" flip-flop changes its output on each clock edge, giving an output which is half the frequency of the signal to the T input. It is useful for constructing binary counters, frequency dividers, and general binary addition devices. It can be made from a J-K flip-flop by tying both of its inputs high.

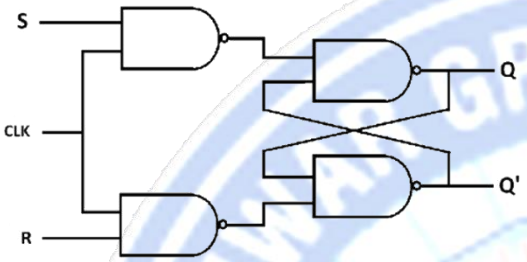
CIRCUIT DIAGRAM:



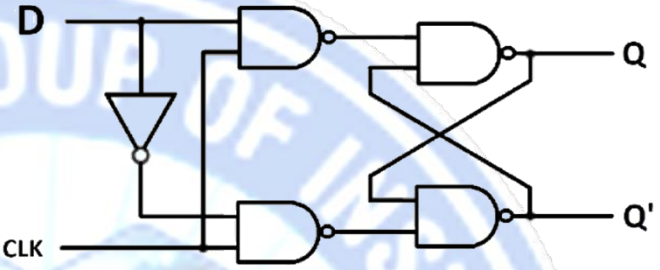
T Flip Flop



JK Flip Flop



SR Flip Flop



D Flip Flop

JK Flip Flop

CLOCK	S	R	Q_{n+1}
1	0	0	No Change
1	0	1	0
1	1	0	1
1	1	1	Qn’

PRECAUTIONS:

1) Make the connections according to the IC pin diagram.
2) The connections should be tight.
3) The Vec and ground should be applied carefully at the specified pin only.

RESULT: Truth table of JK-Flip flop is verified on digital trainer kit.

Practical No: 5

AIM: - Verification of truth table for encoder and decoder ICs, Mux and De-Mux.

APPARATUS REQUIRED: IC 7447, 7-segment display, IC 74139 and connecting leads.

BRIEF THEORY:

DECODER:

A decoder is a device which does the reverse of an encoder, undoing the encoding so that the original information can be retrieved. The same method used to encode is usually just reversed in order to decode. In digital electronics, a decoder can take the form of a multiple-input, multiple- output logic circuit that converts coded inputs into coded outputs, where the input and output codes are different. e.g. n-to-2n, binary-coded decimal decoders. Enable inputs must be on for the decoder to function, otherwise its outputs assume a single "disabled" output code word. In case of decoding all combinations of three bits eight (23-8) decoding gates are required. This type of decoder is called 3-8 decoder because 3 inputs and 8 outputs. For any input combination decoder outputs are 1.

ENCODER:

An encoder is a device, circuit, transducer, software program, algorithm or person that converts information from one format or code to another, for the purposes of standardization, speed, secrecy, security, or saving space by shrinking size. An encoder has M input and N output lines. Out of M input. lines only one is activated at a time and produces equivalent code on output N lines. If a device output code has fewer bits than the input code has, the device is usually called an encoder. For example Octal- to-Binary Encoder take 8 inputs and provides 3 outputs, thus doing the opposite of what the 3-to-8 decoder does. At any one time, only one input line has a value of 1. The figure below shows the truth table of an Octal-to-binary encoder.

For an 8-to-3 binary encoder with inputs 10-17 the logic expressions of the outputs YO-Y2 are: YO 11+13+ 15 +
17 Y1 12+13 + 16 +
17 Y2 14+ 15 + 16
+17

DEMULTIPLEXER:

Demultiplexer means generally one into many. A demultiplexer is a logic circuit with one input and many output. By applying control signals, We can steer the input signal to one of the output lines. The ckt. has one input signal, m control signal and n output signals. Where 2n=m. It functions as an electronic switch to route an incoming data signal to one of several outputs.

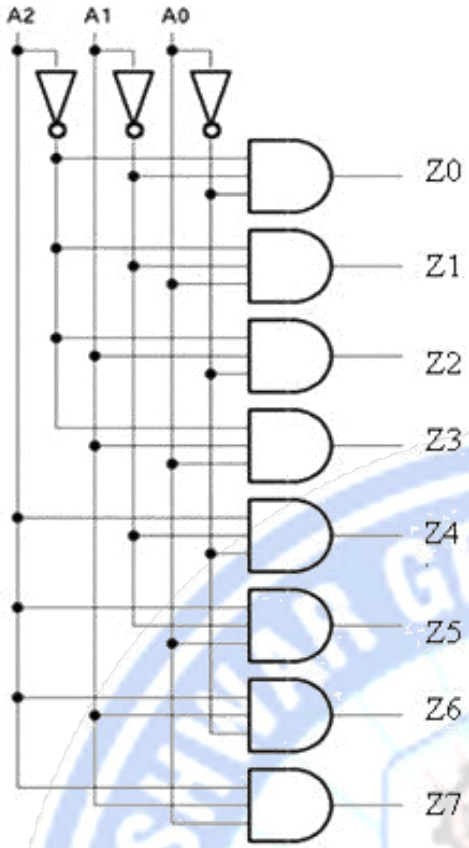


Fig: 3:8 Decoder

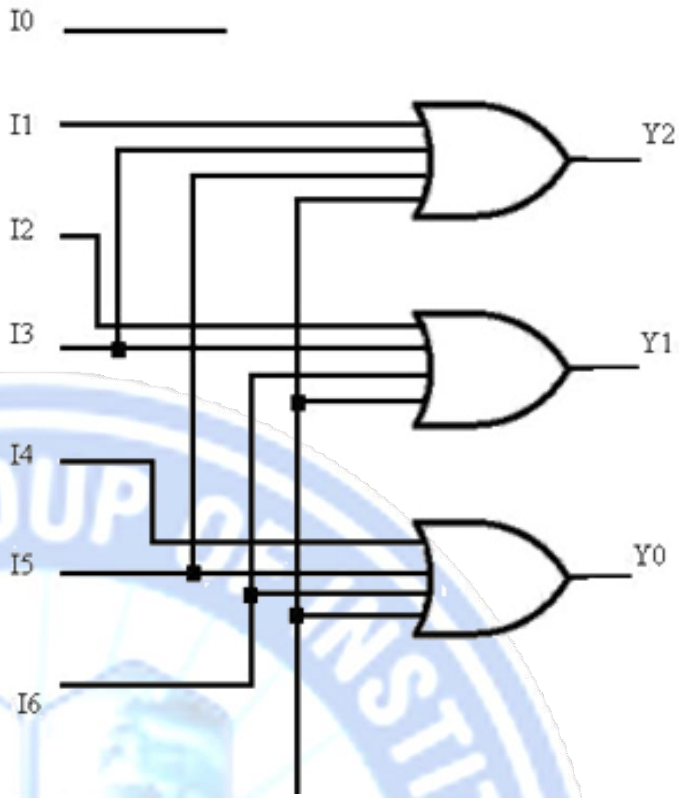


Fig: 3:8 Encoder

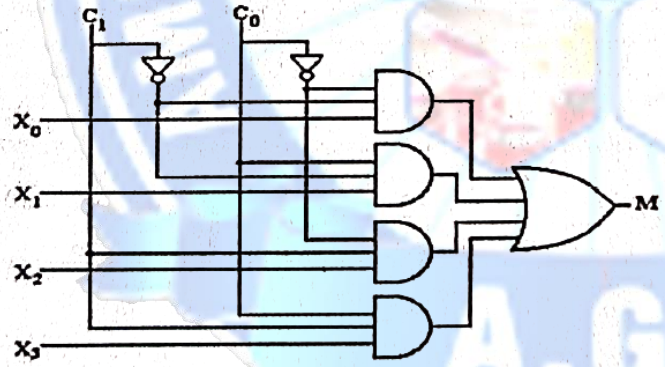


Fig: 1 Mux

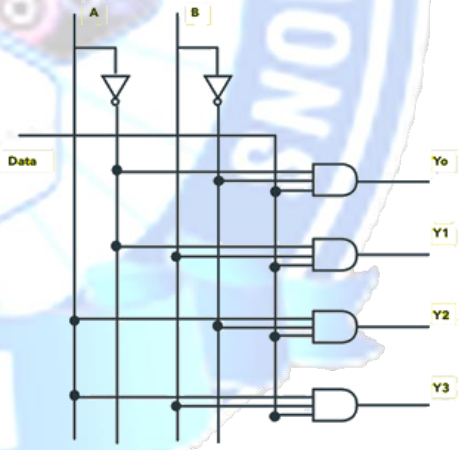


Fig: 4:1 DeMux

PROCEDURE:

1) Connect the circuit as shown in figure.
2) Apply Vcc & ground signal to every IC.
3) Observe the input & output according to the truth table.

OBSERVATION TABLE:

Truth table for Decoder:

Inputs			Outputs							
A	**B**	**C**	**D0**	**D1**	**D2**	**D3**	**D4**	**D5**	**D6**	**D7**
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1
Output Function			$\overline{abc}$	$\overline{a}bc$	$\bar{a}b\bar{c}$	$\bar{a}bc$	$a\overline{bc}$	$a\bar{b}c$	$ab\bar{c}$	abc

Truth table for Encoder

10	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**Y2**	**Y1**	**Y0**
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1

Truth table for Demux

Output select lines		**Output selected**
S1	**S0**	
0	0	O0
0	1	O1
1	0	O2
1	1	O3

PRECAUTIONS:

1) Make the connections according to the IC pin diagram.
2) The connections should be tight.
3) The Vec and ground should be applied carefully at the specified pin only.

RESULT: Encoder/ decoder Multiplexer and demultiplexer have been studied and verified.

Practical No: 6

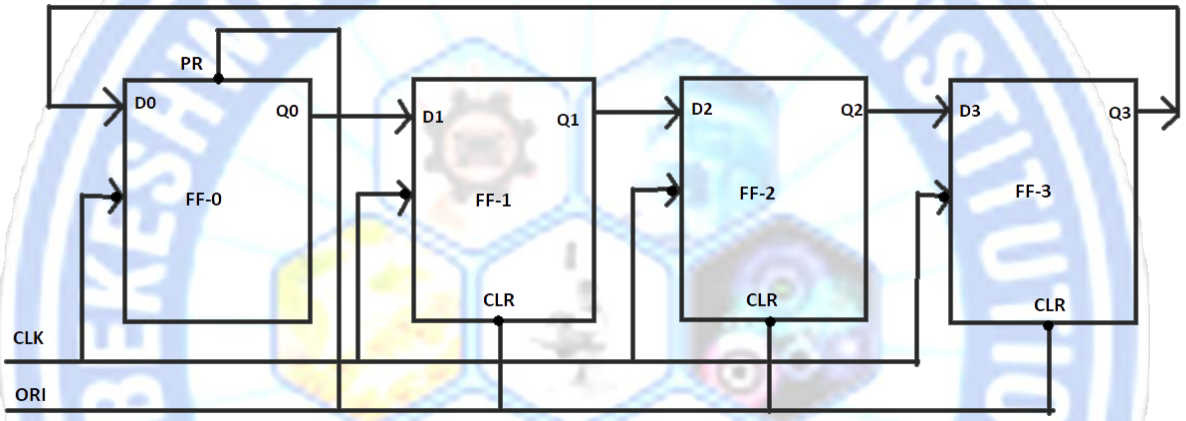
AIM: - To design a 4-bit ring counter and verify it's operation.

Apparatus required: - Asynchronous Counter IC 7490, IC 74193, power supply, connecting wires etc.

Theory:

A ring counter is a typical application of the shift resister. The ring counter is almost the same as the shift counter. The only change is that the output of the last flip-plop is connected to the input of the first flip-flop in the case of the ring counter but in the shift resister it is taken as output. Except for this, all other things are the same.

Circuit Diagram for Ring Counter:-



Ring Counter

In this diagram, we can see that the clock pulse (CLK) is applied to all the flip-flops simultaneously. Therefore, it is a Synchronous Counter. Also, here we use Overriding input (ORI) for each flip-flop. Preset (PR) and Clear (CLR) are used as ORI. When PR is 0, then the output is 1. And when CLR is 0, then the output is 0. Both PR and CLR are active low signal that always works in value 0.

PR = 0, Q = 1

CLR = 0, Q = 0

These two values are always fixed. They are independent of the value of input D and the Clock pulse (CLK). Working - Here, ORI is connected to Preset (PR) in FF-0 and it is connected to Clear (CLR) in FF-1, FF-2, and FF-3. Thus, output Q= 1 is generated at FF-0, and the rest of the flip-flop generates output Q = 0. This output Q = 1 at FF-0 is known as Pre-set 1 which is used to form the ring in the Ring Counter.

Truth Table for ring counter:-

OR	CLK	Q0	Q1	Q2	Q3
Low	X	1	0	0	0
High	Low	0	1	0	0
High	Low	0	0	1	0
High	Low	0	0	0	1
High	Low	1	0	0	0

This Preseted I is generated by making ORI low and that time Clock (CLK) becomes don't care. After that ORI is made to high and apply low clock pulse signal as the Clock (CLK) is negative edge triggered. After that, at each clock pulse, the preseted 1 is shifted to the next flip-flop and thus forms a Ring. From the above table, we can say that there are 4 states in a 4-bit Ring Counter.

4 States are:

0 0 0 0

0 1 0 0

0 0 1 0

0 0 0 1

In This way can design a 4-bit Ring Counter using four D flip-flops.

PRECAUTIONS:-

1) The continuity of the connecting terminals should be checked before going.
2) It should be care that the values of the components of the circuit is does not exceed to their ratings (maximum value).
3) Before the circuit connection it should be check out working condition of all the Component.

RESULT:- Design and verification of 4 - bit ring counter is done.