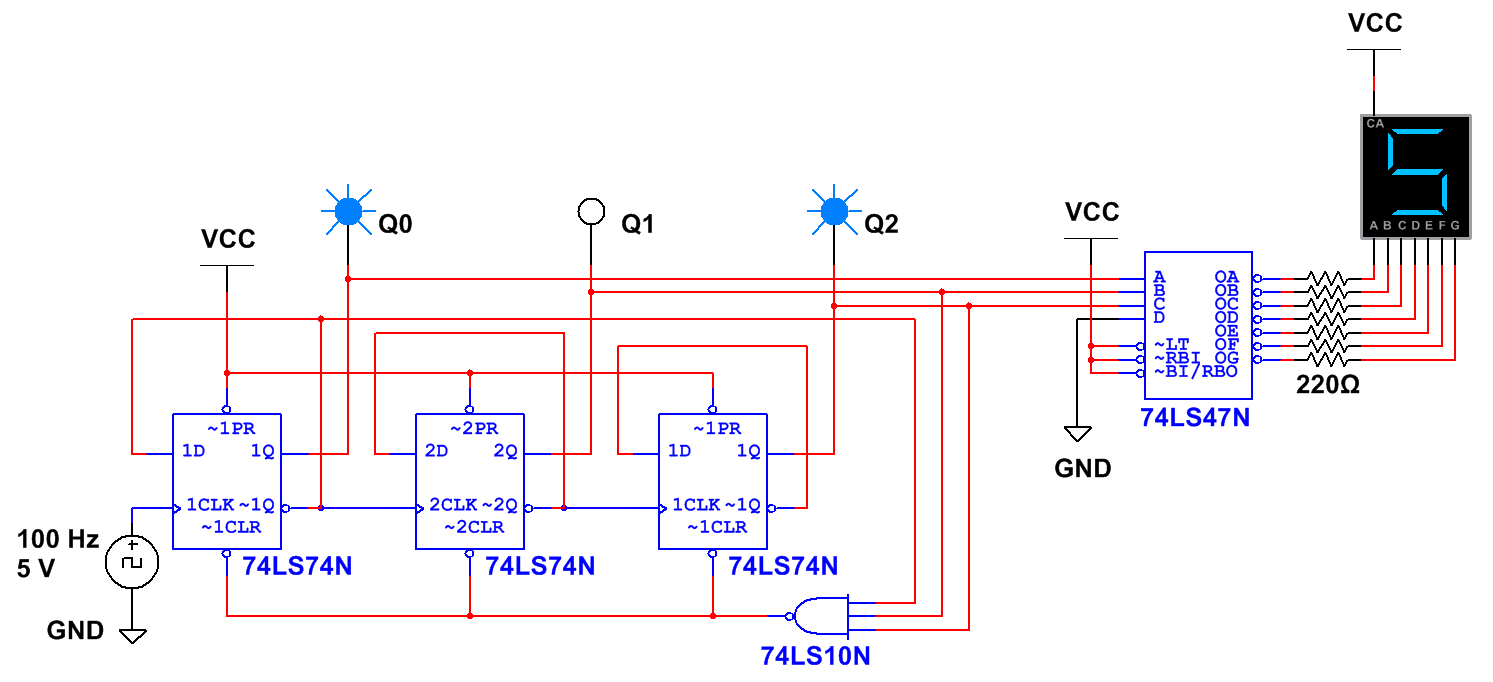


**Activity 3.2.2 SSI Asynchronous Counters:  
Modulus Counters on a PLD**

**Procedure**

**Simulation (Design Mode)**

1. The circuit shown below is a 3-Bit Mod-6 Up Counter implemented with 74LS74 D flip-flops. In this design the count will be displayed on a common anode seven-segment display using a 74LS47 encoder.   
   This design will count from 0 to 5 and then repeat (Mod 6).



**3-Bit Mod-6 Up Counter with D Flip-Flops**

* 1. Make the necessary modification to this circuit to change the count to 2 (010) to 6 (110). This is now a Mod-5 Up Counter with a start of 2 (010). Run the simulation and verify that the circuit is working as expected. If not, review your circuit, make any necessary corrections, and retest. Use a 74LS48 and a common cathode seven-segment display for this simulation in preparation for the next step.

1. The asynchronous modulus counters examined in this activity were all designed using D flip-flops. Design a 3-Bit Mod-6 Up Counter (0-5 count) using the 74LS76 J/K flip-flop.