Circuit Theory and Electronics Fundamentals

Department of Electrical and Computer Engineering, Técnico, University of Lisbon
Mestrado em Engenharia Aeroespacial

Laboratory 3 Report

Group 7

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Contents

1 Introduction

The objective of this laboratory assignment is to design a AC DC converter keeping in mind that it must be cost efficient. The circuit and its organization can be seen in Figure 1. The values used in this circuit for the resistors and capacitor can be found in Table 1.

In Section 2, a theoretical analysis of the circuit is presented. In Section 3, the circuit is analysed by simulation, and the results are compared to the theoretical results obtained in Section 2. The conclusions of this study are outlined in Section 5.

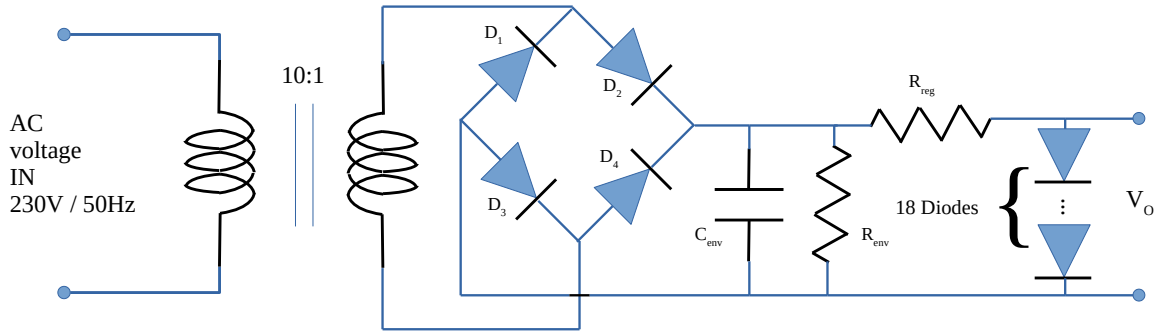

Figure 1: Circuit topography

Name	Value [Ohm/F]
R_env	70k
R_reg	6.08k
C_env	354u

Table 1: Resistor and Capacitor values used in the circuit.

2 Theoretical Analysis

In this section, the circuit shown in Figure 1 is analysed theoretically.

Firstly, we use an envelope detecter composed of a full wave rectifier, a resistor and a condensor to convert the AC signal to a DC signal (by using a full wave rectifier instead of a half wave rectifier we ensure that the voltage ripple is smaller). Here the model used for the envelope detector is different from the one used in Ngspice, as, for converting the alternate current, we obtain the absolute value of the current, instead of using diodes to process this, contrary to the circuit in Ngspice.

Afterwards, with the use of a voltage regulator made of a resistor and 18 diodes in series, we decrease the ripple and ajust the voltage to the wanted value. On the other hand, here we used an more approximate diode model with the expressions presented in lecture 14.

Below are presented the graphics for the results obtained. In Figure 2 it can be observed the voltage after the full-wave rectifier and on the terminals of the envelop circuit.

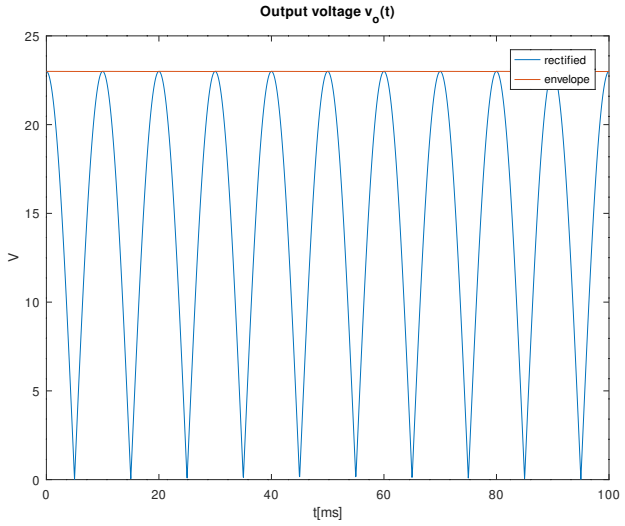

Figure 2: Voltage in the terminals of the full-wave rectifier and the envelope detector.

In Figure 3 it can be observed the voltage in the terminals of voltage regulator circuit, which, as we can observe, the output voltage is very close to 12V and with very reduced ripple. This allows us to conclude that objective of the cicuit has been achieved. These can be further confirmed by looking at the ripple and average voltages, and the merit obtained in Table 2.

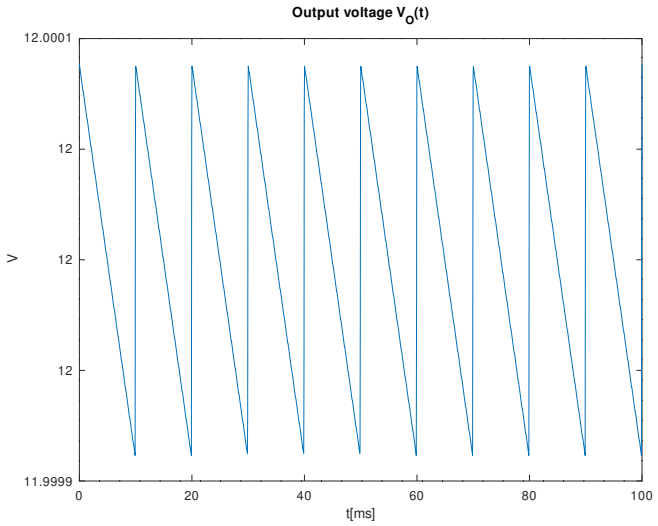

Figure 3: Voltage in the terminals of voltage regulator cicuit.

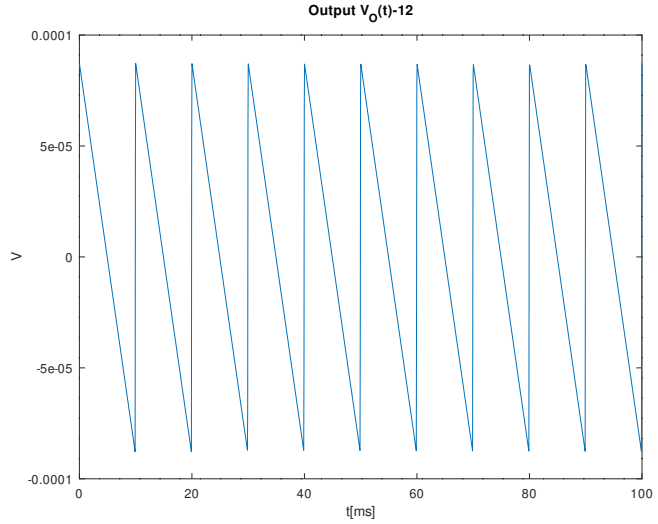

Figure 4: Output voltage - 12V : AC voltage oscilation of output voltage.

Finally, in Table 2 we can observe the merit, the average DC output and the output voltage ripple.

Name	**Value**
Average Voltage	12.000000
Ripple	0.000175
Cost	432.280000
Merit	13.133719

Table 2: Average voltage, ripple, cost and merit of the circuit developed in Octave.

3 Simulation Analysis

In this section, we will show the results of the Ngspice simulation. Here the results were obtained with the complex default diode model used in the program, eventually leading to small discrepancies from the theoretical methods.

Below are presented the graphics for the results obtained. In Figure 5 it can be observed the voltage on the terminals of the envelop circuit.

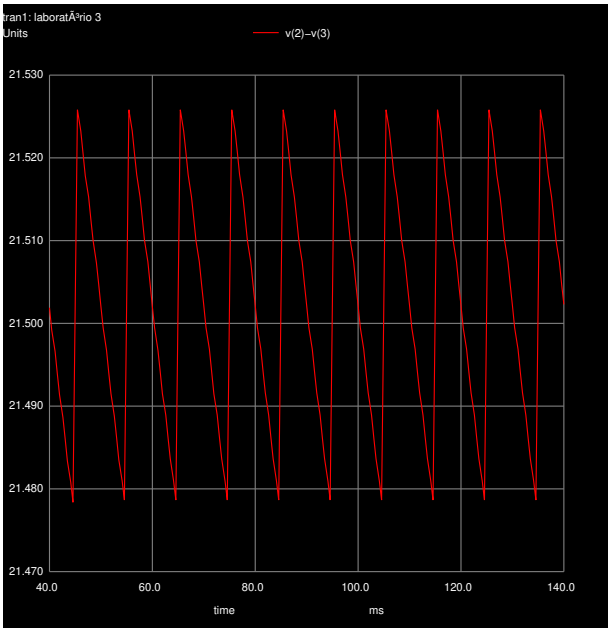

Figure 5: Voltage in the terminals of the envelope detector.

In Figure 6 it can be observed the voltage in the terminals of voltage regulator circuit, which, as we can observe once again, the output voltage is very close to 12V and with very reduced ripple, similarly to the results obtained in Octave.

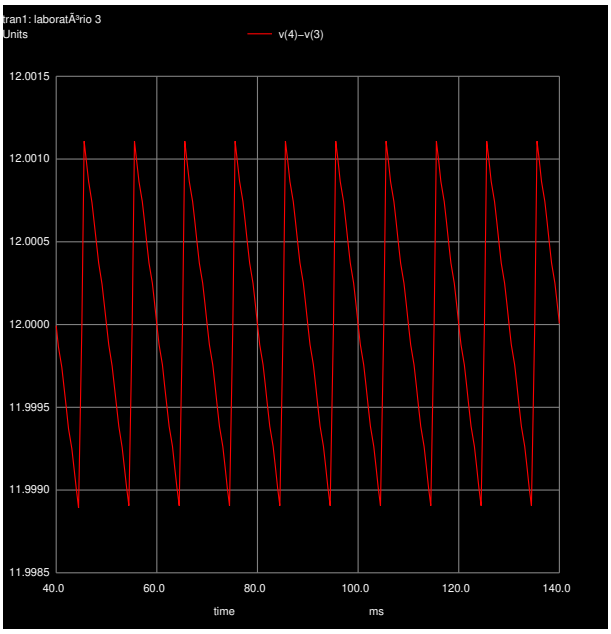

Figure 6: Output voltage of the circuit.

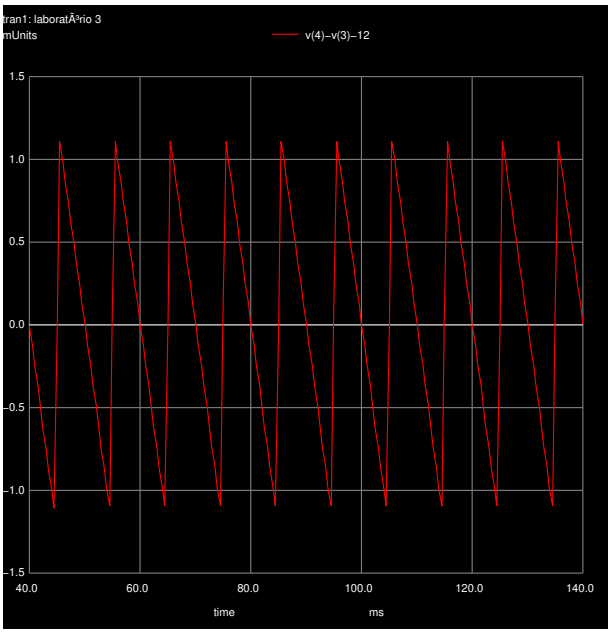

Figure 7: Output voltage - 12V : AC voltage oscilation of output voltage.

The Table 3 shows the average DC output and the output voltage ripple. Comparing the Table 2 with 3, we see that the difference between the output voltage is null and the difference between the output ripples is justified by the different models employed (Ngspice's model being more accurate).

Name	**Value**
maximum(v(4)-v(3))-minimum(v(4)-v(3))	2.217048e-03
mean(v(4)-v(3))	1.200000e+01

Table 3: Average voltage and ripple of the circuit developed in Ngspice.

4 Octave and Ngspice Comparison

Name	Value
Average Voltage	12.000000
Ripple	0.000175
Cost	432.280000
Merit	13.133719

Name	Value
maximum(v(4)-v(3))-minimum(v(4)-v(3))	2.217048e-03
mean(v(4)-v(3))	1.200000e+01

Table 4: Average voltage and ripple comparison of the circuit developed. To the left we can observe the reults from Octave and on the right, Ngspice. As to be expected, there is little discrepancy due to the non-linear nature of the components.

5 Conclusion

The objective of this laboratory assignment has been accomplished as can be seen by the results obtained. As desired, the average output voltage of circuit is 12V and the ripple is minimal, as can be seen in Table 3. Using these values to calculate the merit of the circuit, for a **cost of 432.28**, we obtained a **merit of 1.042951** in Ngspice.

Once again, we can note the small difference from the results obtained in Octave due to the non-linearity nature of the diode components.