Circuit Theory and Electronics Fundamentals

Department of Electrical and Computer Engineering, Técnico, University of Lisbon
Mestrado em Engenharia Aeroespacial

Laboratory 4 Report

Group 7

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Contents

1 Introduction

The objective of this laboratory assignment is to design a audio amplifier circuit keeping in mind that it must be cost efficient. The circuit and its organization can be seen in Figure 1. The values used in this circuit for the resistors and capacitor can be found in Table 1.

In Section 2, a theoretical analysis of the circuit is presented. In Section 3, the circuit is analysed by simulation, and the results are compared to the theoretical results obtained in Section 2. The conclusions of this study are outlined in Section 5.

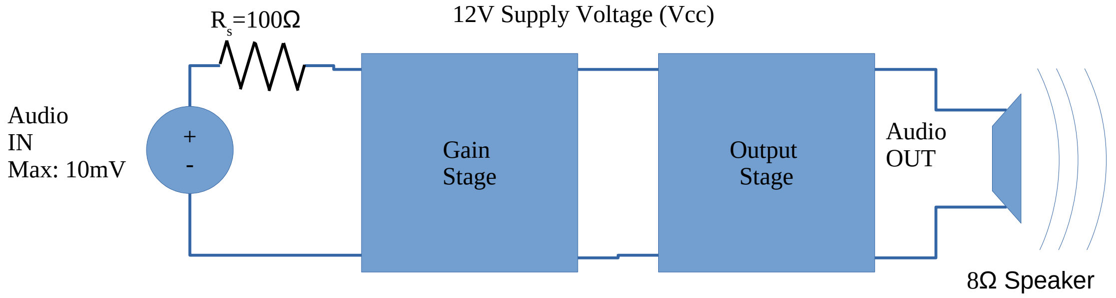

Figure 1: Circuit topography

Name	Value
R_{in}	100 Ohm
R_1	85k Ohm
R_2	20k Ohm
R_c	700 Ohm
R_e	200 Ohm
R_{out}	200 Ohm
C_i	16.25u F
C_b	5m F
C_o	3m F

Table 1: Resistor and Capacitor values used in the circuit.

2 Theoretical Analysis

In this section, the circuit shown in Figure 1 is analysed theoretically.

This circuit is divided in two diferent stages: a gain stage and an output stage. Firstly, the gain stage a cicuit similar to the one in page 5 of the slides of class L17, where it was also introduced a condensator in paralel with resistor Re, between the emitor node and the ground node. This stage of the circuit includes a bias circuit, responsible by making sure that the transistor is operating in the forward active region, and a coupling capacitor that blocks the DC component of the audio input.

On the other hand, in the output stage of the circuit we have a circuit similar to the one in page 14. This one is then responsible for lowering the output impedance so values compatible with the load (8 Ohm Speaker), which is going to be placed in series with another coupling capacitor on the Vo terminals of the circuit shown.

After constructing the theorical model of the circuit we now make use of Operating Point analysis to compute the gain, input and output impedances separately for both stages of the circuit. This analysis was done with resource to the many equations provided by the slides and by the professor.

Finally, we proceeded to do the frequency response analysis of the cicuit, where we obtained Figure 2 by computing the gain $V_o(f)/V_i(f)$.

Below we can observe the values desired for both stages of the cicuit, respectively, Gain Stage in Table 2 and Output Stage in Table 3.

Name	**Value**
Gain DB	43.594833dB
Gain	151.266122
Input Impedance	782.171517 Ohm
Output Impedance	663.764277 Ohm

Table 2: Gain, input and output impedances of the Gain Stage cicuit.

Name	**Value**
Gain	0.987012
Input Impedance	28306.476599 Ohm
Output Impedance	1.596379 Ohm

Table 3: Gain, input and output impedances of the Output Stage cicuit.

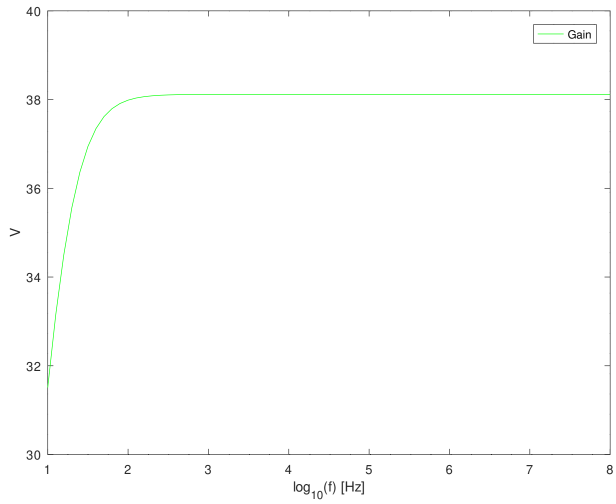

Figure 2: Gain (dB) in frequency response analysis.

Finally, in Table 4 we can observe the voltage gain, the bandwidth and the lower and upper Cutoff Frequency, as well as the impedances of the circuit. On Table 5, we can also observe the total cost and quality of the circuit and the resulting merit, when analysed in Octave.

Name	**Value**
Gain DB	41.931664dB
Gain	124.905964
Lower Cutoff Frequency	21.885107 Hz
Higher Cutoff Frequency	2290076.880516 Hz
Bandwidth	2290054.995409 Hz
Input Impedance	782.171517 Ohm
Output Impedance	4.409832 Ohm

Table 4: Total gain, cutoff frequencies, bandwidth and input and output impedances of the cicuit.

Name	**Value**
Quality	13070145.482690
Cost	8122.450000
Merit	1609.138312

Table 5: Quality, cost and Octave merit of the circuit.

3 Simulation Analysis

In this section, we will show the results of the Ngspice simulation. Here the results were obtained with the complex Philips transistor model given by the Professor, which lead to some differences when compared with the theoretical analysis. This was expected since here We encounter a circuit that is not linear, and, as a result, the theoretical model used is only an approximation of the nonlinear circuit. Below is presented the graph for the results obtained. In Figure 3 it can be observed the gain as a function of the frequency in log10 scale.

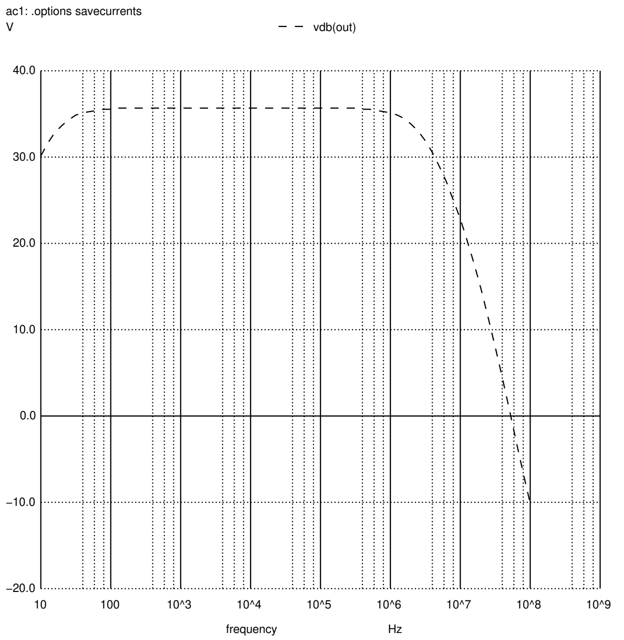

Figure 3: Gain in frequency response analysis.

The Table 6 presents the output voltage gain in the passband, the lower and upper 3dB cut off frequencies, as well as the input and output impedances in Table 7.

Name	**Value**
V Gain	60.9486
Gain DB	35.6993 dB
Bandwidth	2.65029E+06 Hz
CO Freq	15.5501 Hz

Table 6: Voltage gain, bandwidth and lower cutoff frequency.

Name	**Value**
Zo	5.85192 Ohm
Zin	894.193 Ohm

Table 7: Input and output impedances of the circuit.

The Table 8 presents for the NPN V_{CE} and V_{BE}, as well as for PNP V_{EC} and V_{EB}. As it can be seen, $V_{CE} > V_{BE}$ and $V_{EC} > V_{EB}$, which allows us to conclude that the transistors are in forward active region (FAR) as necessary.

Name	Value [V]
v(coll)-v(emit)	7.082747e+00
v(base)-v(emit)	6.923325e-01
v(emit2)	8.910931e+00
v(emit2)-v(coll)	7.198135e-01

Table 8: Verification of the FAR.

Using various values for the coupling capacitor, it became clear that it has a big effect on the lower cutoff frequency. By increasing its value, we were able to get closer to 20Hz, although increasing it has a respective increase in the overall cost of our amplifier. As far as the bypass capacitor is concerned, again by using multiple values for the capacitance we were able to understand that its main purpose it to stabilize the gain, allowing the gain to be stable in the passband that we desire. Here once again a compromise had to be made due to the fact that by increasing the capacitance the cost would also increase. The bypass capacitor will be an open circuit for low frequencies (where the DC is dominant) and a short-circuit for higher frequencies where AC is dominant. As a result, and as mentioned before the primary purpose of this capacitor is to stabilize in the passband that is desired. The R_c resistor was also studied. The higher its resistance got, the higher the gain at the gain stage was. A study was as made to find the optimal value for this resistor. Finally, and as it can be seen in Table 9, our merit was excelent, resulting in great gain, bandwidth, and lower cutoff frequency. In order to achieve these, the cost of the circuit was high, but it was compensated by the high quality, which allowed us to achieve a very high merit, as seen in the table.

Name	Value
Cost	8122.45
Quality	1.03878E+07
Merit	1278.9

Table 9: Cost, quality and merit of the circuit.

4 Octave and Ngspice Comparison

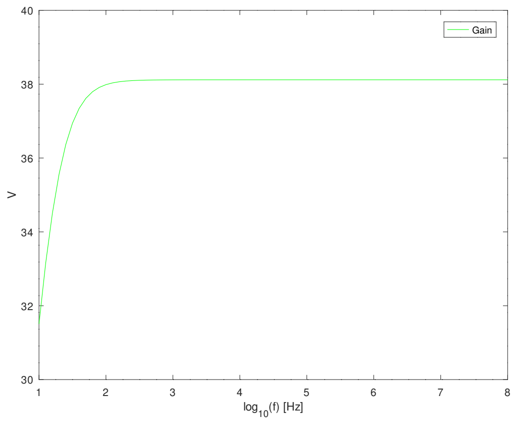

Figure 4: Gain (dB) in frequency response analysis in Octave.

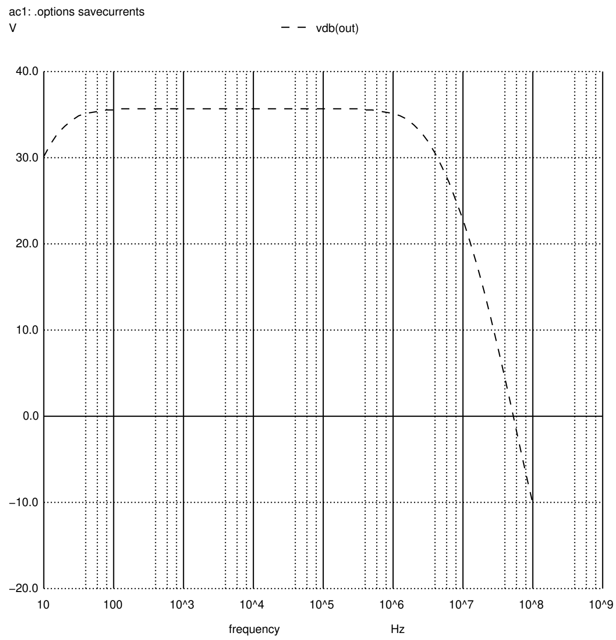

Figure 5: Gain (dB) in frequency response analysis in Ngspice.

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Table 10: Gain and input and output impedances. To the left we can observe the results from Octave and on the right, Ngspice. As to be expected, there is some discrepancy due to the non-linear nature of the components.

5 Conclusion

The objective of this laboratory assignment has been accomplished as can be seen by the results obtained. As desired, the gain is high (aprox. 35.7 dB) and although the cost is big the performance is excellent.

Despite our efforts to get equal results with the different analysis, we concluded that, due to the non-linearity of the components of the circuit, particularly the transistors, it was impossible to obtain the exact same results. The model used by Ngspice is far more complex than the one used in the theoretical analysis.

Comparing the output impedances and the input impedances we can see that even though they are not exactly the same, they are similar. Comparing the graphics we observe similar curves with similar CO frequencies.

In conclusion, as can be seen in Table 9 for a **cost of 8122.45**, we obtained a **merit of 1278.9** in Ngspice, which we found to be excellent results.