Architecture Specification

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This document contains three parts:

- the complete definition of one single SHAPES tile paths;
- the implemented sub-set of paths for the single-tile architecture;
- the extensions for the multi-tile SHAPES platform.

1 Complete Definition of One SHAPES Tile

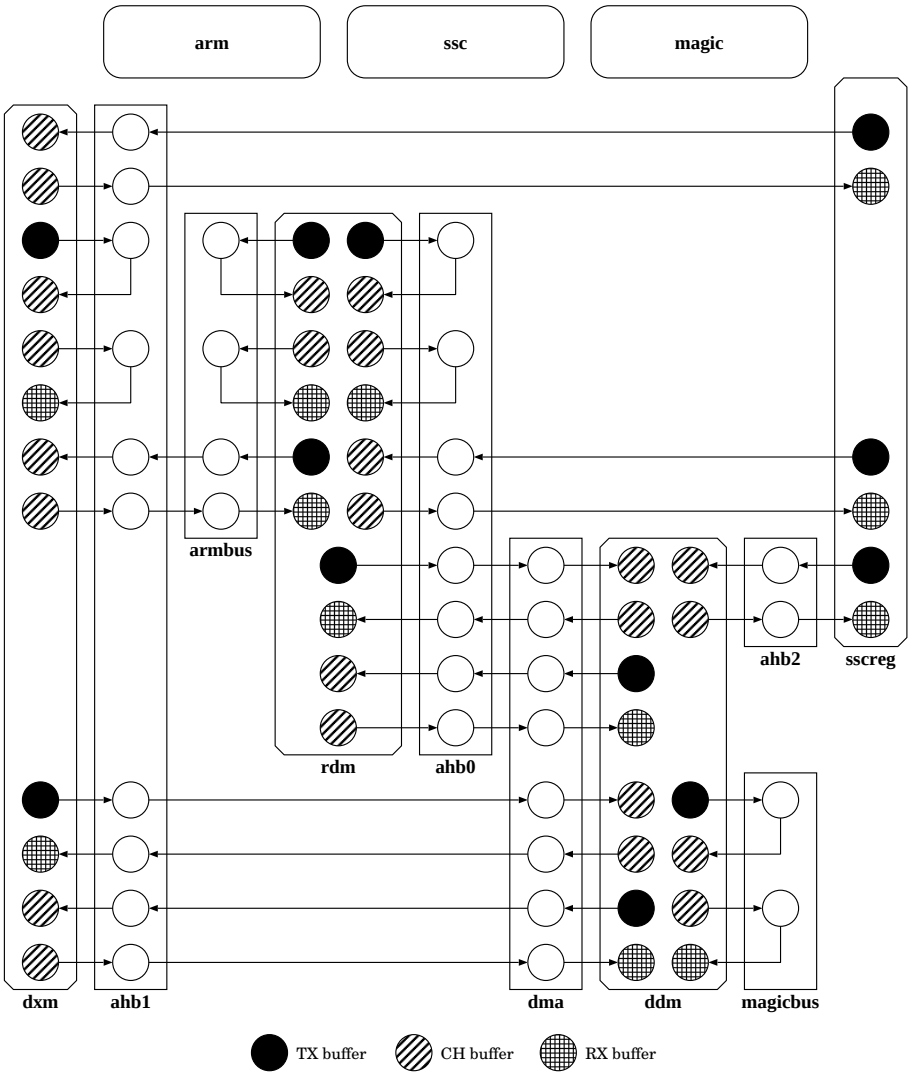

Figure 1: One Tile Complete Architecture.

```
<architecture>
  <!-- arm subsystem -->
  <processor name="arm" type="RISC">
    <configuration name="memory" value="ddm"/>
  </processor>

```

```
07  <memory name="rdm" type="RAM">
08  </memory>
09
10  <hw_channel name="armbus" type="BUS">
11  </hw_channel>
12
13  <!-- magic subsystem -->
14  <processor name="magic" type="DSP">
15    <configuration name="memory" value="ddm"/>
16  </processor>
17
18  <memory name="ddm" type="RAM">
19  </memory>
20
21  <hw_channel name="magicbus" type="BUS">
22  </hw_channel>
23
24  <hw_channel name="dma" type="DMA">
25  </hw_channel>
26
27  <!-- distributed external memory -->
28  <memory name="dxm" type="DXM">
29  </memory>
30
31  <!-- ssc subsystem -->
32  <processor name="ssc" type="POT">
33    <configuration name="memory" value="sscreg"/>
34  </processor>
35
36  <memory name="sscreg" type="RAM">
37  </memory>
38
39  <!-- ahb multi-layered bus -->
40  <hw_channel name="ahb0" type="BUS">
41  </hw_channel>
42
43  <hw_channel name="ahb1" type="BUS">
44  </hw_channel>
45
46  <hw_channel name="ahb2" type="BUS">
47  </hw_channel>
48
49
50  <!-- arm paths -->
51  <writepath name="rdmdxm">
52    <processor name="arm"/>
53    <txbuf name="rdm"/>
54    <hw_channel name="armbus"/>
55    <hw_channel name="ahb1"/>
56    <chbuf name="dxm"/>
57  </writepath>
58
59  <readpath name="dxmrdm">
60    <processor name="arm"/>
61    <chbuf name="dxm"/>
62    <hw_channel name="ahb1"/>
63    <hw_channel name="armbus"/>
64    <rxbuf name="rdm"/>
65  </readpath>
66
67  <writepath name="rdmrdmoverarm">
68    <processor name="arm"/>
69    <txbuf name="rdm"/>
70    <hw_channel name="armbus"/>
71    <chbuf name="rdm"/>
72  </writepath>
73
74  <readpath name="rdmrdmoverarm">
75    <processor name="arm"/>
76    <chbuf name="rdm"/>
77    <hw_channel name="armbus"/>
78    <rxbuf name="rdm"/>
79  </readpath>
80
```

```
81  <writepath name="armrdmddm">
82    <processor name="arm"/>
83    <txbuf name="rdm"/>
84    <hw_channel name="ahb0"/>
85    <hw_channel name="dma"/>
86    <chbuf name="ddm"/>
87  </writepath>
88
89  <readpath name="armddmrdm">
90    <processor name="arm"/>
91    <chbuf name="ddm"/>
92    <hw_channel name="dma"/>
93    <hw_channel name="ahb0"/>
94    <rxbuf name="rdm"/>
95  </readpath>
96
97  <writepath name="dxmdxm">
98    <processor name="arm"/>
99    <txbuf name="dxm"/>
100   <hw_channel name="ahb1"/>
101   <chbuf name="dxm"/>
102 </writepath>
103
104 <readpath name="dxmdxm">
105   <processor name="arm"/>
106   <chbuf name="dxm"/>
107   <hw_channel name="ahb1"/>
108   <rxbuf name="dxm"/>
109 </readpath>
110
111 <writepath name="rdmrdmoverahb">
112   <processor name="arm"/>
113   <txbuf name="rdm"/>
114   <hw_channel name="ahb0"/>
115   <chbuf name="rdm"/>
116 </writepath>
117
118 <readpath name="rdmrdmoverahb">
119   <processor name="arm"/>
120   <chbuf name="rdm"/>
121   <hw_channel name="ahb0"/>
122   <rxbuf name="rdm"/>
123 </readpath>
124
125 <writepath name="dxmddm">
126   <processor name="arm"/>
127   <txbuf name="dxm"/>
128   <hw_channel name="ahb1"/>
129   <hw_channel name="dma"/>
130   <chbuf name="ddm"/>
131 </writepath>
132
133 <readpath name="ddmdxm">
134   <processor name="arm"/>
135   <chbuf name="ddm"/>
136   <hw_channel name="dma"/>
137   <hw_channel name="ahb1"/>
138   <rxbuf name="dxm"/>
139 </readpath>
140
141 <!-- magic paths -->
142 <writepath name="ddmdxm">
143   <processor name="magic"/>
144   <txbuf name="ddm"/>
145   <hw_channel name="dma"/>
146   <hw_channel name="ahb1"/>
147   <chbuf name="dxm"/>
148 </writepath>
149
150 <readpath name="dxmddm">
151   <processor name="magic"/>
152   <chbuf name="dxm"/>
153   <hw_channel name="ahb1"/>
154   <hw_channel name="dma"/>
```

```
155     <rxbuf name="ddm"/>
156   </readpath>
157
158   <writepath name="ddmddm">
159     <processor name="magic"/>
160     <txbuf name="ddm"/>
161     <hw_channel name="magicbus"/>
162     <chbuf name="ddm"/>
163   </writepath>
164
165   <readpath name="ddmddm">
166     <processor name="magic"/>
167     <chbuf name="ddm"/>
168     <hw_channel name="magicbus"/>
169     <rxbuf name="ddm"/>
170   </readpath>
171
172   <writepath name="magicddmrdm">
173     <processor name="magic"/>
174     <txbuf name="ddm"/>
175     <hw_channel name="dma"/>
176     <hw_channel name="ahb0"/>
177     <chbuf name="rdm"/>
178   </writepath>
179
180   <readpath name="magicrdmddm">
181     <processor name="magic"/>
182     <chbuf name="rdm"/>
183     <hw_channel name="ahb0"/>
184     <hw_channel name="dma"/>
185     <rxbuf name="ddm"/>
186   </readpath>
187
188   <!-- ssc paths -->
189   <writepath name="sscregdxm">
190     <processor name="ssc"/>
191     <txbuf name="sscreg"/>
192     <hw_channel name="ahb1"/>
193     <chbuf name="dxm"/>
194   </writepath>
195
196   <readpath name="dxmsscreg">
197     <processor name="ssc"/>
198     <chbuf name="dxm"/>
199     <hw_channel name="ahb1"/>
200     <rxbuf name="sscreg"/>
201   </readpath>
202
203   <writepath name="sscregrdm">
204     <processor name="ssc"/>
205     <txbuf name="sscreg"/>
206     <hw_channel name="ahb0"/>
207     <chbuf name="rdm"/>
208   </writepath>
209
210   <readpath name="rdmsscreg">
211     <processor name="ssc"/>
212     <chbuf name="rdm"/>
213     <hw_channel name="ahb0"/>
214     <rxbuf name="sscreg"/>
215   </readpath>
216
217   <writepath name="sscregddm">
218     <processor name="ssc"/>
219     <txbuf name="sscreg"/>
220     <hw_channel name="ahb2"/>
221     <chbuf name="ddm"/>
222   </writepath>
223
224   <readpath name="ddmsscreg">
225     <processor name="ssc"/>
226     <chbuf name="ddm"/>
227     <hw_channel name="ahb2"/>
228     <rxbuf name="sscreg"/>
```

```
229   </readpath>
230 </architecture>
```

Listing 1: XML description of the VSP.

2 Implemented SHAPES Single-Tile Architecture

The implemented SHAPES tile is a sub-set of the architecture illustrated in the previous section, actually implementing just three on-tile communication paths:

- two possibilities for the ARM communication, i.e. one path via the internal memory (RDM) and one via external memory (DXM);
- one path for the DSP communication, i.e. via external memory (DXM).

```
01   <!-- on-tile communication paths -->
02
03   <!-- arm paths via dxm-->
04   <writepath name="rdmtodxm">
05     <processor name="arm"/>
06     <txbuf name="rdm"/>
07     <hw_channel name="armbus"/>
08     <hw_channel name="ahb1"/>
09     <chbuf name="dxm"/>
10   </writepath>
11
12   <readpath name="dxmfromrdm">
13     <processor name="arm"/>
14     <chbuf name="dxm"/>
15     <hw_channel name="ahb1"/>
16     <hw_channel name="armbus"/>
17     <rxbuf name="rdm"/>
18   </readpath>
19
20   <!-- arm paths via rdm-->
21   <writepath name="rdmtordm">
22     <processor name="arm"/>
23     <txbuf name="rdm"/>
24     <hw_channel name="armbus"/>
25     <chbuf name="rdm"/>
26   </writepath>
27
28   <readpath name="rdmfromrdm">
29     <processor name="arm"/>
30     <chbuf name="rdm"/>
31     <hw_channel name="armbus"/>
32     <rxbuf name="rdm"/>
33   </readpath>
34
35   <!-- magic paths via dxm-->
36   <writepath name="ddmtodxm">
37     <processor name="magic"/>
38     <txbuf name="ddm"/>
39     <hw_channel name="dma"/>
40     <hw_channel name="ahb1"/>
41     <chbuf name="dxm"/>
42   </writepath>
43
44   <readpath name="dxmfromddm">
45     <processor name="magic"/>
46     <chbuf name="dxm"/>
47     <hw_channel name="ahb1"/>
48     <hw_channel name="dma"/>
49     <rxbuf name="ddm"/>
50   </readpath>
```

Listing 2: Implemented on-tile communication paths.

3 Two-Tiles Architecture with a Global Naming Convention

A global naming convention for the different hardware elements in the multi-tile SHAPES architecture is used. The convention for the global naming is: ‘‘`tile_number.HWelement_number`’’. This allows the easy identification of the different elements and their location.

Listing 3 describes:

- two identic RDT tiles, i.e. `tile_0` and `tile_1`, where all the elements are named `tile_0.*` and `tile_1.*`, respectively;
- three intra-tile communication paths: two possibilities for the ARM communication, i.e. one path via the internal memory (RDM) and one via external memory (DXM), and one path for the DSP communication, i.e. via external memory (DXM);
- two inter-tile communication paths via DNP, one for the ARM and the other for the DSP.

The inter-tile communication is done via a network of directly connected DNPs using a toroidal mesh topology. The channel buffer involved in the inter-tile communication is located in the DXM of the receiving tile. Therefore, the inter-tile communication paths are defined as follows:

- **Write path.** The write path traverses both the local DNP and the DNP of the receiving tile, transferring data in the channel buffer located on the DXM of the receiving tile. For example, the ARM processor on the `tile_0` communicates with `tile_1` as follows: `tile_0.ARM --- tile_0.RDM --- tile_0.AHB --- tile_0.DNP --- tile_1.DNP --- tile_1.DXM`.
- **Read path.** On the reading path, processors collect data from the local DXM, following the same path and the same protocol as for the intra-tile communication.

Figure 2 represents both the inter- and intra- tile communication paths for the DSP and ARM processors located on the TILE_0 (`tile_0.arm` and `tile_0.magic`, respectively) and those located on the TILE_1 (`tile_1.arm` and `tile_1.magic`, respectively).

```
01 <architecture name="SHAPES multi-tile">
02 <!-- 2 Tiles communicating via the mesh of DNPs -->
03
04 <!-- tile_0 -->
05 /*+ TILE_0 RDT subsystem      ***************/
06 /*+ all elements are named: tile_0.element_i*/
07   <!-- tile_0 arm subsystem -->
08   <processor name="tile_0.arm" type="RISC">
09   </processor>
10
11   <memory name="tile_0.rdm" type="RAM">
12   </memory>
13
14   <hw_channel name="tile_0.armbus" type="BUS">
15   </hw_channel>
16
17   <!-- tile_0 magic subsystem -->
18   <processor name="tile_0.magic" type="DSP">
19   </processor>
20
```

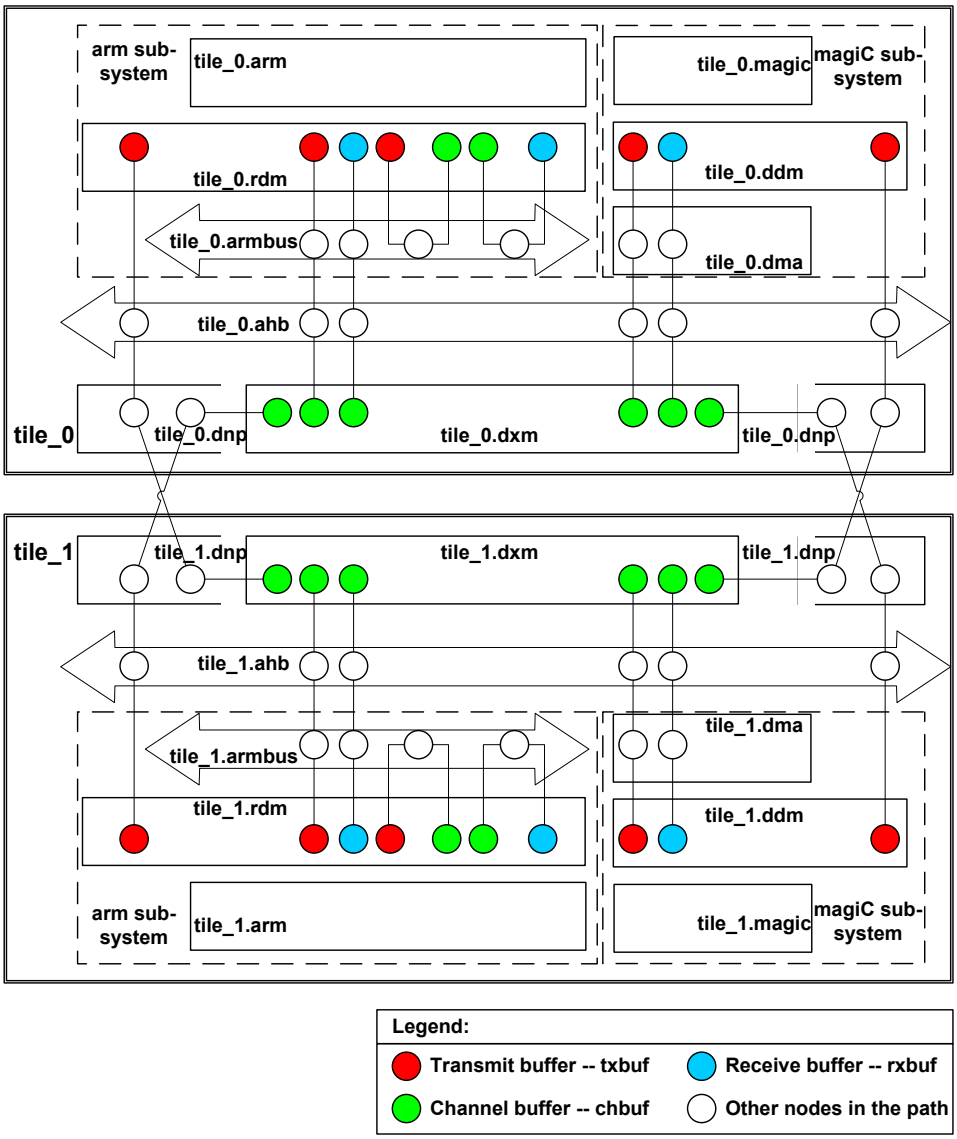

Figure 2: Example for the intra-tile communication paths.

```
21  <memory name="tile_0.ddm" type="RAM">
22  </memory>
23
24  <hw_channel name="tile_0.magicbus" type="BUS">
25  </hw_channel>
26
27  <hw_channel name="tile_0.dma" type="DMA">
28  </hw_channel>
29
30  <!-- tile_0 distributed external memory -->
31  <memory name="tile_0.dxm" type="DXM">
32  </memory>
33
34  <!-- tile_0 ahb multi-layered bus -->
35  <hw_channel name="tile_0.ahb0" type="BUS">
36  </hw_channel>
37
38  <hw_channel name="tile_0.ahb1" type="BUS">
39  </hw_channel>
40
41  <!-- tile_0 dnp -->
42  <hw_channel name="tile_0.dnp" type="SPI">
43  </hw_channel>
```

```
44
45 /*+ TILE_0 intra-tile communication paths              **************/
46 /*+ arm implements 2 types of communication: via dxm and via rdm    */
47 /*+ magic implements 1 type of communication: via dxm **************/
48   <!-- tile_0 intra-tile communication paths -->
49   <!-- tile_0 arm paths via dxm-->
50   <writepath name="tile_0.rdmtodxm">
51     <processor name="tile_0.arm"/>
52     <txbuf name="tile_0.rdm"/>
53     <hw_channel name="tile_0.armbus"/>
54     <hw_channel name="tile_0.ahb1"/>
55     <chbuf name="tile_0.dxm"/>
56   </writepath>
57
58   <readpath name="tile_0.dxmfromrdm">
59     <processor name="tile_0.arm"/>
60     <chbuf name="tile_0.dxm"/>
61     <hw_channel name="tile_0.ahb1"/>
62     <hw_channel name="tile_0.armbus"/>
63     <rxbuf name="tile_0.rdm"/>
64   </readpath>
65
66   <!-- tile_0 arm paths via rdm-->
67   <writepath name="tile_0.rdmtordm">
68     <processor name="tile_0.arm"/>
69     <txbuf name="tile_0.rdm"/>
70     <hw_channel name="tile_0.armbus"/>
71     <chbuf name="tile_0.rdm"/>
72   </writepath>
73
74   <readpath name="tile_0.rdmfromrdm">
75     <processor name="tile_0.arm"/>
76     <chbuf name="tile_0.rdm"/>
77     <hw_channel name="tile_0.armbus"/>
78     <rxbuf name="tile_0.rdm"/>
79   </readpath>
80
81   <!-- tile_0 magic paths via dxm-->
82   <writepath name="tile_0.ddmtodxm">
83     <processor name="tile_0.magic"/>
84     <txbuf name="tile_0.ddm"/>
85     <hw_channel name="tile_0.dma"/>
86     <hw_channel name="tile_0.ahb1"/>
87     <chbuf name="tile_0.dxm"/>
88   </writepath>
89
90   <readpath name="tile_0.dxmfromddm">
91     <processor name="tile_0.magic"/>
92     <chbuf name="tile_0.dxm"/>
93     <hw_channel name="tile_0.ahb1"/>
94     <hw_channel name="tile_0.dma"/>
95     <rxbuf name="tile_0.ddm"/>
96   </readpath>
97
98 /*+ TILE_0 inter-tile communication paths (via DNP) */
99 <!-- tile_0 ARM inter-tile communication paths -->
100   <writepath name="tile_0.rdmtodnp">
101     <processor name="tile_0.arm"/>
102     <txbuf name="tile_0.rdm"/>
103     <hw_channel name="tile_0.ahb0"/>
104     <hw_channel name="tile_0.dnp"/>
105     <hw_channel name="tile_1.dnp"/>
106     <chbuf name="tile_1.dxm"/>
107   </writepath>
108
109 <!-- tile_0 DSP inter-tile communication paths -->
110   <writepath name="tile_0.ddmtodnp">
111     <processor name="tile_0.magic"/>
112     <txbuf name="tile_0.ddm"/>
113     <hw_channel name="tile_0.ahb0"/>
114     <hw_channel name="tile_0.dnp"/>
115     <hw_channel name="tile_1.dnp"/>
116     <chbuf name="tile_1.dxm"/>
117   </writepath>
```

```
118
119 <!-- tile_1 -->
120 /*+ TILE_1 RDT subsystem      ***************/
121 /*+ all elements are named: tile_1.element_i*/
122   <!-- tile_1 arm subsystem -->
123   <processor name="tile_1.arm" type="RISC">
124   </processor>
125
126   <memory name="tile_1.rdm" type="RAM">
127   </memory>
128
129   <hw_channel name="tile_1.armbus" type="BUS">
130   </hw_channel>
131
132 /*+ tile_1: the same elements as the RDT tile_0******/
133 ...
134 /*+ TILE_1 inter-tile communication paths (via DNP) */
135 <!-- tile_1 ARM inter-tile communication paths -->
136   <writepath name="tile_1.rdmtodnp">
137     <processor name="tile_1.arm"/>
138     <txbuf name="tile_1.rdm"/>
139     <hw_channel name="tile_1.ahb0"/>
140     <hw_channel name="tile_1.dnp"/>
141     <hw_channel name="tile_0.dnp"/>
142     <chbuf name="tile_0.dxm"/>
143   </writepath>
144
145 <!-- tile_1 DSP inter-tile communication paths -->
146   <writepath name="tile_1.ddmtodnp">
147     <processor name="tile_1.magic"/>
148     <txbuf name="tile_1.ddm"/>
149     <hw_channel name="tile_1.ahb0"/>
150     <hw_channel name="tile_1.dnp"/>
151     <hw_channel name="tile_0.dnp"/>
152     <chbuf name="tile_0.dxm"/>
153   </writepath>
154
155 </architecture>
```

Listing 3: The `architecture.xml` file.