EEE 342 Laboratory Experiment 3 Margin Analysis of a System Work Report

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1. Introduction

In this laboratory experiment we are assigned to theoretically find gain, phase and delay margins of a feedback controller system. Then experimentally find gain and delay margin to compare our analytic approximation with real data.

2. Laboratory Content

Part 1: Margin Estimation

In order to analyze the system we first need to construct it. We are asked to select the PI controller that provides the least settling time. This is the first PI controller since it was designed to have the least settling time. This controller has the transfer function of

$G_C(s)$ =

12.69 s + 223.4

17.6 s

Continuous-time transfer function.

Also the transfer function of the DC motor plant is

$G_P(s)$ =

-1.181 s^2 + 215.4 s + 4158

0.02728 s^3 + 5.544 s^2 + 17.6 s

Continuous-time transfer function.

Then the open loop transfer function becomes

$G(s) = G_P(s)*G_C(s)$

-1.181 s^2 + 215.4 s + 4158

0.02728 s^3 + 5.544 s^2 + 17.6 s

Continuous-time transfer function.

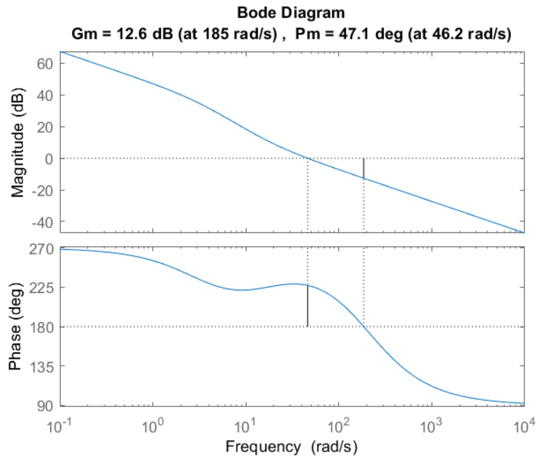

Fig. 1: Bode plot of the open loop transfer function

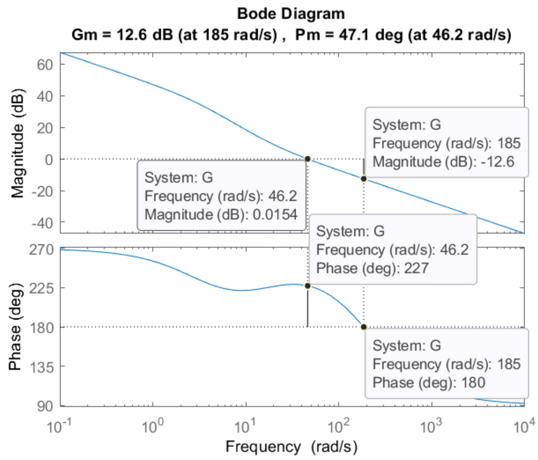

Fig. 2: Theoretical Gain and Phase Margins on Bode Plot

Gain margin is the reciprocal of the gain at the frequency where the transfer function has π rad of phase. This corresponds to 12.6 dB at 185 rad/s which is

$$GM = 4.2658$$

Also phase margin is the difference between the phase of the transfer function at the frequency where the magnitude of the transfer function is 1 and π rad. This corresponds to

$$PM = 227.1-180 = 47.1 \text{ degrees} = 0.8221 \text{ rd}$$

At frequency ω_x = 46.2 rd/s. From these values we can calculate the delay margina as follows

$$DM = \frac{PM}{\omega_x} = \frac{0.8221}{46.2} = 0.0178s = 17.8ms$$

Our delay margin is 17.8 ms.

Part 2: Margin Verification

In this part of the experiment we tried to find the gain and delay margin of the closed loop system by trial and error. In order to do so, we used the Simulink system design. Our design for finding the gain margin is

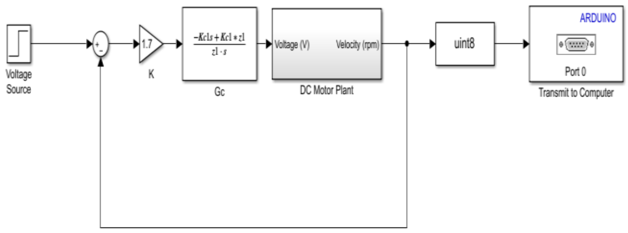

Fig. 3: Simulink Design for Finding Gain Margin

We have used the reference input as 40u(t), step input with amplitude 40. In order to, find the gain margin we have started the value of the gain from the theoretical gain margin and we have observed that the system is unstable for that gain. Then we decreased the gain. When we have reached to gain of 1.8 our observed response was the following

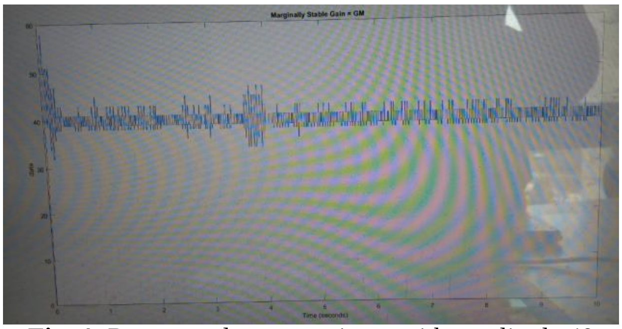

Fig. 4: Response due to step input with amplitude 40 with gain of 1.8

One can say that the system is marginally stable at gain 1.8. Also our actual gain margin is in between 1.7 and 1.9 as it can be seen from the following plot

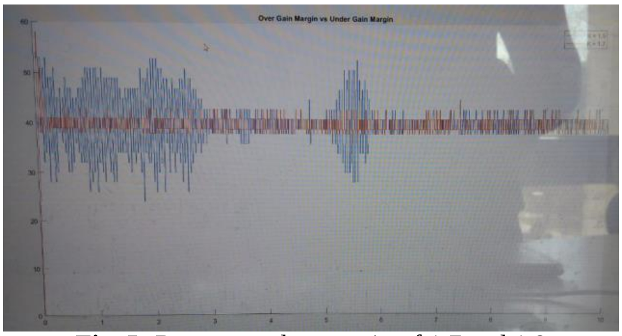

Fig. 5: Responses due to gain of 1.7 and 1.9

Blue plot is the step response due gain of 1.9 and the red plot is the step response due step input with amplitude 40. It can be seen that the gain margin is between 1.7 and 1.9 since at gain of 1.7 the system is stable and at gain of 1.9 the system is unstable. Our approximate result to gain margin 1.8 is appropriate. This gain margin is significantly smaller with respect to theoretical calculations, which is 4.2658. This due to reason that we have approximated the transfer function of the DC motor plant as a first order transfer function at the previous experiment. However, the system is actually nonlinear. This is why the real margin is smaller than the theoretical estimate. After gain margin evaluation we have used the following Simulink design to find the real delay margin

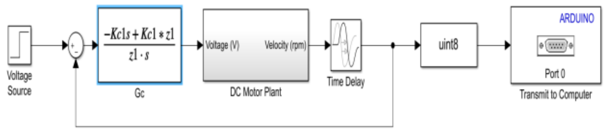

Fig. 6: Simulink Design for Finding Delay Margin

Once again in order to find the real delay margin we have started from the theoretical delay margin but system was stable. However, as we decreased the delay the system remain unstable. Our possible minimum delay that we can measure is 10ms since it is the sampling rate of the Arduino we have used. Then we have taken the data for 10ms delay and no delay.

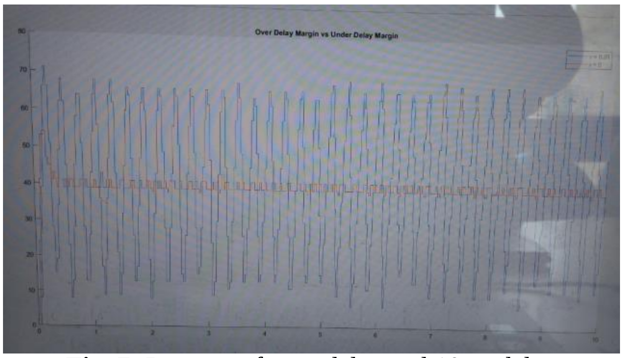

Fig. 7: Response for no delay and 10ms delay

The blue plot is the response due to 10ms delay and the red plot is the response due to no delay. As one can see that 10ms delayed closed loop system is unstable but no delay system is stable. However, since we cannot measure a delay between 0 and 10ms we can only say that our delay margin is in between 0 and 10ms. This again smaller than the theoretical calculations. Theoretically we have estimated that the delay margin is 17.8ms. Real value is smaller than the theoretical estimate because system is nonlinear and we approximated the DC motor plant as a first order system but the system is actually nonlinear.

3. Conclusion

To conclude, in this laboratory experiment we have analyzed the system we have designed in the previous experiment. This analysis had two parts, theoretical and experimental. In the theoretical part we have estimated the gain, phase and delay margin using the bode plot of the open loop system. In the experimental part we have used trial and error procedure to find the real gain and delay margin. Actual results are significantly smaller with respect to theoretical results due to our linear first order approximation to nonlinear nature of DC motor plant, which was expected. This laboratory experiment was important because understanding the margins of the system helps us to understand system in terms of our limits for closed loop systems in terms of gain, phase and delay. Also we once again experienced difference between real nonlinear system and our linear approximations to it.

APPENDIX

```
Gc = tf([-Kc1,Kc1*z1],[z1,0])
G = Gc*Gp
bode(G)
margin(G)
figure
plot(titrek)
title('Marginally Stable Gain
= GM')
figure
hold on
plot(titrek1)
plot(titrek2)
legend('K = 1.9','K = 1.7')
title('Over Gain Margin vs
Under Gain Margin')
figure
hold on
plot(delay_titrek)
plot(delaysiz_titrek)
legend('\tau = 0.01','\tau =
0')
title('Over Delay Margin vs
Under Delay Margin')
```