**Margin Analysis of a System**

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1. **Introduction**

The aim of this laboratory assignment is to understand and get familiar with margins, which are gain phase and delay margin. We estimate these margins using mathematical models and verify them.

1. **Laboratory Content**
   1. **Margin Estimation**

In the previous laboratory assignment, we had designed three PI controllers. The bode diagram of our open loop transfer function is:

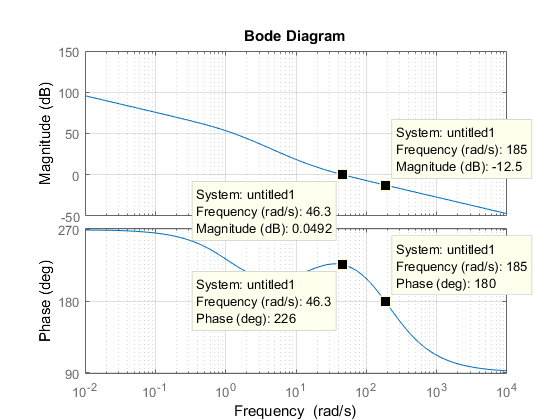


Figure 1: Bode Diagram with Margin Data Points

For phase margin, we look at the frequency where the magnitude is 1, i.e. 0 dB. This frequency is observed on the Bode plot as At this frequency, on the phase plot, the corresponding phase is Then the Phase Margin (PM) is:

To calculate the Gain Margin (GM), we find the frequency where the phase is and find the corresponding gain on this frequency. As it can be seen from the Bode phase plot, the phase becomes at the and the gain at that frequency is -12.5 dB. Then, our gain margin is

0 – (-12.5) = 12.5 dB

This margin corresponds to the gain K:

Delay Margin (DM) is where is the frequency where the gain is 0 dB. In our case, is found as . Therefore, delay margin is:

* 1. **Margin Verification**

To verify these estimated margins, we use DC motor hardware. For input, we configured our system and increased the gain K until we find the gain that makes the system uınstable. We had found K1 = 29.4372 in the previous lab and now, we have several trails to find that gain:

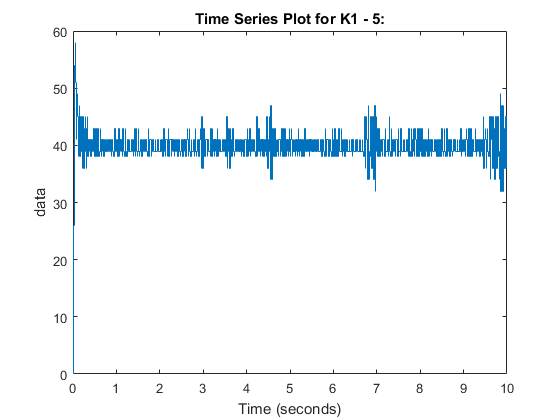


Figure 2: Response of the system with gain K1-5

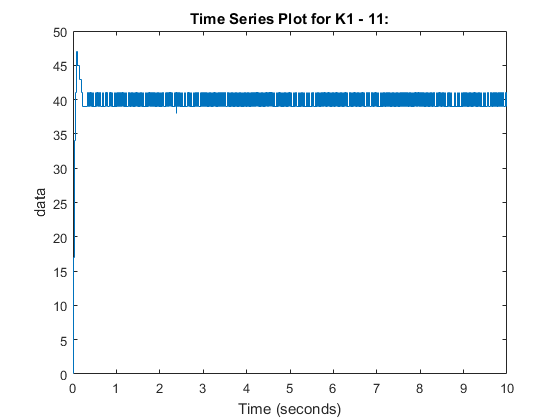
Figure 3: Response of the system with gain K1-6

Figure 4: Response of the system with gain K1-11

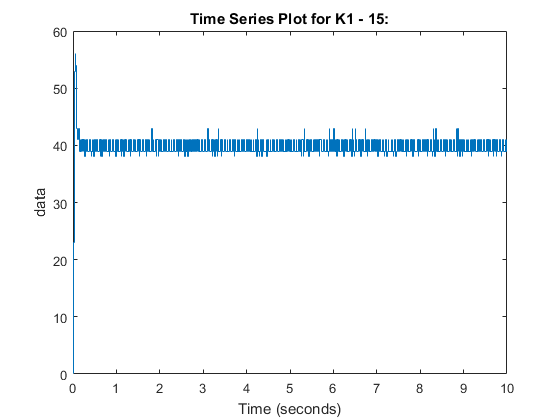
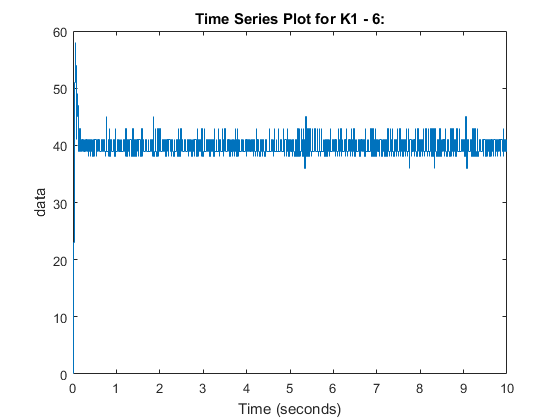


Figure 5: Response of the system with gain K1-15

According to these trial and errors, the gain that makes the system unstable is:

Therefore, experimentally, our gain margin is observed as 18.4.

The second part of the experiment is about delay margin and its verification using hardware. Again, as we did for gain margin, we find the delay that makes the system unstable by trial and error.

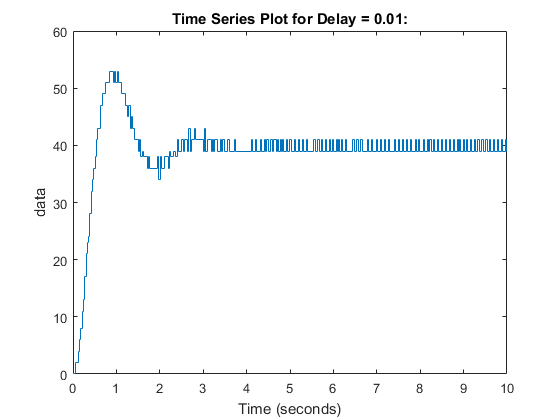


Figure 6: Response of the system with delay = 0.01 s

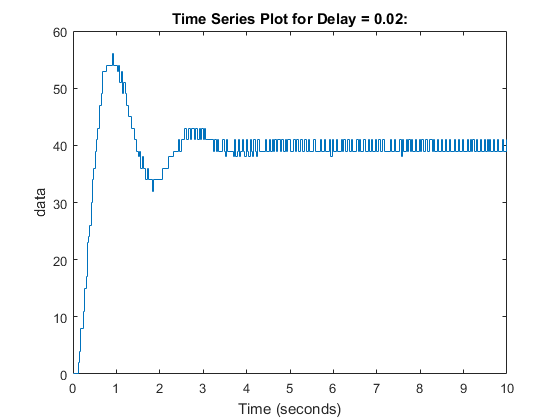


Figure 7: Response of the system with delay = 0.02 s

Figure 8: Response of the system with delay = 0.035 s

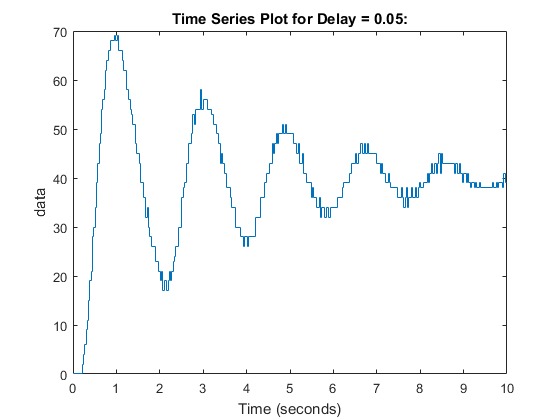
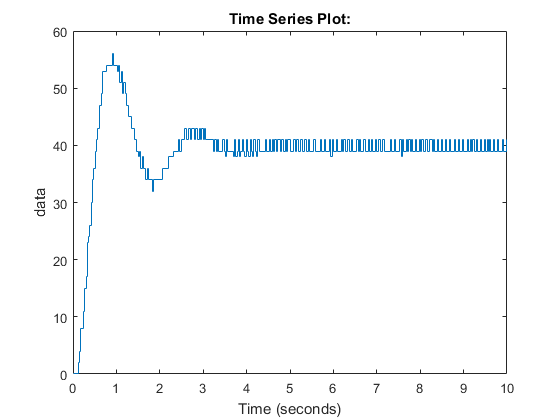


Figure 9: Response of the system with delay = 0.05 s

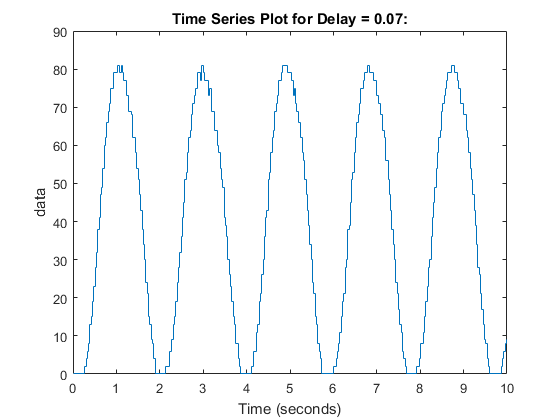
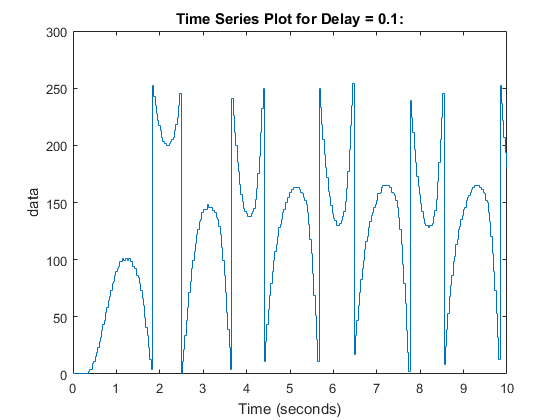


Figure 10: Response of the system with delay = 0.07 s

 Figure 11: Response of the system with delay = 0.1 s

According to these trial and errors, the delay margin that makes the system unstable is:

1. **Conclusion**

**REFERENCES**

1. Dorf, Richard C., and Robert H. Bishop. *Modern Control Systems*. 13th ed., Pearson, 201

**APPENDIX**