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EE 202 Section 1

EEE 202 CIRCUIT THEORY

LAB 3

Software Implementation

In this lab experiment, we are expected to design a circuit which creates a specific $8V_{pp}$ waveform from $5V_{pp}$ square wave. The rise and fall times of this waveform must be 3ms and it must remain in its maximum voltage for 2ms. Also, it must start to rise after the falling edge of the square wave. The input and target waveforms are given below (Figure 1).

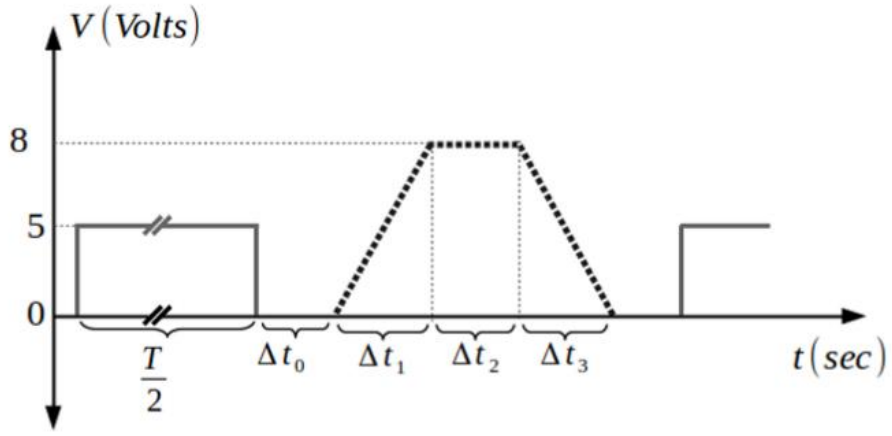

Figure 1: Input is square wave, Target is dashed line

Briefly all the restrictions to create this waveform are given below (Figure 2).

$$\Delta t_0 = 3ms, \quad \Delta t_1 = 3ms, \quad \Delta t_2 = 2ms, \quad \Delta t_3 = 3ms$$

Input peak voltage: $5V$

Output peak voltage: $8V$

Input frequency: $f < 50Hz, \quad T = \frac{1}{f}$

Figure 2: Wanted features of input and output

To form this signal wave, 3 different type op-amp circuit will be used. Comparator circuits are going to create the $8V_{pp}$ square wave, integrator circuit will create the slopes with specific rise or fall time, and finally subtractor circuit will create the delay at the maximum voltage.

Comparator Circuit:

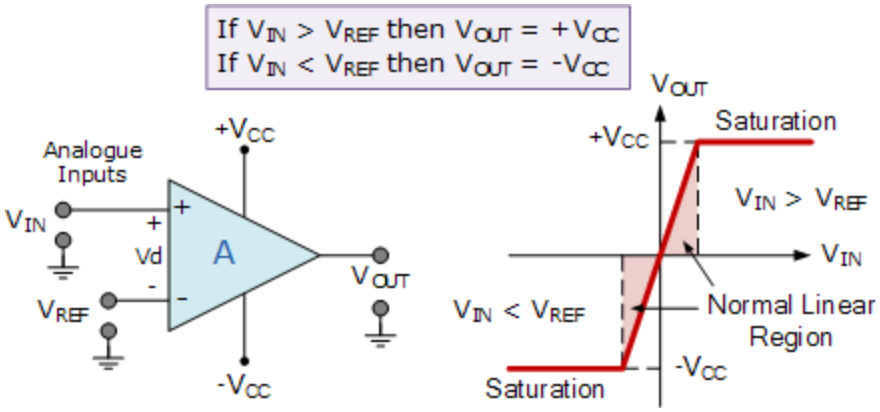

Figure 3:

Comparator circuit compares the given inputs. If the input voltage on the V_+ is bigger than V_- , it outputs $+V_{CC}$ (max saturation), If the input voltage on the V_- is bigger than V_+, it outputs $-V_{CC}$ (min saturation), the relation is shown in Figure 3.

Normally to create 8V voltage we need to connect $+V_{CC}$ to 8V; however, LM324 automatically decrease it around 1.5V because of its inner impedance. Thus, 9.5V will be connected to $+V_{CC}$.

To create the $8V_{pp}$ voltage with 3ms delay, 1.5V will be connected to V_- while an RC circuit is connected to V_+. Behind the logic of this design is that in the RC circuit output voltage cannot be increase suddenly, so up to a point output voltage will be smaller than 1.5V voltage

and so the op-amp will output its min saturation ground. In this way 3ms delay is created. To find the required resistor and capacitor values the formula below is used.

$$V_{out} = V_{final} + (V_{initial} - V_{final}) * e^{-t/RC}$$

V_{final}= 0V, $V_{initial}$= 5V for the square wave, V_{out}= 1.5V by delay logic, and t= Δt_0=3ms so the equation below is obtained.

$$1.5V = 5V * e^{-3ms/RC}$$

By the equation above $R * C = 2.49 * 10^{-3}$.

C is chosen as 10nF, and R is chosen as 249KΩ

The final design is shown below in Figure 4, where VCC= 9.5V, V1_5=1.5V. Also, its simulation result is given in Figure 5.

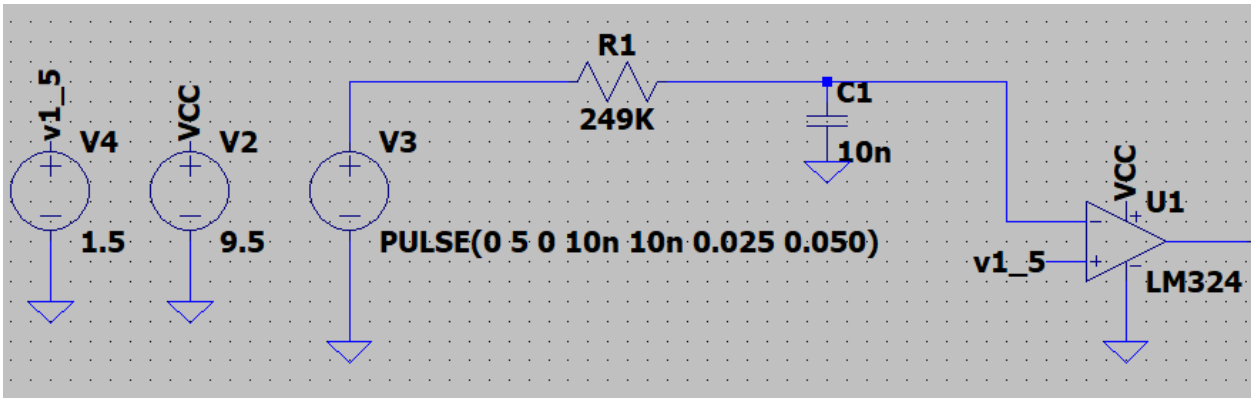

Figure 4: Final circuit design for comparator circuit

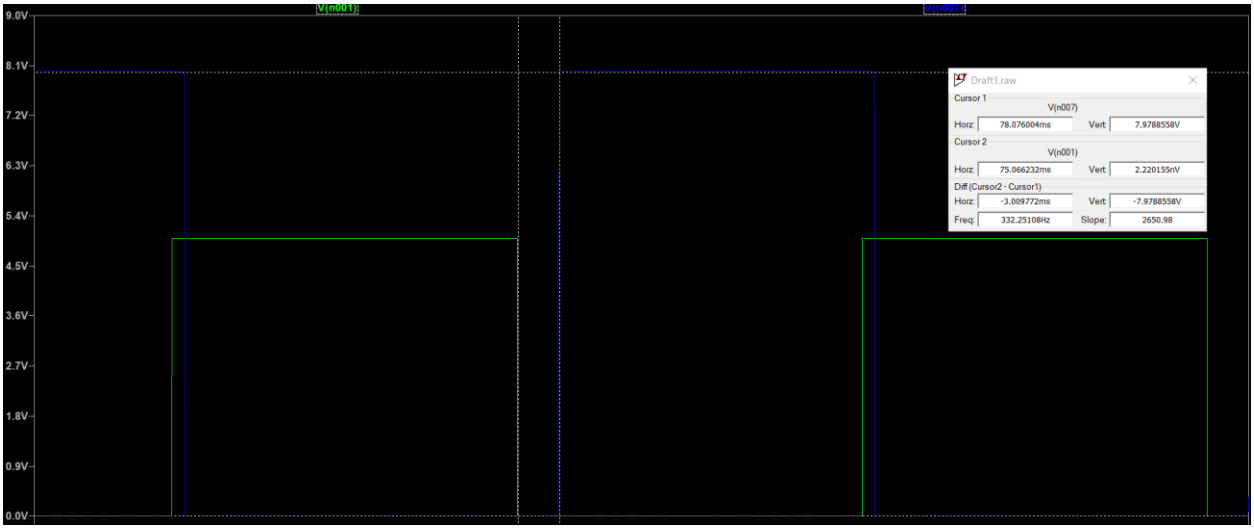

Figure 5: Simulation result in the circuit in Figure 4, $8V_{pp}$ square wave is obtained with Δt_0=3ms delay

Integrator Circuit:

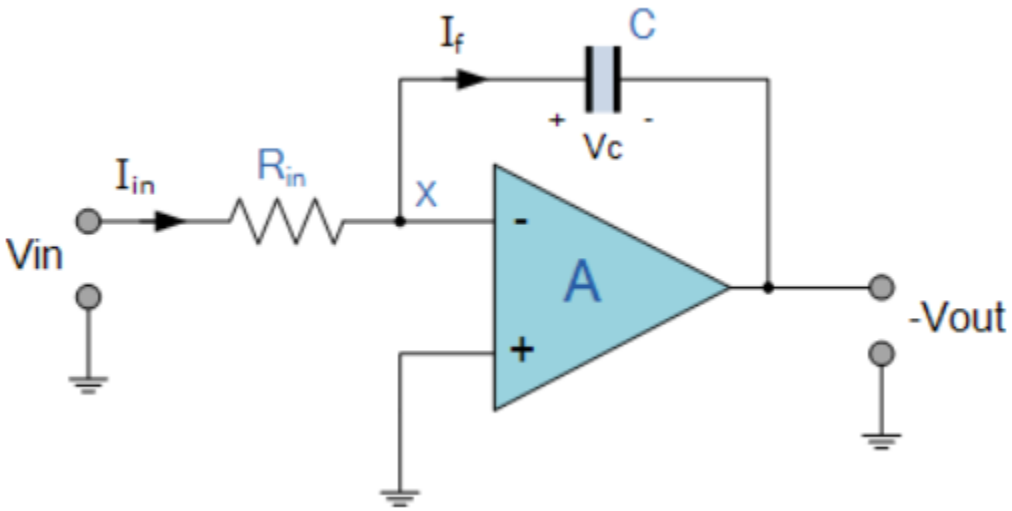

Figure 6: Sample Integrator circuit figure

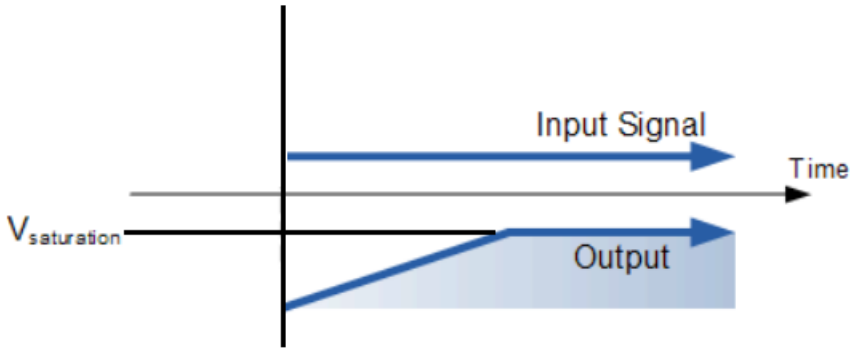

Figure 7: Sample integrator circuit input and output

Integrator circuit consists of resistor and capacitor (it can be done in inductor and resistor as well), a sample integrator circuit is shown in Figure-6. This circuit integrates the input signal and gives integration result as result. The sample relation is shown in Figure 7.

In our circuit we need to create a slope with 3ms delay at the falling edge. Which will be serve as both rising and falling edge after subtraction. To calculate the value of needed resistor and capacitor. The current relation below is used.

$$\frac{V_{input} - V_{-}}{R} = i = C * \frac{dV_c}{dt} = C * \frac{d(V_{output} - V_{-})}{dt}$$

For ideal op-amps it is known that V_{-}=V_{+}, in the circuit 1.5V is connected to V_{+}. Therefore, V_{-}=$V_{+} = 1.5V$.Also $V_{max}$for input is 8V. Using these equations in the equation above, the equation below is obtained.

$$\frac{V_{input} - V_{-}}{RC} = \frac{8V - 1.5V}{RC} = \frac{d(V_{output} - 1.5V)}{dt} = \frac{d(V_{output})}{dt}$$

By integrating both sides the equation below is obtained. Keeping in mind the output must be 8V since we just want to have 3ms delay without changing amplitude of the signal.

$$\int_0^{3ms} \frac{6.5V}{RC} = V_{output} = 8V$$

By the equation above RC $= 0.8125 * 3 * 10^{-3}$.

C is chosen as 10nF again; therefore, R is 243.75K, but 244K will be used for the convenience.

The final circuit is given below in Figure 8.

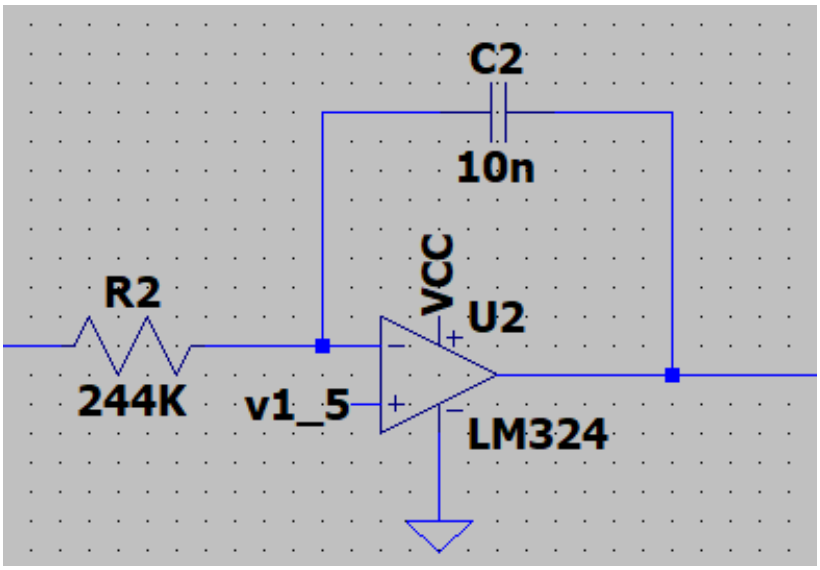

Figure 8: Final circuit design for integrator circuit

The simulation result for this circuit is given below in Figure 9 that shows the needed slope in 3ms.

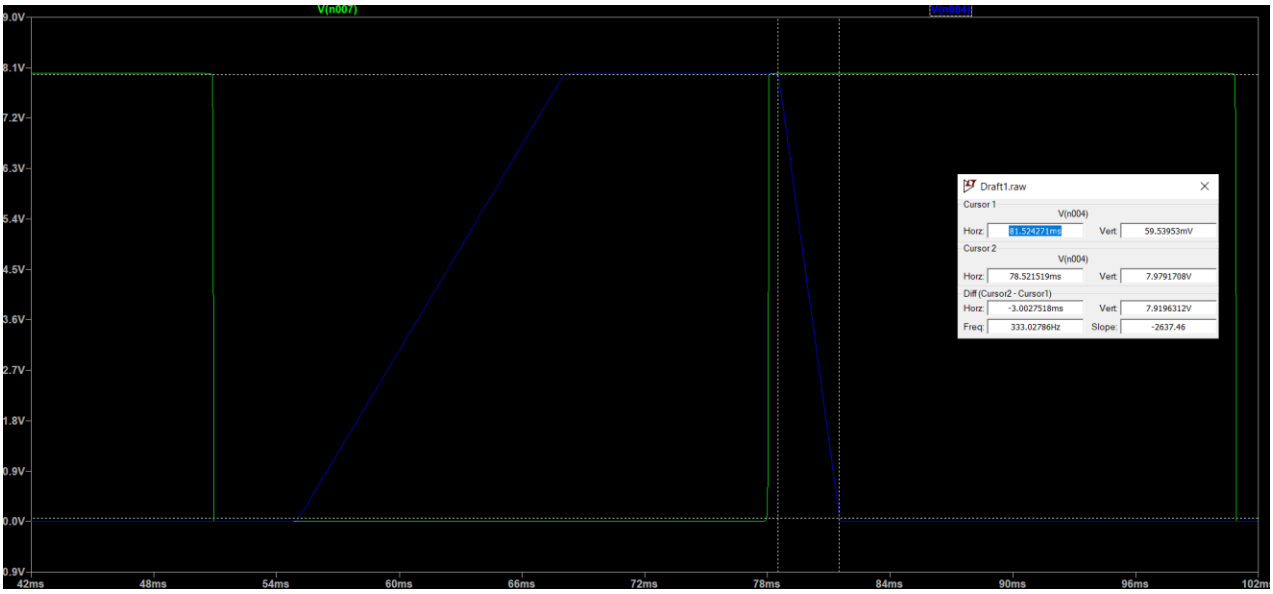

Figure 9: Simulation result in the circuit in Figure 8, a slope in 3ms is created

Subtractor Circuit:

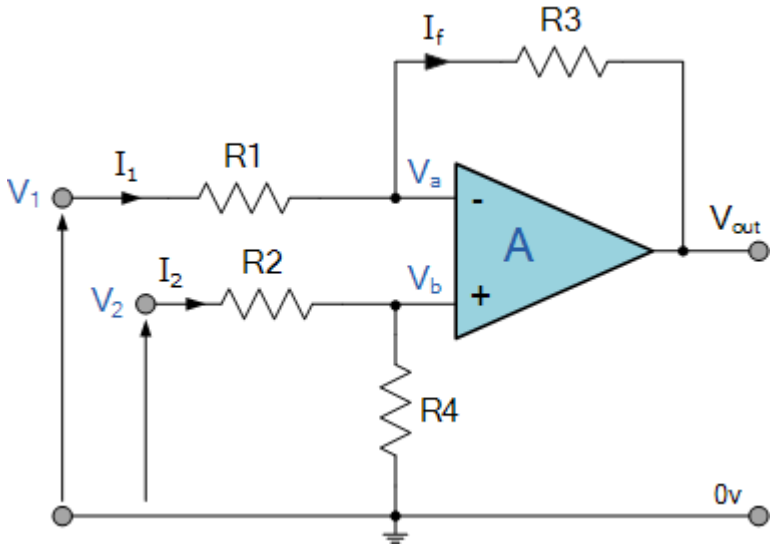

Figure 10: Sample integrator circuit figure

Subtractor circuit only consists of resistors and op-amp. When all the in resistors in the Figure 10 above are chosen equal, it gives $V_2 - V_1$ as output. Its proof is given below.

$$V_- = V_+ = V_2 \frac{R_4}{R_2+R_4}$$

$$\frac{V_1 - V_-}{R_1} = \frac{V_- - V_{out}}{R_3}$$

By using both equations above the equation below is obtained.

$$\frac{V_1 - V_2 \frac{R_4}{R_2+R_4}}{R_1} = \frac{V_2 \frac{R_4}{R_2+R_4} - V_{out}}{R_3}$$

By simplifying the equation above the equation below is obtained.

$$V_{out} = V_2 * \frac{R_4}{R_2+R_4} * \frac{R_1 + R_3}{R_1} - V_1 * \frac{R_3}{R_1}$$

If all the resistors are chosen equally the final relation is obtained.

$$V_{out} = V_2 - V_1$$

The final circuit is given below in Figure 11.

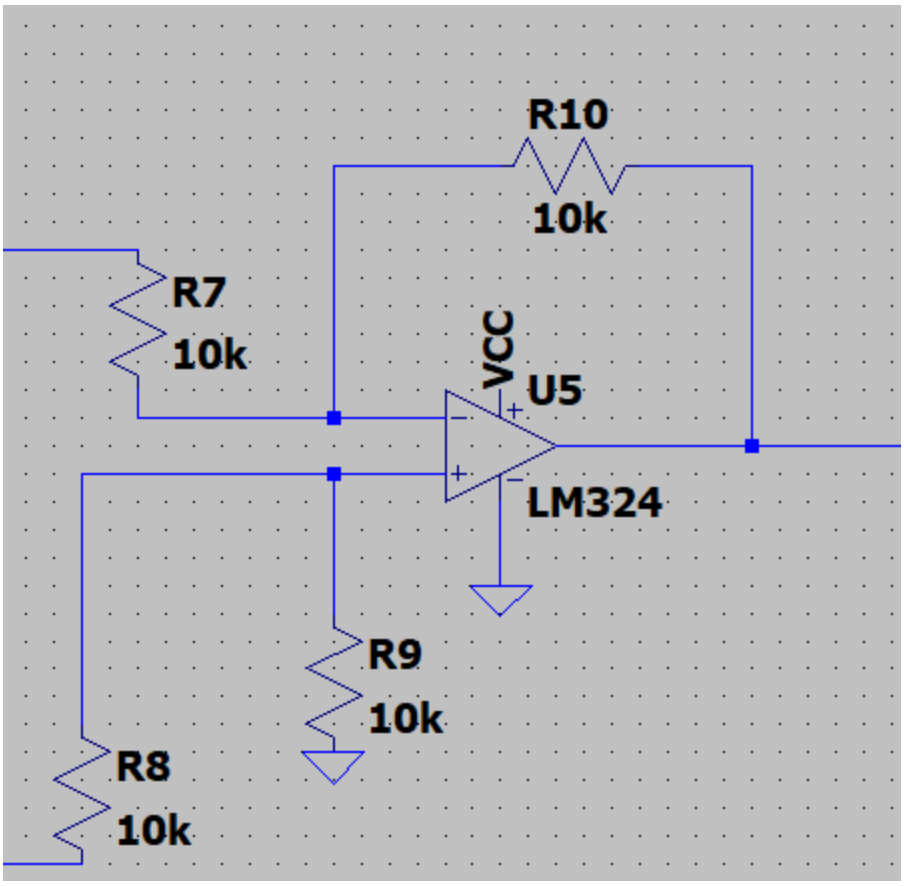

Figure 11: Final circuit design for subtractor circuit

However, until now only upside is created, for the downside same things will be done with one difference. For the second comparator circuit delay must be set to 8ms ($\Delta t_0 + \Delta t_1 + \Delta t_2$) instead of 3ms. It is because to have the 2ms delay (Δt_2) at the max amplitude of the needed signal.

$$1.5V = 5V * e^{-8ms/RC}$$

By the equation above $R * C = 6.64 * 10^{-3}$.

C is chosen as 10nF, and R is chosen as 664KΩ

The complete circuit for the downside is given below in Figure 12.

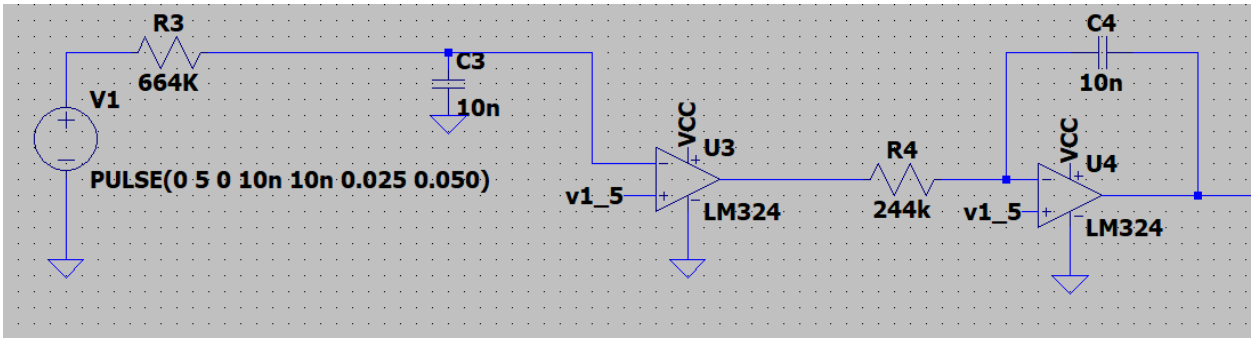

Figure 12: Final circuit for the downside of subtractor

After completing all the needed relations, the complete circuit is given below in Figure 13.

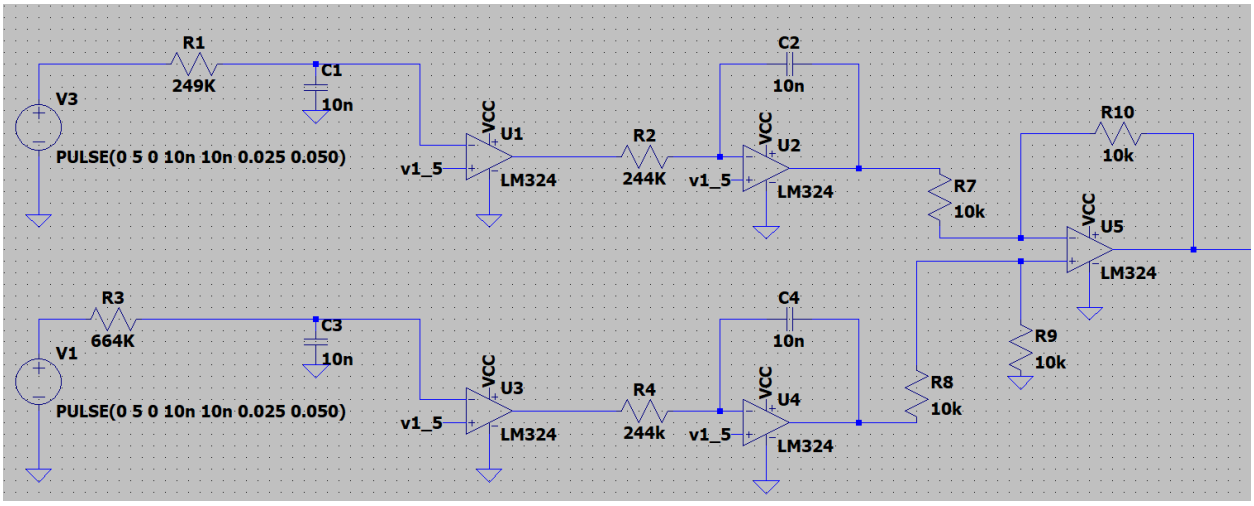

Figure 13: Designed circuit

Its simulation result is given below in Figure 14. However, there is a mistake in this circuit Δt_0 is changed.

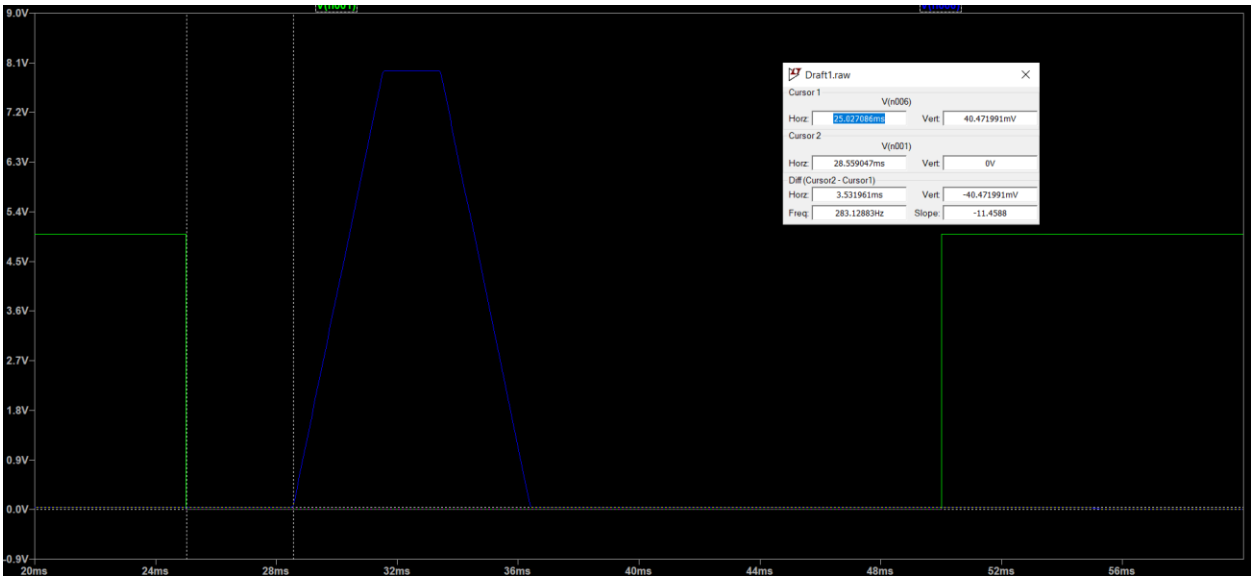

Figure 14: The problem with the circuit in Figure 13, Δt_0 is increased

The change of the Δt_0 is raised from the capacitor in the integrator circuit, since the capacitor created a delay. The delay is 0.5ms. Therefore, to get rid of this delay, in the first circuit the delay is chosen as 3.5ms instead of 3ms.

$$1.5V = 5V * e^{-{-3.5ms}/{RC}}$$

By the equation above $R * C = 2.22 * 10^{-3}$.

C is chosen as 10nF, and R is chosen as 222KΩ

Finally, the complete circuit is given below in Figure 15.

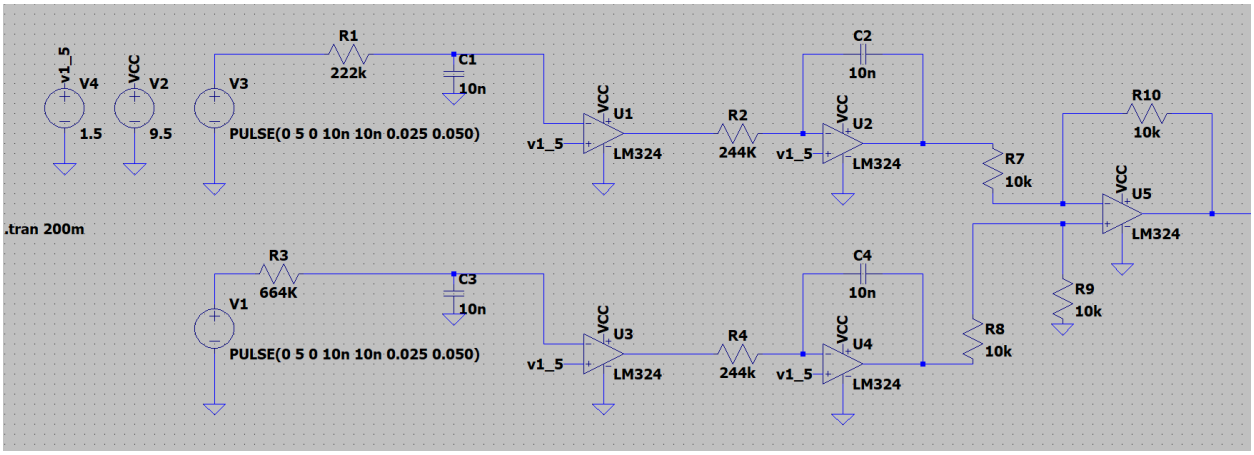

Figure 15: The final circuit after the change of R1

Simulation results for the circuit in Figure 15 is given below in Figure 16, Figure 17, Figure 18, Figure 19.

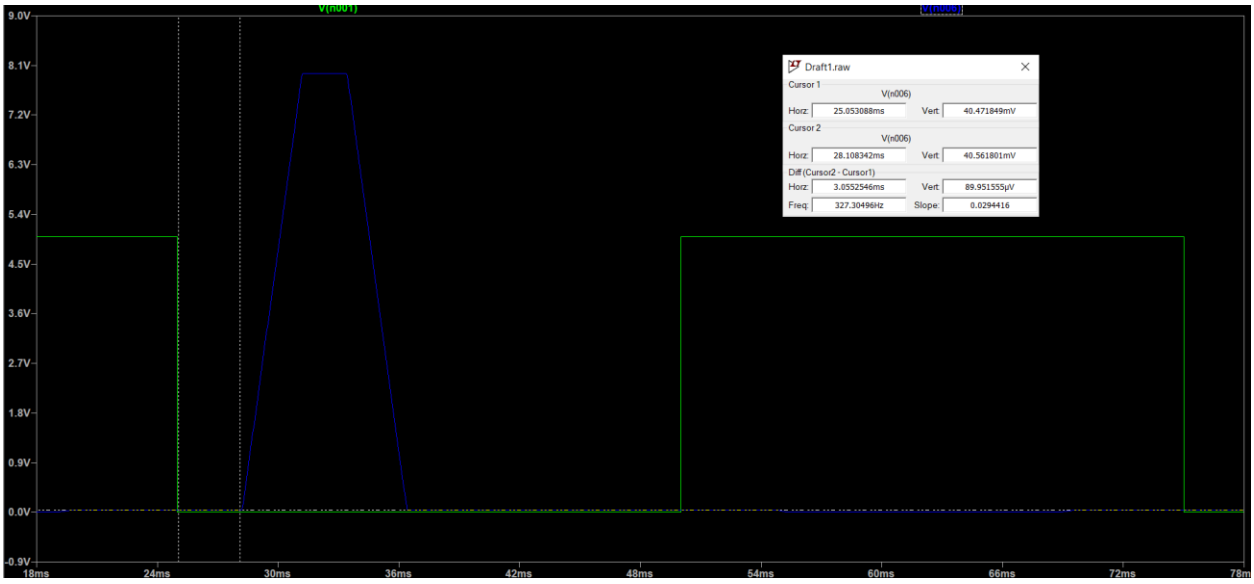

Figure 16: Result 1 of final circuit, $\Delta t_0 = 3ms$

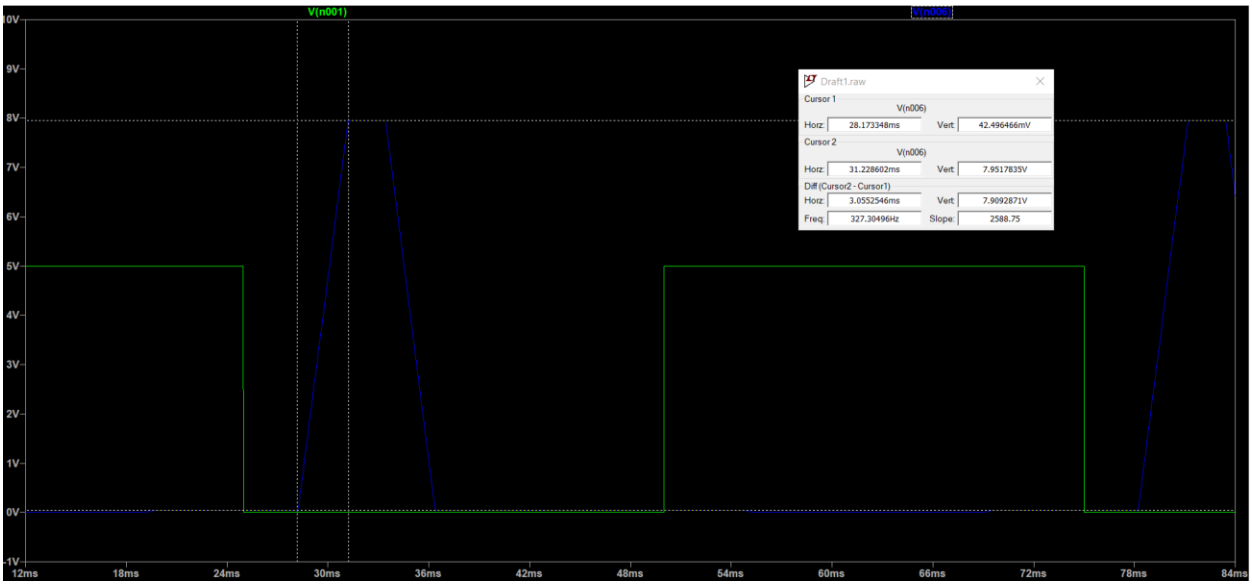

Figure 17: Result 2 of final circuit, $\Delta t_1 = 3ms$

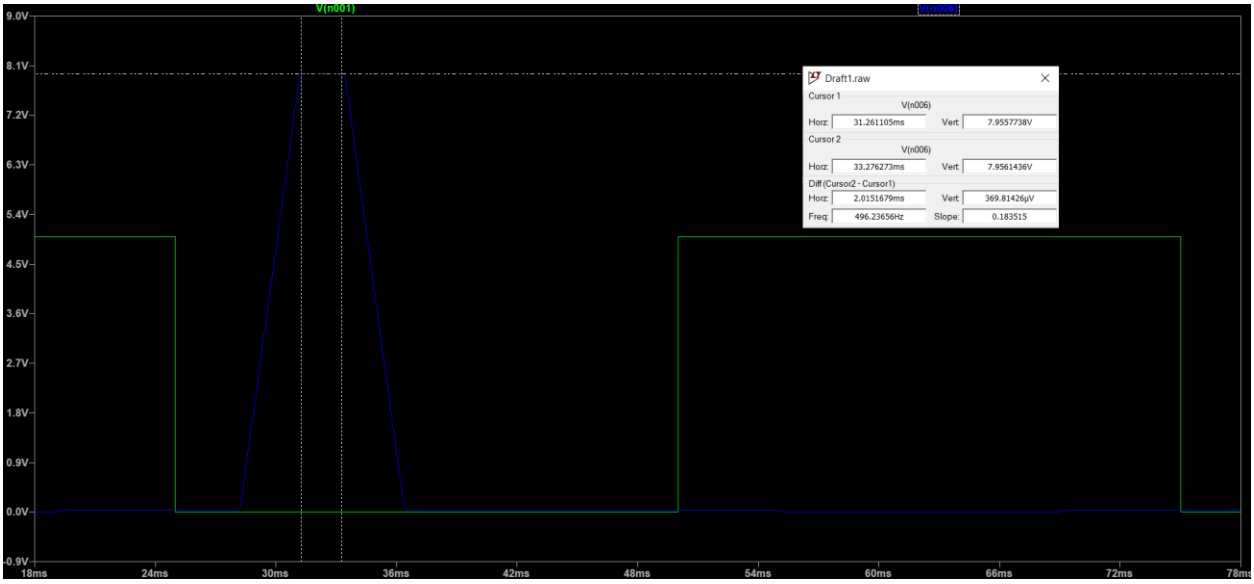

Figure 18: Result 3 of final circuit $\Delta t_2 = 2ms$, Amplitude of the signal is 8V.

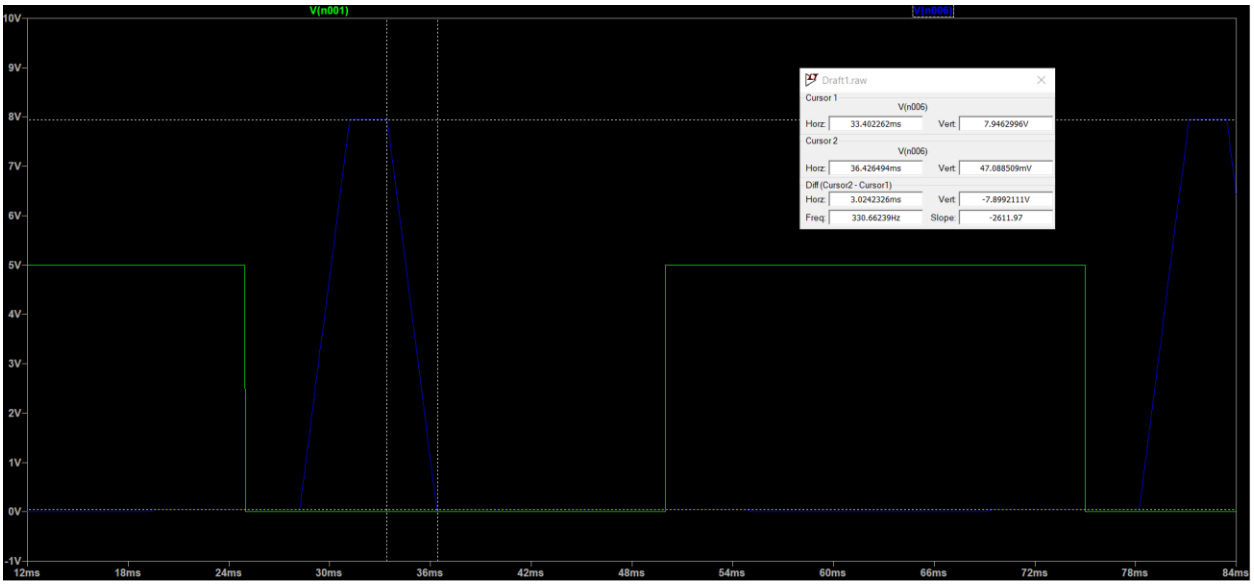

Figure 19: Result 4 of final circuit $\Delta t_3 = 3ms$

Hardware Implementation

In the hardware implementation part I used the same circuit that I used in the software implementation which is given in Figure 15. In the hardware implementation part, the data sheet of LM324 is used to be sure about connections that is given below in Figure 20.

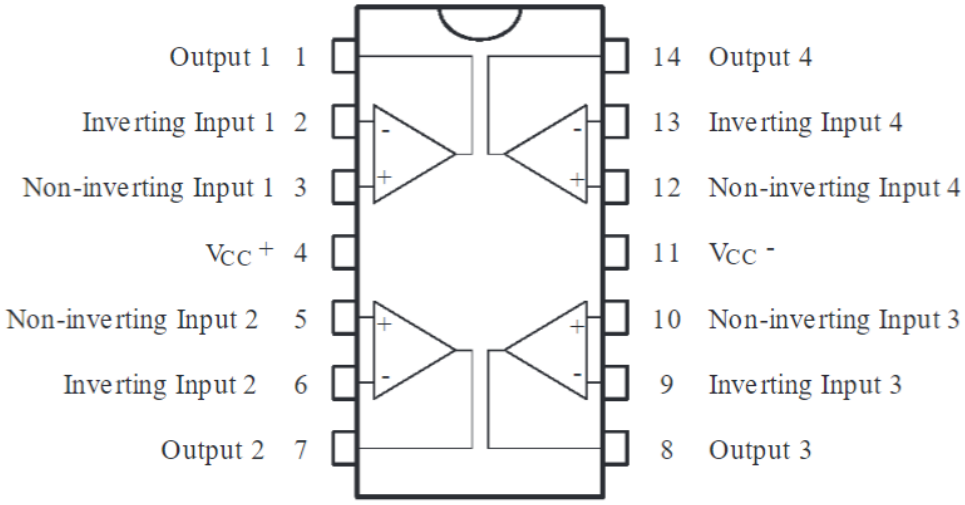

Figure 20: Real LM-324 op-amp scheme

To obtain the needed waveform in Figure 1, the same circuit from software implementation part is used which is Figure 15. The real-life implementation on breadboard is given below in Figure 21.

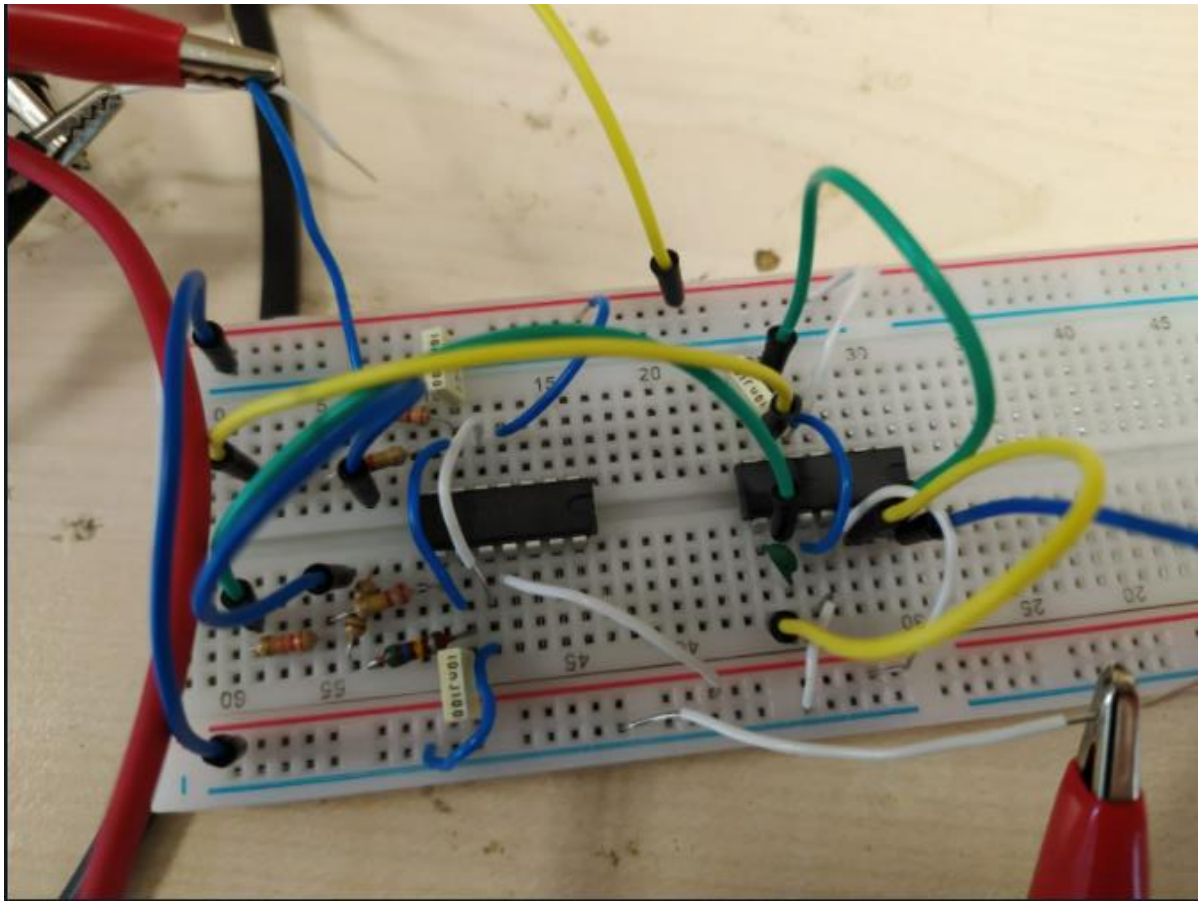

Figure 21: Real life implementation

After creating the real-life circuit, needed delays has measured using oscilloscope. The results are given below in Figure 22, Figure 23, and Figure 24.

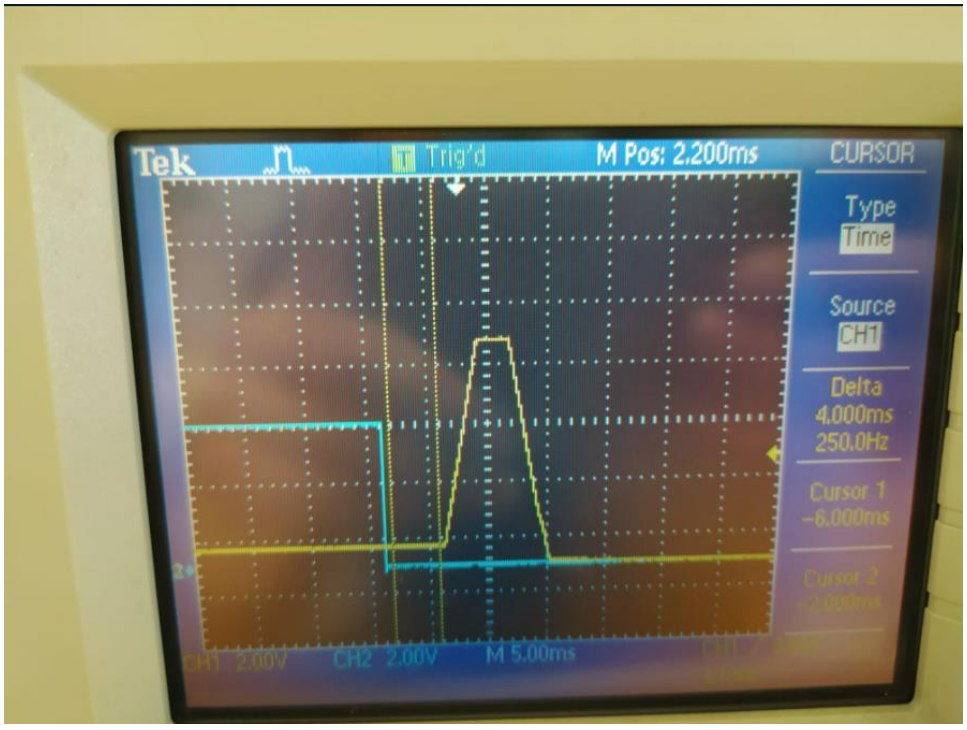

Figure 22: Result 1 of final circuit, $\Delta t_0 = 4ms$, amplitude of wave is 7.9V

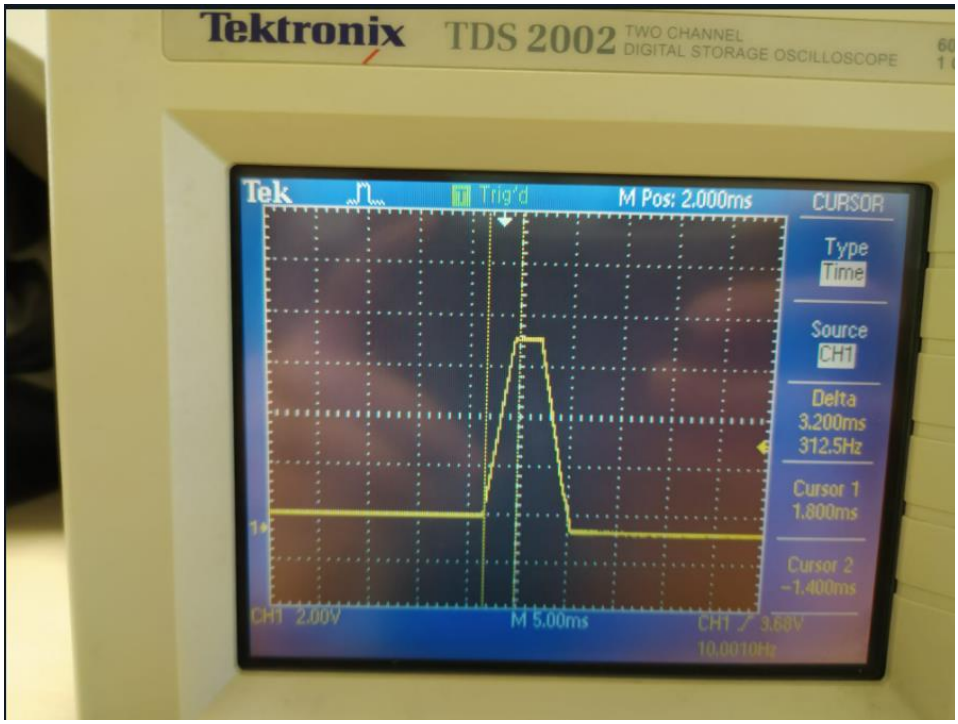

Figure 23: Result 2 of final circuit, $\Delta t_1 = 3.2ms$

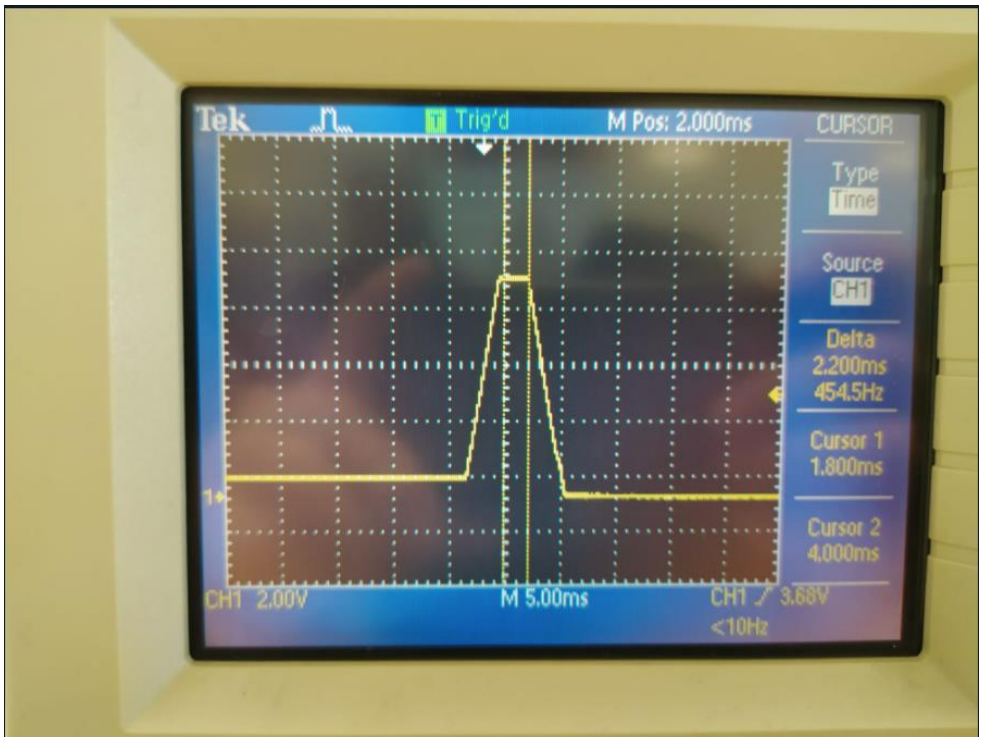

Figure 24: Result 3 of final circuit, $\Delta t_2 = 2.2ms$

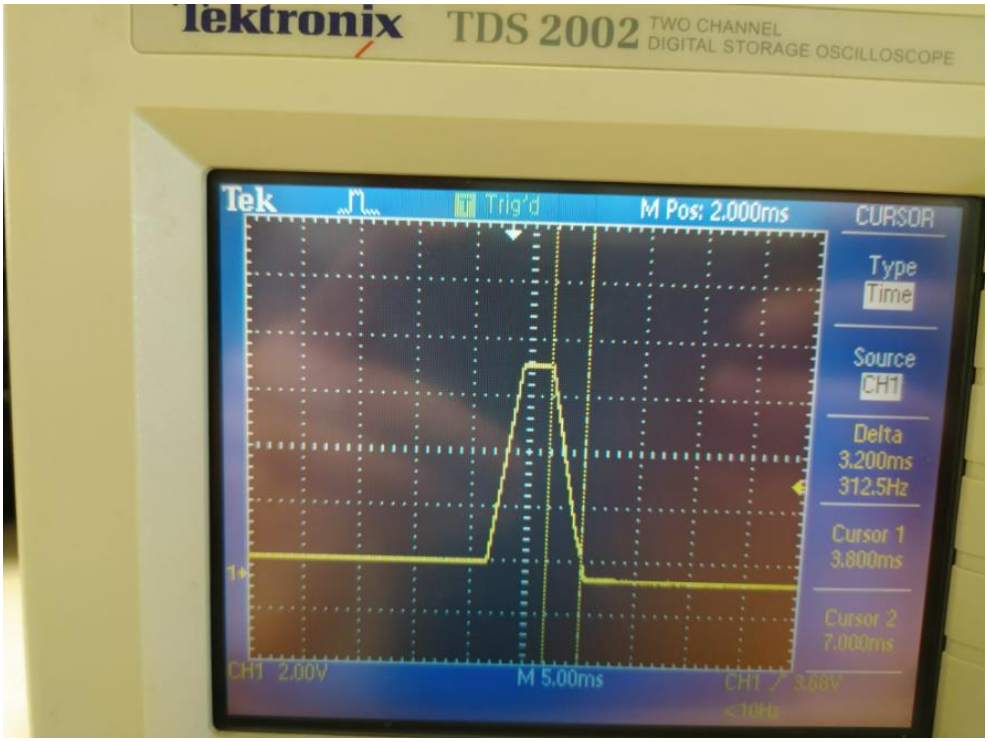

Figure 25: Result 4 of final circuit, $\Delta t_3 = 3.2ms$

Conclusion

In this lab experiment op-amps are used for different reasons. Firstly, they are used to create a delay and changing the amplitude of given input to wanted value. Secondly, they are used to create a slope in wanted time and finally an op-amp is used to subtract a signal from the other one. Therefore, in this experiment usages of op-amps are covered and understand better. Also, it is realized that according to created delay and given input they can be usable for different reasons. However, there were some errors that I encountered in the hardware implementation part. Generally, those errors are raised from the sensitivity of op-amps. They are so sensitive that everything must be connected properly, otherwise the outputs can be so different. Also, one of the difficulties for this lab was that the real-life implementation can be confusing in some points since its in an IC. Fortunately, after some struggle I get better result by checking my circuit but there were still some errors that raised from real life factors such as other resistances.